IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received December 17, 2018, accepted January 9, 2019, date of publication January 22, 2019, date of current version March 18, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2893654

Three-Level Equilibrium Strategy of DC Voltage Balance Control for H-Bridge Cascaded Active Power Filter

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ABSTRACT The H-bridge cascaded active power filter (APF) has broad application prospect in the harmonic procession of high voltage field. Due to differences between H bridges, the imbalance of DC side voltages affects not only compensation effect, but also the safe and stable operation of APF. By derivation of the power exchange model between APF and the power grid, the voltage balance among phases is achieved by the five-order zero-sequence voltage, and the global voltage balance is achieved by the fundamental positive-sequence active current. By appending an active voltage vector in the AC side of each H-bridge, the voltage balance is achieved within the single phase. This three-level equilibrium strategy controls each DC side voltage at the given value eventually. At the same time, the cascaded APF compensates harmonic and reactive current and reduces THD of the grid current. The feasibility of the method is verified by simulation and experimental results under low voltage conditions and provides the basis for application of the APF to a higher voltage level.

INDEX TERMS Compensation effect, harmonic procession, five-order zero-sequence voltage, active voltage vector.

I. INTRODUCTION

With the development of new energy, H-bridge cascaded multilevel topology [1]–[4] has been applied more frequently in power flow control, power electronic transformer, static synchronous compensator, APF and also has become a hot research in high voltage and high power fields. To suppress harmonics in the grid, APF needs to work at a higher switching frequency, but its capacity is limited in high power situation, carrier-phase-shifted pulse width modulation can solve conflicts between the capacity of power switching tube and switching frequency well, which make it suit for the application of H-bridge cascaded APF in high voltage situation.

The balance of DC capacitor voltage in H-bridge cascaded APF is directly related to the quality of AC side voltage, output compensation current and voltage stress of each main switch. Therefore, a steady DC voltage is the premise of running the H-bridge cascaded APF safely and reliably. However, the DC side capacitors in each H-bridge are mutual-independent, and the differences in parallel loss, hybrid loss, input pulse delay and grid voltage distortion [5]–[7] can result the imbalance of DC side voltage.

Now there are two kinds of methods used in the balance of DC voltage: One is to realize the voltage balance through the energy exchange with the external circuit. The DC voltage balancing strategy on the basis of the energy exchange with DC bus and that with AC bus is respectively put forward in [8]. However, the strategy with complex circuit, which costs more is also low in the control efficiency. The other is to realize the voltage balance by improving the control algorithm [9]–[17]. The voltage balancing algorithm is mainly conducted in two levels: phase level and inter-phase level. In terms of voltage balance among phases, [9] proposes to add a balance control loop in each phase, so as to control the voltage balance through controlling the active power. However, it causes the unbalance current; [10] tries to realize the voltage balance by injecting the negative sequence current, but the additional negative sequence current also causes pollution on the grid and affects its compensation performance. As for the voltage balance within single phase, [11] tries to realize the voltage balance by adjusting the phase-shifting angle in each unit, but the phase-shifting angle is narrow in large-capacity converter, so adjusting the phase-shifting angle inappropriately will cause unstable system. [12] adopts

the method of panning the modulation wave up and down. Although it is easy to be realized digitally, a great fluctuation appears in the DC side; [13] directly achieves the PI control in the DC voltage of each H-bridge, but the design of PI parameters in this method is not clear. It is difficult to choose the parameters of the PI controller if the cascaded H-bridge is large in number.

Three-phase uncontrolled bridge rectifier circuit is the main source of harmonic current generation. In three-phase three-wire system, mathematical expressions of the active power absorbed by the cascaded H-bridge APF are derived in this paper. According to the characteristics that the three-phase bridge rectifier circuit produces 6k±1(k = 1, 2, 3 . . .) order harmonics, when cascaded H-bridge APF compensates the harmonics, in order to balance the total voltage of each phase, this paper puts forward to inject high-order zero-sequence voltage to the output invert voltage of cascaded APF to regulate the absorption of active power (concrete implementation is injected into five-order zero-sequence voltage); the voltage balance within single phase is achieved by superposing a voltage vector in AC side of each H-bridge which has same or opposite phase with compensating current; the average value of all DC side voltages are under control by fundamental positive-sequence active current. Finally, each DC side voltage is maintained at the given value.

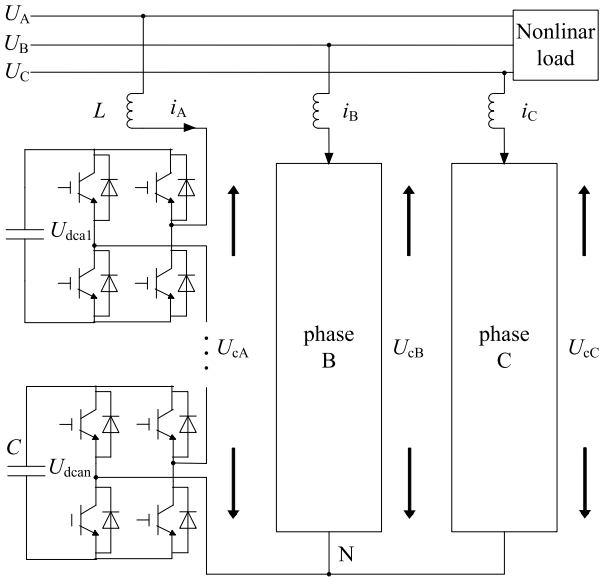

FIGURE 1. Main circuit topology of a H-bridge cascaded APF system.

II. GUIDELINES FOR MANUSCRIPT PREPARATION

The main circuit of H-bridge cascaded APF which adopts star connection is shown in Figure 1.

U_A, U_B and U_C represent three-phase grid voltages and U_{cA}, U_{cB} and U_{cC} represent AC side invert voltages of APF. $U_{dc1} \ldots U_{dcn}$ are capacitor voltages and capacitance is C. The number of H-bridges in each phase is n. The grid reactor is L. i_A, i_B and i_C represent compensating current of APF. N is the neutral point.

Supposing that U_m is the valid value of phase voltage, then system voltage is:

$$\begin{aligned} U_A &= \sqrt{2}U_m \sin(\omega t) \\ U_B &= \sqrt{2}U_m \sin(\omega t - 2\pi/3) \\ U_C &= \sqrt{2}U_m \sin(\omega t + 2\pi/3) \end{aligned} \tag{1}$$

The output compensating current of APF is:

$$\begin{aligned} i_A &= \sum_{\substack{n=1,6k\pm1 \\ k=1,2,3K}} \sqrt{2}I_{mn} \sin(n\omega t + \varphi_n) \\ i_B &= \sum_{\substack{n=1,6k\pm1 \\ k=1,2,3K}} \sqrt{2}I_{mn} \sin(n\omega t + \varphi_n - 2n\pi/3) \\ i_C &= \sum_{\substack{n=1,6k\pm1 \\ k=1,2,3K}} \sqrt{2}I_{mn} \sin(n\omega t + \varphi_n + 2n\pi/3) \end{aligned} \tag{2}$$

I_{mn} is the effective value of n-th harmonic current and φ_n is the initial phase angle of n-th harmonic current. Single-phase bridge rectifier circuit produces odd-harmonic current and three-phase bridge rectifier circuit generates 6k±1 (k = 1, 2, 3 . . .) order harmonic current. Applications of this circuit are very universal, which is also the main source of harmonic current. Resistance-inductance load rectification circuits neglect commutation and current fluctuation. When the inductance is large enough, the load current of phase A is 120° square wave in the positive and negative half-cycle, and it is carried on Fourier decomposition in formula (3).

$$\begin{aligned} i_{LA} = \frac{2\sqrt{3}I_d}{\pi}[&\sin\omega t - \frac{1}{5}\sin(5\omega t) - \frac{1}{7}\sin(7\omega t) \\ &+ \frac{1}{11}\sin(11\omega t) + \frac{1}{13}\sin(13\omega t) - \ldots] \end{aligned} \tag{3}$$

I_d is valid value of output current in the rectifier side and there is $I_d = \sqrt{2/3}I_{LA}$. I_{LA} represents valid value of load current. If the cascaded APF can compensate harmonics within 25 times, then:

$$\begin{aligned} i_A = \frac{2\sqrt{3}I_d}{\pi}[&\frac{1}{5}\sin\omega t + \frac{1}{7}\sin(7\omega t) - \frac{1}{11}\sin(11\omega t) \\ &- \frac{1}{13}\sin(13\omega t) + \ldots] \end{aligned} \tag{4}$$

The valid value of each harmonic current is inversely proportional to its harmonic order from (4), so $I_{m5} > I_{m7} > I_{m13}$.... When the switching frequency is fixed, the order of harmonic is larger, the number of pulses which are used to equal harmonic is smaller in harmonic cycle, and the fitting effect becomes worse. For instance, the cascaded APF outputs five-order zero-sequence voltage to regulate active power absorbed by each phase, and its value is:

$$U_{zero} = \sqrt{2}U_{z5} \sin(5\omega t + \varphi_{z5}) \tag{5}$$

U_{z5} and φ_{z5} are effective value and initial phase angle respectively, and output invert voltage needs to offset grid voltage, so the output invert voltage is:

$$\begin{aligned} U_{cA} &= U_A + U_{LA} + U_{zero} \\ U_{cB} &= U_B + U_{LB} + U_{zero} \\ U_{cC} &= U_C + U_{LC} + U_{zero} \end{aligned} \tag{6}$$

U_{LA}, U_{LB} and U_{LC} are equal to reactor voltages. Averaging the input power of APF, the input power of single phase in fundamental period is:

$$P_X = \frac{1}{T}\int_0^T U_{cX} i_X \mathrm{d}t \quad (X = A,B,C) \tag{7}$$

In symmetrical three-phase system, the fifth harmonic current which APF needs to compensate is negative sequence. According to the orthogonal characteristic of trigonometric function, the active power absorbed from power grid in each phase is:

$$\begin{aligned} P_A &= U_m I_{m1} \cos(\varphi_1) + U_{z5} I_{m5} \cos(\varphi_{z5} - \varphi_5) \\ P_B &= U_m I_{m1} \cos(\varphi_1) + U_{z5} I_{m5} \cos(\varphi_{z5} - \varphi_5 - 2\pi/3) \\ P_C &= U_m I_{m1} \cos(\varphi_1) + U_{z5} I_{m5} \cos(\varphi_{z5} - \varphi_5 + 2\pi/3) \end{aligned} \tag{8}$$

From (8), it can be found that the active power is composed of two parts. One is fixed active power which is produced by the fundamental positive sequence voltage and current, and it is used to compensate the average loss of each phase. The other is active power adjustment produced by zero-sequence voltage and its corresponding current. Due to differences between the modules, $P_A \neq P_B \neq P_C$ generally exists. The active power adjustment is:

$$\begin{aligned} \Delta P_A &= U_{z5} I_{m5} \cos(\varphi_{z5} - \varphi_5) \\ \Delta P_B &= U_{z5} I_{m5} \cos(\varphi_{z5} - \varphi_5 - 2\pi/3) \\ \Delta P_C &= U_{z5} I_{m5} \cos(\varphi_{z5} - \varphi_5 + 2\pi/3) \\ \Delta P_A + \Delta P_B + \Delta P_C &= 0 \end{aligned} \tag{9}$$

Supposing the active power adjustment of each phase can be adjusted respectively by fundamental zero-sequence, five-order zero-sequence, seven-order zero-sequence voltage, then:

$$\begin{aligned} \Delta P_A &= U_{z1} I_{m1} \cos(\varphi_{z1} - \varphi_1) = U_{z5} I_{m5} \cos(\varphi_{z5} - \varphi_5) \\ &= U_{z7} I_{m7} \cos(\varphi_{z7} - \varphi_7) \\ \Delta P_B &= U_{z1} I_{m1} \cos(\varphi_{z1} - \varphi_1 + 2\pi/3) \\ &= U_{z5} I_{m5} \cos(\varphi_{z5} - \varphi_5 - 2\pi/3) \\ &= U_{z7} I_{m7} \cos(\varphi_{z7} - \varphi_7 + 2\pi/3) \\ \Delta P_C &= U_{z1} I_{m1} \cos(\varphi_{z1} - \varphi_1 - 2\pi/3) \\ &= U_{z5} I_{m5} \cos(\varphi_{z5} - \varphi_5 + 2\pi/3) \\ &= U_{z7} I_{m7} \cos(\varphi_{z7} - \varphi_7 - 2\pi/3) \end{aligned} \tag{10}$$

Formula (11) can be derived from (10).

$$\begin{aligned} U_{z1} I_{m1} &= U_{z5} I_{m5} = U_{z7} I_{m7} \\ \varphi_{z1} - \varphi_1 &= -(\varphi_{z5} - \varphi_5) = \varphi_{z7} - \varphi_7 \end{aligned} \tag{11}$$

APF mainly compensates harmonic current and the fundamental current is relatively small, so $I_{m5} > I_{m1}$. Combining $I_{m5} > I_{m7}$, it can be seen that in need of adjusting the same active power, the amplitude of five-order zero-sequence voltage is smaller than fundamental zero-sequence and seven-order zero-sequence voltage, so over-modulation and distortion of the output invert voltage caused by the large fundamental zero-sequence voltage can be avoided. Therefore in order to redistribute active power between three phases, the paper selects five-order zero-sequence voltage to change ΔP_A, ΔP_B, ΔP_C.

Formula (9) can be derived from ABC stationary to DQ stationary coordinate system:

$$\begin{aligned} \begin{bmatrix} \Delta P_Q \\ \Delta P_D \end{bmatrix} &= \frac{1}{3}\begin{bmatrix} 2\Delta P_A - \Delta P_B - \Delta P_C \\ \sqrt{3}(\Delta P_C - \Delta P_B) \end{bmatrix} \\ &= U_{z5} I_{m5} \begin{bmatrix} \cos(\varphi_{z5} - \varphi_5) \\ -\sin(\varphi_{z5} - \varphi_5) \end{bmatrix} \end{aligned} \tag{12}$$

The output five-order zero-sequence voltage of APF can be obtained from formula (12):

$$U_{zero} = \frac{\sqrt{2}}{I_{m5}}[\Delta P_Q \sin(5\omega t + \varphi_5) - \Delta P_D \cos(5\omega t + \varphi_5)] \tag{13}$$

Formula (13) is the five-order zero-sequence instruction voltage for the voltage balance among phases. In addition to achieving the voltage balance, it won't produce zero-sequence current, so it won't cause more pollution to the grid.

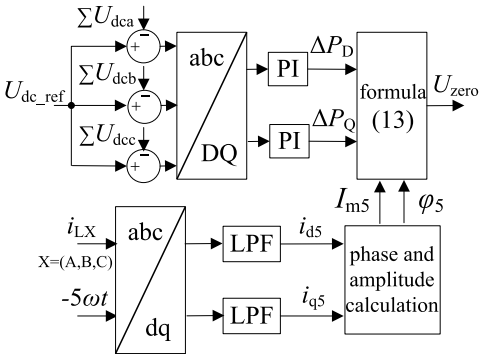

FIGURE 2. Structure diagram of voltage balance among phases.

The control structure of voltage balance among phases is shown in Figure 2. The given voltage is a third of the sum of all DC voltages, and respectively subtracts the sum of voltages in phase A, B and C. These voltage deviations are transformed to DQ stationary coordinate system. The power adjustment ΔP_Q and ΔP_D are obtained after voltage deviations in DQ coordinate system pass through the PI controller. Compensating currents of APF are transformed to five-order negative sequence rotating coordinate system. DC components are obtained after the currents on coordinate axes pass through low pass filter. Then I_{m5} and φ_5 of fifth harmonic current can be calculated by them. The five-order

zero-sequence voltage U_{zero} APF is gained by putting I_{m5}, φ_5, ΔP_D and ΔP_Q into formula (13).

III. VOLTAGE BALANCE CONTROL WITHIN SINGLE PHASE

Voltage balance within single phase is achieved by appending a voltage vector in AC side of each H-bridge which has the same or opposite phase with compensating current. The voltage vector can change active power that H-bridge absorbs or emits, to change the DC side voltage. Supposing the voltage vector is:

$$\Delta U_{cXi} = (U_{dc\_avg} - U_{dcxi})(k_p + k_i/s)i_x K_{ame} \quad (14)$$

U_{dc_avg} and U_{dcxi} represent the average of in-phase voltages and the H-bridge DC bus voltage respectively, k_p and k_i are proportional and integral coefficients of PI regulators for in-phase voltage equalization control. K_{ame} is the amplitude correction coefficient. For the compensating current and voltage vector, the compensation active power in a fundamental cycle is:

$$\Delta P_{Xi} = \frac{1}{T}\int_0^T i_X \Delta U_{cXi} dt = \Delta U_{dcxi}(k_p + k_i/s)K_{ame}\sum_{n=1}^{\infty} I_{mn}^2 \quad (15)$$

When $U_{dcxi} < U_{dc\_avg}$, there is $\Delta U_{dcxi} = U_{dc\_avg} - U_{dcxi} > 0$, so there is $\Delta P_{xi} > 0$. The DC capacitor absorbs active power and its voltage rises. On the contrary, the DC voltage declines.

The voltages in single phase are balanced under the condition that the control strategy can't influence the global and inter-phase voltage balance. When switching frequency is relatively high, the instantaneous compensating current is approximately a constant i_x^c. The modulation mode of H-bridge adopts double-frequency single-polarity SPWM [18], [19]. The DC voltage fluctuation within a switching cycle is:

$$\Delta U_{dcxi} = \Delta Q/C = i_{xC} T_s/C \quad (16)$$

T_s is the switching cycle. ΔQ represents the charge change of H-Bright capacitance.

The total invert voltage of n cascaded H-bridges is:

$$U_{cx} = \sum_{i=1}^{n} d_{xi} U_{dcxi} = \sum_{i=1}^{n} d_{xi} U_{dc\_avg} - \sum_{i=1}^{n} d_{xi}\Delta U_{dcxi} = \sum_{i=1}^{n} dxi U_{dc\_avg} - \sum_{i=1}^{n} \frac{d_{xi} i_{xC} T_s}{C} \quad (17)$$

d_{xi} is the actual duty cycle.

When voltages are unbalanced, the duty cycles of power transistors need to be adjusted. Supposing an average duty cycle output by global voltage control is d_{x0} and duty cycle adjustment of each H bridge is Δd_{xi}, $d_{xi} = d_{x0} + \Delta d_{xi}$. Put it into formula (17) and formula (18) is derived.

$$U_{cx} = nd_{x0}U_{dc\_avg} + \sum_{i=1}^{n} \Delta d_{xi} U_{dc\_avg} - \sum_{i=1}^{n} \frac{d_{x0} i_{xC} T_s}{C} - \sum_{i=1}^{n} \frac{\Delta dxi i_{xC} T_s}{C} \quad (18)$$

The total invert voltage within single phase when the duty cycles aren't adjusted is (19)

$$U_{cx} = \sum_{i=1}^{n} d_{x0} U_{dcxi} = nd_{x0}U_{dc\_avg} - \sum_{i=1}^{n} \frac{d_{x0} i_{xC} T_s}{C} \quad (19)$$

Compar formula (18) with (19), if the invert voltage after duty cycles adjusted remains the same, the following relational formula holds.

$$\sum_{i=1}^{n} \Delta d_{xi} U_{dc\_avg} - \sum_{i=1}^{n} \frac{\Delta d_{xi} i_{xC} T_s}{C} = \left(U_{dc\_avg} - \frac{i_{xC} T_s}{C}\right)\sum_{i=1}^{n} \Delta d_{xi} = 0 \quad (20)$$

To satisfy formula (20), $\sum_{i=1}^{n} \Delta d_i = 0$ is valid. To realize decoupling between voltage balance within single phase and the other two, the duty cycle adjustment of a H-bridge is opposite to the sum of the others in single phase.

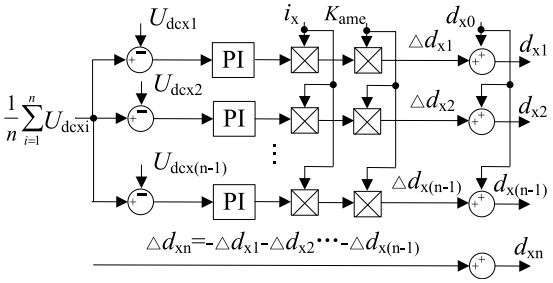

FIGURE 3. Structure diagram of voltage balance within single phase.

Figure 3 shows voltage balance control within one phase. The given value is dynamic average of n DC voltages. Deviations between given voltage and $n-1$ DC voltages pass through PI controllers; the outputs multiply compensating current i_x of each phase. After outputs are corrected by ratio coefficient K_{ame}, the duty cycle adjustments Δd_{xi} is obtained. The adjustment of last H-bridge is opposite to the sum of the others in each phase. The final duty cycle d_{xn} is formed by adding Δd_{xi} to average duty cycle d_{x0} generated from the other two voltage control.When the voltage of a H-bridge increases(decreases), the deviation from the given voltage increases(decreases) accordingly. Δd_{xi} gets smaller(bigger) after PI regulation, which in turn affects the voltage of the H-bridge to decrease(increase)and achieve voltage balance.

IV. GLOBAL VOLTAGE CONTROL

The purpose of global voltage control is the average of all DC voltages equal to reference value. From formula (8), the average voltage can be changed by controlling the fundamental positive-sequence active current.

The structure of global voltage control is shown in Figure 4. Nonlinear load current i_{LX}, compensating current i_X and grid voltage are transformed to dq rotating coordinate system. U^*_{dc} represents given voltage of each H-bridge, and the feedback is average value of all DC side voltages. The deviation passes through PI controller and the output passes through notch filter to remove the interference in feedback voltage, which is added to given current on q axis. Both given current and actual current pass through current controller and the outputs are controlled by feed-forward decoupling. Lastly, they pass through dq inverse transform to get output voltage of each phase U_{cX}.

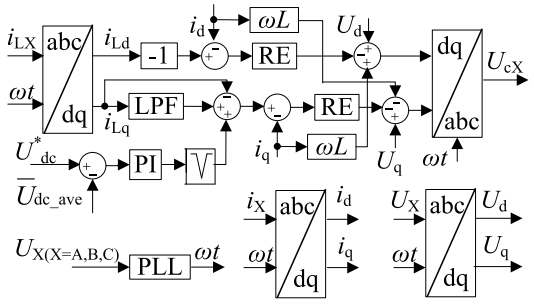

FIGURE 4. Structure diagram of global voltage control.

TABLE 1. Key parameters of H-bridge cascaded APF.

Parameters	Numerical value
Rated voltage/V	380
Inductance /mH	2
DC capacitor /uF	2200
Rated DC capacitor voltage/V	150
Switching frequency /kHz	5
Chain numbers	3
Resistance-inductance Load	37.5Ω+25mH

V. SIMULATION AND EXPERIMENT

The simulation and experiment are completed under low voltage environment; their structural parameters are substantially the same according to Table 1. Different parallel losses which are caused by different parallel resistances to capacitances lead to DC voltage deviations, the three-level equilibrium strategy is applied to stabilize the DC side voltage at the given value.

A. SIMULATION RESULTS

The simulation is studied to verify the correctness of the algorithm about voltage balance. A H-bridge cascaded APF model adopting star connection is built on MATLAB/SIMULINK platform, the simulation model is shown in Figure 5, which includes grid voltage, nonlinear load, H-bridge modular main circuit, grid-connected inductor, modulation wave calculation, CPS-SPWM and measurement module. The grid voltage is used to provide a three-phase

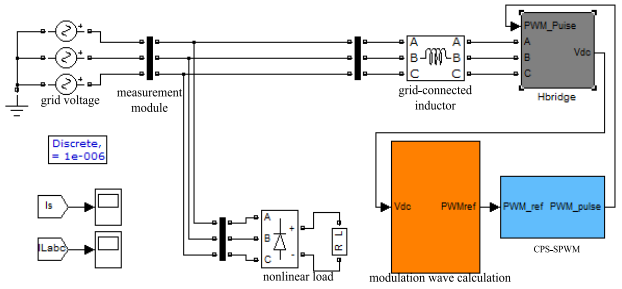

FIGURE 5. Simulation model diagram of H-bridge cascaded APF.

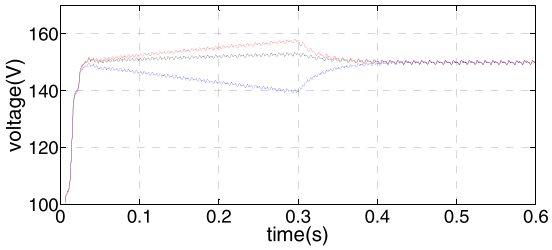

FIGURE 6. Voltage balance control within one phase.

voltage, the function of grid-connected inductor is to store energy and filter harmonics of grid-side current, the object of measurement module is grid-side voltage and grid-side current, modulation wave calculation generates modulation wave by double loop repetitive control of instruction feedforward, and transmits modulation pulse to CPS-SPWM module to generate PWM pulse, the nonlinear load is a three-phase uncontrolled rectifier with resistance-inductance load.

Figure 6 shows changes of three voltages within single phase. The DC side capacitors are respectively parallel with 0.5k, 0.8k and 1kΩ resistances. Before 0.3s, system adopts global voltage control and voltage balance control among phases. Due to different losses in single phase, voltages gradually diverge after rising to given value and deviation becomes larger and larger. But the sum of three voltages keeps constant. At 0.3s, voltages stop diverging by adding voltage control within single phase and they all converge at 150V after 0.1s. The system keeps stable and has small steady-state error.

To cause different losses among phases, DC capacitors of each phase are respectively parallel with 0.5k, 0.8k, 1kΩ resistances. Before 0.3s, system adopts global voltage control and voltage control within single phase. After the average DC voltage rises to given value, the sum of voltages get deviation because of different losses among phases, but the sum of all voltages keeps constant. At 0.3s, voltage balance control among phases is inserted. Figure 7 shows the variation of DC voltages with fundamental zero-sequence voltage control.

Figure 8 shows the given fundamental zero-sequence voltage and the peak value of it is stable at 145V.

Figure 9 shows the variation of the DC voltages among phases with five-order zero-sequence voltage control. Figure 10 shows the given five-order zero-sequence voltage.

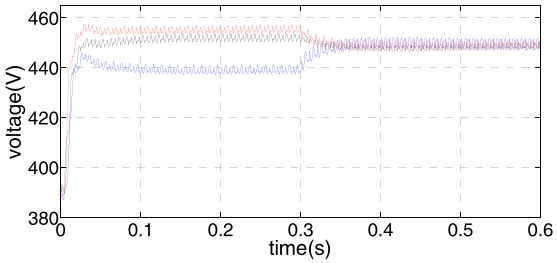

FIGURE 7. Voltage balance control among phases.

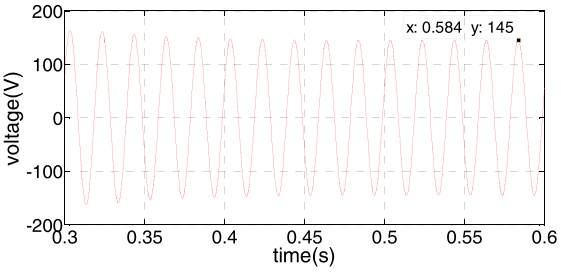

FIGURE 8. Fundamental zero-sequence voltage.

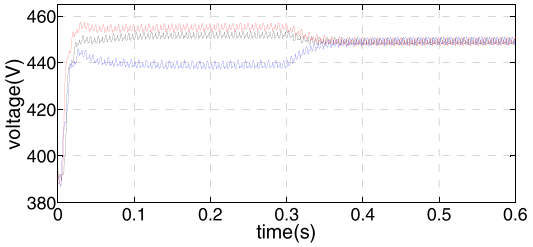

FIGURE 9. Voltage balance control among phases.

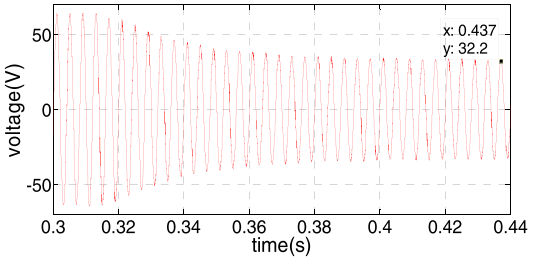

FIGURE 10. Five-order zero-sequence voltage.

Voltages are balanced after 0.1s and the peak value of five-order zero-sequence voltage is stable at about 32V. It can be seen that the value of five-order zero-sequence voltage is smaller than fundamental zero-sequence voltage under the condition that they can achieve the same effect, so it can avoid over-modulation and reduce the probability of invert voltage distortion.

Figure 11 shows the variation of DC voltages among phases when load mutation happens. Three-level equilibrium strategy is used while system is operating. Then load mutation happens at 0.2s. Due to the delay of low-pass filter in harmonic detection process, DC voltages decline and produce deviation. After 0.05s, DC voltages rise to 450V by three-level equilibrium strategy and operate stably.

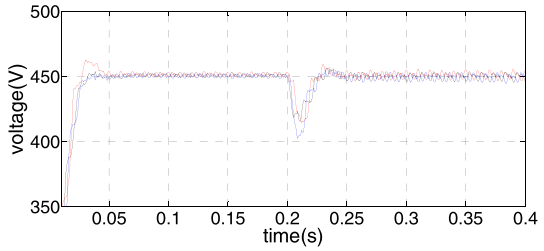

FIGURE 11. Sum of voltages among phases when load mutation happens.

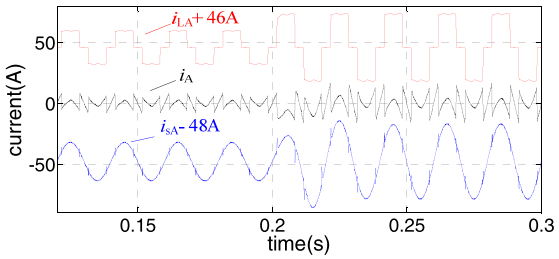

FIGURE 12. Load current, compensating current and grid current after compensation.

Figure 12 shows nonlinear load current, compensating current of APF and compensated grid current. After load mutation, grid current enters steady state after about two power frequency cycles and the respond speed is fast. The THD of grid current drops from 29.96% to 3.23% and current crosses zero point upwardly at integer multiple of the power frequency cycle. It proofs that harmonic and reactive current are well compensated.

B. EXPERIMENT RESULTS

In order to verify the effectiveness of the algorithm, the system uses DSP (TMS320F2812) and CPLD (EPM1270T144C5N) as its controller. DSP performs sampling, data calculation, communication and protection. DSP transmits the modulation instruction obtained by program operation to CPLD. CPLD performs data transportation, protection, generation of multiple carriers and generating 36-way PWM pulses, which are transmitted to the driver board through the optical fiber. The driver chip is the IR2110, the driver plate controls the opening and closing of the switch tube according to the PWM pulse, and thus controls the DC side voltage. The switch tube model is 2MBI75N-060 75A600V. The DC side capacitors are parallel with 10kΩ resistance in phase A and 47kΩ in phase C. Capacitors in phase B are respectively parallel with 1.7k, 3.6k and 5kΩ resistances. The H-bridge cascaded active power filter (APF) has broad application prospect in harmonic procession of high voltage field. The experimental prototype is shown in Figure 13.

In Figure 14, channel 2,3 and 4 show changes of three DC voltages in phase B. They are under the same datum. The system uses three-level equilibrium strategy in initial period. Stage I is shutdown and II is non-control rectification. Owing to different DC losses in phase B, the voltages get deviation. After stage II, APF enters stage III while compensating the

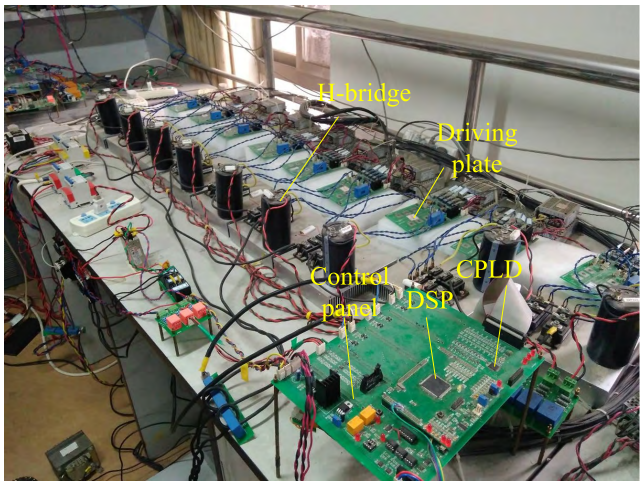

FIGURE 13. Experimental prototype.

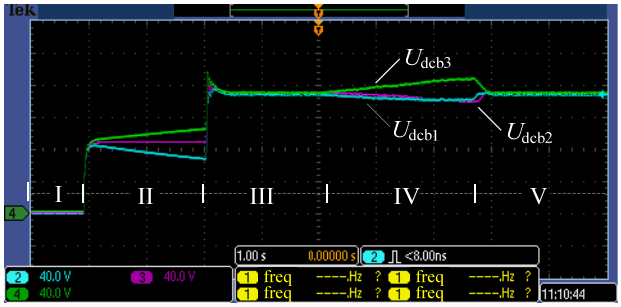

FIGURE 14. Voltage balance control within phase B.

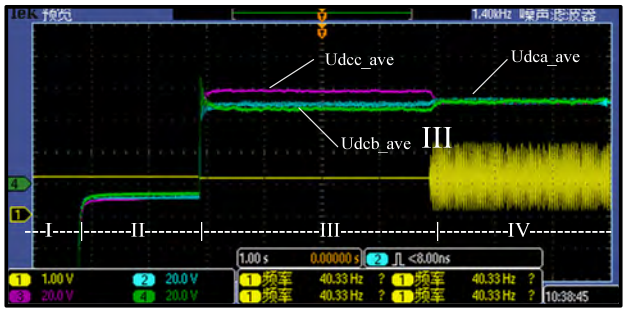

FIGURE 15. Voltage balance control among phases.

harmonic and reactive current. Three voltages rise up and reach the set-voltage after 0.4s. Removing the voltage control in phase B at the end of the stage III, system enters stage IV only using global and inter-phase voltage control. The three voltages are no longer stable and the largest can even rise to 170V (the program adds voltage control in phase B again when the largest reaches 170V, and if not, it will increase to protection value). This not only influences the compensation effect of APF, but also damages the switching tube when the voltage gets too high. When the max voltage reaches 170V, the system enters stage V using three-level equilibrium strategy again. Then three voltages converge to 150V generally and remain stable.

Three voltages respectively from phase A, B, and C are shown in Figure 15. They are under the same datum and have vertical offset of -100V. After stage II, the APF enters stage III while compensating harmonic and reactive current. System adopts global voltage and voltage balance in single phase control. From Figure15, due to different inter-phase losses, voltage in one phase is higher and lower in another phase overall. The inter-phase voltage control is put in after stage III. Three voltages undergo about 0.2s and then reach 150V. Thus all DC voltages run stably at the given value.

Channel 1 shows the variation of calculated five-order zero-sequence voltage in Figure 15. In IV stage, the peak value of five-order zero-sequence voltage is fluctuant; it is bigger when sum of voltages differ greatly between three phases and vice versa. Figure 16 shows a section of the five-order zero-sequence voltage.

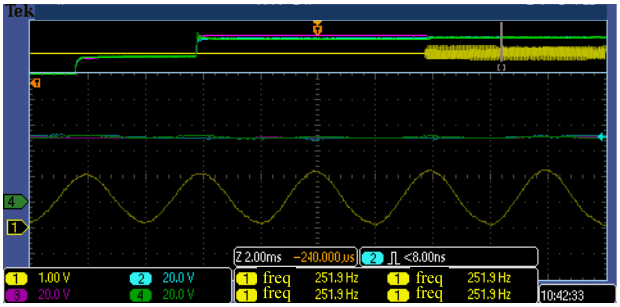

FIGURE 16. Five-order zero-sequence voltage.

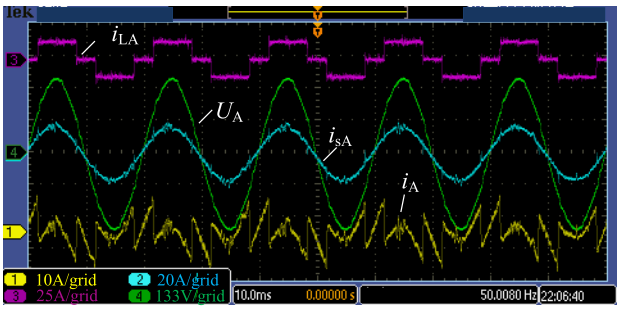

FIGURE 17. Compensating current, grid current after compensation, grid voltage and load current.

TABLE 2. Harmonic contents of grid current before and after compensation.

Harmonic order	Before compensation	After compensation
5	21.22	1.04
7	12.94	1.00
11	8.68	0.79
13	7.37	0.73
17	5.43	0.91
19	5.15	0.81
THD	29.72	4.48

Channel 1 shows compensating current of APF; Channel 2 shows grid current after compensation; Channel 3 shows nonlinear load current and Channel 4 shows grid voltage in Figure 17. It can be seen that the compensated grid current is very close to the sine wave and its phase is consistent with the grid voltage.

Table 2 shows the harmonic contents in grid current before and after compensation. The THD of grid current declines

from 29.72% to 4.48% and the 6k±1 order harmonics generated from nonlinear load are reduced, which indicates the H-bridge cascaded APF realizes the function of harmonic compensation basically.

VI. CONCLUSIONS

The paper takes H-bridge cascaded APF as the research object. Aiming at voltage imbalance of the DC side capacitor, the three-level equilibrium strategy is derived. The voltage balance among phases is achieved by controlling the five-order zero-sequence voltage output from APF, and global voltage stabilization is achieved by controlling the fundamental positive sequence active current. Under these conditions, voltage balance within single phase is achieved by controlling the active voltage vector in the AC side of each H Bridge. Each DC voltage is stable at the given value by three-level equilibrium strategy, and APF obviously compensates harmonic and reactive current meanwhile. This provides the basis for application of APF to a higher voltage level.

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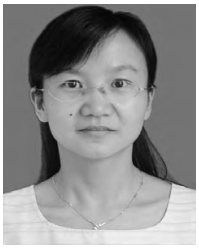

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