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Series Current Flow Controllers for DC Grids

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ABSTRACT Large-scale grid integration of renewables and cross-country border energy exchange may be facilitated by multi-terminal high-voltage direct-current (MTDC) grids. However, as the number of terminals and dc lines increases, power flow management may become a major challenge. This paper addresses such a fundamental issue through the introduction of current flow controllers (CFCs) into the MTDC grid. A CFC is a low power rated controllable voltage source that can enhance system performance by suitably redirecting the power flow at the point of connection. This is achieved through the regulation of the dc line current by introducing a series voltage at the connection node. The characteristics, control, and operation for three configurations of series-connected CFCs are studied. These have been termed a dual-thyristor converter CFC, a cascaded voltage source converter-dc chopper-based CFC, and a dual H-bridge CFC (2B-CFC). A four-terminal MTDC grid has been modeled in Simulink/SimPowerSystems to analyze the dynamic performance of the devices. The simulation results show that all devices are capable of improving system performance. In addition, the CFCs are compared in terms of controllability and dc fault performance. For completeness, a 2B-CFC prototype has been developed to study the impact of a CFC on MTDC grid operation, with an MTDC test rig used to validate simulation results.

INDEX TERMS Current flow controller, dc line, H-bridge, IGBT, multi-terminal HVDC, thyristor, voltage source converter.

I. INTRODUCTION

Decarbonization of the electrical power sector may be facilitated by the large-scale integration of renewable energy into the electricity system. For offshore wind, it is expected that this will be done via voltage source converter (VSC) based high-voltage direct-current (HVDC) links—due to their high efficiency and bulk power transmission over long distances [1]–[4]. Projections indicate that the amount of wind energy in Europe will raise to ≈323 GW by 2030 [5]. Following a suitable coordination of existing point-to-point HVDC links, the delivery of steady and reliable power to onshore ac grids may be ensured by connecting link terminals to additional VSCs to form multi-terminal HVDC (MTDC) grids [6]. An MTDC system will enable cross-country border energy exchanges where the excess energy can be transferred between countries, increasing the functionality and reliability of the network [7].

The deployment of MTDC grids has been hindered by technical challenges, such as the development of dc circuit breakers (DCCBs), communication aspects and the interconnection between different regional systems [8]–[10]. The power transfer capability in a dc grid is uncontrolled and limited by its admittance matrix and cable thermal ratings. In addition, flexible power flow between dc nodes poses significant challenges as the system increases in complexity. In simple grids, power flow control can be precisely achieved by adjusting the voltage set points of each converter [11]–[13]. However, this preciseness decreases with an increase of terminals and branches. Poor grid power flow management could lead to transmission bottlenecks, undesirable power losses and branch overloading [7]. Thus, power flow should be rescheduled between terminals to improve the reliability and efficiency of the dc grid [14].

The previous issues may be relieved by using current flow controllers (CFCs) [15]—inspired by flexible ac transmission systems (FACTS) devices. FACTS equipment is used to regulate key power system parameters by incorporating power electronics devices into the HV side of the ac network to make it electronically-controllable [16]. The flexibility afforded by FACTS devices comes with the possibility to manage reactive power. Although there is no reactive power to be compensated in a dc grid, a CFC may be employed to regulate power flows within the dc network. In this way, a CFC may enable the operation of dc lines/cables within their thermal rating,

a flexible power flow between different systems connected to the dc grid, and an increase/decrease in the amount of power transferred between networks. For instance, a CFC may help the converters to export excess power from one point of the dc grid to another by changing the grid's admittance matrix. During maintenance of converters or cables, a CFC could help to reduce the stress on DCCBs by reducing a dc line current to near zero—thus aiding in the disconnection of lines [17].

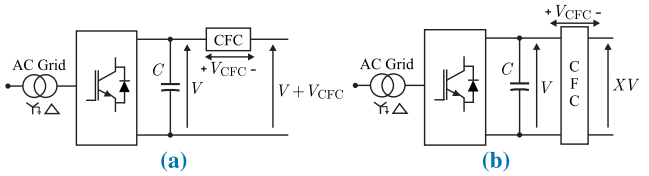

FIGURE 1. Types of CFC: (a) Series-connected; (b) shunt-connected.

CFCs are classified as series or shunt-connected (Figure 1) [15]. Since the dc line resistance is low, a small change in voltage generates a significant current variation which can change the direction of power flow. This feature is exploited by both configurations. The shunt-connected CFC is a dc-dc transformer with step up/down characteristics which can be used to regulate positive and negative pole currents. Its output voltage (XV) is 95-105% of the rated dc line voltage (V), making the power rating of the device 100% under full line current [18]. Although dc-dc transformers have a great controllability over line power flow and eliminate the need of DCCBs by isolating the dc line, their primary use is to interconnect systems with different dc voltages or operating strategies [19]. Conversely, the series-connected CFC is a controllable voltage source. It has a magnitude (V_{CFC}) of 1-5% of the dc grid voltage [18]. The series voltage injection generates a positive resistance effect which increases the dc line current—or alternatively, a negative resistance decreasing line current. Although the dc-dc transformer has a better controllability, its exclusive use for power flow control is not a viable solution in terms of operational and capital costs. A series-connected CFC has lower losses, maintenance and installation costs than its shunt counterpart, thus making it a promising solution for MTDC grid power control.

Substantial research has been dedicated to the development of DCCBs and dc-dc converters [20]–[24], but these efforts have not included series CFCs. Published work on series CFCs is limited, being restricted so far to the analysis of a single device in each publication [25]–[29]. To be able to define the most feasible engineering solution towards deployment in a dc grid, different CFC topologies should be compared using a common platform under similar test conditions before adopting a specific configuration. This paper bridges this gap by presenting the characteristics, range of operation, control, and dynamic operation of series CFC configurations. Three topologies are assessed: dual-thyristor converter CFC (DTC-CFC), cascaded VSC-DC chopper based CFC (CDC-CFC) and dual H-bridge CFC (2B-CFC). A four-terminal MTDC grid and the CFCs have been modeled in Simulink/SimPowerSystems to analyze the dynamic performance of the devices. Simulation results show that the devices successfully achieve flexible power flow control between dc nodes—thus improving system performance by the redirection of power flows in the MTDC grid.

It should be highlighted that the contribution of this work goes beyond carrying out transient simulations to assess the CFC capability to control power flow in a dc grid. A detailed comparison is presented not only in terms of dynamic performance, but also from the viewpoint of controllability and protection. The merits and drawbacks of each configuration under these considerations are critically discussed. Furthermore, this paper presents the performance of different series CFC topologies under dc faults. Such an assessment provides an insight into device protection aiming towards improving the existing configurations to ensure the reliability of a dc grid.

Since simulation-based studies have limitations, the operation and control of a 2B-CFC has been experimentally verified using an MTDC test-rig under steady-state and system disturbance conditions.

II. TOPOLOGY OF SERIES CFCs

A. DUAL THYRISTOR CONVERTER CFC

A thyristor is a unidirectional device carrying current only in one direction (from anode to cathode). This restricts the operation of thyristor-based converters to two quadrants, where a change in the direction of the current requires a voltage polarity reversal.

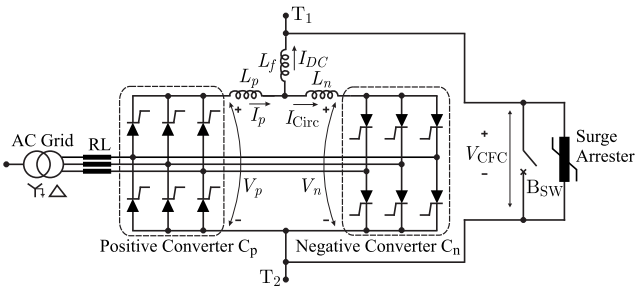

FIGURE 2. Topology of a DTC-CFC.

Figure 2 shows a DTC-CFC. It consists of two three-phase thyristor-based converters connected in anti-parallel to ensure a four-quadrant operation. The CFC may be powered up using a single-phase ac connection, although this may lead to an unbalanced ac system. On the dc side, terminals T_1 and T_2 are connected in series with a dc line and in parallel to a solid-state bypass switch B_{SW} and a surge arrester. This way, if the CFC is not active it is bypassed via B_{SW}. The surge arrester protects the CFC in case of dc faults, where high fault currents could lead to overvoltages.

The firing angles of the converters are related so that both produce the same terminal voltage [30]. While one converter operates as a rectifier, the other acts as an inverter, with

$$\alpha_p + \alpha_n = \pi, \tag{1}$$

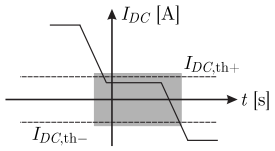

FIGURE 3. DC line current threshold limits.

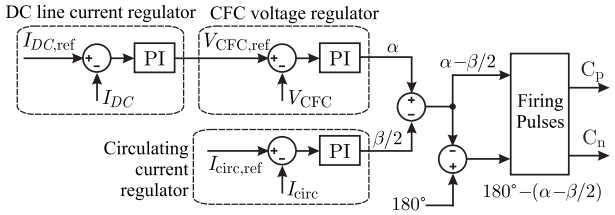

FIGURE 4. Controller structure of a DTC-CFC.

where α_p, α_n are the firing angles of the positive and negative converters. The CFC's dc side voltages are given by

$$V_p = \frac{3\sqrt{2}}{\pi} V_{s,\max} \cos(\alpha_p), \quad V_n = \frac{3\sqrt{2}}{\pi} V_{s,\max} \cos(\alpha_n), \quad (2)$$

where $V_{s,\max}$ is the ac line-to-line voltage and V_p, V_n the positive and negative terminal voltages. Only one converter receives firing pulses at any time, with the other being blocked due to the polarity of the current. The positive converter receives pulses only if the line current is positive and above the threshold value. If the line current is negative and below the threshold value only the negative converter receives firing pulses. When the dc line current falls below the threshold values (see Figure 3), both converters receive firing pulses to enable a smooth change in the direction of the current. Thus, a discontinuous dc line current below the threshold value may exist [31]. In this case, the instantaneous voltage difference between converters causes a circulating current, whose magnitude may be limited via inductors L_p, L_n (see Figure 2). This has to be done with care as it may increase power losses due to the large dc line current flow through the inductor. Alternatively, the circulating current can be regulated as in [32]. In this work, the control structure shown in Figure 4 is used. An angle β is introduced to control the circulating current, where:

$$\begin{aligned} &\alpha_p + \alpha_n = \pi - \beta, \quad \alpha_{p,\mathrm{new}} = \alpha_p - \beta/2, \\ &\alpha_{n,\mathrm{new}} = \alpha_n - \beta/2. \end{aligned} \quad (3)$$

The circulating current controller activates only if the dc line current falls below threshold values $I_{\mathrm{DC,th}+}$ or $I_{\mathrm{DC,th}-}$ shown in Figure 3.

The DTC-CFC controller structure employs nested control loops based on PI controllers (see Figure 4). The inner loop regulates the CFC output voltage, controlling the firing angle of the thyristor bridge. The outer loop regulates the dc line current and generates the reference signal for the inner loop.

Figure 5 illustrates the effect of the circulating current regulator shown in Figure 4. For this example, the dc line current reference has been set below a defined threshold to

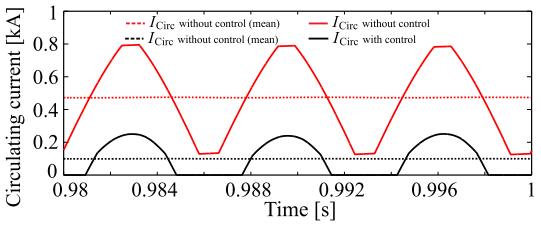

FIGURE 5. Circulating current profile with and without regulation.

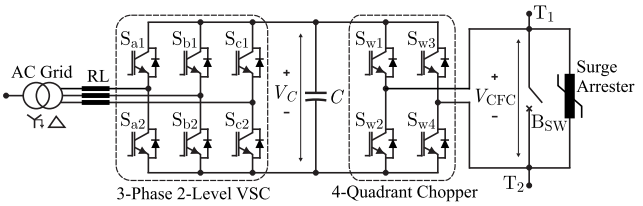

FIGURE 6. Topology of the CDC-CFC.

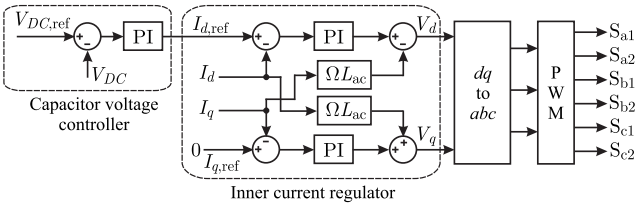

FIGURE 7. Controller structure of three-phase two-level converter.

cause a circulating current between the positive and negative converters. As it can be seen, the current contains both ac and dc components. It can be noticed from Figure 5 (red trace) that its magnitude is considerably larger when the controller is inactive. Thus, an uncontrolled circulating current could lead to additional power losses than when it is regulated.

B. CASCADED VSC-DC CHOPPER BASED CFC

This consists of a three-phase two-level PWM controlled converter and a four-quadrant chopper—with switching modules consisting of anti-parallel connected IGBTs and diodes. This arrangement ensures a bidirectional capability. The CFC is connected to an ac system through a phase reactor and a step-down galvanic isolation transformer (see Figure 6).

The output dc voltage V_{CFC} and the capacitor voltage V_C are related as [33]

$$V_{\mathrm{CFC}} = (2D-1)V_C, \quad -V_C \le V_{\mathrm{CFC}} \le V_C, \quad (4)$$

where D is the duty cycle of the chopper and $0 \le D \le 1$. The two-level converter maintains a constant capacitor voltage while the H-bridge regulates the dc line current by generating a variable mean dc voltage in series with the dc line.

The capacitor voltage controller, shown in Figure 7, is similar to synchronous reference frame-based VSC control schemes. It consists of an inner current loop cascaded with an outer capacitor voltage loop. Import and export of reactive power are avoided by setting the q-axis reference to zero. The H-bridge controller, shown in Figure 8, consists of two cascaded loops; namely, the dc line current

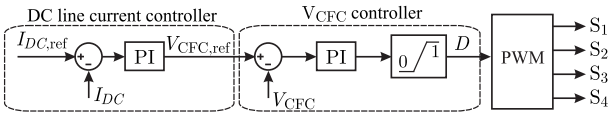

FIGURE 8. H-bridge controller.

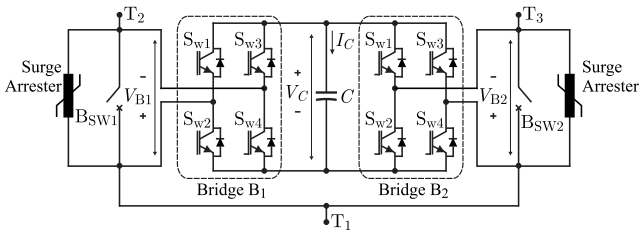

FIGURE 9. Topology of a 2B-CFC.

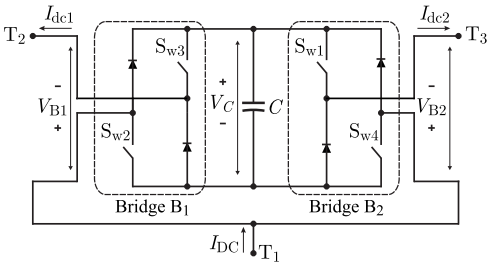

FIGURE 10. Active elements of the 2B-CFC.

controller (outer loop) and the V_{CFC} controller (inner loop). The outer loop regulates the dc line current by generating a reference signal $V_{CFC,ref}$ to the inner loop.

C. DUAL H-BRIDGE CFC

The 2B-CFC consists of two electrically coupled H-bridges and a dc capacitor, as shown in Figure 9. Since the H-bridges are connected in series with dc lines, the power taken from one line is equal to the power added to the other line [34], [35]:

$$V_{B1}I_{DC1} = V_{B2}I_{DC2}. \tag{5}$$

Only two switches per bridge are active during operation, which is decided by the line current direction. Consider the diagram in Figure 10. When current flows from terminal T_1 to terminals T_2 and T_3, switches S_{W2}, S_{W3} of bridge B_1 and S_{W1}, S_{W4} of B_2 are active, while other switches are bypassed through naturally commutated diodes. However, to change the line current only one switch on each bridge has to be modulated.

In the 2B-CFC, one bridge regulates the capacitor voltage to a constant value while the other one controls the dc line current by chopping voltage V_C. When the current directions are the same, voltages V_{B1} and V_{B2} should have an opposite polarity to satisfy the power balance between bridges as given by (5). If the current on one conductor changes its direction, both voltages should have the same polarity. The capacitor voltage must be controlled in all four quadrants.

Figure 11 shows the dc line current through B_2 using a dual bridge modulation, where the switching combinations of the

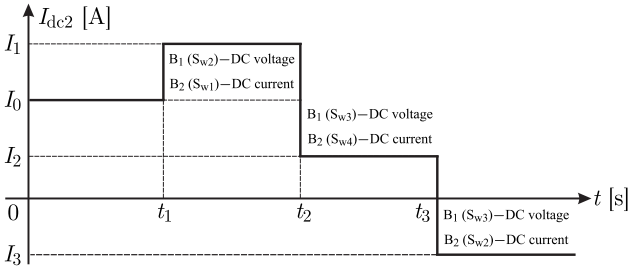

FIGURE 11. Switching elements. Control using dual bridge modulation.

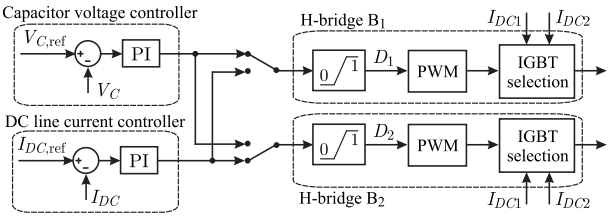

FIGURE 12. Control strategy: dual bridge modulation.

IGBTs change as the direction of the current on the conductor and the line current reference change. The CFC is initially bypassed through bypass switch B_{SW}. It is activated at $t = t_1$ and requested to increase the line current to a value I_1. To achieve this, a positive dc voltage needs to be inserted between T_1 and T_3. This ensures that power is exported from B_2 to B_1. Under this scenario, B_1 (S_{W2}) maintains a constant dc voltage and B_2 (S_{W1}) regulates the dc line current. Now, consider that a new reference I_2 which is lower than the nominal value I_0 is set at $t = t_2$. A negative dc voltage between T_1 and T_3 is required for this operating condition, where power is exported from B_1 to B_2. In this case, switch S_{W3} of B_1 maintains a constant dc voltage and S_{W4} of B_2 regulates the dc line current.

To reverse the direction of the dc line current, S_{W2} and S_{W3} of B_2 should become active, with the active switches on B_1 remaining the same. In addition, the magnitude of the negative voltage between T_1 and T_3 should be increased further. This is exemplified at $t = t_3$, where S_{W3} of B_1 maintains a constant dc voltage, while S_{W2} of B_2 controls the line current.

A block diagram of the control strategy for the 2B-CFC is shown in Figure 12. The capacitor voltage controller is designed to maintain a constant capacitor voltage by regulating the duty cycle of the controlled switch. The dc line current is regulated via the other bridge through a PI controller, which generates a mean dc voltage.

III. MTDC MODELING AND CONTROL

A four-terminal VSC-based MTDC grid has been adopted to demonstrate the dynamics, control and operation of the CFCs presented in Section II. The system under study is shown in Figure 13(a). It has been adapted from [11] and emulates a hypothetical North Sea based meshed dc grid where Grids 1-4 represent Scotland, RG Nordic, England, and RG continental Europe [37], [38]. The CFC locations are

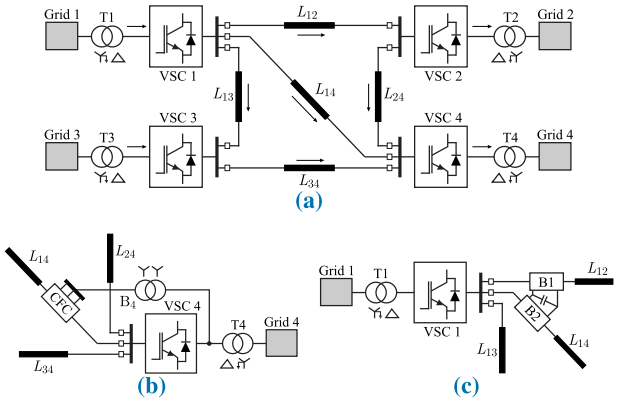

FIGURE 13. (a) Four-terminal VSC-based MTDC grid. (b) Location of DTC and CDC-CFCs. (c) Location of the 2B-CFC.

TABLE 1. Initial dc voltage and power reference values.

Terminal	T_1	T_2	T_3	T_4
$P_{\text{DC,ref}}$ [MW]	800	-	700	−500
$V_{\text{DC,ref}}$ [kV]	-	640	-	-

TABLE 2. DC line parameters [11], [41].

DC Line	L_{12}	L_{13}	L_{14}	L_{24}	L_{34}
Length [km]	125	80	125	160	160
Resistance [Ω]	2.4	1.53	3.84	3.07	3.07
Inductance [mH]	30	19.2	48	38.4	38.4
Capacitance [μF]	19	12.16	19	24.32	24.32

TABLE 3. VSC terminals: system parameters.

Parameter	Value
AC transformer	430 kV/320 kV
Nominal power	1 GW
Phase inductance and resistance	49.89 mH/153.9 mΩ
DC capacitance	500 μF
Converter f_{sw}	1650 Hz
AC frequency	50 Hz
DC voltage	640 kV

shown in Figures 13(b)-13(c). A pole-to-pole dc voltage and power ratings of ±320 kV and 1 GW have been used. Each converter is connected to an ac system with a phase reactor and a transformer. The VSC control strategy uses a *dq* frame scheme to regulate dc voltage or active and reactive power. A master-slave control strategy for the MTDC grid has been adopted.

For the system under study, terminals T_1, T_3 and T_4 are operated under a constant power control mode whereas T_2 acts as a slack busbar maintaining grid power balance (constant dc voltage). Initial reference values are given in Table 1. A positive power flow is given by the arrows in Figure 13(a). The dc lines have been modeled as π sections [39], [40], with parameters given in Table 2 (electrical parameters have been taken from [41] and line lengths adapted from [11]). Table 3 includes the parameters of the VSC terminals.

To ensure the protection of the dc grid, simple solid-state based DCCBs in series with a limiting reactor (50 mH) are

TABLE 4. CFCs system parameters.

Parameter	Type of CFC		
	DTC	CDC	2B
AC transformer [kV]	320/4	320/2.5	-
Nominal power [MW]	8	8	8
Phase inductance [mH]	0.49	0.49	-
Phase resistance	-	-	-
DC capacitance [F]	-	5.2 m	1000 μ
Limit. induct. L_p, L_n [mH]	10	-	-
Smoothing induct. L_f [mH]	70	-	-
Converter f_{sw} [Hz]	-	1650	-
H-Bridge f_{sw} [Hz]	-	1000	1000
AC frequency [Hz]	50	50	-
Capacitor voltage V_C [kV]	-	5	5
V_{CFC} [kV]	±5	±5	-
V_{B1}, V_{B2} [kV]	-	-	±5

considered at both ends of each dc line; an opening time of 2 ms has been adopted [20], [21]. The CFC parameters are given in Table 4. The switches in the CDC and 2B-CFCs can be realized with an IGBT, a field effect transistor, or any other suitable self-commutated semiconductor device that could be connected in series or in parallel to achieve the rated voltage and current ratings. It should be highlighted that the dc capacitance for the CFCs can be selected as a trade-off among the maximum voltage ripple, module voltage rating, power losses and switching frequency. The values shown in Table 4 were obtained by defining the following constraints: a maximum voltage ripple of 10% to minimize the stress level on the capacitor, and maximum power losses of 0.001% of the converter power rating. All PI controller gains from the control schemes can be found in the Appendix.

IV. SIMULATION RESULTS AND ANALYSIS

The system under study (Figure 13) has been modeled using SimPowerSystems. Time-domain simulations and comparisons have been done for the three topologies presented in Section II.

A. CONTROLLABILITY

The controllability of a CFC is defined as the change in the dc line current with respect to the control ratio; i.e. the CFC output voltage. A control ratio of 1 represents the maximum dc voltage generation, with 0 standing for 0 V. To assess controllability on a specific example, the capacitor voltage of the 2B and of the CDC-CFCs has been set to 5 kV (see Table 4). The reference values for the converters are provided in Table 1. The controllability of DTC and CDC-CFCs has been evaluated by connecting the CFC in series with each dc line, whereas the 2B-CFC has been connected at eight different locations to assess different line combinations. In all scenarios, the DTC and CDC-CFCs are connected to the nearest converter's valve side. The initial line current without an active CFC has been defined as the zero compensation mode (ZCM).

Figure 14 shows the change in dc line currents at the maximum control ratio of each device. Results for a DTC-CFC

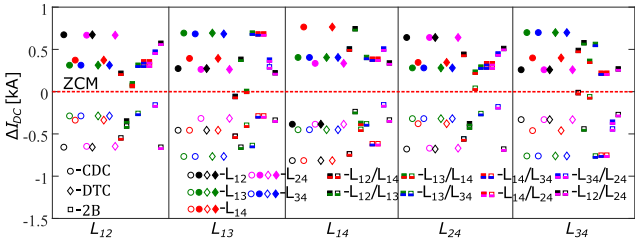

FIGURE 14. Controllability of the different types of CFC.

are represented with diamonds, whereas circles are used for a CDC-CFC and squares for a 2B-CFC. Black, green, red, magenta and blue data points represent the changes in line currents when DTC and CDC-CFCs are installed in series with lines L_{12}, L_{13}, L_{14}, L_{24} and L_{34}, respectively. For the 2B-CFC a combination of two colors is employed, which is determined by the placement of bridges B1 and B2. The controllability plot is divided in two regions. Region 1 is the area above ZCM, where the inserted voltage in series with the dc lines are positive. Region 2 is the area below ZCM, where the inserted voltage is negative.

The results in Figure 14 show that both DTC and CDC-CFCs have a similar level of controllability. It can been observed that the controllability of a dual H-bridge device is significantly affected by its location as the inserted voltages are mainly influenced by the line currents. However, a similar level of controllability compared to DTC and H-bridge based devices can be achieved if the 2B-CFC is placed between appropriate dc nodes; e.g. when it is connected between L_{12} and L_{14}, L_{12} and L_{24}, and L_{13} and L_{34}. Furthermore, controllability can be improved by increasing the capacitor voltage level at the expense of also increasing its power and voltage ratings—the higher the capacitor voltage, the greater the amount of IGBTs required in each bridge/arm.

B. CONTROL, DYNAMICS AND OPERATION

The following simulation conditions have been applied to all of the devices to assess and compare their performance. Initially, the CFCs are bypassed through solid-state bypass switches. At $t = 1$ s, control signals are dispatched to the CFCs requesting to regulate the current of line L_{14} to 600 A. At $t = 2$ s the line current reference is set to 200 A. To demonstrate a four quadrant capability, a line current flow reversal is requested at $t = 3$ s (reference set to -200 A). The operation of the CFC under changes in active power set points in the dc grid while keeping a constant line current reference (-200 A) is assessed during the last part of the simulation. At $t = 4$ s the active power of VSC 1 is set to 900 MW. While keeping the same line current reference, the set points for VSCs 3 and 4 are adjusted to 1000 MW and -800 MW at $t = 4.5$ s, respectively.

1) DTC-CFC

The results for this device are shown in Figure 15. The CFC generates a constant dc voltage rather than a pulsating dc voltage (Figure 15(a)). Pulses for the negative and the positive

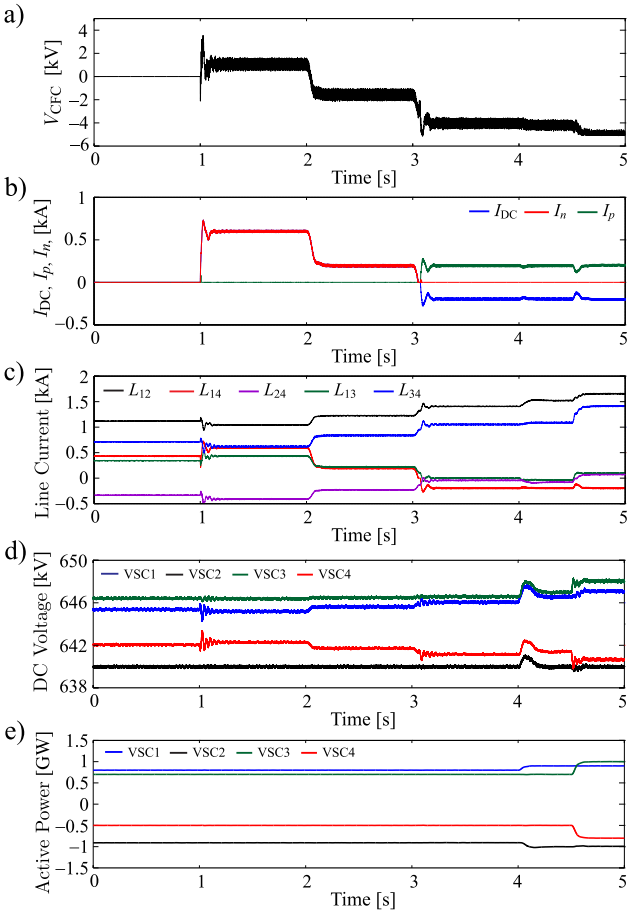

FIGURE 15. Dynamics of the DTC-CFC: (a) CFC capacitor voltage; (b) CFC dc current profile; (c) dc line current profile; (d) VSC voltage; (e) VSC power.

converters are blocked initially. At $t = 1$ s the positive converter is fired to regulate the dc current of L_{14} to 600 A. At the same time the negative converter is blocked and thus the current through the positive converter equals that of the dc line (Figure 15(b)). During the current reversal period the current of L_{14} falls below the threshold value (Figure 15(c)). Thus, for a short period both converters receive pulses and a circulating current flows between them due to an instantaneous voltage difference. The magnitude of this current is limited to ± 100 A by the circulating current controller and inductances L_p, L_n. This allows a smooth dc line current reversal. As shown in Figure 15(b), once the dc line current passes the negative threshold it is no longer provided by the positive converter (becoming zero for it) but by the negative one. After the reference power of the VSCs changes at $t = 4$ s and $t = 4.5$ s (Figure 15(e)), the dc line currents and terminal dc voltages (Figures 15(c)-(d)) reach new steady state values while the controlled line current has remained constant at -200 A. However the required dc voltage has increased due to the new line current distribution.

2) CDC-CFC

Figure 16 shows the results for this device. The capacitor voltage is maintained at 5 kV during the simulation

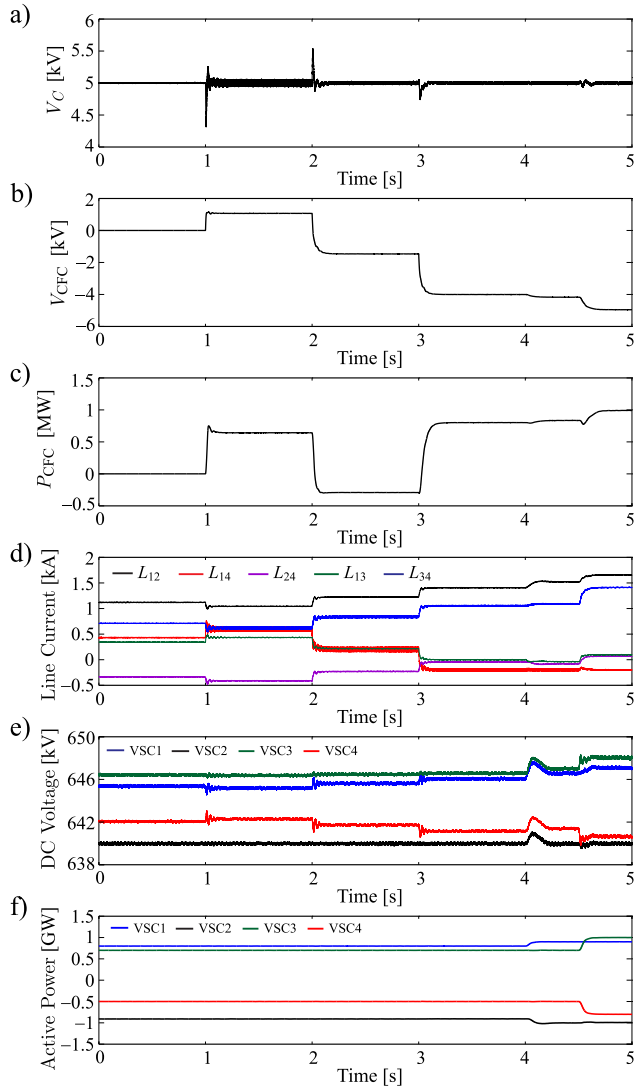

FIGURE 16. Dynamics of the CDC-CFC: (a) CFC capacitor voltage; (b) inserted dc voltage; (c) CFC dc power; (d) dc line current; (e) VSC voltage; (f) VSC power.

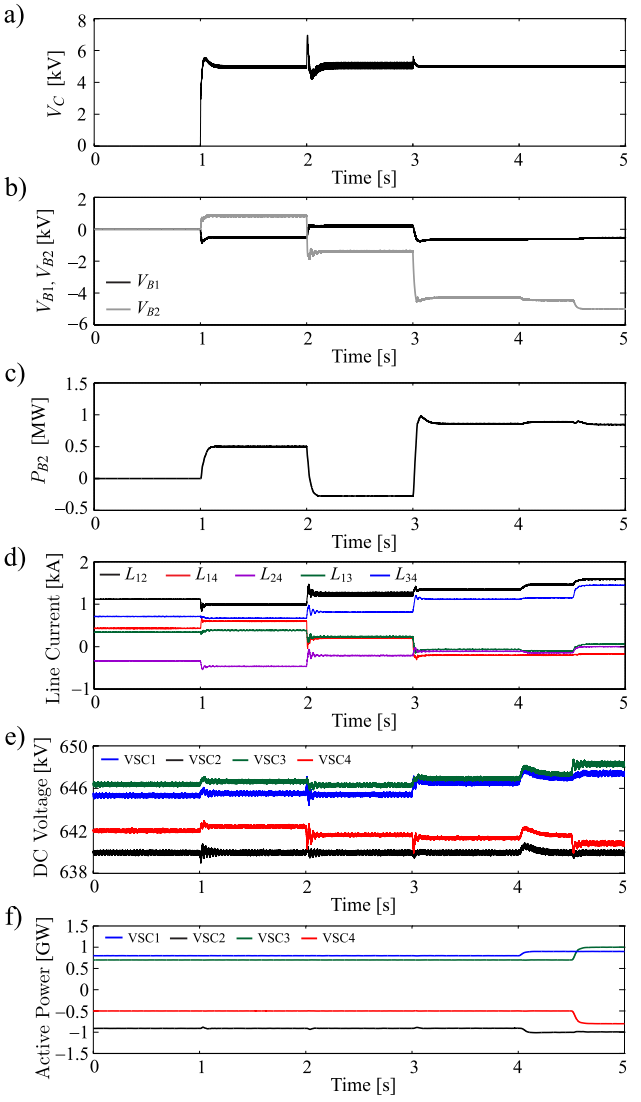

FIGURE 17. Dynamics of the 2B-CFC: (a) CFC capacitor voltage; (b) inserted dc voltages; (c) bridge B_2 power; (d) dc line current profile; (e) VSC voltage; (f) VSC power.

(Figure 16(a)). To increase the line current of L_{14} to 600 A (Figure 16(d)), the CFC generates a positive mean dc voltage V_{CFC} between converters 1 and 2 (Figure 16(b)). As shown on Figure 16(e), the converters adjust their dc voltages to maintain a constant power. For this condition power is exported from the dc grid to the ac side (Figure 16(c)). At $t = 2$ s, the CFC reference is set to 200 A—lower than the initial value $I_0 = 432$ A. A negative mean dc voltage is applied between the terminals to decrease the current flow. Since the current is positive and the applied voltage has changed its polarity, power is exported from the ac network to the dc grid. It can be seen that the CFC is able to carry out a current reversal (-200 A) at $t = 3$ s and that the desired current is achieved by further increasing the voltage magnitude. To maintain the line current constant at -200 A after a positive step change in power at $t = 4$ s (Figure 16(f)), the inserted dc voltage magnitude is increased further (Figure 16(b)). Following the power step changes at $t = 4.5$ s, the device almost reaches its maximum operating point.

3) 2B-CFC

Figure 17 shows the simulation results. At $t = 1$ s, bypass switches are opened and control signals are dispatched to bridges B_1 and B_2. Between $t = 1 - 2$ s, B_1 controls the dc voltage while B_2 generates a positive mean dc voltage between terminals T_1 and T_4 (with respect to T_1). The inserted voltage between T_1 and T_2 is negative; i.e., power is balanced between H-bridges. As shown in Figure 17(e), T_1, T_3 and T_4 have adjusted their voltages to maintain the grid power balance. To regulate the current to 200 A (Figure 17(d)) power should be subtracted from line L_{12} and added to L_{14} (Figure 17(c)). This implies that bridge voltages V_{B1} and V_{B2} should change their polarity (Figure 17(b)). To reverse the line current (at $t = 3$ s) the voltage magnitude between

T_1 and T_4 should be increased further. Since line currents I_{L12} (I_{DC1}) and I_{L14} (I_{DC2}) have opposite sign, V_{B1} and V_{B2} should have the same polarity. As seen in Figure 17(d), the magnitude of I_{L14} remains at -200 A despite the change in the power reference for T_1 at $t = 4$ s (Figure 17(f)). Following the power step changes at $t = 4.5$ s, the CFC reaches its maximum controllability—evidenced by a steady state error of 30 A between the reference set point and the measured line current.

C. DEVICE PROTECTION AND FAILURE CONSIDERATIONS

A major challenge in the development of MTDC systems is grid protection. Due to the low dc side impedance, a dc fault will generate large fault currents. Thus, care should be exercised since a poor protection system may lead to permanent damages. Following this line, an assessment of the proposed CFCs under dc and system faults is fundamental. The devices are equipped with surge arresters, bypass switches (see Figures 2, 6 and 9) and capacitor discharge circuits. After a CFC has been bypassed, its dc capacitor should be drained to a safe level to protect the power electronics modules. This requires an additional discharging circuit where the stored energy can be dissipated through a resistor via a controlled switch.

Bypass switches can be either mechanical or solid-state switches (see Figure 18). During a system or dc fault, the proposed CFC devices based on IGBTs can be disconnected by either activating the bypass switch while blocking the IGBTs or just by bypassing the IGBTs. This way, the DTC-CFC may be disconnected by activating its bypass switch. It must be emphasized that use of mechanical based bypass switches with slow response time (30-40 ms) [44] could increase the CFC power ratings as the fault current cannot be instantly redirected into the bypass switches.

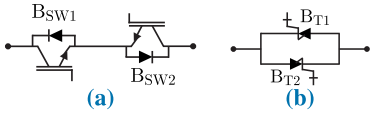

FIGURE 18. Types of solid-state bypass switch. (a) IGBT. (b) Integrated gate-commutated thyristor (IGCT).

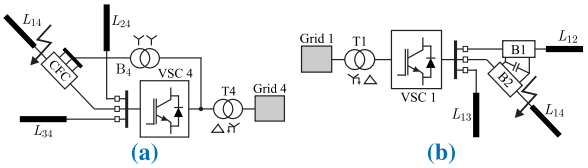

FIGURE 19. DC fault location.

CFC protection during dc faults is mainly determined by the fault current magnitude and the response time of bypass switches. To analyze the impact of a dc fault on the CFCs, a pole-to-pole fault is applied at $t_0 = 1.5$ s. The fault locations are shown in Figure 19. The fault has been applied on the line where the CFCs are installed to maximize its effect. System states during the fault are provided in Table 5.

TABLE 5. System state during dc fault.

Time	System state
t_0	Pole-to-pole fault applied
t_1	Fault detected by CFC, bypass switches activated and control signals disabled
t_2	Opening of DCCBs

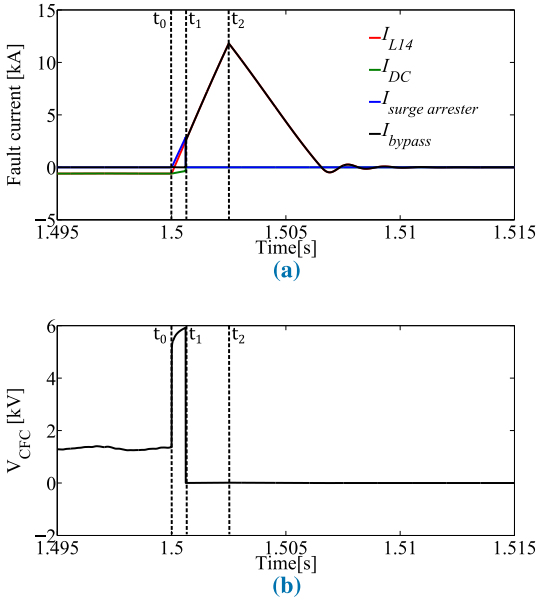

FIGURE 20. Fault response of DTC-CFC. (a) Fault current distribution. (b) Terminal voltage.

Figure 20 shows the response of the DTC-CFC. A surge arrester is installed for overvoltage protection (see Figure 2). At $t = t_1$, the fault current is transferred from the arrester to the bypass switch B_{SW}, with the current through the CFC, I_{DC}, becoming zero. The DCCBs are activated at $t = t_2 = 1.505$ ms to isolate the faulty line. The thyristor modules can hold a very large surge current for several milliseconds; however, they should be immediately bypassed to avoid any contribution from the ac side.

Figure 21 illustrates the voltage and current profiles of the CDC-CFC. Similar test conditions as for the DTC-CFC have been applied. The capacitor is rapidly charged by the fault current between t_0 and t_1, with its voltage being limited by a surge arrester. At $t = t_1$, the fault is detected by the CFC, the control signals are disabled and the IGBTs are blocked; this way, the fault current is redirected to bypass switch B_{SW}. The faulty line DCCBs are opened at $t = t_2$ to isolate the line. The magnitude of the capacitor voltage V_C remains high as no discharging paths are available. As mentioned before, the voltage level can be brought down a safer level by using a controllable discharge circuit.

The performance of the 2B-CFC is shown in Figure 22. After the fault is applied at $t = t_0$, the magnitudes of line currents I_{L12} and I_{L14} rapidly increase, with I_{L12} changing polarity. This occurs as the CFC tries to maintain the line current at the reference value as it has not detected the fault yet.

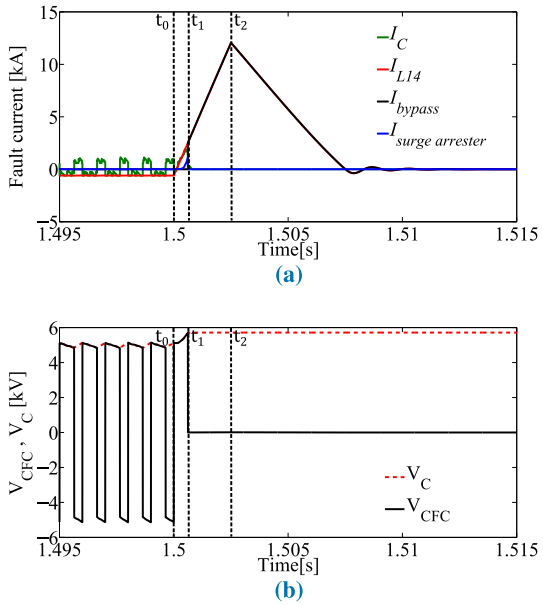

FIGURE 21. Fault response of CDC-CFC. (a) Fault current distribution. (b) Capacitor and H-bridge voltage.

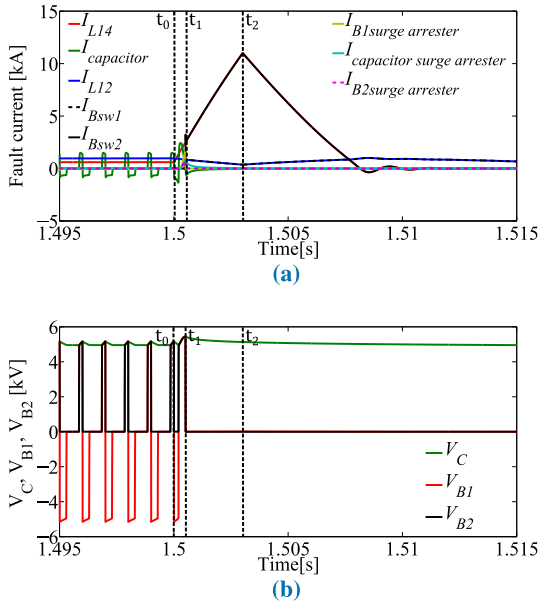

FIGURE 22. Fault response of 2B-CFC. (a) Fault current distribution. (b) Capacitor voltage and H-bridge voltage.

In turn, this causes the capacitor and bridge voltages to build up to a maximum level (limited by commutating part of the fault current into the surge arresters). At $t = t_1$, the CFC detects the fault, the control signals are disabled, the IGBTs are blocked and the bypass switches B_{SW1} and B_{SW2} are activated. The lines are isolated at $t = t_2$ by opening the DCCBs. As it can be observed, the 2B-CFC has shown a similar level of vulnerability as the other CFCs.

In terms of fault management, the proposed CFCs may be affected by dc faults; thus, fast DCCBs and communication are required to ensure a good protection. However, thyristors can hold a large surge current when compared to IGBT devices—this makes the DTC-CFC less vulnerable to a dc fault. From the results presented in this section, it is clear that the bypass switch needs to hold a large current until the fault is cleared. IGCT-based bypass switches may provide a better solution in terms of high fault current handling capabilities and lower on-state losses compared to IGBT-based switches [45]. On the other hand, ac faults could affect the operation of DTC and CDC-CFCs.

Although the results in this section provide an initial insight on the fault responses for the different types of CFCs, further work is necessary for detailed fault studies where frequency dependent models are employed to represent dc lines.

D. A BRIEF DISCUSSION ON CFC TOPOLOGIES

As power flow exchange in DTC and CDC-CFCs occurs between ac and dc points, an ac connection to power up the devices is required—with major cost implications [17]. Such a shortcoming may be relieved by employing a 2B-CFC as it is powered inside the dc grid; thus achieving power flow control through a power exchange between dc points.

A 2B-CFC transfers power between two or more electrically coupled dc nodes. In the presence of two dc lines, failure of either line would make the CFC inactive and it should be bypassed. For dc networks employing busbars with more than two dc lines, multi-port CFCs may be installed to increase the control flexibility and to eliminate contingencies arising from the failure of a single or multiple ports [36]. For instance, a multi-port CFC with n ports (with each port being connected to a dc line) could remain operational as long as the total number of failed ports (or lines) is less than or equal to $n-2$.

CFCs are low power rated devices with few solid state modules. Due to cost implications, these devices will be most likely equipped with a single redundant module. Failure of multiple modules will take the CFC out of service. In particular, ac powered CFCs configurations have less reliability as they can be affected by faults on the ac side of the system; however, their failure will have a minimum impact on the dc grid.

V. EXPERIMENTAL VALIDATION

Simulation results have shown that the 2B-CFC provides the best solution for current control in a meshed dc grid. For completeness, the performance of this device is experimentally validated in this section.

A. TEST-RIG CONFIGURATION

The three-terminal MTDC experimental test-rig in Figure 23 is used to study the impact of the CFC on dc grid performance. It comprises two-level VSCs arranged in a symmetrical monopole configuration and rated at ±125 V and 2 kW. On the converter valve sides, a 140 V ac voltage is established through step-down autotransformers, with the primary sides being connected to a 415 V ac power supply. A DS1005 dSPACE system is used to provide real-time control of the VSCs and the CFC. The dc line and converter parameters are provided in the Appendix. CFC H-bridge

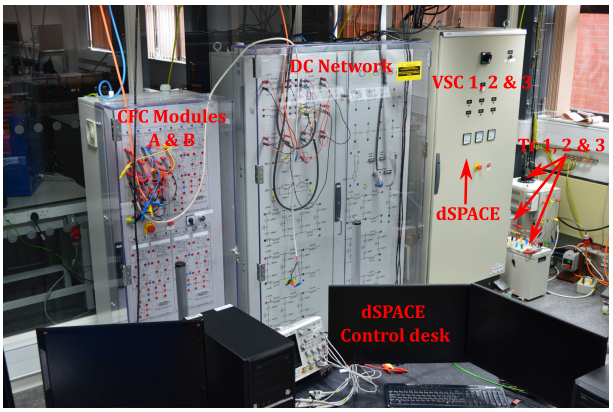

FIGURE 23. HVDC test-rig with embedded CFC.

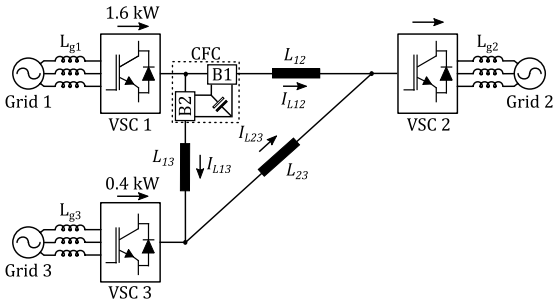

FIGURE 24. Three-terminal MTDC grid with embedded 2B-CFC.

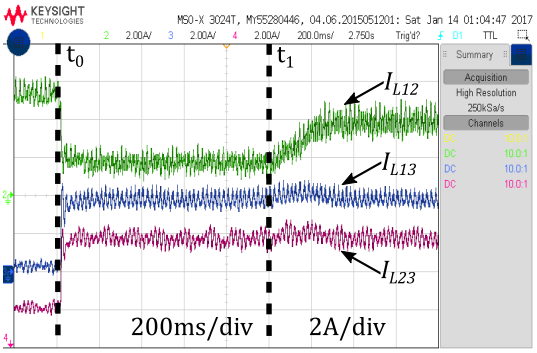

FIGURE 25. DC grid current profile.

modules B1 and B2 are installed in series with lines L_{12} and L_{13} (see Figure 24).

The master-slave control scheme described in Section III has been adopted. Converters 1 and 3 operate in a constant power mode with set points of 1.6 and 0.6 kW, respectively, whereas Converter 2 maintains a constant dc voltage.

B. RESULTS AND ANALYSIS

Figures 25 and 26 show the dc grid response during the transition from bypass operation to line current control. Initially, the CFC's H-bridge modules are bypassed through B_{SW1} and B_{SW2}. At $t_0 = 2$ s, the bypass switches are blocked and switches S_{W2} of bridge B1 and S_{W1} of B2 are modulated to control the CFC capacitor voltage V_C at 5 V and line current I_{L13} at 4 A. To assess the robustness of the control system,

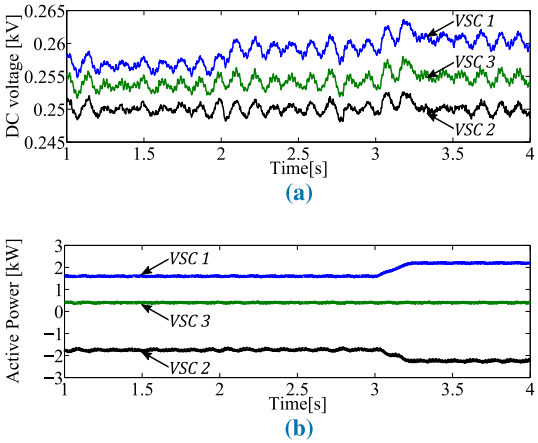

FIGURE 26. Test-rig response: (a) VSC voltages; (b) VSC power.

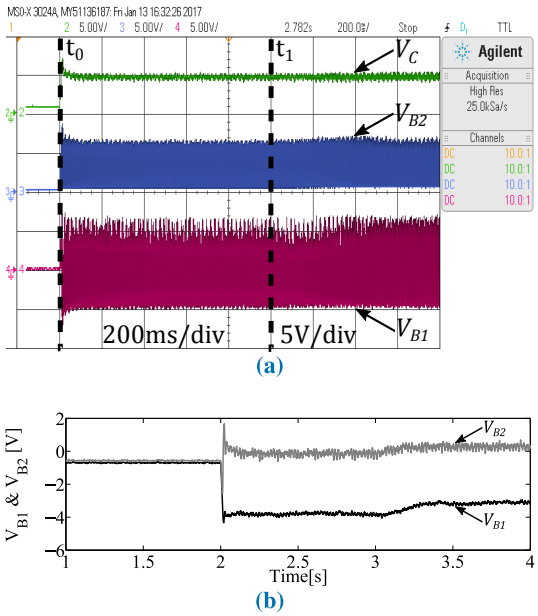

FIGURE 27. CFC dynamics: (a) output (bridges and capacitor) voltages; (b) mean voltage.

a positive ramp power change of 0.6 kW is applied through VSC 1 at $t_1 = 3$ s. Following the ramp change, I_{L13} is maintained at 4 A whereas I_{L12} has increased to 4 A.

The CFC voltage profile is shown in Fig. 27. The required current reduction on line L_{13} is achieved by inserting (mean) dc voltages V_{B1} and V_{B2} in series with L_{12} and L_{13}. Following the power change, V_{B1} decreases and V_{B2} increases as a result of a higher line resistance between VSCs 1 and 3 compared to that between VSCs 1 and 2, V_{B1} and V_{B2}.

It should be highlighted that the forward voltage drop on a semiconductor switch is a big concern in the development of scaled series devices as it significantly affects the current flow between nodes. To improve this issue, MOSFETs could be employed as they exhibit a lower forward voltage drop and power losses compared to IGBTs. The scaled CFC has exhibited a power loss of 20 W (1.25% of the system power rating). On the other hand, the full-scale CFC would exhibit a

power loss of 0.004% only. Switching and conduction losses on power semiconductor switches do not decrease proportionally with the system power rating. According to [17], a maximum of two diodes are inserted into the conduction path during the capacitor charging mode. The typical source-drain voltage of a MOSFET PSMN3R8-100BS is around 0.8 V. Thus, the instantaneous conduction losses during the charge mode are around 12.8 W. If these considerations are taken into account, it can be concluded that the losses exhibited by the CFC are acceptable.

VI. CONCLUSIONS

Power flows can be regulated in an MTDC grid using a CFC—a low power-rated power electronics controlled device. This enables a power transfer either between ac/dc or dc nodes. This paper has evaluated three series-connected CFC topologies. Simulation results show that regardless of the adopted configuration the controllability of the MTDC grid may be increased by a CFC.

Results show that all CFCs exhibit a similar range of dc line current controllability for the same output voltage rating; however, the device's placement within the MTDC grid could affect its controllability. Although the installation of multiple devices within the MTDC grid would relieve this issue, the use of multiple DTC and CDC-CFC devices could not be economically feasible. In contrast, a grid could afford multiple 2B-CFCs due to their lower cost and footprint.

The protection of CFCs is determined by the response time of the DCCBs and bypass switches. All CFCs have showed a similar level of vulnerability under the dc fault. A faster protection system is inevitable to protect the devices against any overvoltage and overcurrent conditions.

A small-scale 2B-CFC prototype has been developed to analyze the impact of a series CFC on dc grid performance. An experimental HVDC test-rig has been used to validate the concept. Experimental results confirm that a small CFC device can effectively control current distribution in a higher rated dc grid. The harmonic contents on dc line currents due to CFC switching can be reduced by either increasing the switching frequency or by installing passive filters.

APPENDIX
CONTROLLER GAINS

The PI controllers are represented in the form: $K(s) = K_p + K_i/s$.

Two-level VSCs: Current: $K_p = 0.98$, $K_i = 5$. DC voltage: $K_p = 0.048$, $K_i = 0.549$. Reactive power: $K_p = 0.15\times10^{-4}$, $K_i = 0.102$.

DTC-CFC: DC line current: $K_p = 2.027$, $K_i = 192.25$. CFC voltage: $K_p = 1.71\times10^{-3}$, $K_i = 1.4258$. Circulating current: $K_p = 21.798\times10^{-3}$, $K_i = 12.11$. *CDC-CFC*: DC line current: $K_p = 1.26$, $K_i = 174.02$. CFC voltage: $K_p = 5.37\times10^{-4}$, $K_i = 0.726$. *2B-CFC*: DC line current: $K_p = 0.031\times10^{-3}$, $K_i = 136.27\times10^{-3}$. Capacitor voltage: $K_p = 1.02\times10^{-3}$, $K_i = 99\times10^{-3}$.

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