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Repeater Insertion to Reduce Delay and Power in Copper and Carbon Nanotube-Based Nanointerconnects

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ABSTRACT Optimal repeater designs are performed for Cu and carbon nanotube (CNT)-based nanointerconnects to reduce the delay and power dissipation. The effects of inductance and metal-CNT contact resistance are treated appropriately. In this paper, the circuit parameters are calculated analytically, while they can be extracted experimentally for a specific foundry at a specific technology node. The particle swarm optimization (PSO) technique is employed to numerically calculate the optimal repeater size and the optimal number of repeaters in the Cu and CNT-based nanointerconnects. The results are verified against the analytical and genetic algorithm results. To facilitate CAD design, the machine-learning neural network (NN) is adopted. The data obtained using the PSO algorithm are used to train the NN and the feasibility of the NN is investigated and validated.

INDEX TERMS Carbon nanotube, copper, nanointerconnect, neural network, particle swarm optimization, repeater insertion, time delay, power dissipation.

I. INTRODUCTION

As the CMOS technology continues to evolve, the IC feature-size continues to shrink, while the IC chip sizes continue to increase due to incorporation of additional functionalities [1], [2]. Unlike the transistor scaling, the scaled interconnects suffer from severely increased time delay, which has become a dominant limitation on performance in today's very large scale integration (VLSI) chip designs. More importantly, according to the ITRS prediction, the current density will soon exceed the maximum ampacity of the traditional copper (Cu) interconnects in the near future [3].

In recent years, various technologies, including innovative conductive materials, architectures, and algorithm optimization, have been introduced for the interconnect applications [4]–[8]. For example, as the effective conductive area of the nanoscale Cu interconnect is dramatically limited, two-dimensional (2D) materials have been proposed as potential diffusion barrier layer for Cu/low- k interconnects

due to their atomically thin properties [9]–[11]. Moreover, carbon nanotube (CNT), which possesses many unique physical properties, has been considered as a promising alternative conductor in the nanoscale ICs [4]. Depending on the number of graphene sheets, CNT can be classified as single-walled CNT (SWCNT) and multi-walled CNT (MWCNT). A SWCNT has only one graphene sheet rolled into cylinder with diameter ranging from 0.4 nm to 4 nm, while an MWCNT can be viewed as a coaxial assembly of cylinders of SWCNTs [12], [13]. To date, numerous efforts have been devoted to modeling, fabrication, and reliability evaluation of the CNT interconnects [14]–[20]. It has been shown that the CNT interconnects have superior electrical performance over their Cu counterparts.

On the other hand, to improve the interconnect performance, the insertion of repeaters is always employed in the design of high-performance ICs [21]. By solving the differential equations, analytical formulas of the optimal repeater size

and number were derived in [22]. Furthermore, the repeater insertion methodologies in the SWCNT bundle and the MWCNT interconnects were studied in [23] and [24], respectively. However, as there exist contact resistances between the metal electrodes and CNTs, each inserted repeater in CNT interconnect would introduce new contact resistances, which surely degrade the interconnect performance [25]. Based on the multivariable curve fitting technique, the closed-form expressions of the optimal repeater size and number were developed in the previous work [26]. It was demonstrated that neglecting the contact resistance leads to significant error in estimation of the optimal repeater size and number in the CNT interconnects. However, the delay-minimal repeater design methodology may lead to overestimation of the repeater number, thereby resulting in excessive power dissipation. To this end, [27] and [28] developed power-optimal repeater insertion methodologies, but they have not taken into account the inductance effect. It is challenging to derive closed-form expressions for the optimal repeater design in an *RLC* interconnect [29], not to mention considering the influence of metal-CNT contact resistance.

To address this issue, a model is developed in this study, where the input variables include the interconnect width, length, and contact resistance at specific technology nodes. Through the particle swarm optimization (PSO) simulations of nanointerconnects [30], a database is created, where the outputs are represented by the optimal repeater size and the optimal number of repeaters. The database is used as input and output to train a machine-learning algorithm to create a mapping between the geometrical parameters and the optimal repeater designs. The rest of this paper is organized as follows. Section II introduces the electrical model of the Cu and CNT-based nanointerconnects. The PSO algorithm is outlined in Section III, with the simulated results validated by the analytical results. In Section IV, the machine-learning methodology is reviewed and applied to map the interconnect parameters to the optimal repeater designs. Conclusions are finally drawn in Section V.

II. INTERCONNECT MODEL

In this study, a typical interconnect structure is considered, as shown in Fig. 1(a) and (b), where R_d and C_d are the driver resistance and capacitance respectively, and C_l is the load capacitance. In Fig. 1, R_{pul} , L_{pul} , and C_{pul} are the per-unit-length (p.u.l.) resistance, inductance, and capacitance of the interconnect, respectively, and R_c denotes the contact resistance. For a specific technology node, the interconnect parameters, including width W , height H , spacing S , inter-layer dielectric (ILD) thickness T , and effective dielectric constant of the surrounding dielectric ϵ_r , are adopted from the ITRS projection and listed in Table 1 [3].

In practical applications, the circuit parameters can be obtained experimentally for a specific foundry process at a specific technology node. In this study, these parameters are calculated analytically.

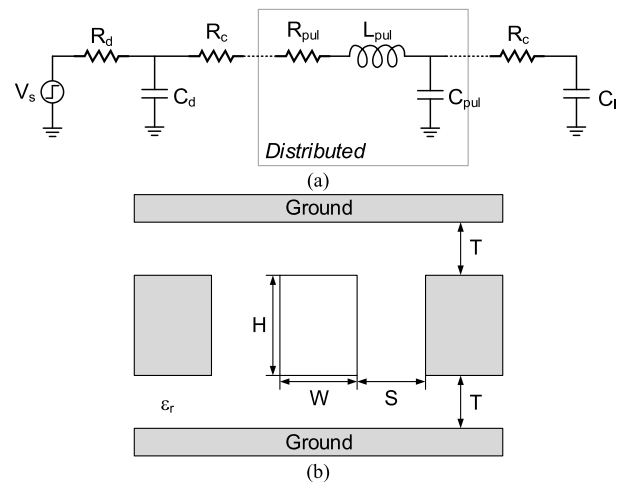


FIGURE 1. (a) Equivalent circuit model of the driver-interconnect-load (DIL) system. (b) Cross section of a typical interconnect configuration in advanced IC designs.

TABLE 1. Global interconnect parameters adopted from the ITRS [3].

| Technology Node | | 14 nm | 7 nm |
|--|-----------------------------|---------------------|---------------------|
| Interconnect width W | | 21.5 nm – 1 μ m | 10.5 nm – 1 μ m |
| Wire aspect ratio (H/W) | | 2.34 | 2.4 |
| ILD aspect ratio (T/W) | | 1.5 | 1.5 |
| Effective dielectric constant ϵ_r | | 2.08 | 1.65 |
| Minimum-sized gate | Driver resistance R_{d0} | 30.3 k Ω | 69.7 k Ω |
| | Driver capacitance C_{d0} | 0.22 fF | 0.13 fF |
| | Load capacitance C_{l0} | 0.15 fF | 0.06 fF |

A. NANOSCALE CU

With the scaling down of the interconnect dimensions, the electron scatterings from the surface and grain boundary become comparable to the electron bulk scattering, thereby leading to a dramatic rise in the Cu resistivity. Moreover, the barrier layer, which is used to prevent atom diffusion into the dielectric, cannot scale rapidly with the interconnect dimensions, and thus increasingly occupies higher fraction of the interconnect cross section area. Here, the barrier thickness is denoted as T_b , and the effective interconnect width and height are $W_{Cu}(= W - 2T_b)$ and $H_{Cu}(= H - 2T_b)$, respectively.

Based on the Fuchs-Sondheimer model and the Mayadas-Shatzkes model, the effective resistivity of the nanoscale Cu interconnects can be given as [31]

$$\rho_{Cu} = \rho_0 \left\{ \frac{1/3}{1/3 - \alpha/2 + \alpha^2 - \alpha^3 \ln(1 + 1/\alpha)} + \frac{3}{8} C (1 - p_{Cu}) \frac{1 + AR}{AR} \frac{\lambda_{Cu}}{W_{Cu}} \right\} \quad (1)$$

with

$$C = 1.2, \quad \alpha = \lambda_{Cu} R_g / (d_g (1 - R_g))$$

where $\rho_0 = 2.04 \mu\Omega \cdot cm$ is the bulk resistivity, $\lambda_{Cu} = 37.3nm$ is the Cu mean free path (MFP), $R_g = 0.22$ is reflectivity coefficient at grain boundaries, $p_{Cu} = 0.41$ is the

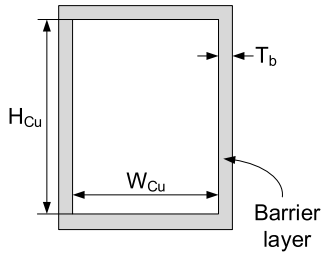


FIGURE 2. Schematic of a Cu interconnect.

specularity parameter of the Cu surface, $AR = H_{Cu}/W_{Cu}$ is the aspect ratio, and d_g is the average distance between grain boundaries, which is set as W_{Cu} [31]. Then, the p.u.l. resistance of the nanoscale Cu interconnect is calculated by $R_{pul} = \rho_{Cu}l / (W_{Cu}H_{Cu})$. In the case of the Cu interconnects, the contact resistance R_c is set as 0.

The p.u.l. capacitance C_{pul} can be extracted using a full-wave electromagnetic simulator (e.g., ANSYS Maxwell). As the capacitance is kept almost unchanged with the increasing width in the case of keeping the wire and ILD aspect ratios constant, C_{pul} is set as $149.4\text{pF}/\mu\text{m}$ and $120.3\text{pF}/\mu\text{m}$ at the 14 nm and 7 nm technology nodes, respectively. Accordingly, the p.u.l. inductance can be calculated by $L_{pul} = \mu_0\epsilon_0\epsilon_r / C_{pul}$.

B. SWCNT BUNDLE

Fig. 3(a) shows the cross-sectional view of a densely packed SWCNT bundle interconnect. In this figure, the SWCNT diameter is denoted as D , and the spacing between adjacent SWCNTs is $\delta = 0.34\text{nm}$, i.e., van der Waal’s gap. The number of the metallic SWCNTs in the bundle can be calculated as [15]

$$N = Fm \cdot \left(N_w N_h - \text{Inter} \left[\frac{N_h}{2} \right] \right) \tag{2}$$

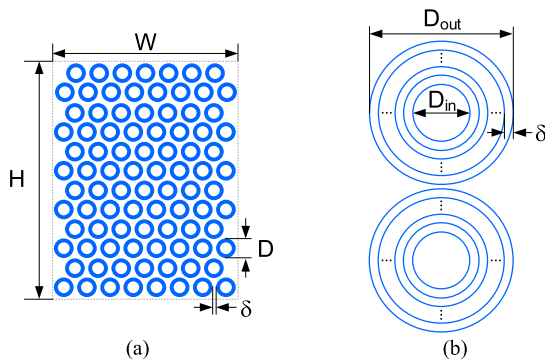


FIGURE 3. Cross-sectional views of (a) SWCNT bundle interconnect and (b) MWCNT interconnect.

where

$$N_w = \text{Inter} \left[\frac{W - D}{D + \delta} \right] + 1 \tag{3}$$

$$N_h = \text{Inter} \left[\frac{2}{\sqrt{3}} \frac{H - D}{D + \delta} \right] + 1 \tag{4}$$

$\text{Inter}[\cdot]$ denotes that only the integer part is taken, and Fm is the fraction of metallic SWCNTs in the bundle. The contact resistance of the SWCNT bundle interconnect is given by

$$R_c = \frac{1}{2N} \left(R_{mc} + \frac{R_Q}{N_{ch}} \right) \tag{5}$$

where $R_Q = h / (2e^2) = 12.9\text{k}\Omega$ is the quantum contact resistance, h is the Planck’s constant, e is the electron charge, $N_{ch} = 2$ is the number of conducting channels for an isolated metallic SWCNT, and R_{mc} is the imperfect contact resistance per tube that highly depends on the fabrication process. The p.u.l. resistance of the SWCNT bundle interconnect is given by

$$R_{pul} = \frac{R_Q}{\lambda_{SWCNT}} \tag{6}$$

where $\lambda_{SWCNT} = 1000D$ is the effective MFP of the SWCNT.

As indicated in the previous study [14], the electrostatic capacitance of the SWCNT bundle is almost the same as that of its Cu counterpart. The quantum capacitance is much larger than the electrostatic one, and therefore can be neglected. The p.u.l. inductance of the SWCNT bundle interconnect can be calculated by

$$L_{pul} = L_K + L_m \tag{7}$$

where $L_K = R_Q / (2v_F N N_{ch})$ and $L_m = \mu_0\epsilon_0\epsilon_r / C_{pul}$ are the kinetic inductance and magnetic inductance, respectively, and $v_F = 8 \times 10^5\text{m/s}$ is the Fermi velocity of CNTs.

C. MWCNT

The cross sectional view of the MWCNT interconnect is illustrated in Fig. 3(b). The aspect ratio $AR(= H/W)$ of the MWCNT interconnect is fixed at 2. This is, two MWCNTs are placed in parallel. As mentioned earlier, an MWCNT can be viewed as a coaxial assembly of cylinders of SWCNTs. The outermost and innermost diameters of the MWCNT are denoted as D_{out} and D_{in} , respectively, and the spacing between adjacent shells is δ . The number of shells in an MWCNT can be calculated as $N = 1 + \text{Inter} \left[(D_{out} - D_{in}) / (2\delta) \right]$, and the diameter of the n th shell in the MWCNT is $D_n = D_{in} + 2(n - 1)\delta$.

According to the pervious study [13], an MWCNT can be modeled as an equivalent single-conductor conductor transmission line model. The contact resistance of the MWCNT interconnect shown in Fig. 3(b) is given as

$$R_c = \frac{1}{4} \left[\sum_{n=1}^N \left(R_{mc} + \frac{R_Q}{N_{ch,n}} \right)^{-1} \right]^{-1} \tag{8}$$

where $N_{ch,n}$ is number of conducting channels of the n th shell in the MWCNT. $N_{ch,n}$ is dependent with the shell diameter, and can be expressed as [32]

$$N_{ch,n} = \begin{cases} 2/3, & D_n < 6 \text{ nm} \\ aD_n + b, & D_n > 6 \text{ nm} \end{cases} \tag{9}$$

where $a = 0.0612\text{nm}^{-1}$ and $b = 0.425$. The p.u.l. resistance of the MWCNT interconnect can be calculated by

$$R_{pul} = \frac{R_Q}{2} \left(\sum_{n=1}^N \lambda_n N_{ch,n} \right)^{-1} \quad (10)$$

where $\lambda_n = 1000D_n$ is the effective MFP of the n th shell in the MWCNT.

Similar to the SWCNT case, the quantum capacitance of the MWCNT can be neglected, and the electrostatic one is extracted by using the full wave electromagnetic simulator. Note that the MWCNT interconnect possesses smaller electrostatic capacitance than the Cu counterpart, which is attributed to their different configurations. In this study, the p.u.l. capacitance of the MWCNT interconnect is $129.12\text{pF}/\mu\text{m}$ and $102.24\text{pF}/\mu\text{m}$ at the 14 nm and 7 nm technology nodes, respectively. The kinetic inductance of the MWCNT interconnect is given as

$$L_K = \frac{R_Q}{2} \left(\sum_{n=1}^N 2v_F N_{ch,n} \right)^{-1} \quad (11)$$

The p.u.l. inductance of the MWCNT interconnect is then calculated by $L_{pul} = L_K + L_M$, where $L_M = \mu_0 \epsilon_0 \epsilon_r / C_{pul}$ is the magnetic inductance.

The repeaters are usually employed in long interconnects to improve the electrical performance. An interconnect with the insertion of equispaced repeaters is shown in Fig. 4. The interconnect is divided into k segments, and each segment has a length of l/k . The repeaters are h times the minimum size, with the driver resistance R_{d0}/h , driver capacitance hC_{d0} , and load capacitance hC_{l0} . The 50% time delay of one segment can be calculated by [24]

$$T_s = \left(1.48\xi + e^{-2.9\xi^{1.35}} \right) \sqrt{L_{pul} \frac{l}{k} \left(C_{pul} \frac{l}{k} + hC_{l0} \right)} \quad (12)$$

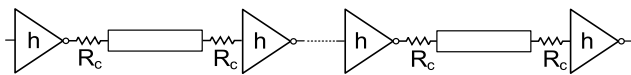


FIGURE 4. Repeater insertion in a long global interconnect of length L .

with

$$\xi = \frac{R_t}{2} \sqrt{\frac{C_{pul} R_T + C_T + R_T C_T (1 + C_{d0}/C_{l0}) + 0.5}{L_{pul} \sqrt{1 + C_T}}} \quad (13)$$

where $R_T = R_{d0}/(hR_t)$, $C_T = hC_{l0}/C_t$, $R_t = R_{pul}l/k + 2R_c$, and $C_t = C_{pul}l/k$. The total time delay is $T_{total} = kT_s$. The energy dissipation P_s consumed by one segment can be approximated as [28]

$$P_s = \left(C_{pul} \frac{l}{k} + h(C_{d0} + C_{l0}) \right) V_{dd}^2 \quad (14)$$

The total power dissipation can be calculated by $P_{total} = kP_s$. The figure-of-merit (FoM) for global interconnect with repeater insertion has the following property:

$$F = (P_{total})^p \cdot (T_{total})^q \quad (15)$$

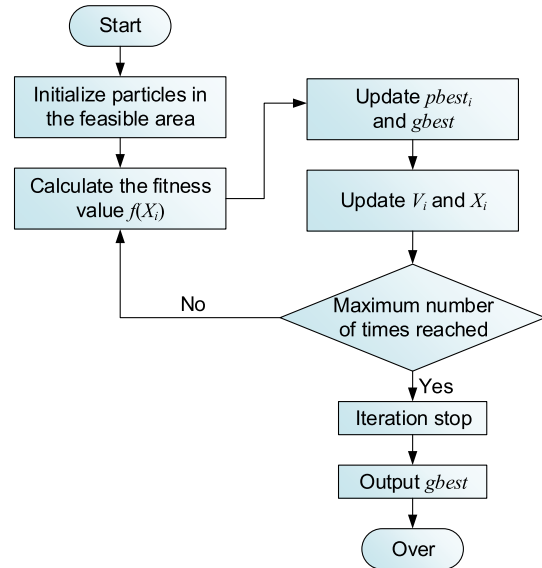


FIGURE 5. Flowchart of the PSO algorithm.

where p and q are weighting factors that can be tuned accordingly. For delay- and power-optimal repeater designs, $\{p, q\}$ are $\{0, 1\}$ and $\{1, 0\}$, respectively. For simplicity, both p and q are set as 1 in this study.

III. PARTICLE SWAM OPTIMIZATION

A. PSO DESCRIPTION

The PSO algorithm is a stochastic procedure that derives from simulation of bird population and fish foraging behavior. Similar to other group intelligence algorithms, the PSO algorithm realizes the search process in the space by mutual cooperation and competition among particles in the group to find the optimal position.

The mathematical description of the PSO algorithm is briefly reviewed as follows. The total number of particles in the swarm is $popsiz$, the dimension of the particle is m , and the termination condition of the algorithm (i.e., the maximum iteration number) is $maxiter$. The flight speed and the position of the i th particle at time t in the search space are defined as

$$V_i(t) = [V_{i1}(t), V_{i2}(t), \dots, V_{im}(t)]^T \quad (16)$$

$$X_i(t) = [X_{i1}(t), X_{i2}(t), \dots, X_{im}(t)]^T \quad (17)$$

and the individual extremum (i.e., the optimal solution that each individual particle has found by far) and the population extremum (i.e., the optimal solution that the entire swarm has ever found) of the i th particle at time t in the search space are

$$pbest_i(t) = [p_{i1}(t), p_{i2}(t), \dots, p_{im}(t)]^T \quad (18)$$

$$gbest(t) = [g_1(t), g_2(t), \dots, g_m(t)]^T \quad (19)$$

The update formulas for all particles in the search space can be expressed as [30]

$$V_{i+1}(t+1) = W_{ei}V_i(t) + c_1r_1(pbest_i(t) - X_i(t)) + c_2r_2(gbest(t) - X_i(t)) \quad (20)$$

$$X_{i+1}(t+1) = X_i(t) + V_{i+1}(t+1) \quad (21)$$

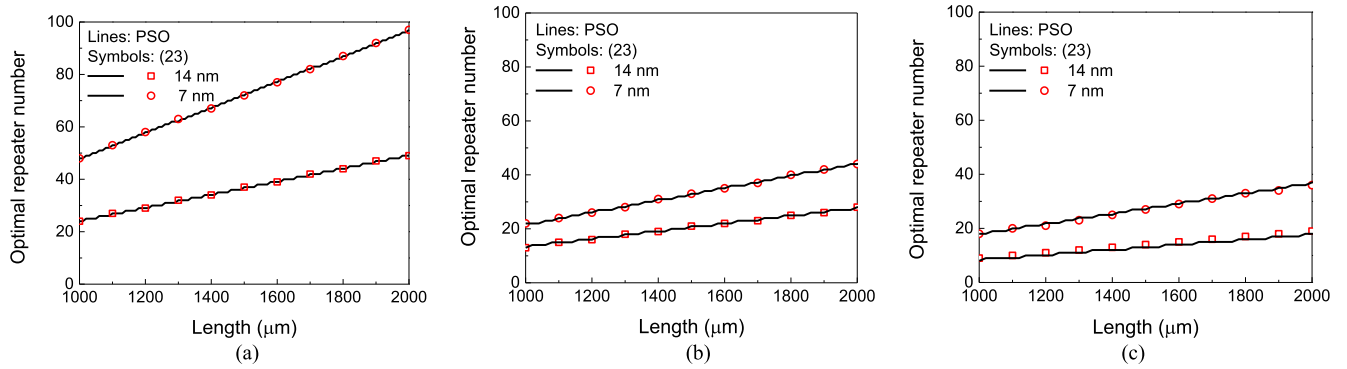


FIGURE 6. Optimal number of the repeaters in (a) Cu, (b) SWCNT bundle, and (c) MWCNT interconnects at the 14 nm and 7 nm technology nodes in the delay-optimal repeater designs.

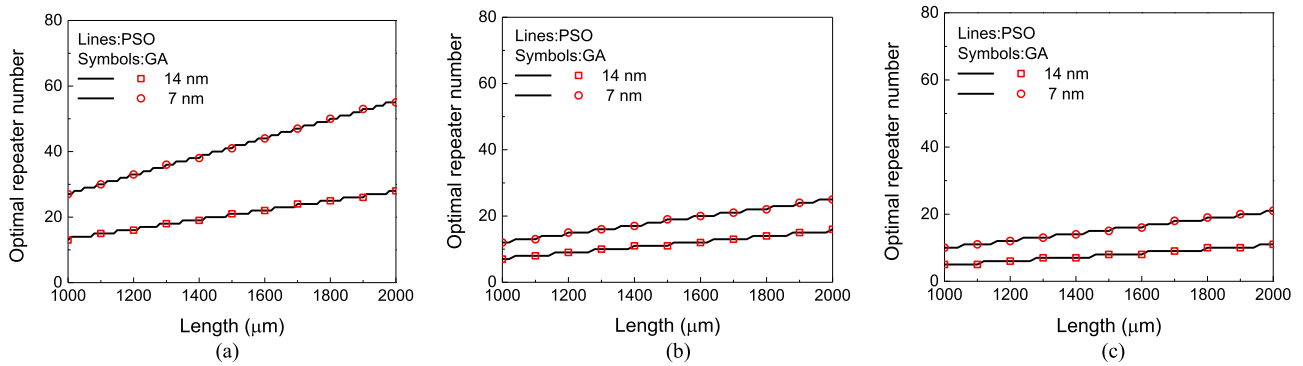


FIGURE 7. Optimal number of the repeaters in (a) Cu, (b) SWCNT bundle, and (c) MWCNT interconnects at the 14 nm and 7 nm technology nodes in the PDP-optimal repeater designs.

where $W_{ei} = W_{max} - (W_{max} - W_{min}) \cdot iter / maxiter$ is the inertia weighting coefficient, which is important as it determines the speed of iteration. $iter$ denotes the current number of iteration. Here, W_{max} and W_{min} are set as 0.9 and 0.4, respectively. By adjusting W_{ei} , both the global and local search capabilities can be tuned. At the early stage of the PSO operation, a large W_{ei} can lead to a strong global search ability, while a small W_{ei} at the later stage can make the particle gradually converge to the global optimum. The implementation of such linearly-decreasing inertia weight method could control the global exploration and local exploitation abilities, thereby improving the speed of convergence and algorithm performance. c_1 and c_2 are the learning factors of the PSO algorithm, and they affect the self-learning ability and social learning ability of the particles. It is generally believed that a large c_1 causes all the particles to linger in local range too much, while a large c_2 causes the particles to fall into local extremum too early, thereby reducing the accuracy of the solution. r_1 and r_2 are the random numbers between [0, 1].

The flowchart of the PSO algorithm is outlined in Fig. 5. At the beginning, the parameters of the particle such as m , W_{ei} , c_1 , and c_2 , as well as a group of particles including the flight speed and the position information, are initialized. Here, m , c_1 and c_2 are set as 2, and $popsiz$ e and $maxiter$ are 50 and 1000, respectively. Then, the fitness value (i.e., the

function value) of each particle in the population is calculated. The fitness value of the i th particle and the best position of the swarm are set as the current individual extremum $pbest_i$ and the total extremum $gbest$, respectively. According to (20) and (21), the flight speed and position of the particles are updated. For all particles, the current position is compared to the best position found previously. If the current position is better, the individual optimal position $pbest_i$ is set as the position of the particle, and the global extrema of the group $gbest$ is then updated. Finally, the searching is stop until the termination condition is satisfied, and the desired result is output. Otherwise, the fitness value $f(X_i)$ is re-calculated to start the cycle over again.

B. VALIDATION

To verify the feasibility of the PSO algorithm in the optimal repeater designs in the Cu and CNT interconnects, the global interconnects are considered. Here, the interconnect widths (the barrier thickness) are set as 21.5 nm (0.9 nm) and 10.5 nm (0.3 nm) at the 14 nm and 7 nm technology nodes, respectively, with other parameters adopted from Table 1. The SWCNT diameter is $D = 1$ nm, and the fraction of the metallic SWCNTs in the bundle is $Fm = 1/3$. The innermost diameter of the MWCNT is assumed as half of its outermost diameter, i.e., $D_{in} = D_{out}/2$.

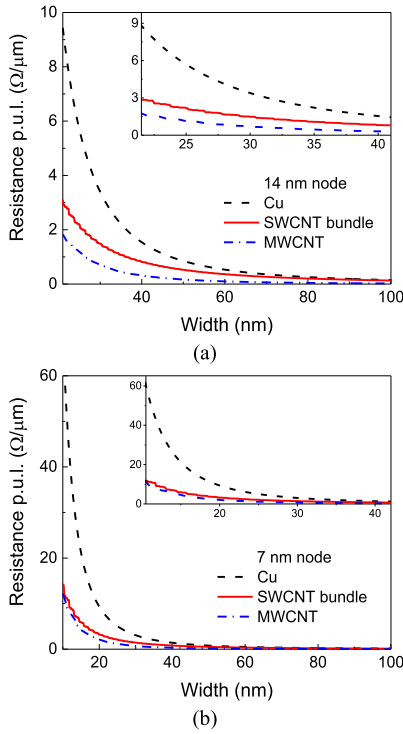


FIGURE 8. P.u.l. resistance of the Cu and CNT interconnects at the (a) 14 nm and (b) 7 nm technology nodes.

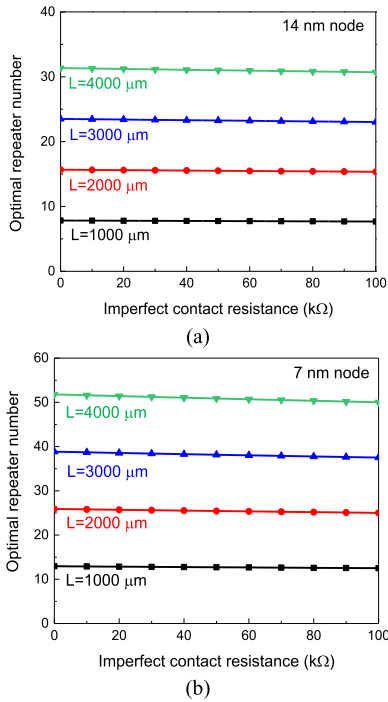


FIGURE 9. Optimal number of repeaters in SWCNT bundle interconnects with different lengths at the (a) 14 nm and (b) 7 nm technology nodes.

At first, the delay-optimal repeater designs (i.e., $p = 0$ and $q = 1$) are studied using the PSO algorithm. For simplicity, the contact resistances in the CNT interconnects are set as zero in the simulations. The optimal repeater size and number

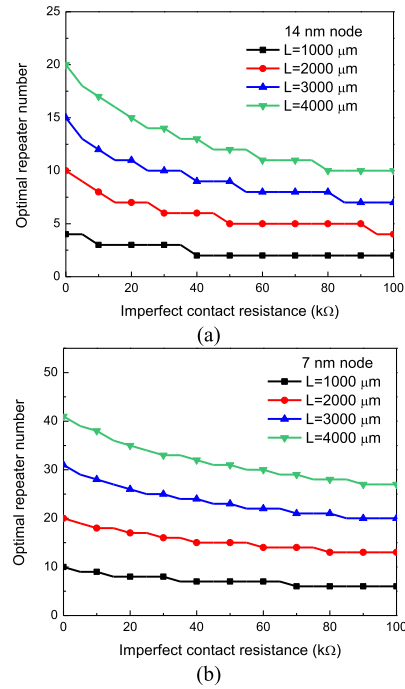


FIGURE 10. Optimal number of repeaters in MWCNT interconnects with different lengths at the (a) 14 nm and (b) 7 nm technology nodes.

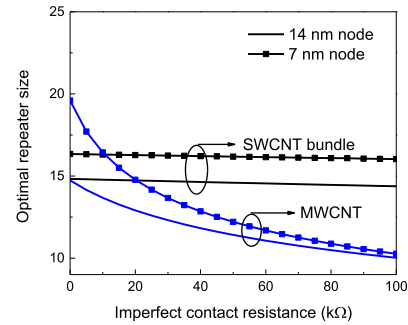


FIGURE 11. Optimal repeater size versus imperfect contact resistance for CNT interconnects at the 14 nm and 7 nm technology nodes.

can be calculated by [22], [24]

$$h_{opt} = \sqrt{\frac{R_{d0}C_t}{R_t C_{l0}}} \frac{1}{\left[1 + 0.18 (T_{L/R})^3\right]^{0.26}} \quad (22)$$

$$n_{opt} = \text{Inter} \left[\sqrt{\frac{R_t C_t}{2R_{d0} (R_{d0} + C_{l0})}} \frac{1}{\left[1 + 0.21 (T_{L/R})^3\right]^{0.28}} \right] \quad (23)$$

where

$$T_{L/R} = \sqrt{\frac{L_{pul}}{R_{pul} [R_{d0} (C_{d0} + C_{l0})]}} \quad (24)$$

As shown in Fig. 6, the numerical results obtained by using the PSO algorithm agree well with the analytical results.

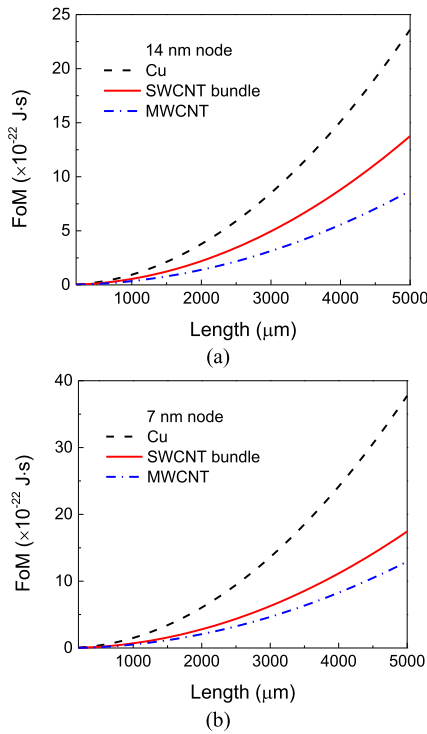


FIGURE 12. Optimized FoMs of the Cu and CNT interconnects with $R_{mc} = 0$ at the (a) 14 nm and (b) 7 nm technology nodes.

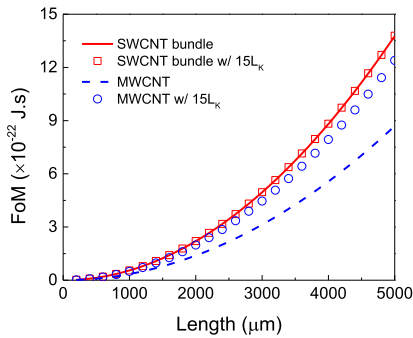


FIGURE 13. Optimized FoM of the CNT interconnects with $R_{mc} = 0$ at the 14 nm technology node with the original and 15 times values of the kinetic inductance.

The CNT interconnects possess smaller optimal number of the repeaters than the Cu counterparts, thereby consuming less power. Moreover, in either cases, with the technology node advanced, the optimal number of the repeaters increases. This is, the power dissipation becomes more significant in advanced technology nodes, and therefore requires special attention. Furthermore, the optimal repeater designs that aim at minimum power-delay product (PDP) are performed using the PSO algorithm, as shown in Fig. 7. Here, p and q are set as 1. The results from the PSO are compared with those from the genetic algorithm (GA). In Fig. 7, the solid lines denote the results from the PSO algorithm, whereas the symbols indicate the results from the GA scheme. With consideration of the power dissipation, the optimal number

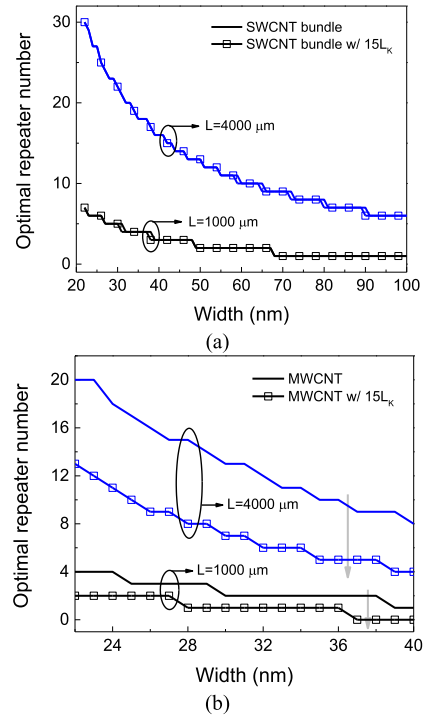


FIGURE 14. Optimal number of repeaters in the (a) SWCNT bundle and (b) MWCNT interconnects with $R_{mc} = 0$ at the 14 nm technology node with the original and 15 times values of the kinetic inductance.

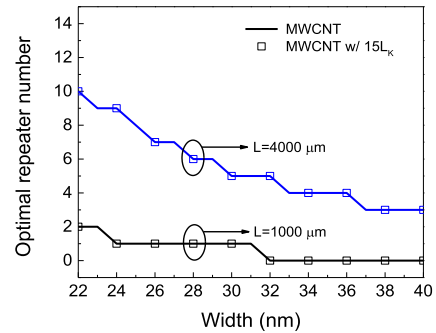


FIGURE 15. Optimal number of repeaters in MWCNT interconnect with $R_{mc} = 100\text{k}\Omega$ at the 14 nm technology node.

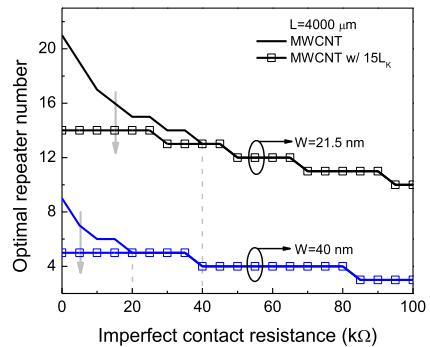


FIGURE 16. Optimal number of repeaters in MWCNT interconnect with length of $4000 \mu\text{m}$ at the 14 nm technology node.

of the repeaters becomes significantly smaller than those in the delay-optimal repeater designs for both Cu and CNT interconnects.

C. RESULTS AND DISCUSSION

According to the ITRS prediction, the width of global interconnect can vary from several tens of nanometers to one micrometer. Fig. 8 shows the p.u.l. resistance versus the width for the Cu and CNT interconnects at the 14 nm and 7 nm technology nodes. The jitter of the curves of the SWCNT bundle interconnect is because the number of SWCNTs in the bundle is an inconsistent function of the interconnect width (as given in (2)-(4)). To make it clear, the resistance curves in the range up to 40 nm width are plotted in the insets of Fig. 8. As illustrated in Fig. 8, the CNT interconnects exhibit superior performance over their Cu counterparts, but their advantages become less significant with the increasing width. As the technology node is advanced, the resistances of the SWCNT bundle interconnect become comparable with those of the MWCNT interconnects due to the reduced MFP of the MWCNTs.

To clarify the impact of imperfect contact resistance on the optimal repeater designs, Figs. 9 and 10 depict the optimal number of repeaters as a function of imperfect contact resistance for the SWCNT bundle and MWCNT interconnects, respectively. The interconnect width is set as the minimum value, and the other parameters are adopted from Table 1. With the increasing imperfect contact resistance, the optimal number of repeaters in the SWCNT bundle interconnect is kept almost unchanged, while it decreases in the MWCNT interconnect. Intuitively, this phenomenon can be explained as follows. As given in (5) and (8), the effective contact resistance of the SWCNT bundle depends on the number of metallic SWCNTs in the bundle, while it is determined by the shell number in the MWCNT interconnect. It is found that the number of metallic SWCNTs in the bundle is much larger than the shell number of the MWCNT interconnect with the same width. For instance, for the minimum-sized global interconnect at the 14 nm technology node, the number of metallic SWCNTs and the shell number of the MWCNTs are 222 and 64, respectively. In comparison with the SWCNT bundle interconnect, the MWCNT interconnect possesses a larger ratio between the contact resistance and the line resistance and is therefore more susceptible to the variation of the contact resistance (see Fig. 10). Moreover, Fig. 11 shows the optimal repeater size of the CNT interconnects as a function of the imperfect contact resistance. Similarly, with the increasing imperfect contact resistance, the optimal repeater size is almost unchanged in the SWCNT interconnects, while it significantly declines in the MWCNT interconnects.

Fig. 12 shows the optimized FoMs of the Cu and CNT interconnects at the 14 nm and 7 nm technology nodes. Here, the imperfect contact resistance is set as zero. It is demonstrated that the CNT interconnects can provide superior performances over their Cu counterpart. As shown in Fig. 7, MWCNT requires a minimal amount of repeaters, thereby saving the power consumption and giving it an edge in performance over the Cu and SWCNT bundle interconnects.

Furthermore, the impacts of the kinetic inductance on the optimal repeater designs of the CNT interconnects

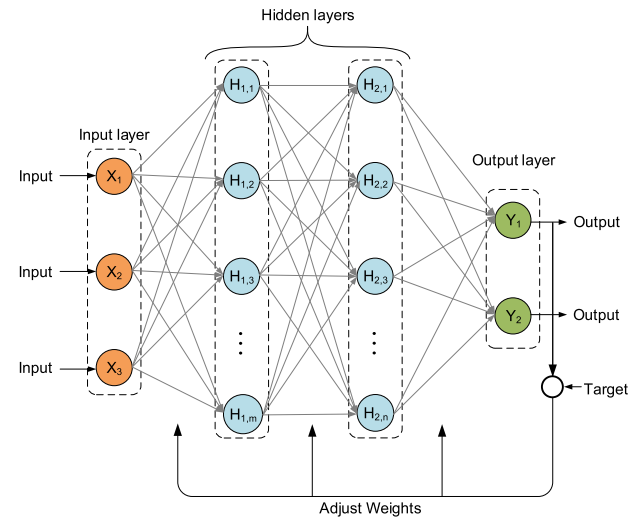


FIGURE 17. Schematic of the back propagation neural network.

are investigated. As indicated in [33], the measured value of the CNT kinetic inductance may be 15 times larger than its theoretical value. Fig. 13 shows the optimized FoMs of the SWCNT bundle and MWCNT interconnects with the different CNT kinetic inductances. As the CNT kinetic inductance rises to 15 times the initial value, the optimized FoM of the SWCNT bundle interconnect is unchanged, while it increases dramatically for the MWCNT. This is because the MWCNT has higher MFP and less number of conducting channels than the SWCNT bundle, and is therefore more susceptible to the variation of CNT kinetic inductance. Fig. 14 shows the optimal number of repeaters in the SWCNT bundle and MWCNT interconnects at the 14 nm technology node. The imperfect contact resistance is set as zero. It is evident that the optimal number of repeaters in the SWCNT bundle interconnect is free from the influence of the kinetic inductance variation, which is consistent with the finding in Fig. 13. However, the optimal number of repeaters in the MWCNT interconnect decreases significantly with the increasing kinetic inductance.

It is known that the influence of the inductance on the interconnect response tends to be trivial as the damping factor increases and the DIL system becomes overdamped [21], [22]. Therefore, as shown in Fig. 15, with R_{mc} increasing to 100 k Ω , the optimal repeater design in the MWCNT interconnect is no longer affected by variation of the kinetic inductance. Fig. 16 shows the optimal number of repeaters in the MWCNT interconnect with different interconnect widths. It can be seen that the influence of the kinetic inductance becomes negligible as the imperfect contact resistance approaches a certain value, which is smaller for larger interconnect width.

IV. MACHINE-LEARNING NEURAL NETWORK

A. NN DESCRIPTION

As more and more data and computing resources become available, machine learning is playing an increasingly

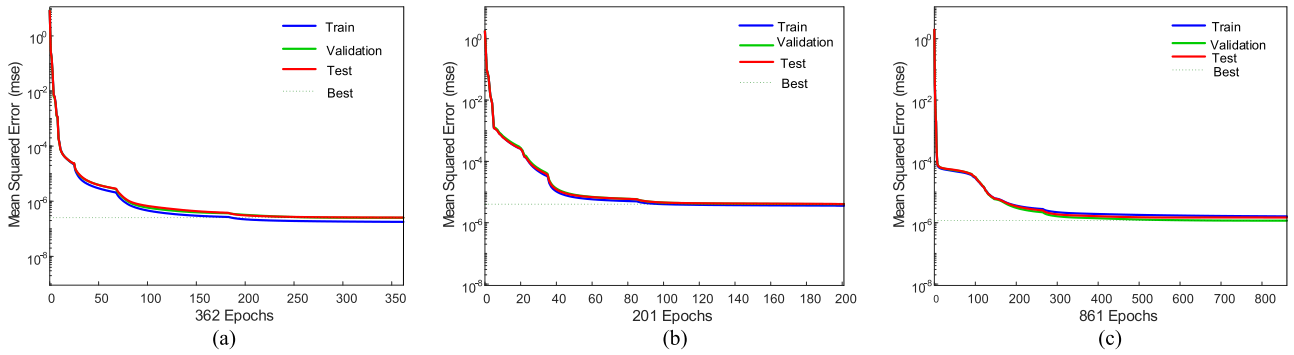


FIGURE 18. Squared error versus epoch curves for (a) Cu, (b) SWCNT bundle, and (c) MWCNT interconnects at the 14 nm technology node in the PDP-optimal repeater designs.

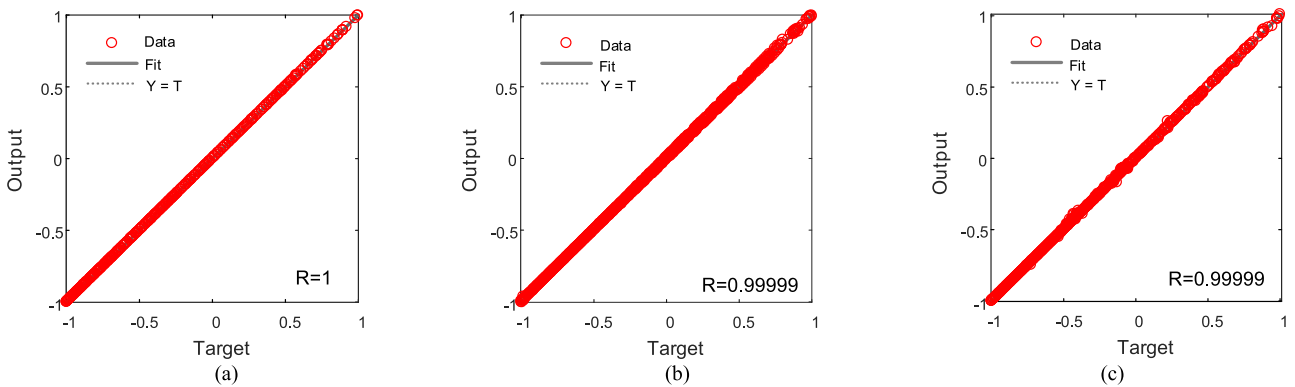


FIGURE 19. NN output versus target regression curves for (a) Cu, (b) SWCNT bundle, and (c) MWCNT interconnects at the 14 nm technology node in the PDP-optimal repeater designs.

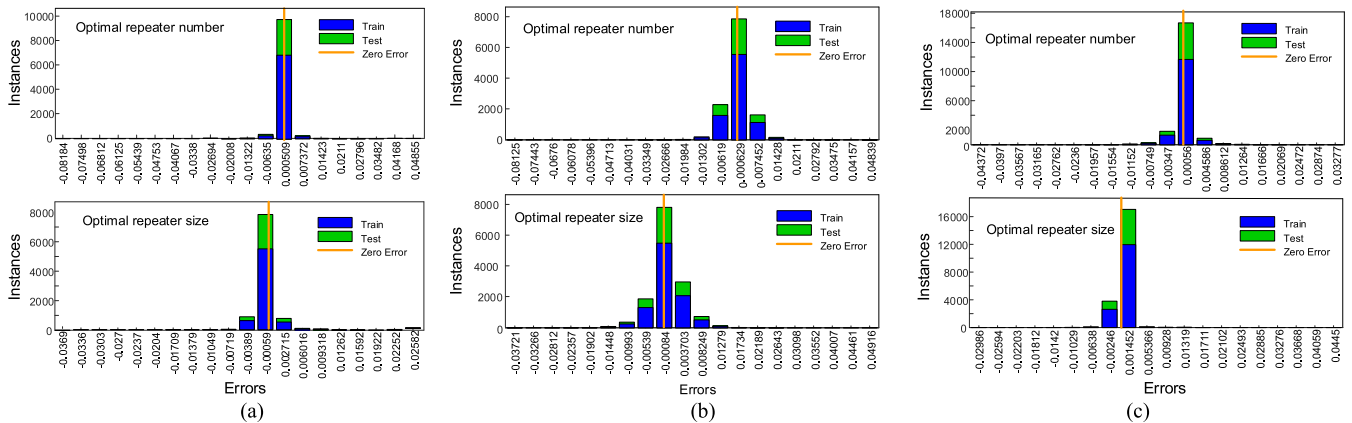


FIGURE 20. Relative errors between outputs and targets for (a) Cu, (b) SWCNT bundle, and (c) MWCNT interconnects at the 14 nm technology node in the PDP-optimal repeater designs.

significant role in various applications. Neural networks (NNs), a typical class of machine-learning algorithms, have recently gained attention as a fast and flexible vehicle to electronic designs [35]–[37].

NNs mimic the structure of human synapse connections to imitate the function of the brain. It consists of a number of interconnected nodes, and each node is a simple processing unit that responds to the weighted sum of its inputs received from other nodes [38]. As shown in Fig. 17, a two-layer

feedforward NN is trained using the back-propagation (BP) algorithm, and the numbers of nodes in these layers are denoted as m and n , respectively. In general, the more nodes used in each hidden layer, the more nonlinear the network can be, and consequently the more accurate the results could become.

In the BP NN shown in Fig. 17, the process of information forward propagation and error back propagation goes round and round. As the core phase of learning, adjusting the

weights is performed through training in which the network outputs match the desired targets approximately. The operation of the BP NN is briefly reviewed as follows. The inputs pass from the input layer to the hidden layer during the forward propagation phase. They are processed by the activation function, and then enter to the output layer. The error back propagation is used for updating the network parameters and minimizing the error function (i.e., the squared error between the outputs and desired targets). Such operation is performed recursively until the accuracy of the outputs meets the pre-set requirements. Here, the Levenberg-Marquardt (LM) algorithm, a nonlinear optimization technique that combines the advantages of both the Gauss-Newton method and the gradient descent method, is applied for training the network [39], [40]. To some extent, the implementation of the LM algorithm can overcome the drawback that training NN using gradient descent method converges slowly and is easy to fall into local minimum point.

B. TRAINING AND VALIDATION

In the data set used for training, the inputs consist of the interconnect width, the interconnect length, and the metal-CNT contact resistance. The corresponding output data, i.e., the optimal repeater size and the optimal number of repeaters, is obtained using the PSO simulations. It is worth noting that although the MWCNTs can always provide superior performance over the Cu counterparts (see Fig. 8), their diameters are limited in the real-world fabrications. Therefore, in establishment of the data set for training NNs, the upper bound of the width of the MWCNT interconnects is set as 40 nm, which can be changed according to the measurements.

In general, to reduce the mapping errors, it is necessary to use a large amount of data for training. In this study, the data set is captured by varying the interconnect width from the minimum value to 100 nm at a step of 1 nm and from 100 nm to 1 μm at a step of 50 nm. As demonstrated in Fig. 9, the influence of the imperfect contact resistance on the optimal repeater design can be neglected in the SWCNT bundle interconnect. Therefore, the imperfect contact resistance is set as zero in the NNs' training for the Cu and SWCNT bundle interconnects. However, for the MWCNTs, the imperfect contact resistance is varied from 0 to 100 k Ω at a step of 5 k Ω , thereby leading to a significantly larger training data set. Moreover, as normalization is a way to simplify calculations and to speed up the convergence of the training network, the data set in this study is normalized to the range [0, 1] by linearization. The numbers of the nodes of two hidden layers are $m = 40$ and $n = 15$, respectively. Here, 70% of the input data is used as the training set, and the rest is used as the test set.

Fig. 18 shows the numbers of iterations of the NNs to achieve convergence for the Cu and CNT interconnects at the 14 nm technology node. Here, the goal of mean square error (MSE) is set as 1×10^{-8} . The recursive process of the learning algorithm stops when the error cannot be reduced anymore. Furthermore, the comparison between the outputs

of the NNs and the desired targets are shown in Fig. 19. In this figures, the solid lines represent the best-fit linear regression line between the outputs and the targets, and the dashed lines are the perfect results (i.e., the outputs is equal to the targets). It can be seen from Fig. 19 that the solid and dashed lines completely overlap with each other, indicating good fit for the problems of the repeater insertion in the Cu and CNT interconnects. The R value, an indication of the correlation between the outputs and the targets, is close to 1, implying that there is an exact linear relationship between the outputs and the targets. Finally, the relative error between the NN outputs and the targets is shown in Fig. 20. It can be seen that the error of the most samples is closed to zero. Using the trained NN, the optimal number of repeaters and the optimal repeater size can be obtained readily. It can be seen in Fig. 21 that the data from the ML overlaid on the results from the PSO algorithm.

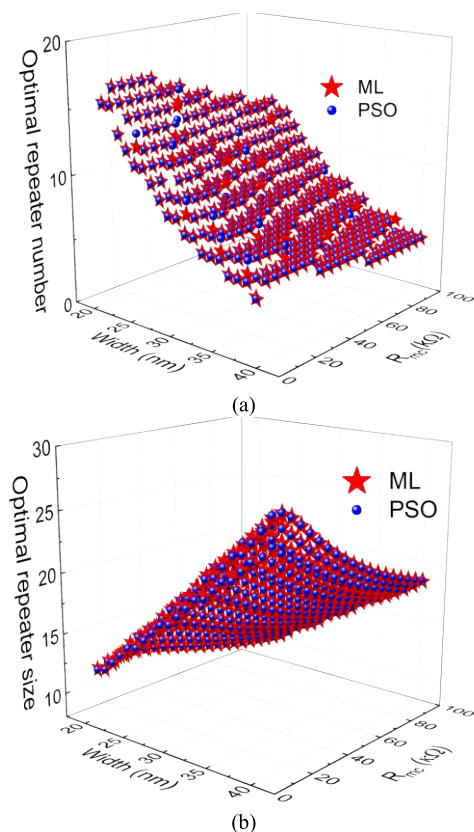


FIGURE 21. Optimal (a) number of repeaters and (b) optimal repeater size of MWCNT interconnects obtained using PSO algorithm and trained NN.

It is well known that NNs have unparalleled advantages in computational efficiency by predicting the optimum directly. This is, NNs require less simulation time than the conventional methods. More precisely, by using the PSO algorithm for handling tens of thousands of data items, the CPU times would exceed approximately 25 h, 25 h, and 55 h for the Cu, SWCNT bundle, and MWCNT interconnects, respectively. However, for the same data sets, the CPU times can be reduced to 4.34 s, 4.07 s, and 4.43 s by using the

trained NNs. Therefore, the implementation of the NNs can drastically save computational time, and is greatly beneficial to the design and optimization of IC layout in future carbon nanoelectronics [41], [42].

V. CONCLUSION

In this paper, the optimal repeater designs were performed for the Cu, SWCNT bundle, and MWCNT based nanointerconnects. Both the time delay and power dissipation were considered and treated appropriately. The PSO algorithm was developed to compute the optimal number of repeaters and the optimal repeater size. In practical applications, the circuit parameters can be obtained experimentally for a specific foundry process at a specific technology node. The effects of the metal-CNT contact resistance and the kinetic inductance on the optimal repeater designs were investigated in detail. It was found that the CNT interconnects have much smaller optimal number of repeaters than their Cu counterparts. As the SWCNT bundle possesses larger number of conducting channels, it is almost free of the influence of the imperfect contact resistance. However, the optimal number of repeaters in the MWCNT interconnect decreases with the increasing imperfect contact resistance. Similarly, the variation of the CNT kinetic inductance, which may be 15 times larger than its theoretical value, has negligible influence on the SWCNT bundle but significant influence on the MWCNT interconnect. However, as the imperfect contact resistance increases, the DIL system tends to overdamped, in which the influence of the kinetic inductance becomes trivial. Finally, the feasibility of the ML NN in optimal repeater designs of the Cu and CNT based nanointerconnects were discussed. It was demonstrated that the trained NNs can predict the optimal number of repeaters and the optimal repeater size rapidly and accurately. The proposed procedure can be applied to the optimal design of interconnect system in nano-CMOS and future nanocarbon-based ICs.

REFERENCES

- [1] J. A. Davis et al., "Interconnect limits on gigascale integration (GSI) in the 21st century," *Proc. IEEE*, vol. 89, no. 3, pp. 305–324, Mar. 2001.
- [2] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proc. IEEE*, vol. 89, no. 5, pp. 602–633, May 2001.
- [3] (2013). *International Technology Roadmap for Semiconductor*. Accessed: Jul. 1, 2017. [Online]. Available: <http://www.itrs2.net/>
- [4] H. Li, C. Xu, N. Srivastava, and K. Banerjee, "Carbon nanomaterials for next-generation interconnects and passives: Physics, status, and prospects," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1799–1821, Sep. 2009.
- [5] C. Pan and A. Naeemi, "A paradigm shift in local interconnect technology design in the era of nanoscale multigate and gate-all-around devices," *IEEE Electron Device Lett.*, vol. 36, no. 3, pp. 274–276, Mar. 2015.
- [6] W.-S. Zhao et al., "Vertical graphene nanoribbon interconnects at the end of the roadmap," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2632–2637, Jun. 2018.
- [7] E. K. Farahani and R. Sarvari, "Design of n-tier multilevel interconnect architectures by using carbon nanotube interconnects," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 10, pp. 2128–2134, Oct. 2015.
- [8] K. Moiseev, A. Kolodny, and S. Wimer, *Multi-Net Optimization of VLSI Interconnect*. New York, NY, USA: Springer, 2015.
- [9] W. S. Zhao, D. W. Wang, G. Wang, and W. Y. Yin, "Electrical modeling of on-chip Cu-graphene heterogeneous interconnects," *IEEE Electron Device Lett.*, vol. 36, no. 1, pp. 74–76, Jan. 2015.
- [10] Z.-H. Cheng et al., "Analysis of Cu-graphene interconnects," *IEEE Access*, vol. 6, pp. 53499–53508, 2018.
- [11] C.-L. Lo et al., "Studies of two-dimensional h-BN and MoS₂ for potential diffusion barrier application in copper interconnect technology," *NPJ 2D Mater. Appl.*, vol. 1, Dec. 2017, Art. no. 42.
- [12] H. Li, W.-Y. Yin, K. Banerjee, and J.-F. Mao, "Circuit modeling and performance analysis of multi-walled carbon nanotube interconnects," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1328–1337, Jun. 2008.
- [13] M. S. Sarto and A. Tamburrano, "Single-conductor transmission-line model of multiwall carbon nanotubes," *IEEE Trans. Nanotechnol.*, vol. 9, no. 1, pp. 82–92, Jan. 2010.
- [14] A. Naeemi and J. D. Meindl, "Design and performance modeling for single-walled carbon nanotubes as local, semiglobal, and global interconnects in gigascale integrated systems," *IEEE Trans. Electron Devices*, vol. 54, no. 1, pp. 26–37, Jan. 2007.
- [15] N. Srivastava, L. Hong, F. Kreupl, and K. Banerjee, "On the applicability of single-walled carbon nanotubes as vlsi interconnects," *IEEE Trans. Nanotechnol.*, vol. 8, no. 4, pp. 542–559, Jul. 2009.
- [16] M. K. Majumder, B. K. Kaushik, and S. K. Manhas, "Analysis of delay and dynamic crosstalk in bundled carbon nanotube interconnects," *IEEE Trans. Electromagn. Compat.*, vol. 56, no. 6, pp. 1666–1673, Dec. 2014.
- [17] A. Maffucci, F. Micciulla, A. E. Cataldo, G. Miano, and S. Bellucci, "Modeling, fabrication, and characterization of large carbon nanotube interconnects with negative temperature coefficient of the resistance," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 4, pp. 485–493, Apr. 2017.
- [18] J. Liang et al., "A physics-based investigation of Pt-salt doped carbon nanotubes for local interconnects," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2017, pp. 3551–3554.
- [19] K. M. Mohsin and A. Srivastava, "Modeling of Joule heating induced effects in multiwall carbon nanotube interconnects," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 11, pp. 3089–3098, Nov. 2017.
- [20] A. Mishra, H. Gossner, and M. Shrivastava, "ESD behavior of MWCNT interconnects—Part I: Observations and insights," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 4, pp. 600–607, Dec. 2017.
- [21] K. Banerjee and A. Mehrotra, "Analysis of on-chip inductance effects for distributed RLC interconnects," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 21, no. 8, pp. 904–915, Aug. 2002.
- [22] Y. I. Ismail and E. G. Friedman, "Effects of inductance on the propagation delay and repeater insertion in VLSI circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 8, no. 2, pp. 195–206, Apr. 2000.
- [23] Q. Lu, Z. Zhu, Y. Yang, and R. Ding, "Analysis of propagation delay and repeater insertion in single-walled carbon nanotube bundle interconnects," *Microelectron. J.*, vol. 54, pp. 85–92, Aug. 2016.
- [24] F. Liang, G. Wang, and W. Ding, "Estimation of time delay and repeater insertion in multiwall carbon nanotube interconnects," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2712–2720, Aug. 2011.
- [25] W.-S. Zhao, G. Wang, L. Sun, W.-Y. Yin, and Y.-X. Guo, "Repeater insertion for carbon nanotube interconnects," *Micro Nano Lett.*, vol. 9, no. 5, pp. 337–339, May 2014.
- [26] P.-W. Liu, Z.-H. Cheng, W.-S. Zhao, Q. Lu, Z. Zhu, and G. Wang, "Repeater insertion for multi-walled carbon nanotube interconnects," *Appl. Sci.*, vol. 8, no. 2, p. 236, 2018.
- [27] K. Banerjee and A. Mehrotra, "A power-optimal repeater insertion methodology for global interconnects in nanometer designs," *IEEE Trans. Electron Devices*, vol. 49, no. 11, pp. 2001–2007, Nov. 2002.
- [28] X.-C. Li, J.-F. Mao, H.-F. Huang, and Y. Liu, "Global interconnect width and spacing optimization for latency, bandwidth and power dissipation," *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2272–2279, Oct. 2005.
- [29] G. Chen and E. G. Friedman, "Low-power repeaters driving RC and RLC interconnects with delay and bandwidth constraints," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 2, pp. 161–172, Feb. 2006.
- [30] J. Kennedy, "Particle swarm optimization," in *Encyclopedia of Machine Learning*. Boston, MA, USA: Springer, 2011, pp. 760–766.
- [31] S. Im, N. Srivastava, K. Banerjee, and K. E. Goodson, "Scaling analysis of multilevel interconnect temperatures for high-performance ICs," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2710–2719, Dec. 2005.
- [32] A. Naeemi and J. D. Meindl, "Compact physical models for multiwall carbon-nanotube interconnects," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 338–340, May 2006.

- [33] J. J. Plombon, K. P. O'Brien, F. Gstrein, V. M. Dubin, and Y. Jiao, "High-frequency electrical properties of individual and bundled carbon nanotubes," *Appl. Phys. Lett.*, vol. 90, no. 6, p. 063106, 2007.
- [34] W.-S. Zhao *et al.*, "High-frequency analysis of Cu-carbon nanotube composite through-silicon vias," *IEEE Trans. Nanotechnol.*, vol. 15, no. 3, pp. 506–511, May 2016.
- [35] C. Gianfagna, H. Yu, M. Swaminathan, R. Pulugurtha, R. Tummala, and G. Antonini, "Machine-learning approach for design of nanomagnetic-based antennas," *J. Electron. Mater.*, vol. 46, no. 8, pp. 4963–4975, Aug. 2017.
- [36] H. Yu, M. Swaminathan, C. Ji, and D. White, "A nonlinear behavioral modeling approach for voltage-controlled oscillators using augmented neural networks," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Philadelphia, PA, USA, Jun. 2018, pp. 551–554.
- [37] Y. Cao, G. Wang, and Q.-J. Zhang, "A new training approach for parametric modeling of microwave passive components using combined neural networks and transfer functions," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 11, pp. 2727–2742, Nov. 2009.
- [38] S. O. Haykin, *Neural Networks and Learning Machines*, 3rd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2009, pp. 1–46.
- [39] K. Levenberg, "A method for the solution of certain non-linear problems in least squares," *Quart. Appl. Math.*, vol. 2, no. 2, pp. 164–168, 1944.
- [40] D. W. Marquardt, "An algorithm for least-squares estimation of nonlinear parameters," *J. Soc. Ind. Appl. Math.*, vol. 11, no. 2, pp. 431–441, Jun. 1963.
- [41] M. M. Shulaker *et al.*, "Carbon nanotube computer," *Nature*, vol. 501, no. 7468, pp. 526–530, Sep. 2013.
- [42] M. M. Shulaker *et al.*, "Three-dimensional integration of nanotechnologies for computing and data storage on a single chip," *Nature*, vol. 547, pp. 74–78, Jul. 2017.



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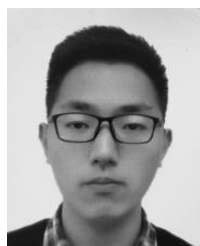
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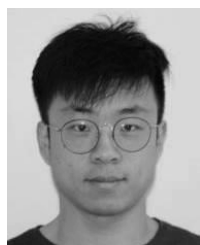
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