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QFN-Packaged Bandpass Filter With Intertwined Circular Spiral Inductor and Integrated Center-Located Capacitors Using Integrated Passive Device Technology

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ABSTRACT This paper describes the implementation of a miniaturized quad flat no-lead (QFN)-packaged bandpass filter (BPF) with a combination of an intertwined circular spiral inductor and two types of integrated center-located capacitors using gallium-arsenide-based integrated passive device (IPD) fabrication technology. Air-bridge structures were introduced into the outer circular spiral inductor to save space and to provide the filter with a compact chip area of $1192.5 \times 1012.7\ \mu m^2$. An equivalent circuit was modeled, the current density and variable dimensional parameters were simulated, and the fabrication process was introduced to achieve a better understanding of the IPD BPF. The proposed device was packaged using the QFN-packaging technology and was measured to possess a single passband with a central frequency of 1.91 GHz (return loss: 28.8 dB) and a fractional bandwidth of 72.69% (insertion loss: 0.62 dB). One transmission zero was obtained on the right side of the passband at 4.78 GHz with an amplitude of 35.95 dB. The fabricated BPF can be used in various *L*-band applications, such as mobile service, satellite navigation, telecommunications, and aircraft surveillance, due to its miniaturized chip size and high-performance characteristics.

INDEX TERMS Air-bridge structure, bandpass filter, capacitor, gallium arsenide, inductor, integrated passive device, QFN package.

I. INTRODUCTION

In many radiofrequency (RF)/microwave applications, filters play an important role, transmitting wanted frequencies while ensuring adequate rejection of the unwanted. The most common types of filters are band-pass, band-stop, low-pass, and high-pass filters, depending on the intended function. In the early stage of RF/microwave engineering, filters constructed using metallic cylindrical or rectangular waveguides were widely used; however, their further application is inhibited by inevitable issues such as high manufacturing cost, large volume, and heavy weight, which limit their integration with other circuits and systems. Along with the rapid expansion of wireless communication systems, microstrip filters have been widely utilized due to their attractive characteristics such as low cost, easy processing, ability to be integrated with active elements, and wide frequency ranges, which can be obtained using a variety of substrate materials. However, microstrip filters usually suffer from high loss, which is mainly introduced by radiation loss and dissipation in the material, especially in the millimeter band.

In the second decade following the invention of the integrated passive device (IPD), wireless communication systems emerged as the earliest large commercial market. Microwave bandpass filters (BPFs) have become increasingly widely utilized in the radio frequency front ends of both receivers and transmitters [1], [2]. The rapid development of modern wireless communication systems coupled with its increasing technical demands has created considerable demand for BPFs with even more stringent requirements: smaller size, better performance, lower cost, etc. [3].

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In the past decades, techniques for fabricating several types of devices, including monolithic microwave integrated circuits (MMICs), micro-electromechanical systems (MEMSs), low-temperature co-fired ceramics (LTCCs), and high-temperature superconductors (HTSs), have been applied to address the ever increasing demands [4]. Gallium arsenide (GaAs) and other advanced III-V materials have enabled the development of MMICs well into the millimeter wavelength range with increased functional capabilities, improved system reliability, and reduced weight, volume, and cost [5]. The major drawback of this technology is that certain parameters can exhibit worse performance when these circuits are used rather than the same devices made from separate components [6]. The MEMS processing technique enables batch fabrication of miniature structures ranging from a few micrometers to millimeters, leading to cost, size, and weight reduction. The ability to integrate mechanical components seamlessly with electronics within the same wafer level is one of the most prominent properties of MEMSs. However, MEMS components suffer from considerably shortened life cycles with uncertainty concerning power handling capability and ultimate dynamic range [7]. LTCC technology consists of a versatile mixture of passive components such as strip lines, filters, antennas, resonators, which are manufactured using inexpensive but highly conductive metals with low electrical resistances and low conductor loss at high frequencies. However, this technology suffers from two major disadvantages. First, the shrinkage of ceramics after firing limits the size of the processed board. Second, modules that require heat dissipation must have heat sinks after heating [8], [9]. HTSs have become attractive due to their very low surface resistances compared with those of even the best normal conducting metals. Furthermore, their low loss properties ensure the fabrication of microwave passive components with far more compact geometries than those attainable using conventional materials. Besides the well-known merits of HTSs, high cost and complexity related to low-temperature operation prevent this technology from widespread application [10].

IPDs are newly developed devices that deliver the desired trade-offs for systems in package integration and enable complete module solutions, thus offering overall better system performance through integration with other functionalities. The IPD fabrication technique is attractive for obtaining simplified and compact passive modules with higher performance than the standard discrete systems due to reduced parasitic effects [11], [12]. Recently, some research groups have been working on BPF implementation using integrated processes such as CMOS and IPD techniques [13], [14]. The CMOS technique is attractive for use in passive microwave circuits for various reasons, such as reduced parasitic effects, smaller chip area, lower power consumption, lower system complexity, and lower integration cost. However, passive on-chip BPFs that consist of spiral inductors usually suffer from ohmic losses, eddy currents, and electromagnetic (EM) interference, which is introduced at RF and thus leads to significant loss on the heavily doped substrate in the standard CMOS epi-based technique [15]. For lumped elements, a lower Q-value is the main issue that affects the device performance but can be addressed using the IPD technique to some extent according to our previous research [16]–[18].

In this article, we report on the design and experimental verification of a wideband BPF, which was implemented on a GaAs substrate using an IPD-based fabrication technique. GaAs substrates have become the second most important semiconductor materials due to their excellent properties of high peak power and near-infrared high repetition frequency. Thus, they have various applications, including medical treatment, information storage, communications, military use, lasing, and sensing [19]–[23]. The proposed IPD BPF was constructed with a combination of an outer intertwined circular spiral inductor and two types of integrated center-located capacitors (interdigital and square parallel lines). In section II, the IPD BPF was subsequently modeled in the form of an equivalent circuit, in which second- and third-order parasitic effects introduced under high frequency were considered. Then, in section III, the current distribution was obtained by performing 3D EM simulations to verify the relationship between the current distribution and operating frequency. Next, in section IV, the influences of three different dimensional parameters on the relationships between the respective S-parameters and frequency were explored by conducting 25 simulation trials. The fabrication process is described in section V to illustrate the development of this module based on IPD fabrication technology. The fabricated device was packaged using quad flat no-lead (QFN) packaging technology, which offers good thermal and electrical performances. Finally, the packaged device was mounted on a printed circuit board (PCB) through gold wire-bonding for the final measurement and evaluation in section VI.

II. EQUIVALENT CIRCUIT MODELING

A. CIRCUIT SIMPLIFICATION

Fig. 1(a) provides a 3D view of the QFN-packaged onboard device. An enlarged version of the fabricated IPD BPF chip with some magnified parts is illustrated in Fig. 1(b). Two series-wound capacitors are located at the center of a circle-shaped outer spiral inductor, which is composed of three laminated conductor layers. The air-bridge structures as well as the capacitors can be seen clearly in Fig. 1(b). The three laminated layers are composed of copper/gold and are called the bond, text, and lead layers, from bottom to top. The detailed topologies of these three layers are illustrated in Figs. 2(a)–(c), and their geometric parameters are summarized in Tables I–III. The proposed IPD BPF chip was fabricated on a GaAs substrate with the thickness of 200.1 μm, dielectric constant of 12.85, and tan(δ) value of 0.006.

The proposed device is based on a low-order resonator, which consists of capacitors and inductors connected together and thus has the following resonant frequency:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}, \tag{1}$$

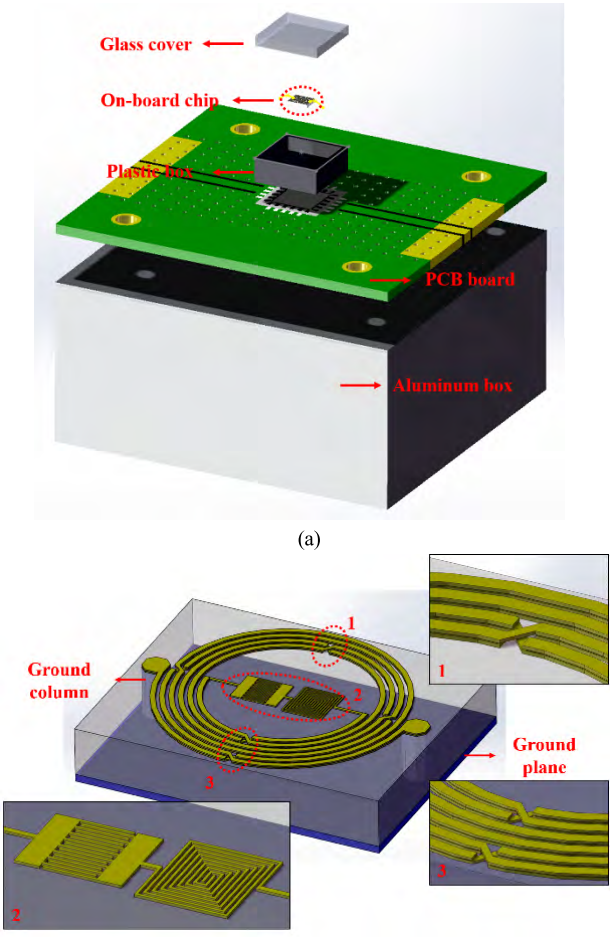

FIGURE 1. 3D view of the packaged IPD BPF with its enlarged layout. (a) Expanded view of the QFN-packaged onboard device. (b) Enlarged layout of the proposed IPD BPF, showing the three laminated layers (bottom to top: bond layer, text layer, lead layer).

where C and L are the total capacitance and inductance, respectively.

B. EQUIVALENT CIRCUIT AND EQUATIONS

Fig. 3 depicts the equivalent circuit model, where L_0 and R_0 are the inductance and resistance, respectively, of the input/output pads and terminations of the input/output port. L_i, R_i, and C_i, where $i = 1, 2, 3$, are the inductance, resistance, and coupling capacitance between turns of the bond, text, and leads layers, respectively, and can be derived using the following equations:

$$L_i = 0.002l\left(ln\frac{2l}{W+t} + 0.50049 + \frac{W+t}{3l}\right) \quad (2)$$

$$R_i = \frac{\rho \cdot l}{W \cdot \delta\left(1 - e^{t/\delta}\right)} \quad (3)$$

$$C_i = \frac{1}{L_i\left(2\pi \cdot f_0\right)^2}, \quad (4)$$

where l, W, and t are the total length, width, and thickness of the metal line, respectively. ρ is the resistance coefficient

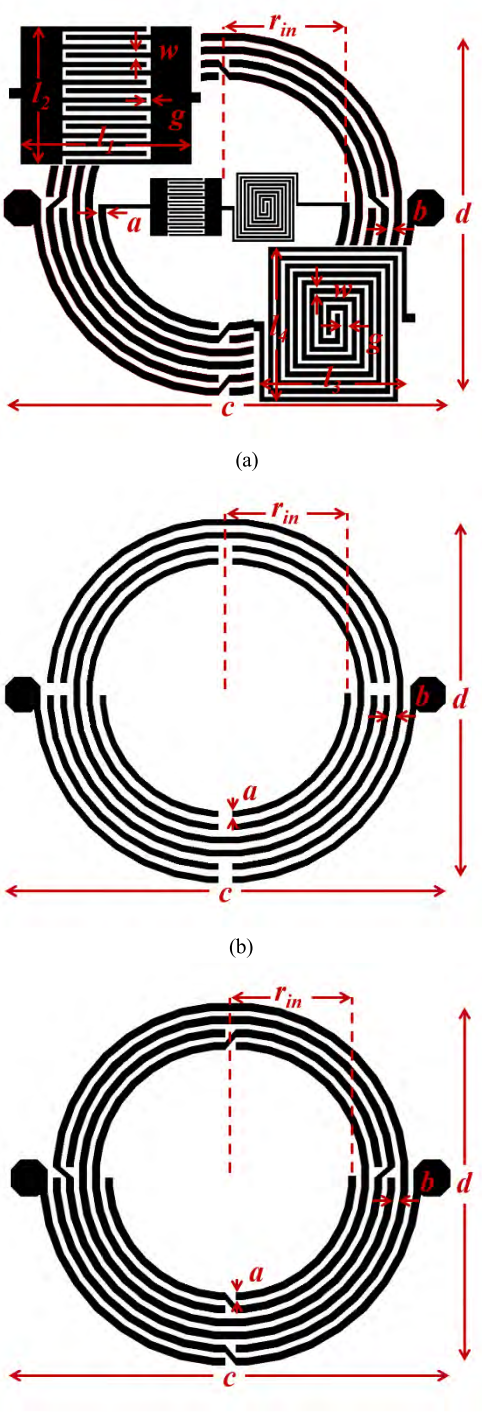

FIGURE 2. Configurations of three laminated layers from bottom to top. (a) Bond layer. (b) Text layer. (c) Lead layer.

of the material, f_0 is the resonant frequency, and δ is the skin depth given by

$$\delta = \sqrt{\frac{\rho}{\pi \cdot \mu_0 \cdot f}}, \quad (5)$$

where μ_0 is the vacuum permeability and f is the operation frequency.

TABLE 1. Dimensional parameters of bond layer.

Parameter	a	b	c	d	r_{in}	Thickness
Unit (μm)	20	15	1192.5	1012.7	300	5

Parameter	w	g	l_1	l_2	l_3	l_4
Unit (μm)	5	5	190	155	175	185

TABLE 2. Dimensional parameters of text layer.

Parameter	a	b	c	d	r_{in}	Thickness
Unit (μm)	16	19	1188.5	1008.7	300	1.8

TABLE 3. Dimensional parameters of lead layer.

Parameter	a	b	c	d	r_{in}	Thickness
Unit (μm)	20	15	1192.5	1012.7	300	5

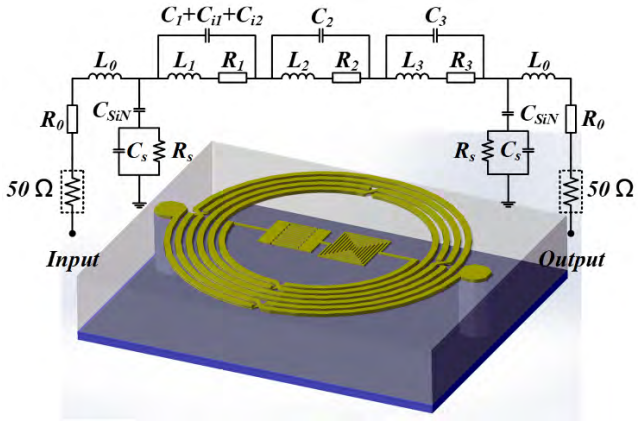

FIGURE 3. Equivalent circuit of the proposed IPD BPF.

The parasitic-induced capacitance between the lossy substrate and planar pattern takes the form of C_{SiN} and can be calculated using

$$C_{SiN} = \frac{S_{ind} \cdot \varepsilon_{SiN}}{2d_{SiN}}, \tag{6}$$

where S_{ind} is the area of the pattern, ε_{SiN} is the permittivity of the SiN layer, and d_{SiN} is the distance between the spiral and the substrate.

The resistance and capacitance of the GaAs substrate were modeled by R_s and C_s, respectively, and are given by [24], [25]

$$R_s = \frac{2}{W \cdot l \cdot G_{sub}} \tag{7}$$

$$C_s = \frac{W \cdot l \cdot C_{sub}}{2}, \tag{8}$$

where G_{sub} and C_{sub} are the conductance and capacitance per unit area of the substrate, respectively.

Furthermore, C_{i1} and C_{i2} are the capacitances of the inner interdigital and square parallel line capacitors, respectively, in the bond layer and can be derived as follows [26]–[28]:

$$C_{i1} = (\varepsilon_r + 1) * l_{i1} * [(n-3) * C_1 + C_2], \tag{9}$$

where ε_r is the dielectric constant of the material, l_{i1} and n is the length and number of the fingers of the interdigital capacitor, respectively, C_1 (the interior) and C_2 (the two exterior) are the capacitances per unit length of the fingers of the interdigital capacitor and can be given as follows:

$$C_1 = 4.409 \tanh\left[0.55\left(\frac{h}{W_{i1}}\right)^{0.45}\right] \times 10^{-6}(pF/\mu m) \tag{10}$$

$$C_2 = 9.92 \tanh\left[0.55\left(\frac{h}{W_{i1}}\right)^{0.5}\right] \times 10^{-6}(pF/\mu m), \tag{11}$$

where W_{i1} is the width of the fingers of the interdigital capacitor, and

$$C_{i2} = \varepsilon_0 \varepsilon_{eff} \frac{K(k)}{K(k')}, \tag{12}$$

where ε_0 is the vacuum permittivity, ε_{eff} is the effective permittivity of the square parallel line capacitor (single layer coplanar stripline), and can be expressed as

$$\varepsilon_{eff} = 1 + \frac{1}{2}(\varepsilon_r - 1)\frac{K(k)K(k_1')}{K(k')K(k_1)}, \tag{13}$$

where K is the elliptical integral of the first kind, and parameters k, k', k_1, and k_1' are given as

$$k = \sqrt{1 - \left(\frac{a}{b}\right)^2}, \tag{14}$$

$$k' = \sqrt{1 - (k)^2}, \tag{15}$$

$$k_1 = \sqrt{1 - \frac{\sinh^2(\pi a/2h)}{\sinh^2(\pi b/2h)}}, \tag{16}$$

$$k_1' = \sqrt{1 - k_1^2}, \tag{17}$$

where a and b represent the half of the inner and outer edge-to-edge length of the two adjacent conductors, respectively, and h denotes the thickness of the substrate.

III. CURRENT DISTRIBUTION SIMULATION WITH VARIOUS FREQUENCIES

A. ADAPTIVELY SELECTED FREQUENCY POINTS

Considering that performing computations over a wide frequency range can consume more CPU time and disk space for storage, the frequency points were selected adaptively by using Advanced Design System (ADS) software to ensure accurate interpolation with regards to frequency, as Fig. 4(a) illustrates. For each simulation frequency point, 20 points of the maximum value of current density are picked up and listed in momentum visualization window, as illustrates in Fig. 4 (b). The average values of current density of each simulation frequency were calculated and drawn together

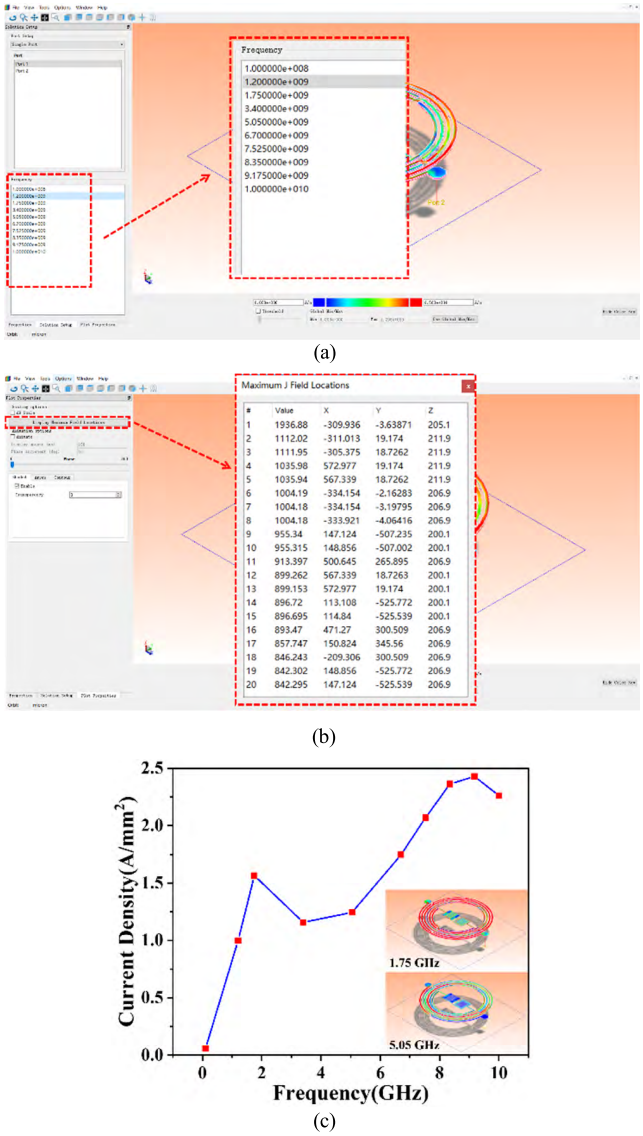

FIGURE 4. Simulation frequencies and current densities simulated using the ADS Momentum 3D Planar EM Simulator. (a) Adaptively selected simulation frequency points in the solution setup tab with the frequency list enlarged in the middle. (b) 20 maximum current dense points with their location information. (c) Current density-frequency illustration with the current density distributions simulated using frequencies of 1.75 GHz and 5.05 GHz on the bottom left.

in Fig. 4 (c), which shows the variation of current density under different frequencies with the effects of 1.75 GHz (the nearest frequency point to resonant mode) and 5.05 GHz (the nearest frequency point to the transmission zero) on the simulated current density throughout the proposed IPD BPF on the bottom right. The simulated current density rises to its first peak at 1.75 GHz from 57.00 A/m^2 to 1565.12 A/m^2, after falls down to 1157.52 A/m^2 at 3.4 GHz, then increases to the peak of 2428.75 A/m^2 at 9.175 GHz. The directions of current flow in the wires determine the effect of coupling, which is positive if the currents in the two adjacent lines are in the same direction and negative if they are in opposite directions.

B. EFFECTS ON CURRENT DISTRIBUTION UNIFORMITY BY OPERATING FREQUENCY AND LOCATION

A significant issue related to the spiral conductor analysis lies in the fact that the current distribution along a metal line has strong functional relationships with its operating frequency and location. The current in a metal line is uniformly distributed at direct current; while, when an alternating current is applied, it creates an associated alternating magnetic field that introduces eddy current, altering the uniformly distributed current to be nonuniform, which is a prominent mechanism and affects the chip performance. In general, the eddy current is introduced under a time-varying magnetic field and manifests itself as proximity and skin effects [29]. According to the 3D EM and partial element equivalent circuit simulations, the current distribution in a metal line generally features an attenuation from the inner side (the closer to the center of the device) to the outer side (the side farther from the center of the device). Furthermore, the attenuation is more severe in the inner wires coupled with the increase in frequency. The abovementioned phenomenon was verified by our 3D EM current simulations with the area of interest indicated by the red dashed line near the output port in Fig. 5. It is obvious that the current distribution in the indicated part attenuates from the inner side to the outer side and that this attenuation becomes clearer as the frequency increases from 3.40 GHz to 5.05 GHz, 6.70 GHz, and 7.52 GHz. These four frequencies were selected in a continuous manner after 1.75 GHz, which is near the resonant mode and yields the highest intensity distributed across almost all the areas of the chip. Moreover, it has been demonstrated in [30] where the proximity effect between the turns of a spiral inductor (generally on a cross-sectional view of the inductor where the thickness of the conductor is relatively smaller than the width) that are in the same plane can be neglected at around 1 GHz. At higher frequency, the current simulation results show that the current is tend to concentrate in the areas of the metallic trace farthest away from the nearby conductor, which carries current in the same direction, and the concentration becomes more prominent with frequency goes up.

IV. FILTER ANALAYSIS BASED ON VARIOUS PARAMETERS

Fig. 6(a) presents the simulation results, where markers m1 and m2 indicate the frequency and amplitude of the two lowest points, S11 and S21, respectively. In addition, a schematic of the IPD BPF inside the working window of the software is included as an inset at the bottom right.

To obtain a better understanding of the influences of different parameters on the performance, the inner radius r_{in}, line spacing b, and line width a were selected for further simulation and analysis. Table IV provides the dimensional information obtained in all 25 trials that we conducted while varying these three parameters. The simulated variations resulting from adjusting these three parameters are depicted in Figs. 6(b)–(d), which illustrate the shifting of the frequency and magnitude of m1 and m2. Here, the line spacing and line

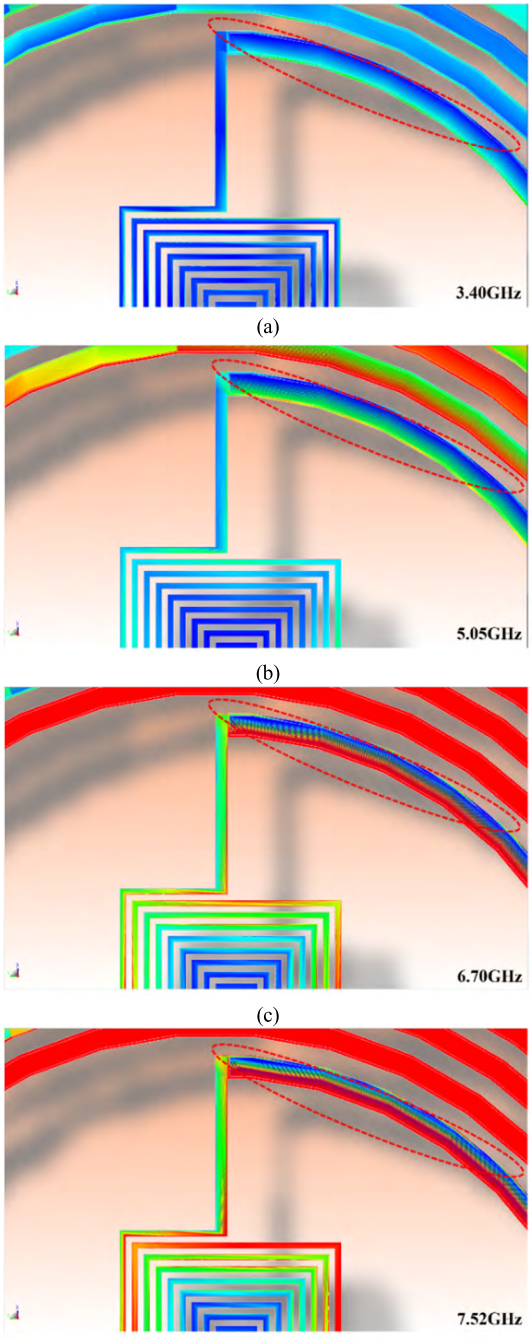

FIGURE 5. Current density contours at the near output port with the relevant part indicated by the red dashed line according to simulations performed using the ADS Momentum 3D Planar EM Simulator at frequencies of (a) 3.40 GHz, (b) 5.05 GHz, (c) 6.70 GHz, and (d) 7.52 GHz.

width are based on the bond and lead layers. Referring to Tables I–III, we know that the dimensions (conductor width a, conductor spacing b, length c, and width d) differ somewhat among the bond, lead, and text layers. The frequencies of both m1 and m2 tend to shift lower in response to a larger inner radius and a wider conductor width, while the situation is the opposite when the conductor spacing increases.

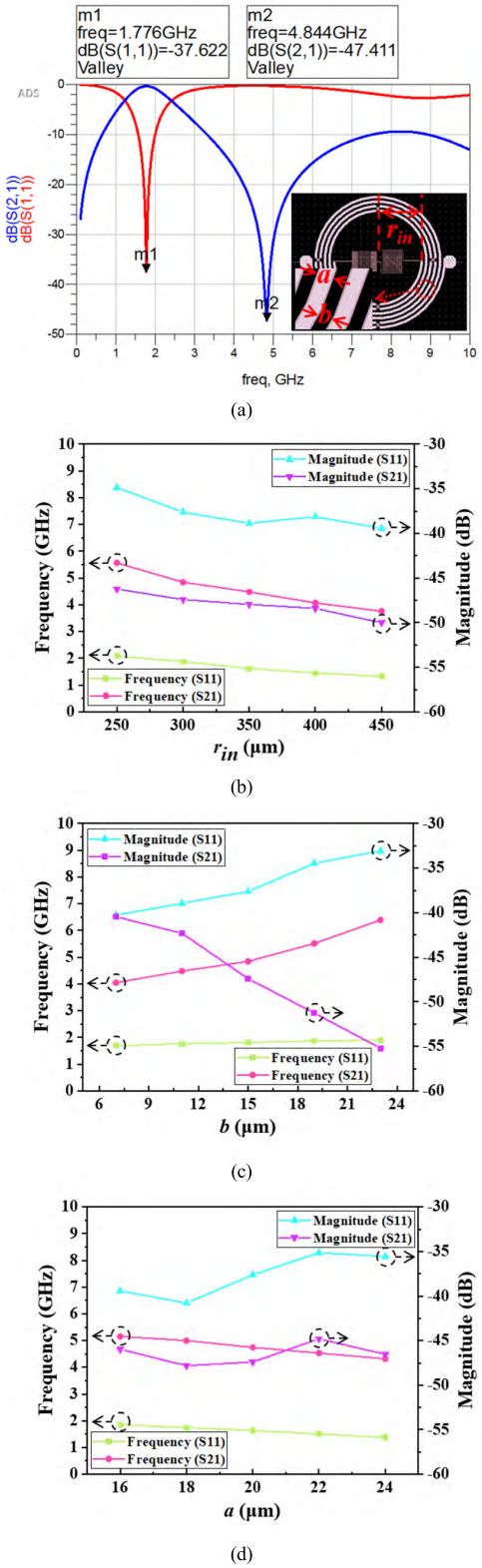

FIGURE 6. Simulation results illustrating the influences of three parameters on the relationship between S-parameter and frequency. (a) Simulated S-parameters with two markers showing the location and magnitude information in data display window, and top view of the proposed IPD BPF layout. (b) Inner radius r_{in}. (c) Line spacing b. (d) Line width a.

TABLE 4. Dimensional information of the simulated IPD BPF obtained by varying three parameters.

Variable parameter	Bond layer			Text layer			Lead layer		
	Inner radius	Line width	Line spacing	Inner radius	Line width	Line spacing	Inner radius	Line width	Line spacing
Inner radius (μm)	250	20	15	250	16	19	250	20	15
	300	20	15	300	16	19	300	20	15
	350	20	15	350	16	19	350	20	15
	400	20	15	400	16	19	400	20	15
	450	20	15	450	16	19	450	20	15
	Inner radius	Line width	Line spacing	Inner radius	Line width	Line spacing	Inner radius	Line width	Line spacing
Line width (μm)	300	16	15	300	12	19	300	16	15
	300	18	15	300	14	19	300	18	15
	300	20	15	300	16	19	300	20	15
	300	22	15	300	18	19	300	22	15
	300	24	15	300	20	19	300	24	15
	Inner radius	Line width	Line spacing	Inner radius	Line width	Line spacing	Inner radius	Line width	Line spacing
Line spacing (μm)	300	20	7	300	16	11	300	20	7
	300	20	11	300	16	15	300	20	11
	300	20	15	300	16	19	300	20	15
	300	20	19	300	16	23	300	20	19
	300	20	23	300	16	27	300	20	23

Furthermore, according to Fig. 6(b), the influence on S21 is more obvious than that on S11. Thus, Figs. 7(a)–(c) are provided for better illustration of the parametric influence on S21, which shows that the conductor spacing variation has a more substantial influence on S21, especially in the areas outside the passband.

V. IPD BPF FABRICATION AND PACKAGING

Fig. 8 shows schematics of the fabrication process of the IPD BPF, which was manufactured on a 6-inch GaAs substrate. First, an ultrasonic acetone bath, isopropyl alcohol (IPA) treatment, and deionized (DI) water were employed, in that order, on the GaAs substrate to remove ionic contaminants, organic impurities, and native chemical oxide from the wafer surface (Step 1). To obtain an even wafer surface without roughness issues or other surface defects, plasma-enhanced chemical vapor deposition was employed to deposit a 0.2-μm-thick SiNx layer (relative permittivity: 7.5, loss tangent: 0.002) as a passivation layer (Step 2). This deposition was performed in a chamber with a mixture of SiH_4 and NH_3 at a ratio of 1:19, a temperature of 250°, a pressure of 1200 mTorr, a 2000 sccm gas flow, and 100 W of RF power. After deposition of the passivation layer, a 20/80-nm-thick Ti/Au seed layer was formed via sputtering to ensure strong adhesion between the substrate and the first metal layer (Step 3). Then, a spin-coater was used to spin photoresist onto the wafer, and an exposure and development process was applied to define the first metal layer (Step 4). Next, a 4.5/0.5-μm-thick Cu/Au metal layer was plated to form the bottom bond layer (Step 5). This deposition process was performed under a pressure of 5.0×10^{-6} mTorr, and the electron energy was fixed at 10 kV. Moreover, a minimum deposition rate of 0.5 Å/s was set to obtain an accurate layer thickness. The photoresist was removed by a lift-off machine in 90 s using acetone/IPA/DI water. After lift-off, inductively coupled plasma dry etching (SF_6/Ar) was implemented to remove the unwanted seed metal area (Step 6). Then, the photoresist was again applied to the wafer and the second seed metal layer (20/80-nm-thick Ti/Au) was constructed (Step 7) and etched by SF_6/Ar (Step 8). Next, air-bridge post-patterning was conducted by photoresist coating, exposure, and development, in that order (Step 9). To reflow the air-bridge post pattern, a hard baking process was performed with a baking temperature of 130° and a baking time of 180 s. After that, the second metal layer (1.6/0.2-μm-thick Cu/Au) was formed using an electroplating process (Step 10). Similarly, the third seed metal layer (20/80-nm-thick Ti/Au) was defined (Step 11), and then the second air-bridge photoresist

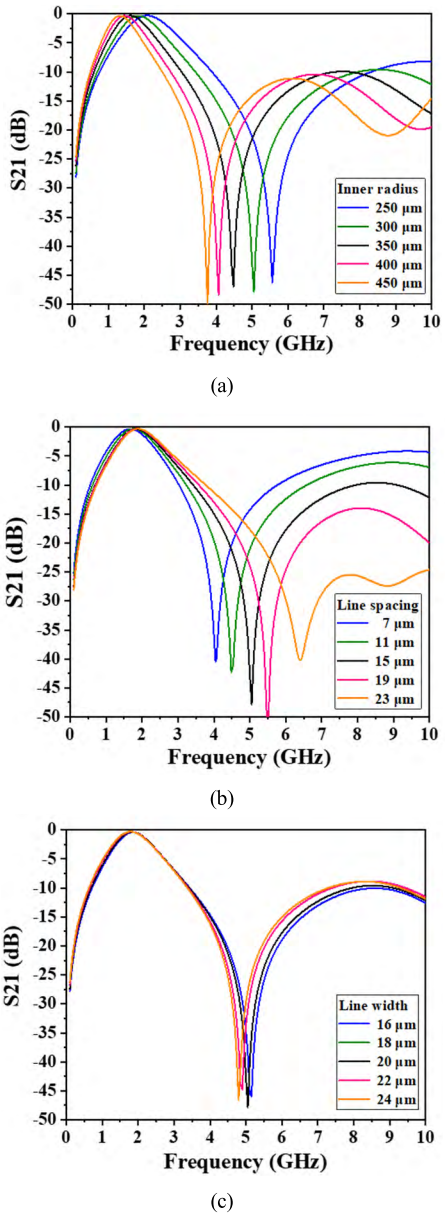

FIGURE 7. Simulated results illustrating the influences of three different parameters on the relationship between S21 and frequency. (a) Inner radius. (b) Line spacing. (c) Line width.

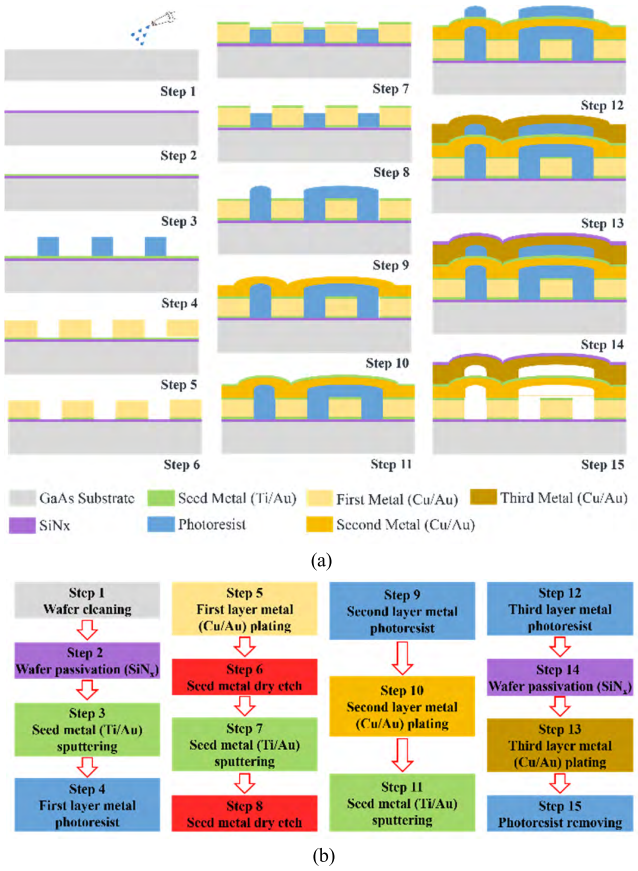

FIGURE 8. Fabrication of the proposed IPD BPF. (a) Fabrication flow diagrams. (b) Fabrication block diagram flow chart.

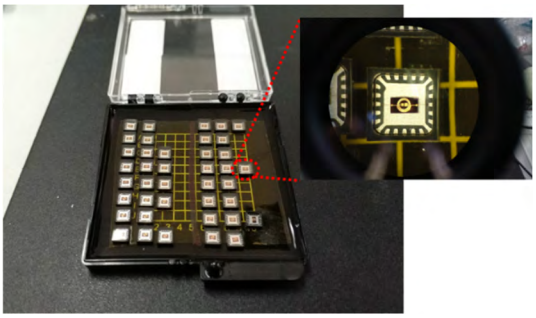

FIGURE 9. Packaged IPD chips and magnified view.

was marked (Step 12) using the same three procedures before deposition of the third metal layer (4.5/0.5-μm-thick Cu/Au) (Step 13). Then, another 0.2-μm-thick SiNx layer was deposited for passivation (Step 14). Finally, the photoresist was removed by a lift-off machine using acetone/IPA/DI water (Step 15).

Plastic encapsulated packaging features versatile footprints, a small profile, and low cost, making it popular among integrated circuit (IC) products. It is estimated that more than 95% of IC products worldwide are packaged in this manner [31]. QFN technology is a type of surface-mount technology that connects ICs to PCB surfaces without through-vias. This technology is attractive for semiconductor packaging today due to its small form factor, low cost, and electrical performances, which are desirable for high-power and high-speed components, including transmitters, transceivers, antennas, and power amplifiers, [32]–[35]. Fig. 9 shows the packaged IPD chips inside the QFN box with dimensions of 4 mm × 4 mm. As Fig. 10 illustrates, the packaged IPD chips were mounted on a PCB for the final measurement.

VI. RESULTS AND DISCUSSION

The proposed IPD BPF was designed and simulated using ADS software and then fabricated for design validation. The transmission and reflection parameters were measured and recorded using an Agilent 8510C vector network analyzer (VNA). A photograph of the measurement setup is shown in Fig. 11(a), and an enlarged view is provided

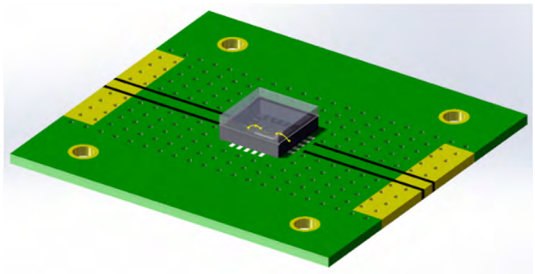

FIGURE 10. Packaged IPD BPF on PCB.

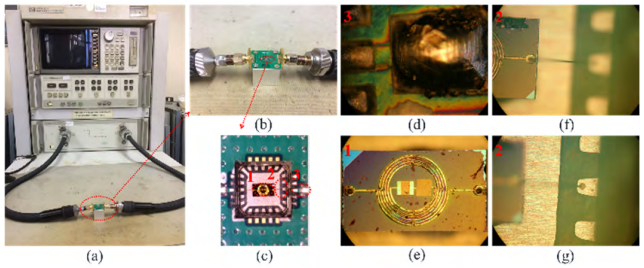

FIGURE 11. S-parameter measurement setup for the proposed IPD BPF with enlarged views of different parts. (a) IPD BPF VNA cable connection. (b) Magnified view of the IPD BPF and its input/output ports. (c) Top view of the packaged chip on the PCB. Microscopic views of (d) the part connecting the packaged chip and PCB, (e) the wire-bonded chip as a top view, (f) the wire-bonding part focused on the chip side, and (g) the wire-bonding part focused on the packaging box side.

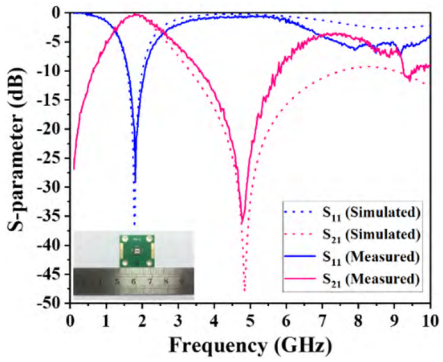

FIGURE 12. Simulated and measured results of the proposed IPD BPF with the fabricated onboard chip on the bottom left.

in Fig. 11(b), where the chip is wire-bonded onto a PCB (2 cm × 2 cm) and then attached to an aluminum cube (2 cm × 2 cm × 2 cm) for decreased noise. The input/output ports of the PCB were both connected to the VNA via cables attached to subminiature version A connectors. Fig. 11(c) shows the packaged onboard chip with four magnified pictures representing its three highlighted parts taken using a Nikon Eclipse L150 microscope. Fig. 11(d) depicts a microscopic view of the wire-bonding part that connects the input/output pads of the IPD BPF and the pads of the PCB, and Fig. 11(e) provides a top view of the fabricated chip obtained using a microscope. Figs. 11(f) and 11(g) show the wire-bonding part connecting the pads of the chip and the inside of the QFN box with its own focus points, respectively. The simulated and measured results of the IPD BPF are presented in Fig. 12, with the packaged onboard device illustrated in the bottom left of the same figure.

TABLE 5. Comparison with other published works.

Ref.	Fabrication process	Circuit area (mm^2)	Passband (GHz)	Fractional bandwidth (%)	IL (dB)	RL (dB)
[36]	Si-IPD	6.96	6.5	107.69 (3 dB)	1.1	15
[37]	Glass-IPD	<1.00	2.6	49.62 (3 dB)	0.6	30
[38]	Si-IPD	0.72	2.4	33.33 (3 dB)	2.3	10
[39]	Si-IPD	3.9	1.7	16 (10 dB)	2.54	12
[40]	Glass-IPD	1.69	2.1	36.73 (10 dB)	3.2	22
This work	GaAs-IPD	1.20	1.91	72.69 (3 dB)	0.6	28

The measured center frequency is 1.91 GHz, and its 3 dB passband is 1.21–2.60 GHz with a fractional bandwidth of 72.69%. There is one transmission zero located on the right side of the passband with a measured frequency of 4.78 GHz and magnitude of 35.95 dB. Comparisons of the proposed IPD BPF with four previously investigated IPD BPFs are provided in Table V, which demonstrates that our device features relatively a small chip area, a wide fractional bandwidth, and good insertion and return losses.

VII. CONCLUSION

A QFN-packaged IPD fabrication technique-based BPF using a combination of an intertwined circular spiral inductor and two types of integrated center-located capacitors as well as air-bridge structures was proposed in this report. The IPD BPF was modeled by using an equivalent circuit considering the second- and third-order parasitic capacitances induced by high frequency. The 3D EM current simulations revealed that the current distribution in a metal line has a functional relationship with its operating frequency and location. Twenty-five simulation trials were performed to explore the relationships between dimensional adjustments and the S-parameter, revealing that increased conductor spacing influences S21 considerably and consequently yields better suppression outside the passband. The device was fabricated on a GaAs substrate for better understanding of the device structure and IPD fabrication technology. The proposed IPD BPF was packaged for measurement using QFN packaging technology for improved electrical performance. The consistency achieved between the theoretical predictions and measurements performed on the fabricated IPD BPF shows that the device is a good candidate for the use in various L-band applications, such as mobile service, satellite navigation, telecommunications, and aircraft surveillance, owing to its miniaturized chip size and high-performance characteristics. However, there are some limitations in this study. First, the proposed IPD BPF is a low-order device, while high-order is preferred for its sharper roll-off property. However, there is a tradeoff between device performance and footprint for the purpose of improving the compactness, which is usually important in commercial production. Second, there are some major reliability and quality challenges associated with QFN

packaging such as short life cycle comparing with quad flat pack packaging under a typical thermal cycling test. Third, the performance of the packaged chip was verified on individually designed PCB, while more performance and reliability tests need to be taken on a real integrated system according to various L-band applications in the future.

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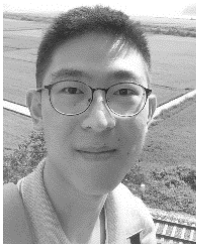

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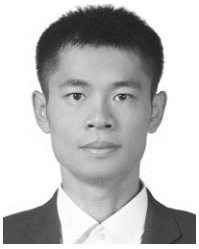

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