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Model-Predictive-Control-Based Flexible Arc-Suppression Method for Earth Fault in Distribution Networks

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ABSTRACT Traditional arc-suppression devices have a weak effect on the arc-extinguishing result of earth fault because of increased active and harmonic components of fault current. To solve the problem, in this paper, a flexible arc-suppression device based on a three-phase cascaded H-bridge (CHB) converter with auxiliary sources is further developed; on this basis, an arc-suppression method based on the improved finite control set model predictive control is proposed. The proposed approach, which uses a combination of two voltage levels in a sampling period to reduce the steady-state current error, controls the CHB converter to inject compensation current into the distribution network. Taking into account the reduction of switching losses and balancing heat in each H-bridge cell, a novel method that causes the switching transitions to be distributed evenly among the H-bridge cells is proposed to select the optimal switching combination. The tracking capability of the improved control method is analyzed, and the parameters affecting the arc-suppression performance are obtained. The simulation and experimental results show that the proposed method achieves an excellent performance of suppressing fault current and extinguishing arc. Moreover, the balance of switching transitions is also achieved.

INDEX TERMS Earth fault, arc suppression, cascaded H-bridge converter, finite control set model predictive control (FCS-MPC).

I. INTRODUCTION

High reliability of power supplies is an important advantage in resonant grounding distribution networks. When a single-phase earth fault occurs, an arc-suppression coil is used to compensate the fault current to suppress the fault arc and then extinguish it [1], [2]. However, the expansion of the distribution network and the use of urban cables have significantly increased the capacitive component of fault current induced by line-to-ground capacitances. Moreover, with massive nonlinear loads and power electronics access to grids, the fault current contains a higher proportion of harmonic components compared to the past. Furthermore, when insulation aging, poor weather, or environmental deterioration occurs in overhead line networks, the active component of fault current will exceed 10% of the capacitive component; such a fault current is more frequent in coastal areas. In these cases, the traditional arc-suppression method has been unable to satisfy the safety requirements because the arc-suppression coil cannot completely compensate fault current, except for the capacitive fundamental component, and the residual current still maintains the fault arc. Such a situation is likely to endanger public and personnel safety or ignite the shrubs [3]–[6].

The distribution network transformed by flexible power electronics is an important trend that can effectively solve some bottlenecks in the development of traditional distribution networks. Because the power converter can control the output current flexibly, it has been used in the arc-suppression field and is known as the flexible arc-suppression device (FASD). Recently, several devices based on power converters have been presented to enhance the arc-suppression performance [4]–[8]. However, for the above FASDs, the absence of fault-tolerant methods reduces the reliability of suppressing arc, once the core power converter fails. Moreover, an additional Z-type transformer used to create a neutral point is required in a medium-voltage distribution network.

At present, the cascaded H-bridge (CHB) converter is widely used in active power filters (APFs) [9], [10] and static synchronous compensators (STATCOMs) [11]–[13] because

of its modularity, extendibility and transformer-less characteristic [14], [15]. To address the aforementioned issues, a FASD based on a three-phase CHB converter, which is directly connected to the bus of distribution networks without the Z-type transformer, was proposed in [16]. The modular and fault-tolerant design can increase the reliability and ensure the normal operation of the device even if parts of components fail [17]. However, the DC-side voltage of the CHB converter exhibits a downward trend because of the energy losses in the arc-suppression process.

For a FASD based on a power converter, the arc-suppression method that allows the device to extinguish the arc is a combination of the arc-suppression principle and control method. Thus, the arc-suppression performance is directly affected by the control method of the power converter. Moreover, the reference of the injected current is irregular and even undergoes sudden changes; therefore, the classical strategies for the control and modulation of the CHB converter cannot be completely in conformity with the arc-suppression demand. In recent years, finite control set model predictive control (FCS-MPC) has been widely used in various power electronics because of its advantages, including flexibility and the easy inclusion of system constraints and nonlinearities. In addition, FCS-MPC does not require the modulation and has the better transient performance compared to classic linear controllers [18], [19]. FCS-MPC has also been applied for the CHB converter [20]–[26]. FCS-MPC is a method of online optimization for each cycle and therefore does not accumulate errors [20], [21]. The main drawback of FCS-MPC is the large computational burden when the number of H-bridge (HB) cells, the sampling frequency or the prediction horizon is high [22]–[26].

In the traditional FCS-MPC method, only one voltage level is applied during the whole sampling period, causing the steady-state error issue [19]. To alleviate this problem and reduce the steady-state error, a FCS-MPC method, where the measurements are taken in the middle of the sampling period and an integral term is applied in cost function, was proposed [27]. Moreover, modulation techniques are added into FCS-MPC again to improve its steady-state performance and get the fixed switching frequency [28]–[30]. In [31], a specific FCS-MPC method in which two voltage levels with variable application durations are utilized in one sampling period (2V-MPC) was proposed. The smaller steady-state current error and zero error at the end of the sampling period are achieved; however, multiple use of the cost function makes the computation burden increase with switching combinations, which is unsuitable to apply in CHB converter with many HB cells. A low-complexity 2V-MPC method that utilizes a pair of adjacent levels in one period was proposed in [32] and [33]; however, more additional switching transitions are required, thereby increasing the losses of the converter. In [34], an improved 2V-MPC method was introduced that maintains the level in the first part of the period and applies the adjacent level in the rest of the period, but the dynamic response is weakened.

For FCS-MPC, Switching combinations need to be selected to generate switching signals to the HB cells. Due to the characteristic of CHB converter, there are a lot of redundant switching combinations so that the control difficulty and computational burden increases significantly. In [35], a FCS-MPC method based on asymmetric DC-side voltage was proposed; there are no redundancies when the asymmetry is trinary so the switching combinations can be obtained directly. For the CHB converter supplied by DC-side capacitors, the redundant switching combinations are utilized to balance the DC-side voltage; therefore the optimal switching combination is selected according to the output voltage level and DC-side voltage [30], [33]. It is difficult for the CHB converter fed by DC voltage sources to select an appropriate switching combination from massive redundancies by FCS-MPC because of the equal DC-side voltage. In [36], each voltage level only corresponds to one switching combination. This method reduces the computation burden and eliminates all the redundancies; however, the switching transitions are not balanced among the HB cells.

This paper presents an arc-suppression method based on an improved 2V-MPC, where a three-phase CHB converter with auxiliary sources is used as the FASD. The proposed FASD can be obtained by transforming the CHB converter based reactive power compensation device, thus significantly reducing the cost of building the FASD and increasing the function of the existing device. The improved 2V-MPC uses a combination of the optimal voltage levels of the previous period and the present period. The proposed method can achieve the lower steady-state current error and maintain the fast dynamic response. Moreover, a novel switching combination selection method is also proposed that can achieve the balance of switching transitions of all HB cells. Furthermore, the tracking capability of the improved 2V-MPC and the parameters affecting the arc-suppression performance are analyzed in this paper. Finally, the feasibility of the proposed arc-suppression method is verified by simulations and experiments.

II. MODEL OF THE PROPOSED FASD AND CURRENT COMPENSATION PRINCIPLE

A. MODEL OF THE DISTRIBUTION NETWORK

A typical 10-kV distribution network with the proposed FASD is shown in Fig. 1. $\dot{E}_{\mathrm{X}}$, $\dot{U}_{\mathrm{X}}$(X = A, B, or C), and $\dot{U}_0$ are the supply voltage, the phase voltage, and the neutral voltage of the distribution network, respectively. r_{X} and C_{X} are the phase-to-ground leakage resistance and capacitance, respectively. The earth fault is assumed to occur in phase A with an earth-fault resistance R_f, and the fault current $\dot{I}_f$ flows into the earth from the fault point. $\dot{I}_{\mathrm{XZ}}$ is the injected current of the FASD, and $\dot{I}_{\mathrm{Xg}}$ is the phase-to-ground current. The FASD consists of a three-phase CHB converter with n HB cells in each phase. The three-phase CHB converter is connected to the three-phase bus through the current limiting resistance R, the filter inductance L and the high voltage switch S_d.

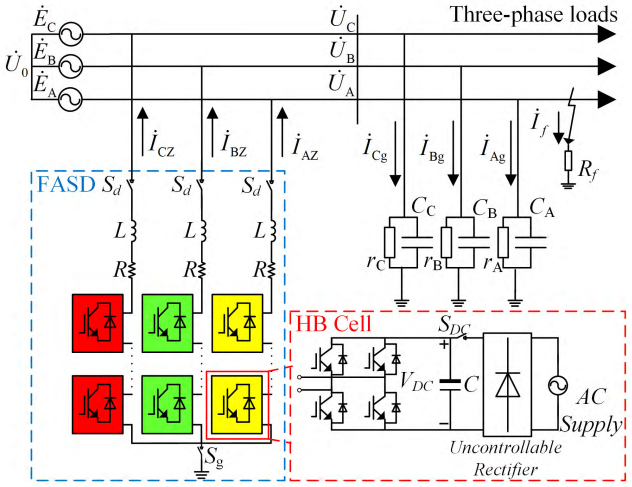


FIGURE 1. Structure of the distribution network using the proposed FASD.

The three-phase CHB converter uses a star-connected structure, and its neutral point is connected to the ground, allowing the CHB converter in each phase to operate independently.

B. ANALYSIS OF THE COMPENSATION CURRENT

To simplify the analysis, the three-phase CHB converter is represented by three controlled current sources, whose current values are $\dot{I}_{AZ}$, $\dot{I}_{BZ}$ and $\dot{I}_{CZ}$. The equivalent circuit of the system is shown in Fig. 2. It is assumed that the current flowing into earth (node D) is positive. The KCL equation on the node D can be obtained as

$$(\dot{I}_{Ag} + \dot{I}_{Bg} + \dot{I}_{Cg}) - (\dot{I}_{AZ} + \dot{I}_{BZ} + \dot{I}_{CZ}) = 0 \tag{1}$$

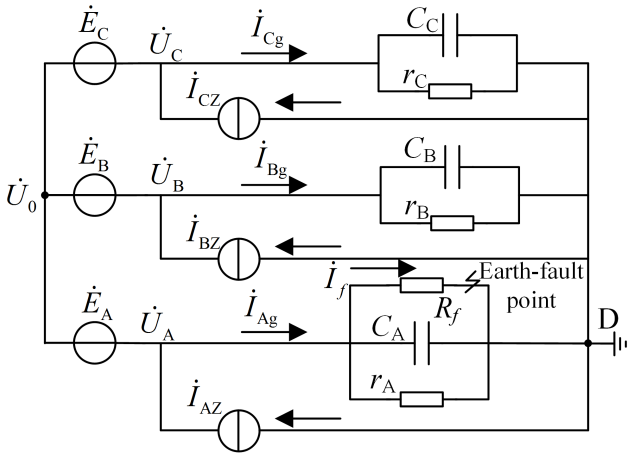


FIGURE 2. Equivalent circuit of the distribution networks.

After the parameters and phase voltages of the distribution network are substituted into (1), the following equation can be obtained:

$$\dot{U}_C(\frac{1}{r_C} + j\omega C_C) + \dot{U}_B(\frac{1}{r_B} + j\omega C_B) + \dot{U}_A(\frac{1}{r_A} + j\omega C_A + \frac{1}{R_f}) - (\dot{I}_{AZ} + \dot{I}_{BZ} + \dot{I}_{CZ}) = 0 \tag{2}$$

It is assumed that the fault-point voltage is equal to the fault-phase voltage. Accordingly, the following expression is obtained for the fault current when the phase-to-ground parameters are unbalanced:

$$\dot{I}_f = \frac{\dot{U}_A}{R_f} = (\dot{I}_{AZ} + \dot{I}_{BZ} + \dot{I}_{CZ}) - \dot{U}_A(\frac{1}{r_A} + j\omega C_A) - \dot{U}_B(\frac{1}{r_B} + j\omega C_B) - \dot{U}_C(\frac{1}{r_C} + j\omega C_C) \tag{3}$$

The fault-phase voltage is $\dot{U}_X = \dot{U}_0 + \dot{E}_X$, and it is assumed that $\dot{E}_A + \dot{E}_B + \dot{E}_C = 0$, $C_A = C_B = C_C = C_0$ and $r_A = r_B = r_C = r_0$. Equation (3) can be simplified as follows:

$$\dot{I}_f = \frac{\dot{U}_A}{R_f} = (\dot{I}_{AZ} + \dot{I}_{BZ} + \dot{I}_{CZ}) - 3\dot{U}_0(\frac{1}{r_0} + j\omega C_0) \tag{4}$$

Thus, the injected current $\dot{I}_Z$ of the FASD satisfies the following equations:

Unbalanced parameters:

$$\dot{I}_Z = (\dot{I}_{AZ} + \dot{I}_{BZ} + \dot{I}_{CZ}) = \dot{U}_A(\frac{1}{r_A} + j\omega C_A) + \dot{U}_B(\frac{1}{r_B} + j\omega C_B) + \dot{U}_C(\frac{1}{r_C} + j\omega C_C) \tag{5}$$

Balanced parameters:

$$\dot{I}_Z = (\dot{I}_{AZ} + \dot{I}_{BZ} + \dot{I}_{CZ}) = 3\dot{U}_0(\frac{1}{r_0} + j\omega C_0) \tag{6}$$

The fault current $\dot{I}_f$ can be compensated and suppressed to zero. Moreover, the fault-phase voltage also drops to zero. If the unbalance factor of the phase-to-ground parameters is low, then (6) can be adopted to calculate the reference current; this approach reduces both the computational burden and the number of collected signals. The injected current of each phase can be arbitrarily assigned, as long as the total amount of injected current can reach the given value. In general, only the fault-phase CHB converter is accessed to the distribution network. However, the other two phases can be used to improve the reliability of the FASD when the fault-phase device fails. Moreover, using two-phase or three-phase converters at the same time can share the total current to avoid large current flowing through the converters and reduce the change rate of the reference. In addition, the FASD based on a three-phase CHB converter can be extended for harmonic suppression, reactive power compensation, over-voltage suppression, and other applications. Because the control of each phase of the CHB converter is decoupled, the analyses in the following sections are based on a single-phase CHB converter.

C. STRUCTURE AND SYSTEM MODEL OF FASD

According to (4) and (4), the fault-phase voltage is suppressed to approximately zero at the steady state of the arc-suppression process. The injected current of the fault phase will be determined by the line impedance and output voltage

$\dot{U}_o$ of the CHB converter as follows:

$$\dot{I}_{AZ} = \frac{\dot{U}_o - \dot{U}_A}{j\omega L + R} \approx \frac{\dot{U}_o}{j\omega L + R} \tag{7}$$

The complex power $\tilde{S}$ of the FASD can be expressed as

$$\tilde{S} = \dot{U}_o \dot{I}_{AZ}^* = P + jQ = U_o I_{AZ} \cos\varphi + jU_o I_{AZ} \sin\varphi \tag{8}$$

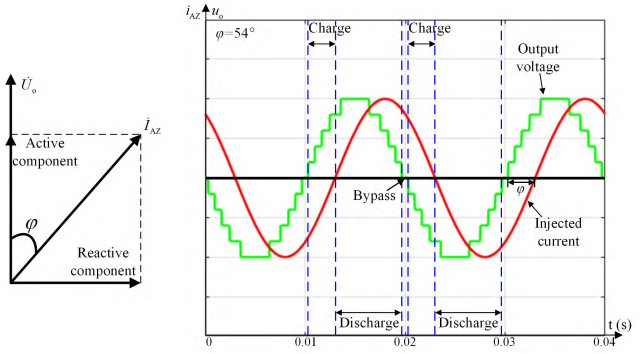


FIGURE 3. Analytical diagram of charge and discharge for the FASD.

where $\dot{I}_{AZ}^*$ is the conjugate complex number of $\dot{I}_{AZ}$; P and Q are the active power and reactive power of the FASD; φ is the impedance angle and $\varphi = \arctan(\omega L/R)$. In an actual circuit, φ must be less than 90 degrees because of the line resistance, and the active power P is positive. The charge and discharge processes of the CHB converter are also represented in Fig. 3. It can be seen that the time of discharge is greater than the time of charge in a cycle. In summary, in the arc-suppression process, the FASD consumes the DC-side energy and cannot obtain power from the distribution network; therefore, it is different from STATCOM or APF, which can achieve the balance of energy exchange with the distribution network. In this paper, the auxiliary source composed of an AC power supply and an uncontrollable rectifier is connected in parallel with the DC-side capacitor to supplement the energy consumed, where C is the DC-side capacitance.

When a single-phase earth fault occurs, the auxiliary source circuit is connected to the DC side of the HB cell of the existing reactive power compensator by closing the switch S_{DC}, and the three-phase CHB converter is simultaneously grounded by closing the grounding switch S_g. At this time, the reactive power compensator is transformed into the proposed FASD.

Fig. 4 shows the topology of a single-phase CHB converter with n HB cells. Because of the large DC-side capacitance, the DC-side voltage accessed to the auxiliary source can be assumed to be stable and balanced. Therefore, the DC side of the HB cell is equivalent to a DC voltage source with a voltage of V_{DC}. u_o is the AC-side output voltage of the CHB converter; u is the voltage at the point where the FASD is accessed; i_Z is the injected current of the CHB converter; S_{ij} denotes the switches in the i-th HB cell. The switching

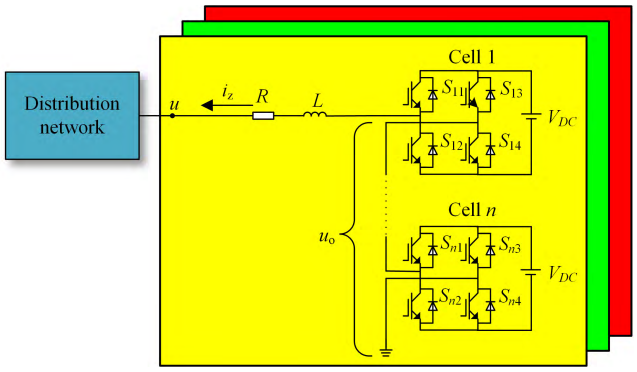


FIGURE 4. Simplified topology of a single-phase CHB converter with n HB cells.

state H_i of the i-th HB cell is defined as

$$H_i = \begin{cases} 1, S_{i1} = S_{i4} = 1, S_{i2} = S_{i3} = 0 \\ 0, \begin{cases} S_{i1} = S_{i3} = 1, S_{i2} = S_{i4} = 0 \\ S_{i1} = S_{i3} = 0, S_{i2} = S_{i4} = 1 \end{cases} \\ 1, S_{i1} = S_{i4} = 0, S_{i2} = S_{i3} = 1 \end{cases} \tag{9}$$

For each HB cell, there is only one situation to create the $+1$ or -1 level, and there are two possible situations to create the 0 level; therefore, a flag is utilized to make the two situations can be selected by turns when 0 level is required. The output voltage level L_V of the single-phase CHB converter is

$$L_V = \sum_{i=1}^{n} H_i \tag{10}$$

The set of possible voltage levels S_{LV} can be expressed as

$$S_{LV} = \{-n, -(n-1), ..., (n-1), n\} \tag{11}$$

The following expression is obtained for the AC-side output voltage u_o

$$u_o = V_{DC} \sum_{i=1}^{n} H_i = V_{DC} L_V \tag{12}$$

Consequently, the differential equation of the injected current of the single-phase CHB converter connected to the distribution network can be obtained as

$$u_o - u = L\frac{di_Z}{dt} + Ri_Z \tag{13}$$

III. PRINCIPLE OF THE PROPOSED 2V-MPC METHOD

A. TRADITIONAL FCS-MPC METHOD

The main idea of the FCS-MPC is to predict the injected current of the next sampling period according to the present states and parameters so that an open-loop optimal control is obtained for each sampling period.

Equation (13) can be discretized using Euler approximation, and the discrete-time model for the CHB converter can be expressed as follows:

$$\hat{i}_Z^{L_V}(k+1) = (1 - R\frac{T_s}{L})i_Z(k) + \frac{T_s}{L}[u_o(k) - u(k)] \tag{14}$$

where $i_Z(k)$,$u_o(k)$ and $u(k)$ are the measured values of i_Z, u_o, and u in the k-th sampling period; T_s is the sampling time and $\hat{i}_Z^{L_V}(k+1)$ is the predicted value of the injected current when the voltage level L_V is applied. The equation will be used to compute the predictive injected current for a given voltage level. To obtain the optimal solution and enhance the dynamic response, the predicted value for each possible level generated by the CHB converter must be calculated. Thus, the number of calculations is $2n+1$ for the CHB converter with n HB cells. The following cost function $g(k+1)$ is used to select the optimal voltage level minimizing the cost, from all the possible voltage levels:

$$\arg\min_{L_V \in S_{LV}} g(k+1) = \left| i_Z^*(k+1) - \hat{i}_Z^{L_V}(k+1) \right| \tag{15}$$

where $i_Z^*(k+1)$ is the predicted value of the reference. For a sufficiently small sampling period, it can be assumed that $i_Z^*(k+1) \approx i_Z^*(k)$. The voltage level selected by the cost function is the best in the set S_{LV}, and its predicted value $\hat{i}_Z^{L_{Vop}}(k+1)$ is closer to the reference than that of other voltage levels. When the system is in transient process or the reference undergoes a sudden change, FCS-MPC can immediately adjust the voltage level by the cost function to track the highly dynamic changes, which is the one of advantages for FCS-MPC.

Because the cost function contains only one variable, when $g(k+1)$ is assumed to be 0, the predicted value of the injected current $\hat{i}_Z^{L_V}(k+1)$ in (14) can be replaced by the reference $i_Z^*(k+1)$. The inverse model can be obtained as

$$u_o(k) = \frac{L}{T_s}[i_Z^*(k+1) - i_Z(k)] + Ri_Z(k) + u(k) \tag{16}$$

Considering the maximum output level of the CHB converter and (12), the optimal voltage level $L_{Vop}(k)$ of the k-th sampling period is given as

$$L_{Vop}(k) = \begin{cases} n, & \dfrac{u_o(k)}{V_{DC}} > n \\ round[\dfrac{u_o(k)}{V_{DC}}], & -n \le \dfrac{u_o(k)}{V_{DC}} \le n \\ -n, & \dfrac{u_o(k)}{V_{DC}} < -n \end{cases} \tag{17}$$

The optimal voltage level is the rounded value of the quotient between $u_o(k)$ and V_{DC}. The voltage levels that exceed the upper and lower bounds are forced to the bounds. Regardless of the number of HB cells, only one calculation is required to obtain the optimal voltage level in the inverse model, which reduces the computational burden effectively and does not deteriorate the performance.

B. IMPROVED 2V-MPC METHOD

Fig. 5(a) shows a diagram of the traditional FCS-MPC method, which applies the optimal voltage level $L_{Vop}(k)$ in the whole k-th sampling period. Therefore, the current error $i_{EE}(k+1)$ at the end of the k-th period can be expressed as

$$i_{EE}(k+1) = i_Z^*(k+1) - \hat{i}_Z^{L_{Vop}}(k+1) \tag{18}$$

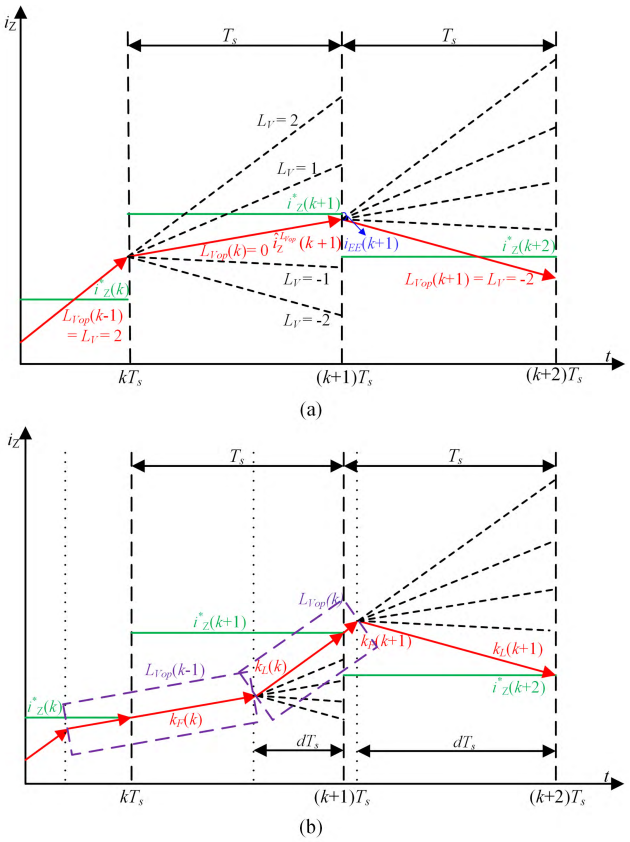


FIGURE 5. Operational diagram of (a) traditional FCS-MPC; (b) improved 2V-MPC.

The extra level can be applied in this sampling period so as to eliminate the current error. Moreover, to ensure that both the extra computational burden and the switching transitions are not significantly increased, the optimal voltage level of the previous period $L_{Vop}(k-1)$ and $L_{Vop}(k)$ can be used as a combination in the k-th sampling period. In this condition, the level increment ΔL_V, namely, the difference between the voltage level of the $(k-1)$-th period and the k-th period, can be derived as

$$\Delta L_V = L_{Vop}(k-1) - L_{Vop}(k) \tag{19}$$

The diagram of the improved 2V-MPC method is shown in Fig. 5(b). In the proposed method, $L_{Vop}(k-1)$ is used as the first level in the k-th sampling period, that is, the voltage level remains invariable in first part of the k-th sampling period. In other words, just one change in level in one period occurs in the middle of the period. Thus, $L_{Vop}(k)$ can be applied in the latter part of the k-th period to ensure that the response is as fast as that of the traditional FCS-MPC method. According to [34], the current slope corresponding to the voltage level can be expressed as

$$k_F = \frac{1}{L}[V_{DC}L_{Vop}(k-1) - u(k) - Ri_Z(k)] \tag{20}$$

$$k_L = \frac{1}{L}[V_{DC}L_{Vop}(k) - u(k) - Ri_Z(k)] \tag{21}$$

where k_F and k_L denote the current slopes of the first part and the latter part, respectively. Under the application of the two voltage levels, the zero current error achieved at the end of k-th period can be expressed by

$$i_Z^*(k+1) = i_Z(k) + k_F(1-d)T_s + k_L dT_s \tag{22}$$

Thus, the duty ratio d can be computed by

$$d = \frac{i_Z^*(k+1) - i_Z(k) - k_F T_s}{(k_L - k_F)T_s} \tag{23}$$

Actually, to achieve the zero error at the end of the period, the adjustment of the optimal voltage level $L_{Vop}(k)$ is required according to $i_{EE}(k+1)$ and ΔL_V. Fig. 6 shows an algorithm flowchart of the improved 2V-MPC method.

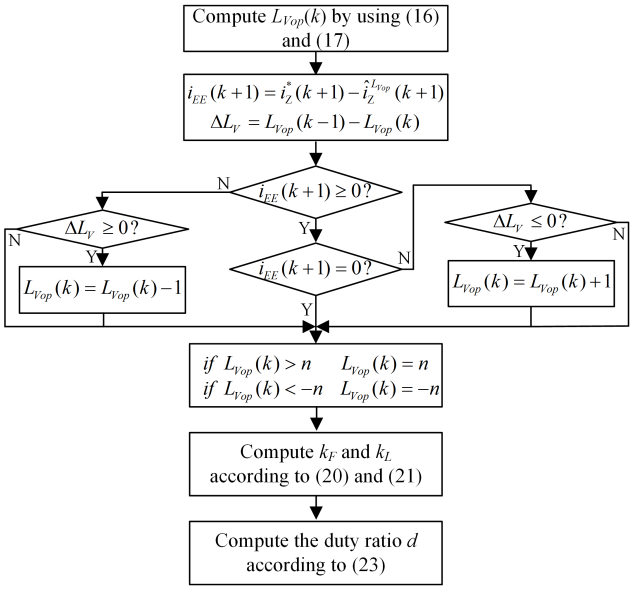


FIGURE 6. Improved 2V-MPC algorithm flowchart.

In the proposed 2V-MPC method, the optimal level $L_{Vop}(k)$ considering all possible levels is applied to achieve faster dynamic response, which is an important characteristic required for the FASD, compared with the method only considering adjacent levels [24], [34]. Moreover, the level $L_{Vop}(k-1)$ is maintained in the first part of the period, meaning that the level changes happening in one period are not more than once.

C. SELECTION OF THE OPTIMAL SWITCHING COMBINATION

With the increase in the number of HB cells, the CHB converter has many switching combinations. According to (9), the total number K of switching combinations is

$$K = 3^n \tag{24}$$

As an example, a single-phase CHB converter with 5 HB cells can generate 11 voltage levels, but the total number of switching combinations is up to 243, which means that there are a large number of redundant switching combinations synthesizing the same voltage levels. The method proposed in [36] makes each voltage level only correspond to one switching combination by the lookup table, eliminating the redundancies completely. However, this method has a problem regarding the imbalance of switching transitions among HB cells. With the increase in runtime, it causes a part of the HB cells to overheat because the number of switching transitions of these HB cells is far higher than those of other ones.

In order to solve the aforementioned problem and select the switching combination, the switching transitions, which correspond to the power losses of power electronic devices, of HB cells are incorporated into the constraints.

Firstly, the switching states of HB cells must satisfy the requirement of the voltage level, that is to say, the total number of the switching states of HB cells is equal to the optimal voltage level. Moreover, the switching transitions in one period should be as low as possible to reduce power losses. Furthermore, the situation of positive and negative switching states cancellation (e.g. the 0 level synthesized by -1 and 1 in a two-cell CHB converter) should be avoided because it reduces the operating efficiency of CHB converter. Thus, three constraints can be obtained as follows:

$$\sum_i^n H_i(k) = L_{Vop}(k) \tag{25a}$$

$$\sum_i^n |\Delta H_i(k)| = \left|L_{Vop}(k) - L_{Vop}(k-1)\right| = |\Delta L_V| \tag{25b}$$

$$\sum_i^n |H_i(k)| = \left|L_{Vop}(k)\right| \tag{25c}$$

where $|\Delta H_i(k)|$ is the number of the switching transitions of the i-th HB cell in the k-th sampling period. In addition, the balance of the switching transition among HB cells needs to be considered, which affects the heat of power electronic devices, and then determines the specification of cooling devices. The balance degree of switching transitions can be expressed by the standard deviation coefficient V_σ as follows:

$$V_\sigma = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}(\sum_{j=1}^{\Delta t}|\Delta H_i(k+j-\Delta t)| - \bar{n}_{st})^2}}{\bar{n}_{st}}, \quad k \geq \Delta t \tag{26}$$

where $\bar{n}_{st}$ is the average value of the switching transitions over multiple periods Δt, and it can be expressed as

$$\bar{n}_{st} = \frac{1}{n}\sum_{i=1}^{n}\sum_{j=1}^{\Delta t}|\Delta H_i(k+j-\Delta t)|, \quad k \geq \Delta t \tag{27}$$

Therefore, the selection of switching combinations is an optimization problem as follows:

$$\begin{aligned} &\arg\min_{S_{sc}(k)} \ V_\sigma \\ &\text{subject to: (25a)} - \text{(25c)} \end{aligned} \tag{28}$$

where $S_{ss}(k)$ is the switching sequence over multiple periods Δt, and $S_{ss}(k) = \{S_{sc}(k-\Delta t+1), \ldots, S_{sc}(k)\}$; $S_{sc}(k)$ is the switching combination of the k-th period, and $S_{sc}(k) = \{H_1(k), \ldots, H_n(k)\}$.

According to (25)–(28), the switching combination will be adjusted and selected according to the switching sequence in the past to solve the optimization problem. The optimization problem can be incorporated into the cost function in view of the principle of FCS-MPC; however, all switching combinations need to be considered and the time complexity is exponential, which is unbearable for CHB multilevel converter. To obtain the optimal switching combination satisfying the constraints within the appropriate time, a novel method is proposed, and its implementation steps are as follows:

Step 1: Sort all HB cells randomly to obtain the random sequence S_{ran} and sort out the present switching states of HB cells. N_1, N_0, and N_{-1} denote the number of HB cells whose switching states are 1, 0 and -1, respectively. Taking the CHB converter with 5 HB cells as an example, as shown in Fig. 7, it is assumed that the original switching combination $S_{sc}(k-1)$ is $\{-1, 0, 1, -1, 0\}$, and the corresponding random sequence $S_{ran}(k)$ is $\{3, 4, 5, 1, 2\}$. In this example, N_1, N_0, N_{-1} and $L_{Vop}(k-1)$ are equal to 1, 2, 2 and -1, respectively.

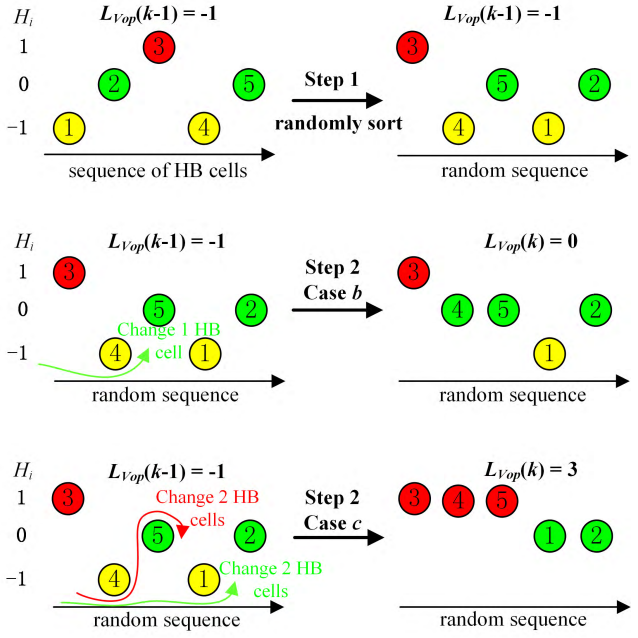


FIGURE 7. Schematic diagram of the process of selecting switching combination.

Step 2: The proposed method has the following cases:

Case a: If $L_{Vop}(k-1) = L_{Vop}(k)$, then skip to Step 3.

Case b: If $L_{Vop}(k-1) < L_{Vop}(k)$ and $L_{Vop}(k-1) + N_{-1} \geq L_{Vop}(k)$, then select the first $|\Delta L_V|$ HB cells, whose switching state is -1, of the random sequence and make their switching states change to 0. Continuing the example, if $L_{Vop}(k)$ is 0, then cell 4 is selected because of the front rank in the random sequence. The switching state of this HB cell is set to 0. Finally, the switching combination $S_{sc}(k) = \{-1, 0, 1, 0, 0\}$ is obtained.

Case c: If $L_{Vop}(k-1) < L_{Vop}(k)$ and $L_{Vop}(k-1) + N_{-1} < L_{Vop}(k)$, then change the switching states of all HB cells that output negative levels to 0 from -1. Next, select the first $(|\Delta L_V| - N_{-1})$ cells, whose switching state is 0, of the random sequence and set their switching states to 1. Continuing the example, $L_{Vop}(k)$ is assumed to be 3, and the switching states of cell 1 and cell 4 are changed to 0. Next, the switching states of cell 4 and cell 5 are set to 1 according to the random sequence. Finally, the switching combination $S_{sc}(k) = \{0, 0, 1, 1, 1\}$ is obtained.

Because the case where $L_{Vop}(k-1) > L_{Vop}(k)$ and $L_{Vop}(k-1) - N_1 \leq L_{Vop}(k)$ is similar to Case b and the case where $L_{Vop}(k-1) > L_{Vop}(k)$ and $L_{Vop}(k-1) - N_1 > L_{Vop}(k)$ is similar to Case c, these cases will not be described further in this paper.

Step 3: The switching combination obtained in Step 2 is converted to the corresponding switching signals assigned to all the HB cells.

Note that the original switching combination of this example is only possible to appear in the beginning of the proposed method. The positive switching states will not coexist with the negative switching states after several periods.

The switching combinations selected by the proposed approach is not the global optimum solution, which could not get the optimal values in some period. However, because of the randomness of the method, the HB cells at the same switching state have the same probability of being selected. According to the law of large numbers, switching transitions among HB cells will be balanced with the increase in runtime. When $\Delta t \to \infty$, there is $V_\sigma \to 0$; therefore, the selected switching combinations can be regarded as the local optimal solution, which is easily applied in the existing devices.

D. TIME-CONSUMPTION ANALYSIS AND IMPLEMENTATION STEPS

Time consumption of each algorithm can be represented by estimating the instruction cycles. Because the basic operations like addition, multiplication and division are used in different algorithms, the instruction set of ARM Cortex-M4 with floating point unit (FPU) shown in Table 1 is utilized as the reference to provide an evaluation criteria for time consumption. In order to reduce the computation burden,

TABLE 1. Instruction cycle of basic operation based on ARM Cortex-M4.

Operation	Cycles	Operation	Cycles
Addition/Subtraction	1	Multiplication	1
Division	14	Compare	1
Absolute value	1	Move	1
Load(lookup table)	n+1	Square-root	14

the operations among parameters including sampling period and filter inductance can be pre-calculated and used as the constants in the algorithm.

The methods compared are divided into two types: current-control MPC and switching combination selection method. The maximum computation of each algorithm under the worst condition is considered, and the results are summarized in Table 2 in form of the total cycles.

TABLE 2. Time consumption results of different algorithms.

Type	Algorithm	Total cycles
Current-control MPC	Traditional FCS-MPC [19]	$12(2n+1)+2$
	General 2V-MPC [31]	$131(2n+1)^2+14$
	Simplified 2V-MPC [31]	$142(2n+1)+14$
	Low-complexity 2V-MPC [32]	110
	Adjacent-level 2V-MPC [34]	40
	Proposed improved 2V-MPC	61
Switching combination selection method	Lookup-table method [36]	$n+1$
	Exhaustive method using cost function [30]	$3^n(21n+41)+3$
	Proposed optimal algorithm	$15n+9$

As can be seen, whether current-control MPC or switching combination selection method, the time consumption of the proposed algorithms is not the lowest. However, their time complexity is in the same order of magnitude as that of the time-saving algorithms.

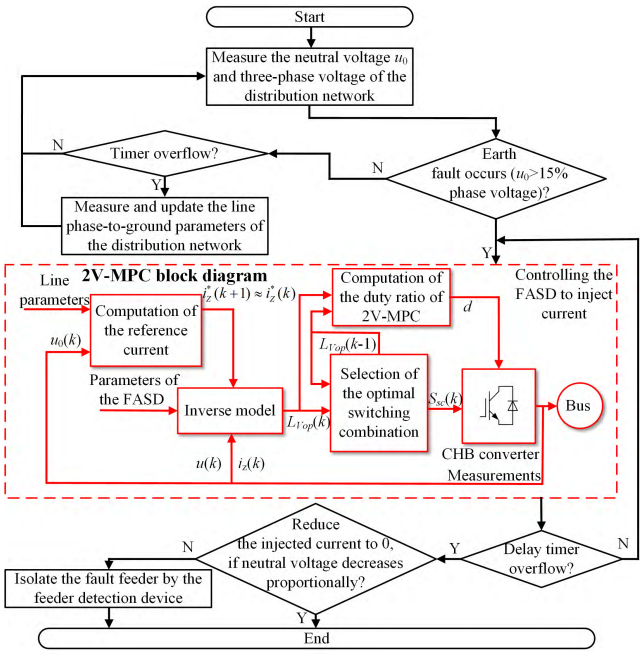


FIGURE 8. Diagram of implementation steps.

The implementation flowchart of the proposed arc-suppression method is illustrated in Fig. 8, which also includes a block diagram of the improved 2V-MPC. First, the neutral voltage and three-phase voltage are measured to detect the earth fault. If the earth fault does not occur, the line phase-to-ground parameters of the distribution network are measured periodically, which can adapt to changes in network topology. Otherwise, the proposed arc-suppression method based on the improved 2V-MPC is applied in FASD, and then a current is injected to the distribution network for compensating the fault current. After a certain delay, the injected current is reduced to check whether a proportional decrease in neutral voltage occurs to identify the type of earth fault. Last, the earth fault is isolated by the feeder detection device if the earth fault is permanent.

IV. ANALYSIS OF THE PROPOSED ARC-SUPPRESSION METHOD

According to (3) and (4), when the injected current is equal to the reference current, the fault current can be completely compensated to 0. Because of restrictions on hardware devices and control strategies, there is an error between the injected current and the reference. Therefore, the current tracking capability of control methods is the main factor that actually affects the arc-suppression performance. The steady-state current error I_{SSE}, which is used to measure the tracking capability, is defined as the average of the absolute differences between the reference and injected current. Fig. 9 shows a typical current tracking process of the improved 2V-MPC at steady state; its current error can be analyzed.

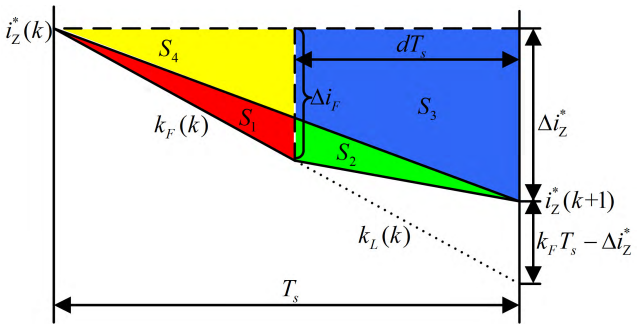


FIGURE 9. Analytical diagram of the current error of improved 2V-MPC.

It is assumed that the current error at the end of the period is equal to zero. The steady-state current error can be obtained as

$$\begin{aligned} I_{SSE} &= \frac{1}{T_s}(S_1+S_2) = \frac{1}{T_s}[(S_1+S_4)+(S_2+S_3)-(S_3+S_4)] \\ &= \frac{1}{T_s}[\frac{1}{2}T_s(1-d)\Delta i_F+\frac{1}{2}T_s d(\Delta i_Z^*+\Delta i_F)-\frac{1}{2}T_s\Delta i_Z^*] \\ &= \frac{1}{2}[\Delta i_F-(1-d)\Delta i_Z^*] \end{aligned} \tag{29}$$

where Δi_F is the current increment of the first part and $\Delta i_F = k_F(1-d)T_s$; Δi_Z^* is the difference between $i_Z^*(k)$ and $i_Z^*(k+1)$; S_1, S_2, S_3 and S_4 stand the areas of the red, green, blue and yellow regions in Fig. 9, respectively.

Therefore, the following equation is deduced:

$$I_{SSE} = \frac{1}{2}(1-d)(k_F T_s - \Delta i_Z^*) \tag{30}$$

For the traditional FCS-MPC method, when the injected current can keep track of the reference steadily, the following relationship is valid:

$$\hat{i}_Z^{L_V}(k+1) \le i_Z^*(k+1) \le \hat{i}_Z^{L_V+1}(k+1) \tag{31}$$

where $\hat{i}_Z^{L_V}(k+1)$ and $i_Z^{L_V+1}(k+1)$ are the predicted values of the injected current when the voltage level is equal to L_V and L_V+1, respectively. Consequently, the current error at the end of the period satisfies the following equation:

$$|i_{EE}(k+1)| = \left|i_Z^*(k+1) - i_Z(k) - k_L T_s\right| \le \frac{1}{2}\frac{V_{DC}T_s}{L} \tag{32}$$

According to (19), there is the following relationship:

$$k_F T_s - \Delta i_Z^* \le (|\Delta L_V| + \frac{1}{2})\frac{V_{DC}T_s}{L} \tag{33}$$

By substituting (23), (32) and (33) into (30), I_{SSE} can be expressed as follows:

$$\begin{aligned} I_{SSE} &\le \frac{\frac{1}{2}(|\Delta L_V| + \frac{1}{2})}{2|\Delta L_V|}\frac{V_{DC}T_s}{L} = \frac{2|\Delta L_V|+1}{8|\Delta L_V|}\frac{V_{DC}T_s}{L} \\ &\approx \frac{V_{DC}T_s}{4L} \end{aligned} \tag{34}$$

It is vital for the FASD to enhance the arc-suppression performance by reducing the steady-state error. To improve the tracking performance, it is necessary to reduce the steady-state current error through reductions of the sampling time T_s and the DC-side voltage V_{DC}, or an increase in the filter inductance L.

Furthermore, the CHB converter must be adapted to the change rate of the reference without leaving the injected current off track. Thus, the change rate of the predictive injected current must satisfy the following equation:

$$\begin{aligned} \max\left[\frac{d\hat{i}_Z^{L_V}(k+1)}{dT_s}\right] &= \max\left[\frac{u_o(k) - u(k) - Ri_Z(k)}{L}\right] \\ &\ge \max\left[\frac{di_Z^*(k+1)}{dT_s}\right] \end{aligned} \tag{35}$$

According to (35), obviously, the maximum output voltage u_{om} of the converter determines the maximum current change rate of the injected current in the case of a given filter inductance L. The appropriate u_{om} can maintain the stable tracking capability of injected current and track highly dynamic changes in the reference current within a few control cycles [29]. Considering the stability under the extreme condition, the u_{om} should be determined in terms of the peak value of phase voltage during normal operation and a certain sufficient margin.

Equation (36) can be evaluated to determine the DC-side voltage and the number of HB cells.

$$V_{DC} = \frac{u_{om}}{n} \tag{36}$$

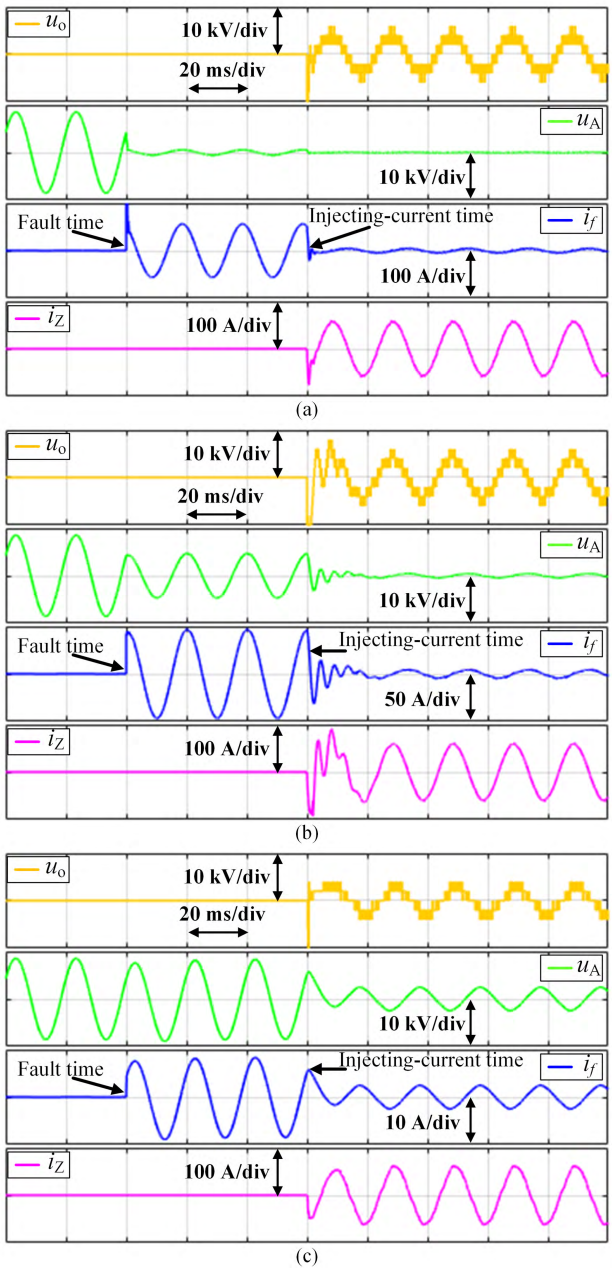


FIGURE 10. Simulation waveforms of the output voltage (u_o), the fault-phase voltage (u_A), the fault current (i_f) and the injected current (i_Z) with (a) 10 Ω earth-fault resistance; (b) 100 Ω earth-fault resistance; (c) 1000 Ω earth-fault resistance.

It can be seen that the DC-side voltage will be decreased with the increase in HB cells, thereby reducing the I_{SSE} in (34). In addition, the increase in HB cells improves the withstand voltage of the CHB converter and reduce the switching frequency of a single HB cell; however, it also increases the cost and control difficulty.

For discrete data, the steady-state current error can be calculated as

$$I_{SSE} = T_s \sum_{k=1}^{1/T_s} \left|i_Z^*(k) - i_Z(k)\right| \tag{37}$$

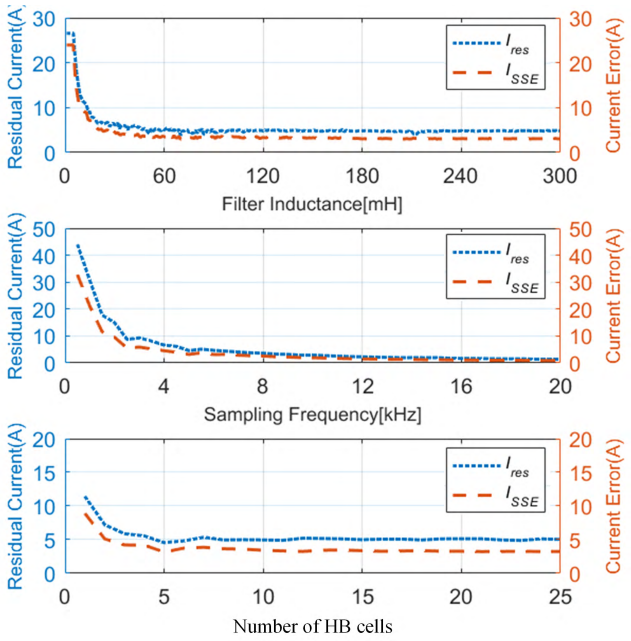


FIGURE 11. Simulation results of the residual current (I_{res}) and the steady-state current error (I_{SSE}) of different parameters.

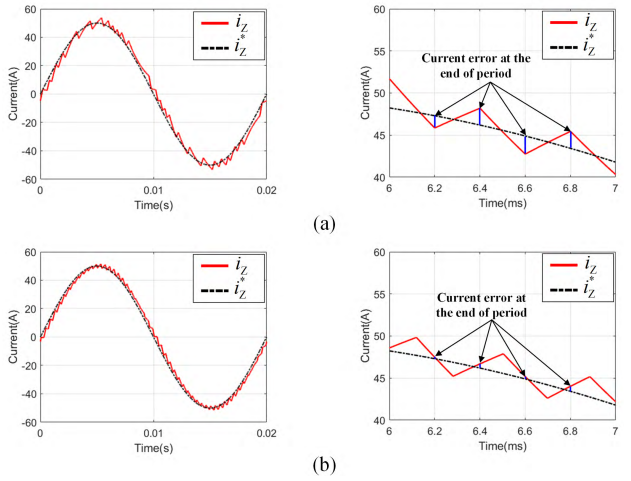


FIGURE 12. Simulation waveforms of the tracking process by using (a) traditional FCS-MPC; (b) improved 2V-MPC.

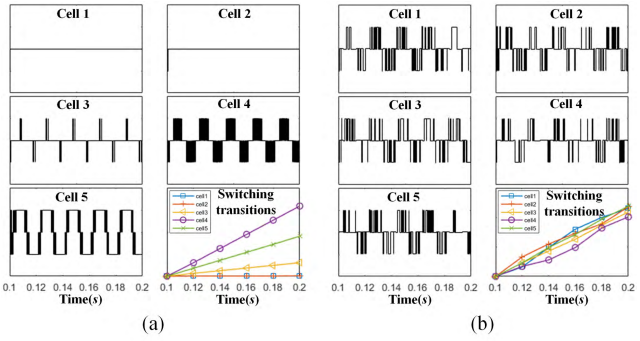


FIGURE 13. Simulation waveforms of the switching states and the number of switching transitions of each HB cell by using (a) lookup-table method; (b) proposed switching combination selection method.

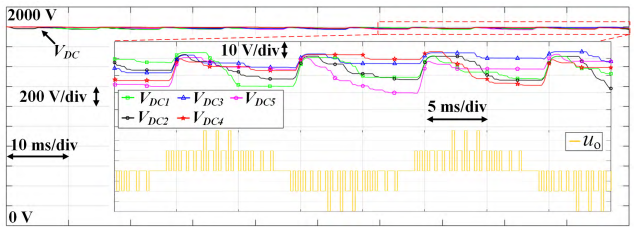


FIGURE 14. Simulation waveforms of the DC-side voltage of HB cells and the voltage level of CHB converter.

TABLE 3. Default parameters of the simulation.

	Parameters	Value
Distribution network	Leakage resistance r_0	30kΩ
	Phase-to-ground capacitance C_0	7μF
	Earth-fault resistance R_f	10Ω, 100Ω, 1000Ω
	Grid frequency f	50Hz
Proposed FASD	Sampling time T_s	200μs
	Filter inductance L	50mH
	The number of HB cells n	5
	DC-side voltage V_{DC}	2000V
	DC-side capacitance C	4000μF
	Current limiting resistance R	30Ω

V. SIMULATION RESULTS

To validate the feasibility of the arc-suppression method in the paper, a simulation model in MATLAB/Simulink for the 10-kV distribution network is shown in Fig. 1. The FASD is connected to the bus of the main transformer outlet. The main parameters of the distribution network are listed in Table 3. The parameters of the FASD are also presented in this table. Note that the certain current limiting resistance is necessary, thus constraining the inject current within the bearable extent and preventing transient shock because the access of FASD is a typical transient process. To compare the change in the waveform before and after the FASD is implemented, the earth fault starts at 0.04 s and the device operates at 0.10 s.

The simulation waveforms of the arc-suppression process are shown in Fig. 10. Fig. 10(a) represents the arc-suppression process when the earth-fault resistance is 10 Ω. When an earth fault occurs, the fault-phase voltage drops, and high current appears at the fault point with violent transient changes. At this time, the fault current has a peak value because the fault-phase voltage is declining and the distribution network has been earthed through the earth-fault resistance. Next, the phase-A CHB converter is accessed to the distribution network and the compensation current starts to be injected. Obviously, the fault-phase voltage is further suppressed to near 0; the fault current also drops to 3.1 A from 40.1 A, which is not adequate to rekindle the arc again. The simulation results of 100 Ω and 1000 Ω earth-fault resistances

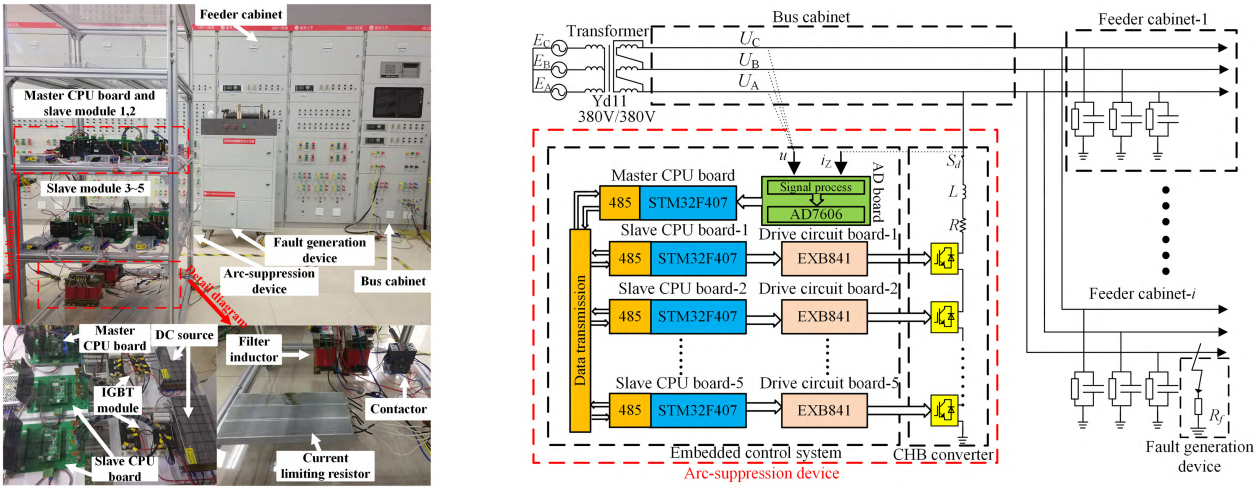


FIGURE 15. Experimental system: (a) laboratory prototypes of the distribution network and the FASD; (b) schematic diagram of the experimental system.

are shown in Fig. 10(b) and (c), respectively. Compared with Fig. 10(a), the fault-phase voltage maintains a higher value and the fault current is lower because of the larger earth-fault resistance. After the compensation current is injected, the fault current undergoes a brief oscillation and then drops into the steady state that can maintain the extinguishing of arc. Note that the injected current is irregular and has sudden changes. The simulation results prove that the proposed arc-suppression method can adapt the situations of different earth-fault resistances in the 10-kV distribution network.

Fig. 11 shows the tracking and arc-suppression performance of different parameters of the FASD, where the root mean square value I_{res} of the residual current and the steady-state current error I_{SSE} are given. It can be verified that the better tracking capability brings the better arc-suppression effect. Moreover, it can validate the positive correlation between I_{res} and I_{SSE}. With the increases in the filter inductance and the number of HB cells (u_{om} stays constant), I_{res} and I_{SSE} drop obviously in the beginning, but they do not vary evidently when the parameters reach a certain value because of the error from replacing $i_{\mathrm{Z}}^{*}(k+1)$ with $i_{\mathrm{Z}}^{*}(k)$. Therefore, increasing the sampling frequency shortens the error between $i_{\mathrm{Z}}^{*}(k+1)$ and $i_{\mathrm{Z}}^{*}(k)$ and can reduce I_{res} and I_{SSE} proportionally.

Fig. 12 shows the tracking process of the traditional FCS-MPC and the improved 2V-MPC. The current error can be eliminated at the end of sampling period by using the improved 2V-MPC. To further assess the performance of the proposed 2V-MPC, the comparative results of two FCS-MPC methods are summarized in Table 4. It can be concluded that the 2V-MPC can effectively reduce the steady-state current error because two voltage levels are applied in one sampling period to achieve the zero error at the end of the period; however, as no switching transition takes place in some periods with the traditional FCS-MPC, the average switching frequency of the 2V-MPC is larger than this one of the traditional MPC. In such a situation, it is considered that the increased switching frequency achieves the further fine tuning of current to obtain the better current accuracy.

TABLE 4. Simulation results by using different methods.

	Traditional FCS-MPC	Improved 2V-MPC
I_{SSE} (A)	5.89	3.43
Average switching frequency of CHB converter (Hz)	3850	5000

Fig. 13 represents the results of the switching states of each HB cell and the switching transitions obtained by using the lookup-table method in [36] and the proposed switching combination selection method. It can be observed from Fig. 13(a) that the switching transitions among cells are extremely unbalanced. Some HB cells (such as cell 4 and cell 5) frequently switch; however, other HB cells (such as cell 1 and cell 2) no longer switch at steady state. Therefore, in the lookup-table method, some HB cells severely heat but others are not fully utilized. In Fig. 13(b), it is clear that the switching transitions are distributed evenly among the HB cells compared with Fig. 13(a). In Table 5, the results of different runtimes can be observed. The standard deviation coefficient V_{σ} will significantly decrease as the runtime increases. This result proves that switching transitions will be more balanced with the continuous operation of the FASD.

Fig. 14 shows the DC-side voltage of each HB cell and the voltage level of the CHB converter in the arc-suppression process. It can be observed that the ripples of the DC-side voltage are less than 1% via the large capacitance and auxiliary source. Therefore, the DC side of the HB cell can be considered to be parallel to a stable DC source.

TABLE 5. Results of switching transitions in different runtimes.

Runtime(s)	Number of switching transitions						Standard deviation coefficient V_σ (%)
	Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Average	
0.5	462	488	508	511	531	500	4.7
1	962	977	1014	1007	1037	999	2.7
2	1957	1941	1995	2042	2054	1998	2.2
3	2926	3020	2959	3048	3035	2998	1.6
5	5040	4933	4985	5006	5020	4997	0.7

VI. PROTOTYPE AND EXPERIMENTAL RESULTS

A FASD prototype that consists of an 11-level CHB converter with 5 HB cells is shown in Fig. 15(a). Each HB cell has two insulated gate bipolar transistor half-bridge modules (Infineon BSM150GB120DLC). Experiments were conducted in a 380-V dynamic simulation distribution network, and a schematic diagram of the experimental system appears in Fig. 15(b). The control method are realized by using a master CPU board and 5 slave CPU boards (ARM Cortex-M4 based STM32F407), and the master-slave communication is achieved by RS485. Thus, the sampling frequency is affected by the performance of CPU and RS485. The DC side of the HB cell equips an 80-V DC source directly. Thus, the maximum output voltage of the prototype is 400 V. The rest of the parameters are consistent with Table 3.

A series of experiments with the same earth-fault resistance as those in the simulation are implemented to further verify the effectiveness of the proposed method at 380 V voltage rank. Fig. 16 shows the experimental waveforms of the arc-suppression process for different earth-fault resistances. When the control system detects the earth fault, it controls the FASD to work and simultaneously control the contactor to close. It can be observed that there is a short delay between the closing-contactor time and the injecting-current time because of the working principle of the contactor. Because of the current limiting resistance, the high transient peak value does not appear in the injected current when the contactor is closed. Moreover, it can be seen that the fast dynamic response is achieved by the improved 2V-MPC method, thereby effectively reducing the setting time. The fault current is suppressed from 1.15 A to 0.25 A, from 0.98 A to 0.18 A, and from 0.54 A to 0.14 A when the earth-fault resistance is 10 Ω, 100 Ω, and 1000 Ω, respectively. In addition, the injected current contains a lot of harmonics in order to track its reference. After the fault current is compensated, it can be seen from Fig. 16 that the harmonic content of the residual current and phase voltage increases evidently because of the low current of experiment system and the current error between the injected current and the fault current. However, when the earth fault occurs, it is acceptable for the uninterrupted operation of distribution network where the security is guaranteed by using FASD to suppress the fault current effectively, even if the harmonics is introduced and then the power quality declines at that time.

The comparative experiments of current tracking are carried out, and the experimental results are illustrated in Fig. 17 and Table 6. It is shown that the traditional

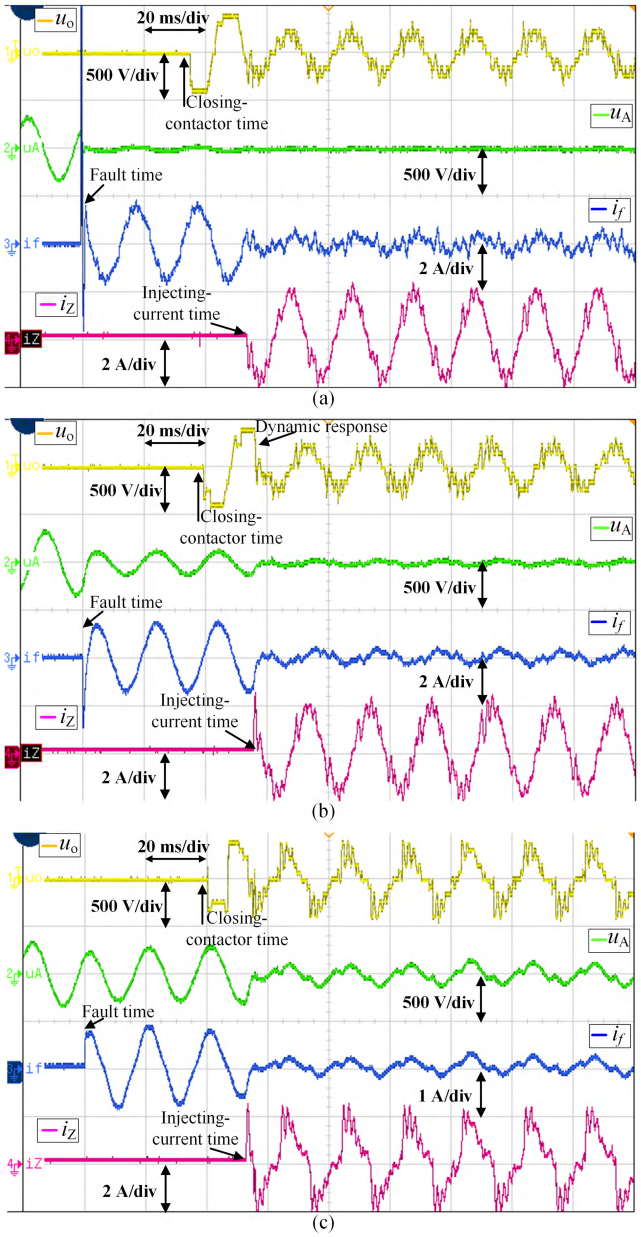


FIGURE 16. Experimental waveforms of the output voltage (u_o), the fault-phase voltage (u_A), the fault current (i_f) and the injected current (i_Z) with (a) 10 Ω earth-fault resistance; (b) 100 Ω earth-fault resistance; (c) 1000 Ω earth-fault resistance.

FCS-MPC method in Fig. 17(a) causes fewer switching transitions because the voltage level of the CHB converter remains constant in some sampling periods. However, the

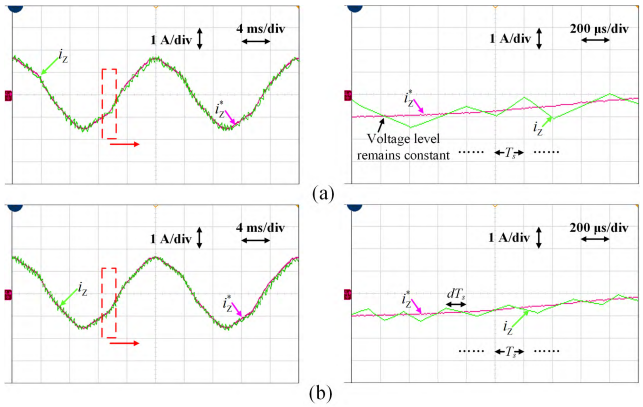


FIGURE 17. Experimental waveforms of the tracing process obtained by using: (a) traditional FCS-MPC; (b) improved 2V-MPC.

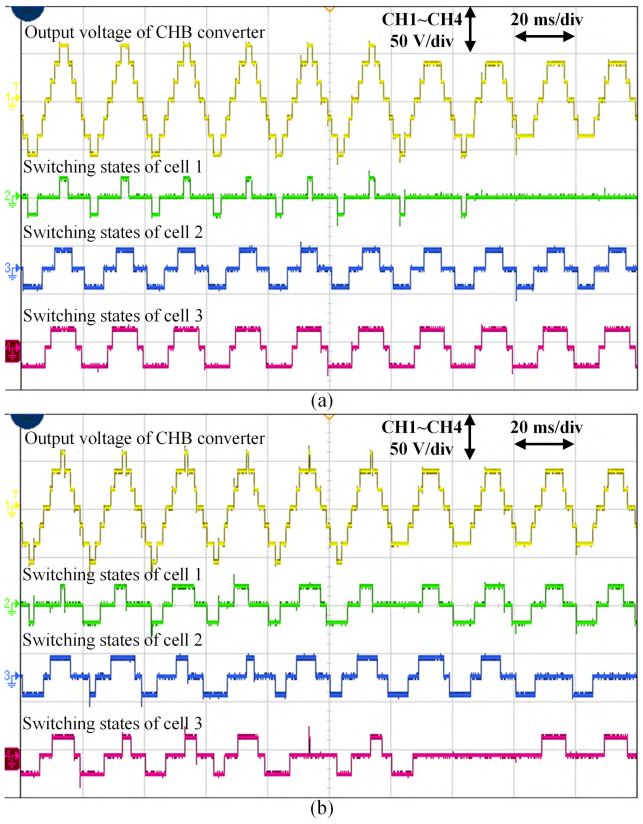


FIGURE 18. Experimental waveforms of the output voltage level of the CHB converter with 3 HB cells by using: (a) lookup-table method; (b) proposed switching combination selection method.

current error is larger than that in Fig. 17(b). In addition, the current error at the end of the sampling period is reduced but does not reach zero because of the measurement error. It can be seen from Table 6, there is in correspondence between the experimental results and the simulation results shown in Table 4. However, its performance enhancement brought by the 2V-MPC method is less than the simulation results, which is caused by the computational delay.

TABLE 6. Experimental results by using different methods.

	Traditional FCS-MPC	Improved 2V-MPC
I_{SSE} (A)	0.198	0.146
Average switching frequency of CHB converter (Hz)	3620	5000

Because of the limit of the number of oscilloscope channels, the waveforms of the voltage level of the CHB converter for only 3 HB cells are shown in Fig. 18. Fig. 18(a) shows that cell 3 outputs voltage most of the time, whereas cell 1 switches only when the maximum voltage is outputted. In contrast, Fig. 18(b) shows that the switching transitions of every HB cell obviously exhibit randomness; thus, switching transitions and the time of output both are distributed evenly among the HB cells.

VII. CONCLUSION

An arc-suppression method based on an improved 2V-MPC was presented in this paper; the proposed method adopts a three-phase CHB converter with auxiliary sources as the FASD. The FASD achieving the stability of the DC-side voltage can ensure steady operation of the arc-suppression process. The combination of two voltage levels in a sampling period is applied in the proposed method to minimize the steady-state current error and reduce the requirement of the sampling frequency of the traditional FCS-MPC. Moreover, the fast dynamic response is inherited by the improved 2V-MPC. Because of the dynamic response and tracking capability of the improved 2V-MPC, the proposed method can achieve an excellent arc-suppression performance and adapt to the situation with different earth-fault resistance values.

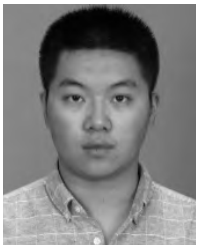
A novel switching combination selection method was proposed. The balanced switching transitions among HB cells can be achieved by this method. The analysis of the parameters of the FASD was also validated. The changes in filter inductance, DC-side voltage and sampling frequency can determine the tracking capability of the improved 2V-MPC and thus further affect the arc-suppression performance. Finally, the proposed methods were verified by the 10-kV simulation system and 380-V experimental platform. Future work will be focused on the realization of the 10-kV prototype as well as the control and switching operation of multiple functions.

REFERENCES

[1] M. F. Guo and N. C. Yang, "Features-clustering-based earth fault detection using singular-value decomposition and fuzzy c-means in resonant grounding distribution systems," *Int. J. Elect. Power Energy Syst.*, vol. 93, pp. 97–108, Dec. 2017.

[2] M. Rošer and G. Štumberger, "Improving the power supply reliability in resonant earthed systems by fault current path control established through Faulted Phase earthing Switch," *Int. J. Elect. Power Energy Syst.*, vol. 64, pp. 714–722, Jan. 2015.

[3] A. M. Dan, Z. Czira, and D. Raisz, "Decreasing the harmonic content of the fault current during single-phase to ground faults in compensated network," in *Proc. IEEE Bucharest Power Tech. Conf.*, Jun./Jul. 2009, pp. 2497–2501.
[4] W. Wang, X. Zeng, L. Yan, X. Xu, and J. M. Guerrero, "Principle and control design of active ground-fault arc suppression device for full compensation of ground current," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4561–4570, Jun. 2017.
[5] M. Janssen, S. Kraemer, R. Schmidt, and K. Winter, "Residual current compensation (RCC) for resonant grounded transmission systems using high performance voltage source inverter," in *Proc. IEEE PES Transmiss. Distrib. Conf. Expo.*, vol. 2, Sep. 2003, pp. 574–578.
[6] P. Wang, B. Chen, C. Tian, B. Sun, M. Zhou, and J. Yuan, "A novel neutral electromagnetic hybrid flexible grounding method in distribution networks," *IEEE Trans. Power Del.*, vol. 32, no. 3, pp. 1350–1358, Jun. 2017.
[7] J. Tian, Q. Chen, L. Cheng, and Y. Zhang, "Arc-suppression coil based on transformer with controlled load," *IET Electr. Power Appl.*, vol. 5, no. 8, pp. 644–653, Sep. 2011.
[8] Y. Qu, W. Tan, and Y. Yang, "H-infinity control theory apply to new type arc-suppression coil system," in *Proc. Int. Conf. Power Electron. Drive Syst.*, 2007, pp. 1753–1757.
[9] Z. Yang, J. Sun, S. Li, M. Huang, X. Zha, and Y. Tang, "An adaptive carrier frequency optimization method for harmonic energy unbalance minimization in a cascaded H-bridge-based active power filter," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1024–1037, Feb. 2018.
[10] L. Wu and W. Mingli, "Single-phase cascaded H-bridge multi-level active power filter based on direct current control in AC electric railway application," *IET Power Electron.*, vol. 10, no. 6, pp. 637–645, Apr. 2017.
[11] Y. Zhang, X. Wu, X. Yuan, Y. Wang, and P. Dai, "Fast model predictive control for multilevel cascaded H-bridge STATCOM with polynomial computation time," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 5231–5243, Aug. 2016.
[12] Y. Zhang, X. Wu, and X. Yuan, "A simplified branch and bound approach for model predictive control of multilevel cascaded H-bridge STATCOM," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 7634–7644, Oct. 2017.
[13] D. Lu *et al.*, "Clustered voltage balancing mechanism and its control strategy for star-connected cascaded H-bridge STATCOM," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 7623–7633, Oct. 2017.
[14] A. Sanchez-Ruiz, M. Mazuela, S. Alvarez, G. Abad, and I. Baraia, "Medium voltage–high power converter topologies comparison procedure, for a 6.6 kV drive application using 4.5 kV IGBT modules," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1462–1476, Mar. 2012.
[15] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.
[16] F. Wang, M. Guo, and G. Yang, "Novel arc-suppression methods based on cascaded H-bridge converter," in *Proc. Asia–Pacific Int. Symp. Electromagn. Compat.*, 2016, pp. 691–694.
[17] Y. Neyshabouri and H. Iman-Eini, "A new fault-tolerant strategy for a cascaded H-bridge based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6436–6445, Aug. 2018.
[18] S. Kouro, P. Cortes, R. Vargas, U. Ammann, and J. Rodriguez, "Model predictive control—A simple and powerful method to control power converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1826–1838, Jun. 2009.
[19] J. Rodríguez *et al.*, "State of the art of finite control set model predictive control in power electronics," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 1003–1016, May 2013.
[20] Y. Yang, H. Wen, and D. Li, "A fast and fixed switching frequency model predictive control with delay compensation for three-phase inverters," *IEEE Access*, vol. 5, pp. 17904–17913, 2017.
[21] P. Karamanakos, K. Pavlou, and S. Manias, "An enumeration-based model predictive control strategy for the cascaded H-bridge multilevel rectifier," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3480–3489, Jul. 2014.
[22] C. Qi, X. Chen, P. Tu, and P. Wang, "Cell-by-cell-based finite-control-set model predictive control for a single-phase cascaded H-bridge rectifier," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1654–1665, Feb. 2018.
[23] Z. Gong *et al.*, "A hierarchical model predictive voltage control for NPC/H-bridge converters with a reduced computational burden," *J. Power Electron.*, vol. 17, no. 1, pp. 136–148, 2017.
[24] P. Cortes, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu-Rub, "Model predictive control of multilevel cascaded H-bridge inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2691–2699, Aug. 2010.
[25] I. Kim, R. Chan, and S. Kwak, "Model predictive control method for CHB multi-level inverter with reduced calculation complexity and fast dynamics," *IET Electr. Power Appl.*, vol. 11, no. 5, pp. 784–792, May 2017.
[26] R. Baidya, R. P. Aguilera, P. Acuña, S. Vazquez, and H. du Toit Mouton, "Multistep model predictive control for cascaded H-bridge inverters: Formulation and analysis," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 876–886, Jan. 2018.
[27] R. P. Aguilera, P. Lezana, and D. E. Quevedo, "Finite-control-set model predictive control with improved steady-state performance," *IEEE Trans Ind. Informat.*, vol. 9, no. 2, pp. 658–667, May 2013.
[28] L. Tarisciotti, P. Zanchetta, A. Watson, S. Bifaretti, and J. C. Clare, "Modulated model predictive control for a seven-level cascaded H-bridge back-to-back converter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5375–5383, Oct. 2014.
[29] C. Townsend, T. J. Summers, and R. E. Betz, "Multigoal heuristic model predictive control technique applied to a cascaded H-bridge StatCom," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1191–1200, Mar. 2012.
[30] C. D. Townsend, T. J. Summers, J. Vodden, A. J. Watson, R. E. Betz, and J. C. Clare, "Optimization of switching losses and capacitor voltage ripple using model predictive control of a cascaded H-bridge multilevel StatCom," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3077–3087, Jul. 2013.
[31] S. Kwak, S.-E. Kim, and J.-C. Park, "Predictive current control methods with reduced current errors and ripples for single-phase voltage source inverters," *IEEE Trans. Ind. Informat.*, vol. 11, no. 5, pp. 1006–1016, Oct. 2015.
[32] Q. Chen, X. Chen, P. Tu, and P. Wang, "Low-complexity two-voltage-based model predictive control for a single-phase cascaded H-bridge inverter," in *Proc. Int. Future Energy Electron. Conf. ECCE Asia*, Jun. 2017, pp. 1440–1444.
[33] C. Qi, X. Chen, P. Tu, and P. Wang, "Deadbeat control for a single-phase cascaded H-bridge rectifier with voltage balancing modulation," *IET Power Electron.*, vol. 11, no. 3, pp. 610–617, Mar. 2018.
[34] F. Ma, Z. He, Q. Xu, A. Luo, L. Zhou, and M. Li, "Multilevel power conditioner and its model predictive control for railway traction system," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7275–7285, Nov. 2016.
[35] M. A. Perez, P. Cortes, and J. Rodriguez, "Predictive control algorithm technique for multilevel asymmetric cascaded H-bridge inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 12, pp. 4354–4361, Dec. 2008.
[36] J. Han, M. Zhao, D. Peng, and T. Tang, "Improved model predictive current control of cascaded H-bridge multilevel converter," in *Proc. IEEE Int. Symp. Ind. Electron.*, May 2013, pp. 1–5.



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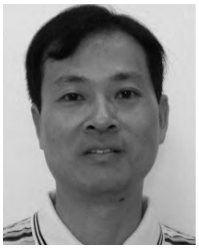

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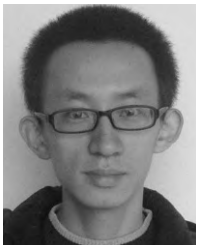

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