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Printed Spiral Resonator for Displacement-Tolerant Near-Field Wireless Energy Transfer

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ABSTRACT Synthesis between the printed spiral coil and the planar interdigital capacitor for near-field wireless energy transfer (WET) is proposed. The proposed amalgamated design is intentionally positioned under several displacements, namely, planar offsets at the z-axis as well as lateral offsets at both the x- and y-axes to investigate tolerance capability. This is particularly crucial in practical circumstances, whereby a perfect alignment between primary and secondary resonators is not usually achieved unless with the integration of magnet plates to aid seamless position latching, otherwise complex adaptive matching circuits are needed to compensate for displacements. At a fixed axial transfer distance of 25 mm, the corresponding maximum simulated and measured transfer efficiency is 73.01% and 71.84%, respectively, under perfect alignment. Sustainable power transfer efficiency (PTE) is demonstrated during a 360° planar clockwise rotation with the step size of 45° and the measured variation ratio is 0.02 while the feasibility of preserving PTE until 0.6 quotients of lateral displacement and axial distance is validated when up to 15-mm lateral offsets occur either from x or y reference planes. It can thus be concluded that the printed spiral resonator proposed appears to be a good candidate to rectify planar and lateral displacements featuring simplicity and space-saving robust structure that necessitates only a minimized footprint, thus paving the way for adaptation in WET applications, such as consumer electronics and implanted medical devices.

INDEX TERMS Near-field wireless energy transfer, planar displacement, lateral displacement, transfer efficiency.

I. INTRODUCTION

The adoption, adaptation and evolution of near-field Wireless Energy Transfer (WET) technology displayed in an extensive range of low and high power applications is overwhelmingly positive, considering the fact that the concept introduced by Nikola Tesla was conceived more than hundred years ago [1]. Electric vehicle charging is an example for power demanding applications [2], [3] typically at kilowatt level. Consumer electronics applications [4] such as wireless charging for smartphones, wearables, tablets, laptop necessitate much lesser power, ranging between microwatt and watt levels. Similar implementations for wireless powering of implanted biomedical devices [5], [6] and structural health monitoring [7] have been achieved with the distinction of lower resonance frequency and smaller footprint.

Vulnerability of Wireless Energy Transfer (WET) systems in terms of loop orientation should not be overlooked, especially with respect to the effect on its performance metrics specifically coupling coefficient and power transfer efficiency [8]. Attenuation of coupling coefficient is inevitable with the increment of distance due to divergence from critical coupling threshold that does not comply with simultaneous conjugate matching between the source and load impedances resulting in the deterioration of power transfer efficiency [9]. As opposed to ideal situation where

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receiver loop resonator is positioned at perfect alignment, displacement, be it planar, lateral or angular, often transpires in practical applications [10].

Composition and construction of transmitting resonator is one of the strategies employed to counteract the adverse effects of non-ideal orientations. By arranging more than one loop in an array structure, a boost of the invulnerability boost to lateral displacement is demonstrated in [11] and [12]. A wider magnetic field generated by an array structure is a recommended option to achieve spatial freedom for applications related to a single mobile receiver [13] or multiple receivers [14]. The inclusion of a metamaterial slab in [15] demonstrates the capability of alleviating losses due to displacements. Constructed by three orthogonal loops in [16] and [17] and two crossed dipoles in [18], a 3-dimensional (3D) structure is explored as an alternate solution to accomplish an alignment-free WET system. Erratically positioned receiving resonators are capable of detecting magnetic flux within source vicinity thanks to an omnidirectional magnetic field generated by a 3D structure using non-identical current control [19].

Reports of enhanced Q-factor are demonstrated with uneven conductor widths and spatial distributions in stacked multi-layer printed spiral resonator [20].Contrary to conventional constant width for all loop turns, gradual reduction of conductive trace widths from the outermost winding to the innermost winding curbs the eddy current induced losses thereby refining the loop's Q-factor [21]. Nevertheless, designing larger constant conductor width for all turns and smaller constant spacing between adjacent conductor trace will only intensify the total resistance [22]. It is also observed that by ensuring ratio between conductor width and spacing as well as innermost side length to be relatively small facilitates the decrement of proximity effects and amelioration of eddy current centered in loop resonator [23]. Although the triple-layer PSC proposed in [20] reports on transfer efficiency boost and robustness towards lateral misalignment, type of impedance transformation network employed is not discussed. As an alternative of spiral resonator, defected ground structure (DGS) is proposed in the mitigation of lateral and planar displacement at 300 MHz band [24]. Established on analytical evaluations of available mutual inductance at ideal orientation, Barakat *et al.* [25] proposed a higher quality factor (Q-factor) of DGS resonators with enhanced tolerance towards lateral misalignment.

Convergence of resonance frequency and realizing maximum WET efficiency is made possible with frequency tuning and impedance matching methods, which counteract mutual inductance variations caused by load or spatial distance deviations between primary and secondary resonators. Appropriate reactive compensation is inherent to attain maximum power transfer efficiency at desired resonance frequency. Resonance tuning and impedance matching is yet another strategy implemented for displacements mitigation. Eteng *et al.* [26] proposed L-match technique at the edge of transmitter resonator which corresponds with the lowest coupling coefficient and the resulting transfer efficiency is preserved despite encountering lateral offsets. Adaptive impedance matching techniques are adopted in alleviating unpredictable displacement [27], [28] and coupling distance variation [29]. Integrating sensing coils which is proposed in [30] is another method to overcome lateral shift variations.

Compromise should be exercised in deciding displacement mitigation strategy between performance, complexity, cost and space constraints. The ultimate drawback of using surface mount device (SMD) components is the additional losses incurred apart from the fact that designers have to deal with negative consequences of having excessive or insufficient amount of soldering on printed circuit board (PCB) which might leads to the occurrence of significant frequency shift from the targeted operating frequency [25], [31]. Moreover, the precise values of SMD components required for impedance matching might not be similar to the available off-the-shelf capacitors. Selecting the smallest tolerance value in order to obtain the nearest possible capacitors value results in the dilemma of precision versus cost-efficiency especially for small scale budget-conscious designers. There are a few identified aspects in which interdigital capacitor is observed to fare better in terms of precision, assembly complexity, compactness and supplementary cost incurred as detailed in Table 1. With the absence of tedious and cautious soldering task, embedded interdigital capacitor is therefore not complex in fabrication and perform better in precision provided that meticulous optimization process is prioritized during design stage. As such, design stage of interdigital capacitor is slightly more intricate. On the other hand, co-planar embedded interdigital capacitor within a substrate is identified to be a favorable lumped element since the footprint of proposed design is not constrained by surface-mount capacitor's height but only by the thickness of substrate and copper. Hence, planar interdigital capacitor (IDC) is proposed as a substitution of capacitive compensation. IDC has been widely

TABLE 1. Comparison between surface-mount capacitor and interdigital capacitor.

Factors	Surface-Mount Capacitor	Interdigital Capacitor
Design stage complexity	Straightforward	Moderate
Precision	Dependent of the availability of tolerance value from off-the-shelves capacitors and skilled soldering technique	Dependent of optimization during design stage of interdigital capacitor model
Assembly Complexity	Moderate. Necessitate additional assembly phase	Simplified. Necessitate only direct fabrication
Compactness	Limited by thickness of substrate and copper as well as additional height of selected surface-mount capacitor	Limited by thickness of substrate and copper only
Supplementary cost incurred	Yes	None

implemented as a passive lumped element in microwave integrated circuits [32]. Porwal *et al.* [33] implements RF sensor by integrating a Spiral Resonator (SR) and an IDC on main microstrip line for GHz operating frequency range. This technique has also been extensively applied in lower MHz frequencies [34], [35].

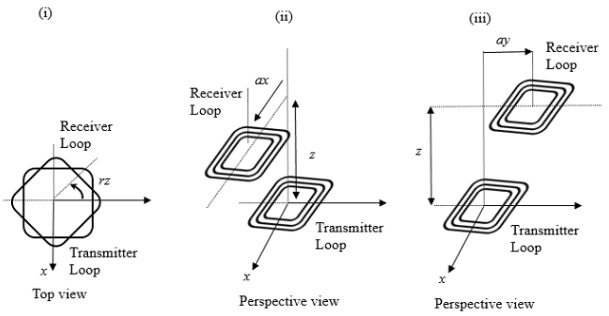

FIGURE 1. Displacements. (i) Planar (*z*-axis plane). (ii) Lateral (*x*-axis plane). (iii) Lateral (*y*-axis plane).

In this paper, a printed spiral coil (PSC) integrated with a series capacitive compensated interdigital capacitor is proposed to investigate the restraint towards offsets either caused by planar or lateral displacements. Planar displacement refers to the angle of rotation, rz when both centers of transmitter and receiver loops are aligned and separated by an axial transfer distance, z. Similarly, at a fixed axial distance specifically 25 mm, the center of receiving loop resonators are shifted by a distance of ax or ay known as lateral displacement at x-axis and y-axis respectively. The aforementioned displacement scenarios are visualized in Fig. 1. Step size for rotation angle is 45° from 0° till 360°. As for lateral displacement analysis, the respective offset at x-axis and y-axis varies from 0 till 25 mm with an incremental size of 5 mm. In the absence of additional and space constricting matching circuits, PSC and IDC is fabricated on a single substrate. Satisfactory performance is obtained in alleviating degradation of transfer efficiency when receiving resonator is subjected to several types of displacement. To the best of our knowledge, there is currently no existing empirical research which addresses displacements effects on transfer efficiency by adopting a synthesized PSC and IDC.

II. PRINTED RESONATOR DESIGN AND FABRICATION

A. PRINTED SPIRAL COIL

Conductor thickness opted is 70 μm to reduce resistance with higher cross-sectional conductive area. By taking precedence of space circumscription comprising of width and length of substrate as well as adequate length for SubMiniature Version A (SMA) connection, the outer side length is predetermined at 52 mm. The correlation between optimal transfer distance, z_{op} and outermost diameter length of bottom layer's loop, db_o at maximum excited magnetic field derived in [31] and [36] yields

$$z_{op} = db_o(2.544)^{-1}. \tag{1}$$

The optimal transfer distance computed is 20.44 mm. However, axial distance, z selected is rounded to 25 mm for ease of measurement based on the available experimental apparatus setup. The width of conductor trace is reduced gradually from outermost width of 1 mm to innermost width of 0.875 mm. The same applies to spacing between conductors but decrement is performed the opposite way from innermost to outermost. Other geometrical parameters are tabulated in Table 2.

TABLE 2. Parameter Properties of PSC and IDC.

Symbol	Parameter	Value (mm)
T_s	Substrate thickness	1.6
t_c	Conductor thickness	0.07
h_f	IDC's finger length	19.8075
w_f	IDC's finger width	0.912
h_{base}	IDC's base length	0.85
w_{base}	IDC's base width	9.672
dt_i	Inner diameter length of top layer SR	29.375
db_i	Inner diameter length of bottom layer SR	31.125
dt_o	Outer diameter length of top layer SR	50
db_o	Outer diameter length of bottom layer SR	52

The self-inductance expression for single sided square printed spiral loop design [37] is given by

$$L_{sq} = 0.635\mu {n_t}^2 d_a[\ln(2.07\varphi^{-1}) + 0.18\varphi + 0.13\varphi^2]. \tag{2}$$

μ, n_t, and d_a denote conductor permeability, number of turns, average side lengths of loop where $d_a = 0.5(d_o + d_i)$ and the outermost and innermost side lengths are represented by d_o and d_i respectively. φ is the conductor fill factor which is equivalent to $(d_o - d_i)\ (d_o + d_i)^{-1}$ [38]. Total inductance is the summation of self-inductance and mutual inductances between turns specifically $n_t(n_t - 1)$ and expressed as [39]

$$M_{ij} = 2\mu(r_i r_j)^{0.5}\beta^{-1}[(1 - 0.5\beta^2)K(\beta) - E(\beta)], \tag{3}$$

$$\beta = 2(r_i r_j)^{0.5}[(r_i + r_j)^2 + z^2]^{-0.5}, \tag{4}$$

$$M = \rho \sum_{i=1}^{n_1}\sum_{j=1}^{n_2} M_{ij}(r_i, r_j, z), \tag{5}$$

where M_{ij} denotes partial mutual inductance between each two turns on a pair of loops with turn radii, r_i and r_j while complete elliptic integrals of the first and second kind are represented by K and E. ρ is the factor which is dependent on loop profile. The relation between mutual inductance and self-inductances of coupled resonators is defined with coupling coefficient, k as

$$k = M(L_1 L_2)^{-0.5}. \tag{6}$$

Critical coupling point implies transition point between under-coupled regime and over-coupled regime which leads to the undesirable frequency splitting phenomenon. Both regime results in the deterioration of transfer efficiency [40]. It is worth noting that maximum power transfer efficiency is attainable at this k_{cp} value given by [41].

$$k_{cp} = [1 + (1 + k^2 Q_1 Q_2)^{0.5}](Q_1 Q_2)^{-0.5} \tag{7}$$

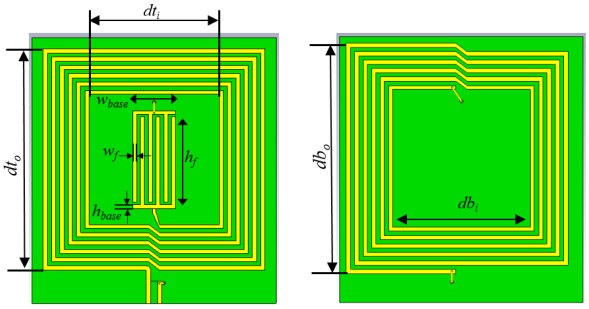

FIGURE 2. Geometry of the proposed PSC and IDC design: Top layer (left) bottom layer (right).

where $Q_1 = \omega L_1 R_1^{-1}$ and $Q_2 \omega L_2 R_2^{-1}$ are the quality factors of primary and secondary resonators while ω denotes angular resonance frequency. PSC resistance can be approximated by [39]

$$R_s = R_{dc} t_c [\delta_{sk}(1 - e^{-t_c/\delta_{sk}})]^{-1} \tag{8}$$

where $R_{dc} = \ell_c[\sigma A]^{-1}$ and $\delta_{sk} = (\phi\mu\sigma)^{-0.5}$ are the DC resistance and skin depth. ℓ_c, σ and t_c refer to the total conductor length, conductivity, cross-sectional area and conductor thickness. μ is the product of permeability of free space, μ_0 and conductor's relative permeability, μ_r.

B. INTERDIGITAL CAPACITOR

An interdigital capacitor is designed in series with a total of six fingers and etched in the center of substrate's top layer. As such, the geometrical constraints of IDC layout are determined by the design of PSC as discussed earlier. The width and length of both IDCs' finger and base are listed in Table 2. The resonance frequency, f_c is defined as

$$f_c = [2\pi (LC)^{0.5}]^{-1}. \tag{9}$$

where L and C denote inductance and capacitance. Tuning of resonance frequency towards 13.56 MHz is performed by optimizing the geometrical properties of IDC [42]. The number of fingers, n_f, width, w_f and length, h_f of IDCs' finger as well as base length, h_{base} are inversely proportional to the resonance frequency. Since capacitance is proportional to the reciprocal of resonance frequency, impedance matching is achievable at the targeted operating frequency by manipulating the aforementioned geometrical parameters.

Estimation of capacitance value for interdigital capacitor can be computed by the following expressions based on conformal mapping approach [43]

$$C_{idc} = n_p \ell_o \Big[\{4\varepsilon_0 K(k_1')(K(k_1))^{-1}\} + \{2\varepsilon_0(\varepsilon_r - 1)K(k_2')(K(k_2))^{-1}\} \Big] \tag{10}$$

where the number of IDC finger pairs, overlapping of finger lengths, free space permittivity (8.854 x 10^{-15} F/mm), dielectric constant of substrate and complete elliptic integrals of the first and kind are symbolized by n_p, ℓ_c, ε_0, ε_r and K.

Computation for k_1, k_1', k_2 and k_2' are

$$k_1 = \Big[1 + (2w_f)(w_f + 2g_f)^{-1}\Big] \cdot \times \Big[\Big\{\big[1 + \big((2w_f)(g_f)^{-1}\big)\big]^{-1}\Big\}^{0.5}\Big], \tag{11}$$

$$k_1' = [(1 - k_1^2)]^{0.5}, \tag{12}$$

$$k_2' = AB^{-1}[\{(C - B^2)(C - A^2)^{-1}\}]^{0.5}, \tag{13}$$

$$A = \sinh\left(0.25\pi w_f T_s^{-1}\right), \tag{14}$$

$$B = \sinh\left(0.5\pi T_s^{-1}(0.5w_f + g_f)\right), \tag{15}$$

$$C = \sinh^2\left(0.5\pi T_s^{-1}(1.5w_f + g_f)\right), \tag{16}$$

$$k_2 = [(1 - (k_2')^2)]^{0.5}. \tag{17}$$

w_f, g_f and T_s refer to finger width, gap between fingers and thickness of substrate. Once values of k_1 and k_2 are determined, Hilberg's approximation below [44] is used to solve the elliptic integral function.

$$\frac{K(k_i)}{K(k_i')} \approx \frac{2}{\pi} \ln\left[2\sqrt{\frac{1 + k_i}{1 - k_i}}\right], \quad \text{for } 0.707 \le k_i \le 1 \tag{18}$$

$$\frac{K(k_i)}{K(k_i')} \approx \frac{\pi}{2}\left\{\ln\left[2\sqrt{\frac{1 + k_i}{1 - k_i}}\right]\right\}^{-1}, \quad \text{for } 0 \le k_i \le 0.707 \tag{19}$$

C. DESIGN STRATEGY

Fig. 3 encapsulates the simulation strategy employed by taking inspiration from iterative design procedure introduced in [39] with the exclusion of analytical modeling. The preliminary two stages are related in the design and enhancement steps for PSC and IDC. With the aid from a full-wave electromagnetic simulator, CST Microwave Studio, the synthesized PSC and IDC structure is designed and optimized using the frequency domain solver which is grounded on Finite Integration Technique (FIT).

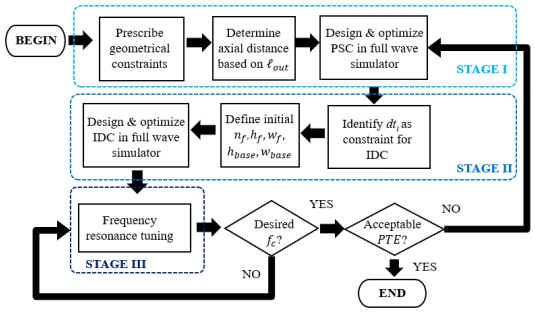

FIGURE 3. Simulation strategy.

The final procedure grounded on exploratory approach is the tuning of resonance frequency. The first stage will be repeated again should PTE fall below the acceptable threshold. As pointed out in [45], contemplation on either having highest PTE or acceptable efficiency is attributed to the contradiction between acquiring maximum PTE at nearest

optimal transfer distance and furthest transfer distance possible. Since the opted transfer distance is not at the optimal transfer distance with strongest coupling as computed in (1), acceptable efficiency of 70% is selected as in [46]. The prescribed acceptable efficiency serves as a benchmark in the optimization approach for printed spiral resonator design.

The performance of resonator designed is ascertained by evaluating WET power transfer efficiency (PTE). This is derived from simulated S-parameters, specifically the magnitude of transmission coefficient, S_{21} as shown from the following equation [47].

$$PTE = |S_{21}|^2. \tag{20}$$

Apart from the equation above, derivation of maximum obtainable efficiency is dependent on coupling coefficient, k and Q-factor as shown in (21) [48]. The root square of $k^2Q_1Q_2$ is equivalent of kQ, another important performance indicator for coupled resonators [49]. Derivation of kQ is also possible from impedance matrix components [50] as $|Z_{21}|(ESR)^{-1}$ where $ESR = [(R_{11}R_{22}) - (R_{12}R_{21})]^{0.5}$ is the Equivalent Scalar Resistance of two-port system.

$$PTE_{max} = [k^2Q_1Q_2][1 + (1 + k^2Q_1Q_2)^{0.5}]^{-2}. \tag{21}$$

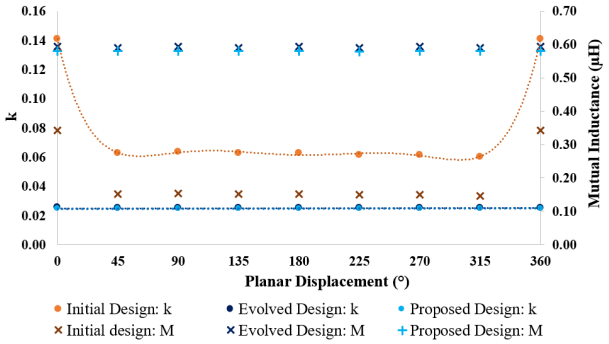

FIGURE 4. Simulated coupling coefficient and mutual inductance for initial, evolved and proposed designs under planar displacement.

Evolution of proposed design with synthesized IDC comes from an initial PSC design followed by an evolved PSC design. Initial design stems from a conventional single-sided printed spiral resonator with six loop turns, n using a single series lumped element for resonance frequency tuning while the evolved design is a double-sided printed spiral resonator with a total of twelve loops and a single series lumped element. Computed capacitance for resonance frequency tuning of the initial design using (9) is 56.76 pF. The subsequent optimized capacitance value for tuning is 57 pF. However, drastic degradation of mutual inductance from 0.34 μH to 0.15 μH is observed when receiving resonator is positioned at 45° of planar offset as depicted in Fig. 4. From Fig. 5, gradual decline of coupling coefficient implies that initial paired resonators have manoeuvre into under-coupled regime. Coupling coefficient is discovered to reduce by more than half as compared to k value during non-displacement orientation which is way below than the required critical coupling at 0.1455.

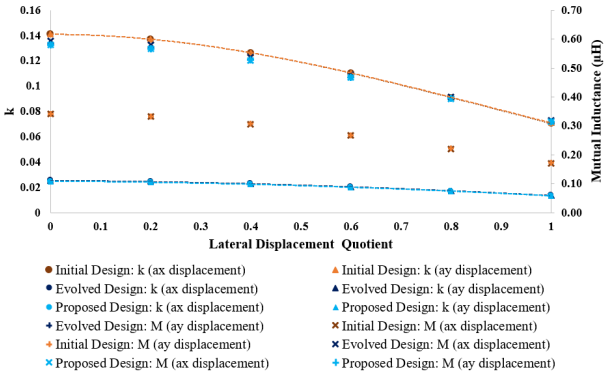

FIGURE 5. Simulated coupling coefficient and mutual inductance for initial, evolved and proposed designs under lateral displacement.

By introducing additional loops at the bottom of the substrate resembling to a flat bifilar coil and through meticulous geometrical parameters enhancement, the inductance of evolved design is increased by about 9.6 times as compared to the initial design without increasing the substrate's dimensions. Top and bottom of substrate share similar number of loops. The tuning capacitance for the second design has reduced to 3.28 pF. From the simulated magnetic field strength as illustrated in Fig. 6, initial design exhibits weak H-field which demands proper alignment in ensuring minimum power transfer. On the other hand, the second design demonstrates dispersed magnetic field intensity over wider area. As such, it becomes a remedy for severe impact on transfer efficiency over varied rotational angles at z-axis.

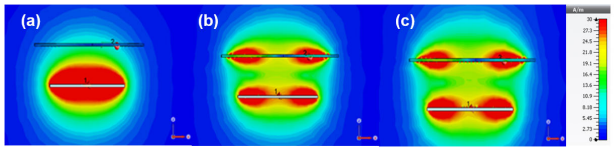

FIGURE 6. Simulated H-field on *xz*-plane at *y*=0: (a) initial, (b) evolved and (c) proposed designs under planar displacement, *rz*= 45°.

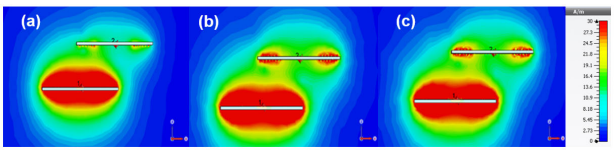

FIGURE 7. Simulated H-field on *xz*-plane at *y*=0: (a) initial, (b) evolved and (c) proposed designs under lateral displacement, *ax*=25 mm.

Using heuristic approach, exploitation on geometrical layout performed in full-wave electromagnetic simulator yields an inhomogeneous spatial distribution and width trace of evolved design that reveals improved magnetic field intensity even under x and y axis of lateral offset scenarios at 25 mm as depicted in Fig. 7 and Fig. 8. Inner diameter length of top and bottom layer, dt_i and db_i can be derived as

$$dt_i = dt_o - \left[(n_t - 1)\{2(w_1 + s_1) + \alpha\}\right] - 2w_{n_t}, \tag{22}$$

$$db_i = db_o - \left[(n_b - 1)\{2(w_1 + s_1) + 1.5\alpha\}\right] - 2w_{n_b} \tag{23}$$

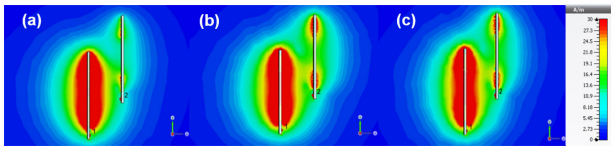

FIGURE 8. Simulated H-field on *yz*-plane at *x*=0: (a) initial, (b) evolved and (c) proposed designs under lateral displacement, *ay*=25 mm.

where n_t and n_b are the number of turns on top and bottom layer, w_1 and s_1 are the outermost trace width and spacing for both top and bottom layer. α is the variable constant used during the optimization PSC design. $w_{n_{t,b}}$ and $s_{n_{t,b}}$ represent the trace width and spacing of *nth* number of turns either on top or bottom layer which are given by (24) and (25) respectively. It is worth mentioning that only a single variable constant, α is used here to speed up time required for optimization.

$$w_{n_{t,b}} = w_1 - \left[(n_{t,b} - 1)\alpha\right], \tag{24}$$

$$s_{n_{t,b}} = s_1 + \left[(n_{t,b} - 1)\alpha\right]. \tag{25}$$

The evolved design is then extended to the third proposed design whereby series capacitor modeled as a lumped element is removed and replaced with planar interdigital capacitor model. Computed capacitance value based on (10) to (19) yield an approximation of 3.43 pF which is almost similar with the capacitive compensation value employed for the second design. Extracted parameters for three simulated designs are shown in Table 3.

TABLE 3. Comparison between extracted parameters of initial, evolved and proposed designs without displacement.

Parameter	Initial Design	Evolved Design	Proposed Design
L_s (μH)	2.43	23.39	23.39
Computed C_{tune} (pF)	56.76	5.89	5.89
Optimized C_{tune} (pF)	57	3.28	3.43
M (μH)	0.34	0.59	0.58
R_s (Ω)	0.955	6.732	7.799
Q	218	298	258
k	0.1409	0.0254	0.0248
k_{cp}	0.1455	0.0290	0.0290
kQ	30.73	7.56	6.39
PTE (%)	71.30	76.61	73.01

Referring to Fig. 9 and Fig. 10, sustaining kQ over non-ideal orientations are feasible with both evolved and proposed designs. Performance improvement can be inferred by the minimum variation ratios of k and kQ under each type of displacement as tabulated in Table 4. Variation ratios of k and kQ are computed as $VR_k = (k_{max} - k_{min})(k_{max})^{-1}$ and $VR_{kQ} = (kQ_{max} - kQ_{min})(kQ_{max})^{-1}$ respectively. Smallest possible variation ratio suggests reduced sensitivity towards coupling variations caused by imperfect alignment between a paired resonators. The proposed design displays smallest variation ratio for k and kQ under planar and lateral offsets. Percentage of reduction, ΔVR compares the respective variation ratios between the second and first design as well as between the proposed and second design.

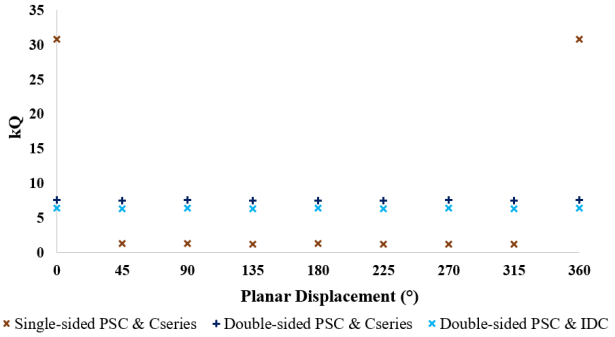

FIGURE 9. Simulated *kQ* for initial, evolved and proposed designs under planar displacement.

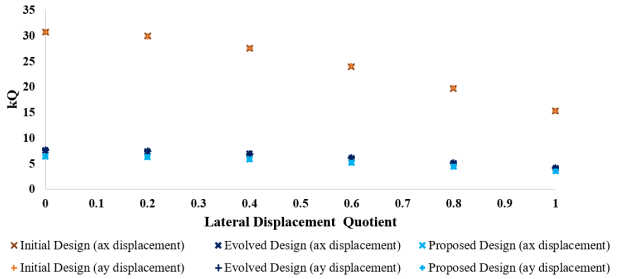

FIGURE 10. Simulated *kQ* for initial, evolved and proposed designs under lateral displacement.

TABLE 4. Summary of displacement-tolerant performance for simulated designs.

Designs		Initial	Evolved	Proposed
rz Displacement	VR_k	0.572	0.007	0.003
	ΔVR_k (%)	N/A	-98.8	-57.1
	VR_{kQ}	0.960	0.012	0.010
	ΔVR_k (%)	N/A	-98.8	-16.7
ax Displacement	VR_k	0.500	0.463	0.458
	ΔVR_k (%)	N/A	-7.4	-1.1
	VR_{kQ}	0.504	0.462	0.459
	ΔVR_k (%)	N/A	-8.3	-0.6
ay Displacement	VR_k	0.496	0.460	0.456
	ΔVR_k (%)	N/A	-7.3	-0.9
	VR_{kQ}	0.503	0.460	0.458
	ΔVR_k (%)	N/A	-8.5	-0.4

III. RESULT AND DISCUSSION

The proposed design is fabricated on a double-sided FR-4 with dielectric constant of 4.7 as illustrated in Fig. 11. The overall dimension is 55 mm × 60 mm. A common practice is to drill two holes to pave way for wire connection between the top and bottom layers. The reason behind not opting for direct through hole via design is due to the fabrication limitation imposed by the present available facilities in laboratory.

As shown in Fig. 12, the experimental setup to assist planar displacement is executed with two dissimilar dimensions of acrylic sheets (15 mm × 15 mm × 2 mm and 10 mm × 10 mm × 2 mm) separated by nylon PCB standoffs. The axial separation selected is 25 mm. The receiving resonator is positioned on top of a smaller size acrylic board and manually rotated

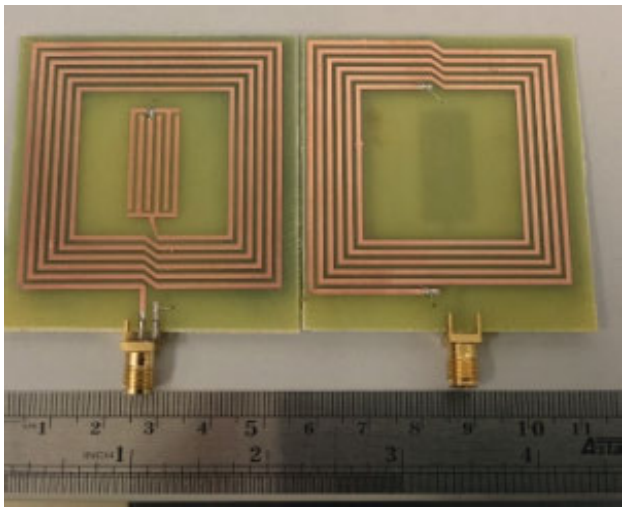

FIGURE 11. Fabricated printed spiral coil assembled with interdigital capacitor: Top (left); bottom (right).

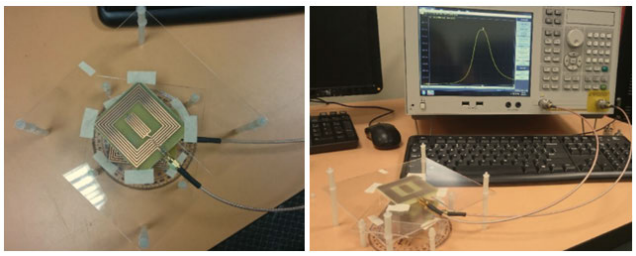

FIGURE 12. Measurement setup for planar displacement: Top view (left); perspective (right).

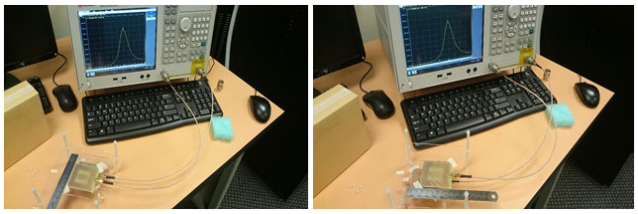

FIGURE 13. Measurement setup for lateral displacement: *x*-axis (left); *y*-axis (right).

based on a protractor placed underneath. The corresponding measurement setup is depicted in Fig. 13. Measurement tool employed is Keysight Vector Network Analyzer (VNA) E5071C applicable for designs with frequency ranging from 9 kHz till 6.5 GHz.

Referring to Fig. 14, the simulation results are validated with good resemblance from the measurements when receiving loop is deliberately rotated at various angles *rz*. Only minor resonance frequency shifting is observed. Table 5 lists peak power transfer efficiencies, PTE_{peak} and the corresponding peak resonance frequencies, f_{peak} for both simulated and measured results. Fig. 15 illustrates the combined PTE_{peak} under planar displacement. In order to gauge the link

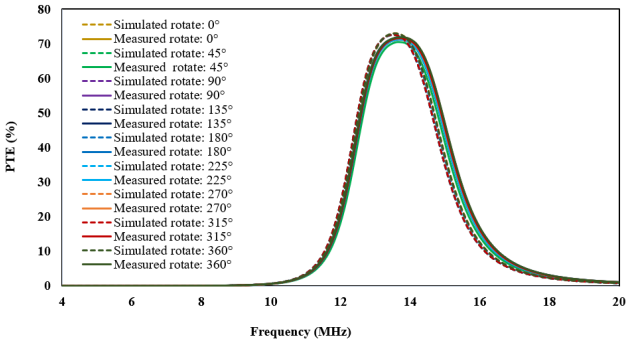

FIGURE 14. Comparison of the simulated and measured PTE under planar displacement.

TABLE 5. Peak power transfer efficiency under planar displacement.

Angle	Simulated		Measured	
rz (°)	f_{peak} (MHz)	PTE_{peak} (%)	f_{peak} (MHz)	PTE_{peak} (%)
0	13.568	73.01	13.680	71.84
45	13.504	72.62	13.680	70.52
90	13.552	72.95	13.680	71.81
135	13.504	72.54	13.680	71.28
180	13.552	72.91	13.680	71.28
225	13.552	72.58	13.680	71.29
270	13.552	72.99	13.680	71.65
315	13.504	72.60	13.680	71.67
360	13.568	73.00	13.760	71.91

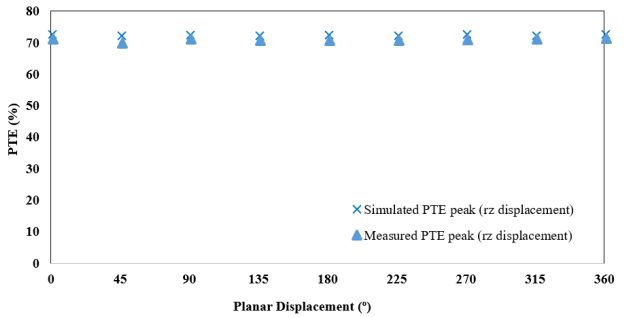

FIGURE 15. Comparison of the simulated and measured peak PTE under planar displacement.

performance, variation ratio, *VR* is computed as [51]

$$VR = (PTE_{peak_{max}} - PTE_{peak_{min}})(PTE_{peak_{max}})^{-1}. \quad (26)$$

Variation ratio of measured PTE when secondary resonator is subjected to rotational offsets is 0.02. A near-uniform transfer efficiency is displayed which attests to its tolerance capacity under rotational offsets with reference to *z*-axis. It is worth mentioning that since axial distance selected is a non-optimal distance which differs from recommended distance in (1), excited magnetic field is therefore less than the maximum which serves as an indicator of a reduced transfer efficiency possibility even when both resonators are perfectly aligned or in other words when *rz* is equivalent to zero. As such, the corresponding maximum simulated and measured transfer efficiency is only at 73.01% and 71.84% respectively.

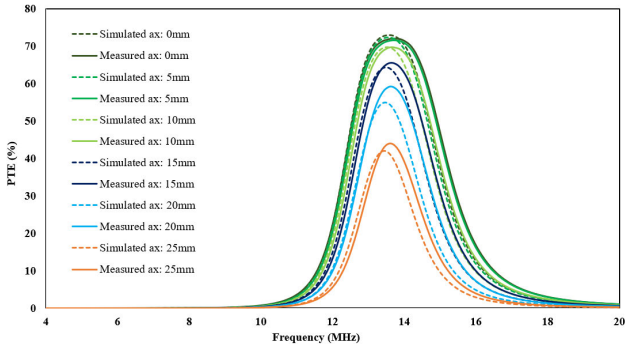

FIGURE 16. Comparison of the simulated and measured PTE under *x*-axis lateral displacement.

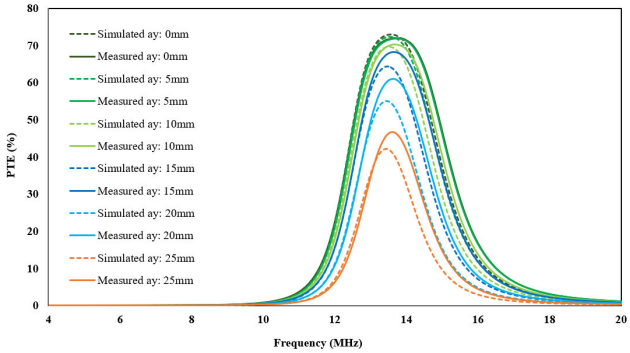

FIGURE 17. Comparison of the simulated and measured PTE under *y*-axis lateral displacement.

TABLE 6. Peak power transfer efficiency under *x*-axis lateral displacement.

Quotient	Simulated		Measured	
ax/z	f_{peak} (MHz)	PTE_{peak} (%)	f_{peak} (MHz)	PTE_{peak} (%)
0	13.568	73.02	13.680	72.06
0.2	13.552	72.31	13.680	71.66
0.4	13.520	69.74	13.680	69.77
0.6	13.488	64.30	13.600	65.63
0.8	13.472	55.02	13.600	59.17
1	13.408	41.97	13.600	44.01

Fig. 16 and Fig. 17 portrays the combined simulated and measured results when various offsets of ax and ay are being considered. Both plots depict reasonable agreement with simulator outcomes except slight resonance frequency shifting observed. Peak power transfer efficiencies for both simulated and measured results under the corresponding displacement categories are tabulated in Table 6 and Table 7. Quotient computed refers to the ratio of lateral displacement to the axial distance which is pre-set at 25 mm. As shown in Fig. 18, sustainable efficiency until quotient 0.6 is feasible when 15 mm lateral offsets occur either from x or y reference planes before the transfer efficiencies began to display significant decay owing to coupling decrement.

Table 8 shows comparison between the proposed design in this work with other published works related to planar and lateral compensation designs. Only [16] and [24] display robustness towards both planar and lateral misalignments while others mainly emphasized on lateral misalignment-insensitive designs. Proposed design appears to excel in terms of simplicity in addition to exhibiting tolerable planar and lateral displacement centring around 13.56 MHz frequency band.

TABLE 7. Peak power transfer efficiency under *y*-axis lateral displacement.

Quotient	Simulated		Measured	
ay/z	f_{peak} (MHz)	PTE_{peak} (%)	f_{peak} (MHz)	PTE_{peak} (%)
0	13.568	73.02	13.680	72.06
0.2	13.536	72.27	13.760	71.87
0.4	13.504	69.72	13.680	70.26
0.6	13.552	64.39	13.680	68.23
0.8	13.440	55.01	13.600	60.93
1	13.440	42.09	13.600	46.68

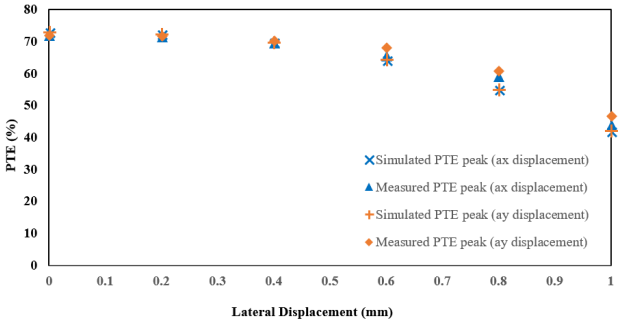

FIGURE 18. Comparison of the simulated and measured peak PTE under lateral displacement at *x*- and *y*-axis.

TABLE 8. Comparison with published works.

Ref	[24]	[25]	[16]	[26]	[20]	This work
f_c (MHz)	300	300	80.2	13.56	13.56	13.56
Resonator type	DGS (semi H)	DGS (semi-elliptic)	3-D SCMR (circular)	PSC (circular)	PSC (triple layer)	PSC (double-sided)
do_{tx} (mm)	21	40	100	84.82	23	52
do_{rx} (mm)	21	40	100	29.98	23	52
Assembly Complexity	Moderate	Moderate	High	Moderate	Moderate	Simple
Capacitor Type	SMD	SMD	Through-hole	SMD	N/A	IDC
Planar shift	$\geq$50% (z-axis: $\pm$50°)	No	>30% (z-axis: +360°), >30% (x-axis: +272°)	No	No	>70% (z-axis: +360°)
Lateral shift	>50% (x-axis: +4mm, y-axis: +11mm)	>50% ($\pm$30 mm)	>30% (+102 mm)	>60% ($\pm$45.4 mm)	>60% (+20 mm)	>50% (+20 mm)
z (mm)	25 (1.19 do_{tx})	40 (do_{tx})	120 (1.2 do_{tx})	30 (0.35 do_{tx})	10 (0.43 do_{tx})	25 (0.48 do_{tx})

IV. CONCLUSION

A synthesized printed spiral coil and planar interdigital capacitor on a single printed circuit board is presented. Occupying only at a minimized footprint of 55 mm × 60 mm

× 1.6 mm, maximum simulated and measured transfer efficiency of 73.01% and 71.84% is achieved under perfect alignment where displacement is nil. The measurement results under planar and lateral displacements corroborates with simulated outcomes. When the secondary resonator is subjected to rotational planar displacement, variation ratio of transfer efficiency is 0.02. Even though transfer efficiency variations under x-axis and y-axis lateral displacements are slightly higher at 0.39 and 0.35 respectively, robustness of energy transmission link is still viable with the proposed design. It can thus be concluded that the printed spiral resonator proposed serves as a potential candidate for planar and lateral displacements suppression apart from minimal complexity, space and cost-conscious design for near-field WET applications namely consumer electronics and biomedical devices. Practicality of proposed design in the aforementioned applications is in line with the commonly occurring reduced power transfer efficiency due to the lack of perfectly-aligned positioning between source and receiver.

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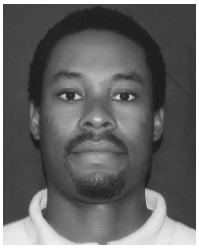

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