IEEE Access
Multidisciplinary : Rapid Review : Open Access Journal

Received December 14, 2018, accepted December 28, 2018, date of publication January 14, 2019, date of current version February 6, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2892592

Drift-Diffusion Versus Monte Carlo Simulated ON-Current Variability in Nanowire FETs

DANIEL NAGY[1], GUILLERMO INDALECIO[1,2], ANTONIO J. GARCÍA-LOUREIRO[1], GABRIEL ESPIÑEIRA[1], MUHAMMAD A. ELMESSARY[3,4], KAROL KALNA[3], AND NATALIA SEOANE[1]

[1]Centro Singular de Investigación en Tecnoloxías da Información, University of Santiago de Compostela, 15782 Santiago de Compostela, Spain
[2]Institute for Microelectronics, TU Wien, 1040 Vienna, Austria
[3]Nanoelectronic Devices Computational Group, Swansea University, Swansea SA1 8EN, U.K.
[4]Department of Engineering Mathematics and Physics, Mansoura University, Mansoura 35516, Egypt

Corresponding author: Daniel Nagy (daniel.nagy@usc.es)

This work was supported in part by the Spanish Government under Project TIN2013-41129-P and Project TIN2016-76373-P, in part by Xunta de Galicia and FEDER funds under Grant GRC 2014/008, in part by the Consellería de Cultura, Educación e Ordenación Universitaria (accreditation 2016-2019), under Grant ED431G/08, and in part by the Centro de Supercomputación de Galicia (CESGA) for the computer resources provided. The work of G. Indalecio was supported by the Programa de Axudas á Etapa Posdoutoral da Xunta de Galicia under Grant 2017/077. The work of N. Seoane was supported by the RyC program of the Spanish Ministerio de Ciencia, Innovación y Universidades under Grant RYC-2017-23312.

ABSTRACT Variability of semiconductor devices is seriously limiting their performance at nanoscale. The impact of variability can be accurately and effectively predicted by computer-aided simulations in order to aid future device designs. Quantum corrected (QC) drift-diffusion (DD) simulations are usually employed to estimate the variability of state-of-the-art non-planar devices but require meticulous calibration. More accurate simulation methods, such as QC Monte Carlo (MC), are considered time consuming and elaborate. Therefore, we predict TiN metal gate work-function granularity (MGG) and line edge roughness (LER) induced variability on a 10-nm gate length gate-all-around Si nanowire FET and perform a rigorous comparison of the QC DD and MC results. In case of the MGG, we have found that the QC DD predicted variability can have a difference of up to 20% in comparison with the QC MC predicted one. In case of the LER, we demonstrate that the QC DD can overestimate the QC MC simulation produced variability by a significant error of up to 56%. This error between the simulation methods will vary with the root mean square (RMS) height and maximum source/drain *n*-type doping. Our results indicate that the aforementioned QC DD simulation technique yields inaccurate results for the ON-current variability.

INDEX TERMS Drift-diffusion, line edge roughness, metal gate granularity, Monte Carlo, quantum corrections, nanowire FET.

I. INTRODUCTION

Gate-All-Around (GAA) nanowires (NWs) are showing arguable promise to be the leading architecture for future technological nodes adopted by industry [1]–[5], due to their superior electrostatic control of the channel, thus allowing further scaling of the gate length in comparison with the currently used Fin Field-Effect Transistor (FinFET) architecture [6]. However, the devices in the deep nano-regime suffer from various sources of variability which could greatly affect their performance and yield [7]–[9]. These sources of variability are related to either the fabrication process or material properties. The most significant sources are: random dopants (RD), oxide thickness variation (OTV), metal gate work-function granularity (MGG), and line edge roughness (LER) [7]–[13]. Therefore, a rigorous study of all aspects of device performance, including their resistance against variability sources [3], [4], [14], [15], is critical. This study is often carried out using computer aided design tools because they are proven to be an economically efficient way to do the ground work [15]–[19]. However, choosing the right simulation tool without appropriate in-sight can be a cumbersome task.

Generally, three methods are commonly used for nanoscaled device simulations [16], [17]: (i) quantum corrected (QC) drift-diffusion (DD), (ii) QC Monte Carlo (MC) and (iii) fully quantum-mechanical Non-Equilibrium Green's

 This work is licensed under a Creative Commons Attribution 3.0 License. For more information, see http://creativecommons.org/licenses/by/3.0/

Functions (NEGF). The later is the most accurate but also the most computer intensive method that is generally used for ultra small nanoscale transistors in which quantum effects are expected to be significant [16], [17], [20]. Therefore, the use of NEGF for statistically significant variability studies, where hundreds of simulations are required, is computationally prohibitive. The QC MC method is commonly employed for the investigations of the device ON-region where carrier scattering and non-equilibrium transport play an important role [16], [17], [20]. An advantage of the MC over the NEGF is that the implementation of multiple scattering mechanisms into the MC simulator is less complex in comparison with the NEGF method. Finally, the QC DD is the least computationally expensive method and often used for variability studies in the sub-threshold region [3], [15], [16], [21], that involve simulations of thousands of individual devices. In our case, the QC DD method takes about three times less computational time than the QC MC method. However, the QC DD is disadvantaged by a requirement to calibrate QC parameters against either MC, NEGF or experimental data [3], [21], [22]. It was previously shown that QC DD is unable to perform ON-current variability study for planar MOSFETs without an underestimation because the QC DD cannot capture non-equilibrium effects [21], [23]. A similar rigorous study for non-planar multi-gate transistors is missing from the literature. More importantly, the QC DD method is still being used in state-of-the-art device variability study [15], [18], [22], [24]–[28] believing that properly calibrated QC DD simulations will yield to accurate statistical predictions.

In this paper, we aim to establish how accurate the QC DD method is when applied to the ON-region variability in comparison with the more rigorous QC MC simulation technique. We compare the results obtained by applying two of the main variability sources affecting the device reliability, the MGG and LER, on a state-of-the-art 10 nm gate length Si GAA NW FET that has been scaled down from an experimental device [29], [30].

II. METHODOLOGY AND DEVICE DESCRIPTION

In this work, we employ a well established in-house simulation toolbox [31]–[33] that includes 3D DD and MC transport models which use the finite element (FE) method for accurate mesh description of a simulation domain. The accurate description of the device nanoscale dimensions is of great importance for accurate simulations in the deep nano-regime because quantum-mechanical confinement in a device channel can significantly affect transport at nanoscale [34].

As mentioned before, the DD approach requires calibration for the simulations. In this study, we use the readily available MC simulation toolbox to guide the calibration of the QC DD. The model used by the DD simulator is the Caughey-Thomas doping dependent low-field electron mobility model [35], together with perpendicular (critical electric field) and lateral (saturation velocity) electric field models [36]. The calibration parameters used with the DD simulator are found in [33]. The MC toolbox accounts for all relevant electron scattering mechanisms in the silicon transistor: acoustic and non-polar optical phonons (intra- and inter-valley) [37], [38], ionised impurity scattering using the third body exclusion by Ridley [39], [40], and interface roughness (IR) scattering using Ando's model [41]. The electron screening in the electron-ionised impurity scattering uses a static screening model [42] with Fermi-Dirac statistics in which the Fermi energy and electron temperature are calculated self-consistently in a real space of device simulation domain.

We have already argued that quantum confinement effects will play a significant role in transport at nanoscale dimensions. Therefore, we use 3D density-gradient (DG) QCs in the DD simulations and 2D Schrödinger based equation corrections (SCH) in the MC. The former has the disadvantage that it requires fitting against the MC data, as aforesaid, meanwhile the later QC approach is calibration free. In case of the DG method, we use electron effective masses as calibration parameters to account for the quantum capacitance (shift of the threshold voltage). The fitting parameters used with the DG method are found in [43]. More details about the QC DD simulation methodologies can be found in [44] and [45] and about the QC MC in [32], [46], and [47].

Finally, the in-house simulation toolbox can account for the following sources of variability: OTV, MGG, LER, gate edge roughness (GER), and RD [31]. In this work, we will focus on the two most influential ones [7] for GAA NW FET: MGG and LER as illustrated in Fig. 2. Note that the same random profiles are used in both simulation techniques, the QC DD and QC MC, for a fair comparison of each variability study. Moreover, the QC DD calibration parameters are not adjusted for each of the profiles but use the values calibrated for the ideal device as this is the standard approach. The 2D Schrödinger equation in the QC MC simulations is solved for each random profile of a device as this method does not require additional calibration.

In case of the MGG variability, we use the Poisson-Voronoi diagrams approach [48] to create the metal grains for the metal gate contact of the simulated device. This method is believed to mimic more accurately the realistic metal gates [48] than the square grains approach [49], [50]. Furthermore, the MGG profile is characterized by a grain size (GS) and by a work function value (WFV) [48]. For the current study, we have chosen the titanium nitride (TiN) which is commonly used as a gate material [51]. The metal has experimentally observed WFVs of 4.6 eV and 4.4 eV with a probability of 60% and 40% formation, respectively [52].

In case of the LER variability, we create the uncorrelated profiles using Fourier synthesis with Gaussian autocorrelation approach [53]. These are characterized by the correlation length (CL) and the root mean square (RMS) values [43], [53]. The current study is limited to a CL of 20 nm and to experimentally observed RMS heights, ranging between 0.3 and 1.0 nm [11], [29].

A device used in this study is based on a 10 nm gate length GAA NW FET that was scaled down from an exper-

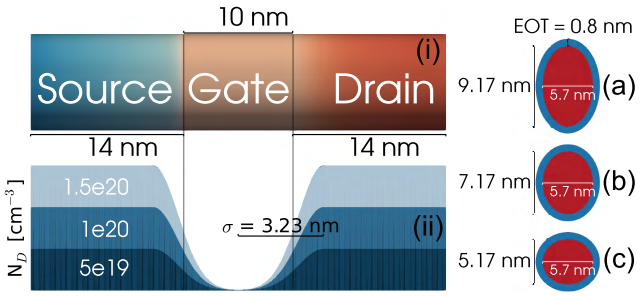

FIGURE 1. (i) Schematic for the 10 nm gate length GAA NW [30] and (ii) Gaussian doping profiles along the transport direction for three concentrations of N_D. (right) Cross-sectional view of the channel for the (b) ideal device and two cases when the Fin height was (a) elongated and (c) shortened.

FIGURE 2. Schematic for the 10 nm gate length GAA NW [30] affected by LER and MGG variability sources. The LER profile is projected along the transport direction (x-axis) and affects the dimension of only the z-axis. The MGG profile with different work function is projected to the gate area [52].

imental device [29] following the ITRS [54] guidelines as shown in [30]. The device schematic and dimensions are shown in Fig. 1(i). It has a uniformly *p*-type doped channel (1×10^{15} cm^{-3}), a Gaussian *n*-type doping, with a maximum N_D (see Fig. 1(ii)) and a lateral straggle (σ) of 3.23 nm, and an EOT of 0.8 nm. Finally, it has an elliptical channel cross-section with dimensions of 7.17 nm and 5.7 nm as shown in Fig. 1(b).

III. IDEAL GAA NW FET

Even though GAA NWs are considered to be major contenders for future technology nodes, they might be unable to deliver a large enough ON-current (I_{ON}) [33], [55] in circuits, which may be one of the main limiting factors for the adaptation of the technology. One way to overcome this issue could be by increasing the maximum N_D of the S/D region. For this reason we have increased the reversed engineered *n*-type doping concentration of N_D from 5×10^{19} that provided a perfect match to the experimental I-V curve [30] to 1×10^{20} and to 1.5×10^{20} cm^{-3}. Note that the σ was kept constant as shown in Fig. 1(ii). We have found that, compared to $N_D = 5 \times 10^{19}$ cm^{-3}, I_{ON} has increased by 40 % and 60 % for N_D of 1×10^{20} and 1.5×10^{20} cm^{-3}, respectively. Note that I_{ON} is I_D at $V_G = V_{DD}+V_T$, where V_T is the threshold voltage and $V_{DD} = 0.7$ V. Both the QC MC and the well calibrated QC DD simulated I_D-V_G characteristics are shown in Fig. 3 for the aforementioned cases. Note that the calibration of

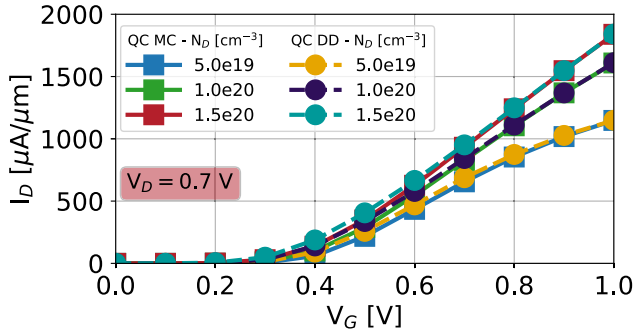

FIGURE 3. Simulated I_D-V_G characteristics for the 10 nm gate length GAA NW [30] at $V_D = 0.7$ V with a channel orientation of ⟨110⟩. Three different doping concentrations are presented for N_D: 5×10^{19}, 1×10^{20} and 1.5×10^{20} cm^{-3}. Full lines correspond to 3D QC MC simulations, while dashed lines refer to calibrated (against the QC MC) 3D QC DD simulations.

the QC DD is achieved by adjusting the mobility model and QC parameters as described in detail in [43]. To assess the validity of the calibration for the QC DD simulator, two extreme cases of channel height for the NW were chosen as shown in Fig. 1(a) and (c). In each case, the height is increased/decreased symmetrically by 1 nm for an N_D of 1.5×10^{20} cm^{-3}, without changing any of the calibration parameters. It was found that the QC DD results produce a negligible error, up to 3 %, for both modified devices when compared to the results obtained from the QC MC.

IV. MGG VARIABILITY

We have generated 300 random profiles with GSs of 3, 5 and 7 nm [52] for a meaningful statistical study of the MGG induced variability. These profiles were also applied to three maximum doping concentrations N_D to extensively investigate the capabilities of the QC DD and QC MC models. Note that the same MGG profiles are used in both simulation techniques, the QC DD and QC MC, for a fair comparison.

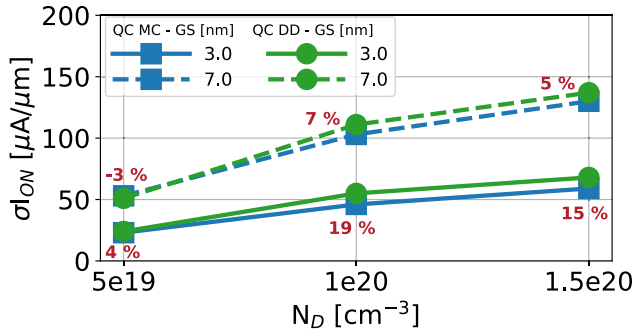

FIGURE 4. σI_{ON} due to MGG vs N_D from the QC DD and the QC MC simulations using 300 profiles. The difference between the QC DD and QC MC simulation results are indicated in percentage.

Fig. 4 shows the standard deviation (σ) of the I_{ON} against the maximum N_D. Both simulation methods show an increasing σI_{ON} with an increasing N_D. However, the difference between the σI_{ON} (indicated by percentage in the figure) predicted by both simulation methods is dependent on both

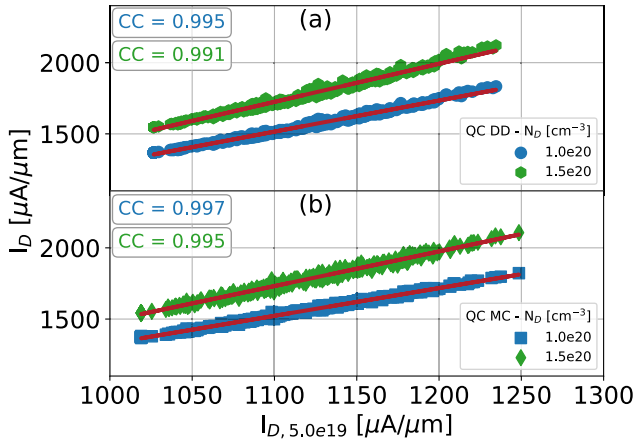

FIGURE 5. Scatter plots compare the simulations with $N_D = 1.5 \times 10^{20}$ cm^{-3} and 1×10^{20} cm^{-3} against $N_D = 5 \times 10^{19}$ cm^{-3} obtained from (a) QC DD and (b) QC MC. The GS is 7 nm.

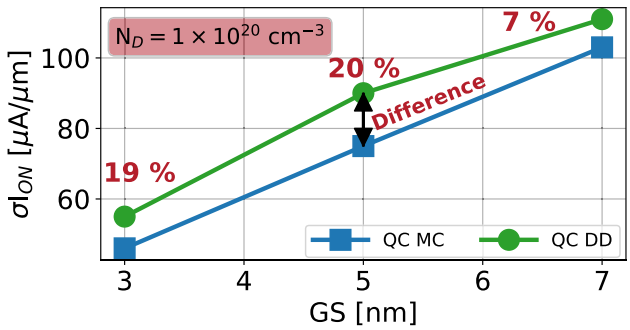

FIGURE 6. σI_{ON} due to MGG vs GS for a $N_D = 1 \times 10^{20}$ cm^{-3} obtained from the QC DD and the QC MC simulations. The difference between QC DD and QC MC are indicated in percentage.

the doping value and the grain size. For instance, for a N_D of 1×10^{20} cm^{-3}, the error in the predicted values by QC DD when compared to QC MC ones range from 7 % (7 nm GS) to 19 % (3 nm GS). Fig. 5 compares I_{ON} at $N_D = 5 \times 10^{19}$ against I_{ON} at $N_D = 1 \times 10^{20}$ and 1.5×10^{20} cm^{-3} obtained from the (a) QC DD and (b) QC MC simulations. There is a large correlation, as indicated by the correlation coefficients (CCs), between the I_{ON} values produced by both simulation methods. This means that the same profiles produce a similar variability even when the N_D is increased. Finally, investigation of the effect of the GS is shown in Fig. 6. Both simulation methods predict an increasing σI_{ON} with an increasing GS. However, the QC DD method leads to an overestimation of the MGG variability of around 20 % for GSs equal or lower than 5 nm. Furthermore, analysis of the mean (Δ) I_{ON} showed a negligible difference between the QC DD and QC MC methods.

A Fluctuation Sensitivity Map (FSM) [56] that analyzes the spatial effect of the MGG variability in key figure of merits (FoMs) (e.g. I_{ON}) is employed in order to reveal the most sensitive regions of the studied device to the MGG. The procedure is as follows: (i) a single synthetic profile is created, which has a WFV localized in a small strip wrapped around the gate (see example in Fig. 7(a)), (ii) this profile is then swept along the transport direction and the profile related to I_{ON} is extracted, and (iii) all the simulated profiles and their corresponding I_{ON} are used to create a 2D FSM as shown in Figs. 7(b) and (c) for the QC DD and QC MC simulations, respectively.

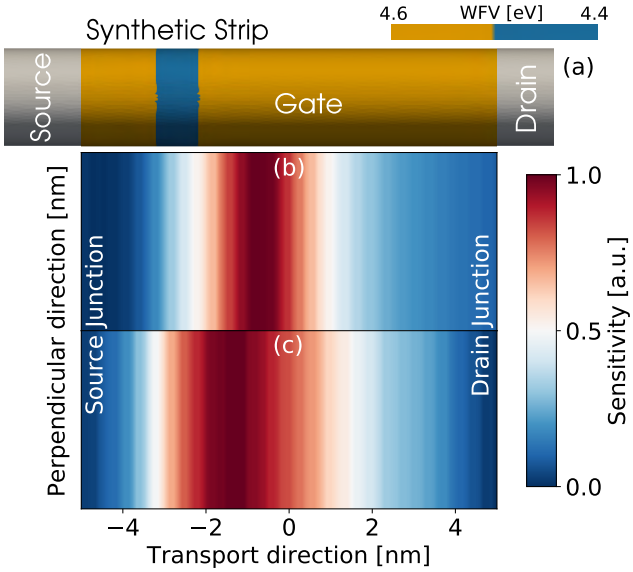

FIGURE 7. The schematic of the GAA NW FET gate area (a) with a single synthetic profile strip wrapped around the gate. The FSM for the I_{ON} are simulated assuming *n*-type source/drain concentration (N_D) of 1×10^{20} cm^{-3} using (a) QC DD and (b) QC MC techniques. 100 synthetic gate profiles with a width of 0.1 nm are simulated.

Thanks to the FSM technique, we are able to identify that for a 10 nm gate length GAA NW the most sensitive region of the gate is away from the centre of the gate, close to the gate-source junction. However, for the QC MC the maximum value is centered at around −1.8 nm while the QC DD predicts the maximum value at around −1.2 nm. Moreover, the QC DD predicts the highest sensitive effective area to be smaller than that shown by the QC MC results. Thus, we know that a change in the WFV in the aforementioned region will play a significant role in the σI_{ON} values.

V. LER VARIABILITY

Section III has shown that the QC DD calibrated to the QC MC simulations can predict the same I_{ON} for the NW FET. This ability has important implications for a LER induced variability study because the LER causes a fluctuation in the channel dimension along the transport direction. However, what is the accuracy of the QC DD produced variability when the channel cross-section dimension fluctuates? To answer this question, we generate 300 random LER profiles assuming a correlation length (CL) of 20 nm for four experimentally observed RMS heights [11], [29], [30] and three maximum doping concentrations N_D. The same LER profiles are used for both simulation techniques, the QC DD and QC MC, for a fair comparison.

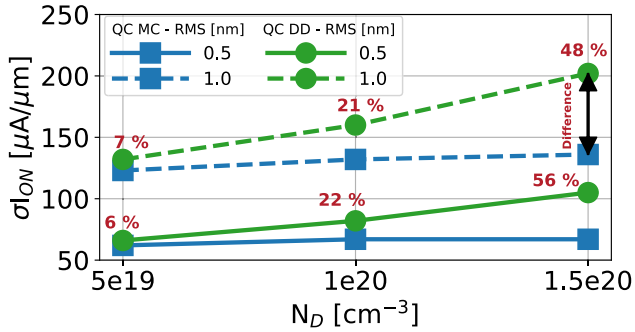

FIGURE 8. σI_{ON} due to LER vs N_D from the QC DD and the QC MC simulations using 300 profiles. The LER characteristic values are: CL = 20 nm and RMS heights of 1.0 and 0.5 nm. The difference between the QC DD and QC MC simulation results are indicated in percentage.

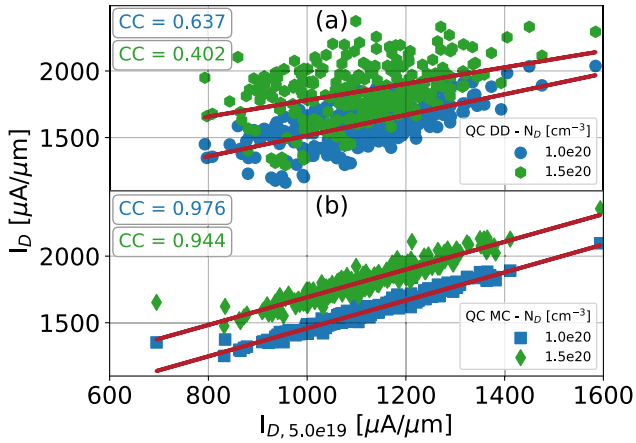

FIGURE 9. Scatter plots compare the simulations with $N_D = 1.5 \times 10^{20}$ cm^{-3} and 1×10^{20} cm^{-3} against $N_D = 5 \times 10^{19}$ cm^{-3} obtained from (a) QC DD and (b) QC MC simulations, respectively. The RMS height is 1 nm.

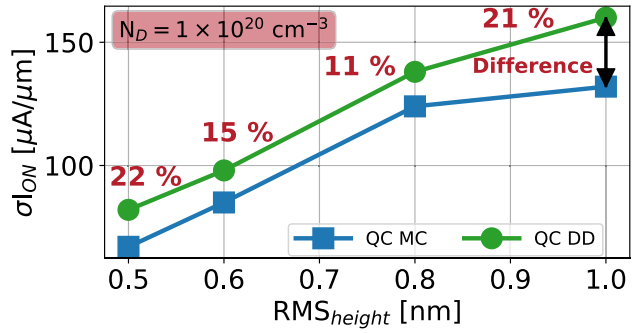

FIGURE 10. σI_{ON} due to LER vs RMS height for a $N_D = 1 \times 10^{20}$ cm^{-3} obtained from the QC DD and the QC MC simulations. The difference between QC DD and QC MC are indicated in percentage.

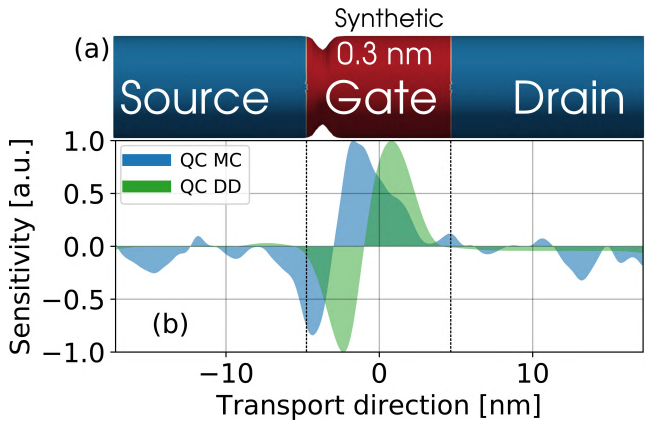

FIGURE 11. The GAA NW FET schematic (a) is scaled to the I_{ON} FSM (b). 100 synthetic profiles with a width deformation are simulated for N_D of 1.5×10^{20} cm^{-3} using QC DD and QC MC techniques as indicated.

Fig. 8 shows the standard deviation (σ) of the I_{ON} against the maximum N_D. The predicted σI_{ON} by the QC DD and QC MC simulation techniques has very similar values, with a difference of up to 7 %, for the devices with a N_D of 5×10^{19} cm^{-3}. Yet, the error in the estimation given by the QC DD simulations increases with N_D reaching a staggering 56% difference when compared to the results from QC MC simulations for a N_D of 1.5×10^{20} cm^{-3}. Finally, note that σI_{ON} is practically constant with dependence on N_D when obtained from the QC MC simulations, whereas the QC DD results predicts an increasing σI_{ON} with N_D. Note that the difference in the predicted behaviour lays in the implementation of quantum correction methods as well as the different models, classical DD vs. semi-classical MC. The Schrödinger based quantum corrections in the QC MC simulations are able to accurately capture the physics when some modification in the device architecture occurs, for example, doping, LER, MGG, etc. However, the simulation approach using density gradient quantum corrections would require adjusting the calibration parameters for each of the aforementioned modifications against a more complex simulation model. Furthermore, the MC method accounts for non-equilibrium electron transport as well as the inclusion of the important scattering models, which the DD model is not capable of. Further analysis of this behaviour is shown in Fig. 9 that compares I_{ON} at $N_D = 5 \times 10^{19}$ against I_{ON} at $N_D = 1 \times 10^{20}$ and 1.5×10^{20} cm^{-3}. The correlation between the I_{ON} values produced by the LER profiles from the QC DD simulations (Fig. 9(a)) is lower than for the QC MC ones (Fig. 9(b)) as indicated by the correlation coefficients (CCs). Finally, observe that the regression lines (red lines in Fig. 9) are shifted by a constant value for the QC MC obtained results and yet, for the QC DD ones, they also change the slope. The investigation of the effect of RMS height is shown in Fig. 10. The QC DD results give up to 22 % overestimation of a predicted σI_{ON} from the QC MC simulations. Additional analysis of the ΔI_{ON} showed a negligible difference between the QC DD and QC MC methods.

FSM [43] introduced in Section IV is also used to analyze the spatial effect of the LER variability induced by I_{ON}. The procedure is similar to the one used for the MGG variability: (i) a single synthetic profile is created, which has a Gaussian vertical deformation localized in a small region of the device (see Fig. 11(a)), (ii) the profile is then swept along the transport direction and a profile related to I_{ON} is

extracted, and (iii) each profile and the corresponding I_{ON} are used to create a 1D FSM as shown in Fig. 11(b). Note that a synthetic deformation for the LER can lead to an increase (negative sensitivity) or decrease (positive sensitivity) of the I_{ON}. Therefore, the normalized scale from -1 to 1 is used. Fig. 11 shows that the QC MC technique predicts the most sensitive regions to the LER variability closer to the source-gate junction than the locations predicted by the QC DD technique. Notice that there is not only a shift between the QC DD and QC MC largest absolute sensitive areas, but also the magnitude of the sensitivity is different. Finally, we can say that if a change in the diameter of a NW FET occurs near the middle of the gate or around the source-gate junction, it will heavily impact the I_{ON}, as shown by the FSM. However, changes in other parts of the NW FET dimensions will only have a negligible influence in the I_{ON}.

VI. CONCLUSION

We have demonstrated that using more accurate simulation tools such as a QC MC is critical to make a correct estimate of the ON-current variability in nanowire transistors at nanoscale when a dimension of the device is varied.

The findings for simulations of variability induced by the MGG can be summarized as:

- the difference in the predicted σI_{ON} values by the QC DD and QC MC method are dependent on GS, for example with a GS of 7 nm it is 7 %, yet for 3 nm it increases to 19 % at a N_D of 1×10^{20} cm^{-3};
- the difference between the QC DD and QC MC predicted σI_{ON} does not show a clear dependence on the N_D values;
- both the N_D and GS related σI_{ON} obtained from the QC DD simulations predict a similar behaviour to the QC MC results;
- the most sensitive region of the device to the MGG variability is wrongly predicted by the QC DD as compared to the QC MC simulations.

The findings for the simulation of the LER induced variability are different:

- the QC DD technique largely overestimates σI_{ON} for large N_D values (up to 56 % error) and RMS heights (up to 22 % error);
- the N_D related σI_{ON} obtained from the QC MC simulations predicts a constant variability, whereas the QC DD results in an increasing of σI_{ON};
- the most sensitive region of the device to the LER variability is wrongly predicted by the QC DD as compared to the QC MC simulations.

Furthermore, the ΔI_{ON} in both cases showed a negligible difference between the QC DD and QC MC methods. Moreover, the difference between results obtained from the QC DD and QC MC simulations of the LER cannot be predicted and the error between the two may be significant, which could lead to misleading predictions in the resistance against variability sources of future novel devices. We therefore warn against the use of purely classical techniques for variability studies that involve the variation of the channel cross-section in the ON-region regardless their calibration against reliable data. This is because the QC DD method has fixed calibration parameters which are "device dimension specific" while the QC MC uses the calibration free 2D Schrödinger equation to account for the actual quantum-mechanical confinement effect.

ACKNOWLEDGMENT

The authors would like to thank Centro de Supercomputación de Galicia (CESGA) for the computer resources provided.

REFERENCES

[1] O. Badami, F. Driussi, P. Palestri, L. Selmi, and D. Esseni, "Performance comparison for FinFETs, nanowire and stacked nanowires FETs: Focus on the influence of surface roughness and thermal effects," in *IEDM Tech. Dig.*, Dec. 2017, pp. 13.2.1–13.2.4.

[2] M. Li *et al.*, "Sub-10 nm gate-all-around CMOS nanowire transistors on bulk Si substrate," in *Proc. Symp. VLSI Technol.*, Jun. 2009, pp. 94–95.

[3] K. Nayak, S. Agarwal, M. Bajaj, K. V. R. M. Murali, and V. R. Rao, "Random dopant fluctuation induced variability in undoped channel Si gate all around nanowire n-MOSFET," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 685–688, Feb. 2015.

[4] Y.-S. Wu and P. Su, "Sensitivity of gate-all-around nanowire MOSFETs to process variations—A comparison with multigate MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3042–3047, Nov. 2008.

[5] S. Barraud *et al.*, "Opportunities and challenges of nanowire-based CMOS technologies," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Oct. 2015, pp. 1–3.

[6] J.-S. Yoon, T. Rim, J. Kim, M. Meyyappan, C.-K. Baek, and Y.-H. Jeong, "Vertical gate-all-around junctionless nanowire transistors with asymmetric diameters and underlap lengths," *Appl. Phys. Lett.*, vol. 105, no. 10, p. 102105, 2014.

[7] N. Seoane *et al.*, "Comparison of fin-edge roughness and metal grain work function variability in InGaAs and Si FinFETs," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1209–1216, Mar. 2016.

[8] X. Wang, A. R. Brown, B. Cheng, and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs," in *IEDM Tech. Dig.*, Dec. 2011, pp. 5.4.1–5.4.4.

[9] R. Wang *et al.*, "Investigation on variability in metal-gate Si nanowire MOSFETs: Analysis of variation sources and experimental characterization," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2317–2325, Aug. 2011.

[10] T. Matsukawa *et al.*, "Suppressing V_t and G_m variability of FinFETs using amorphous metal gates for 14 nm and beyond," in *IEDM Tech. Dig.*, Dec. 2012, pp. 8.2.1–8.2.4.

[11] S. Bangsaruntip *et al.*, "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," in *IEDM Tech. Dig.*, Dec. 2009, pp. 1–4.

[12] T. Linton, M. Chandhok, B. J. Rice, and G. Schrom, "Determination of the line edge roughness specification for 34 nm devices," in *IEDM Tech. Dig.*, Dec. 2002, pp. 303–306.

[13] S.-D. Kim, H. Wada, and J. C. S. Woo, "TCAD-based statistical analysis and modeling of gate line-edge roughness effect on nanoscale MOS transistor performance and scaling," *IEEE Trans. Semicond. Manuf.*, vol. 17, no. 2, pp. 192–200, May 2004.

[14] A. Paul *et al.*, "Comprehensive study of effective current variability and MOSFET parameter correlations in 14 nm multi-fin SOI FINFETs," in *IEDM Tech. Dig.*, Dec. 2013, pp. 13.5.1–13.5.4.

[15] A. Asenov *et al.*, "Variability aware simulation based design-technology cooptimization (DTCO) flow in 14 nm FinFET/SRAM cooptimization," *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1682–1690, Jun. 2015.

[16] L. Selmi *et al.*, "Modelling nanoscale n-MOSFETs with III-V compound semiconductor channels: From advanced models for band structures, electrostatics and transport to TCAD," in *IEDM Tech. Dig.*, Dec. 2017, pp. 13.4.1–13.4.4.

[17] D. Vasileska, S. M. Goodnick, and G. Klimeck, *Computational Electronics: Semiclassical and Quantum Device Modeling and Simulation*. Boca Raton, FL, USA: CRC Press, 2010. [Online]. Available: https://www.taylorfrancis.com/books/9781420064841

[18] A. Asenov, Y. Wang, B. Cheng, X. Wang, P. Asenov, T. Al-Ameri, and V. P. Georgiev, "Nanowire transistor solutions for 5nm and beyond," in *Proc. 17th Int. Symp. Qual. Electron. Design (ISQED)*, Mar. 2016, pp. 269–274.
[19] A. Khodadadian, L. Taghizadeh, and C. Heitzinger, "Three-dimensional optimal multi-level Monte–Carlo approximation of the stochastic drift–diffusion–Poisson system in nanoscale devices," *J. Comput. Electron.*, vol. 17, no. 1, pp. 76–89, Mar. 2018.
[20] C. Medina-Bailon *et al.*, "MS-EMC vs. NEGF: A comparative study accounting for transport quantum corrections," in *Proc. Joint Int. EUROSOI Workshop Int. Conf. Ultimate Integr. Silicon (EUROSOI-ULIS)*, Mar. 2018, pp. 1–4.
[21] U. Kovac, C. Alexander, G. Roy, C. Riddet, B. Cheng, and A. Asenov, "Hierarchical simulation of statistical variability: From 3-D MC with '*ab initio*' ionized impurity scattering to statistical compact models," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2418–2426, Oct. 2010.
[22] Y. Wang *et al.*, "Variability-aware TCAD based design-technology co-optimization platform for 7 nm node nanowire and beyond," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2016, pp. 1–2.
[23] C. Alexander, G. Roy, and A. Asenov, "Random-dopant-induced drain current variation in Nano-MOSFETs: A three-dimensional self-consistent Monte Carlo simulation study using '*ab initio*' ionized impurity scattering," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3251–3258, Nov. 2008.
[24] S. M. Nawaz, S. Dutta, A. Chattopadhyay, and A. Mallik, "Comparison of random dopant and gate-metal workfunction variability between junctionless and conventional FinFETs," *IEEE Electron Device Lett.*, vol. 35, no. 6, pp. 663–665, Jun. 2014.
[25] T. Yu, R. Wang, R. Huang, J. Chen, J. Zhuge, and Y. Wang, "Investigation of nanowire line-edge roughness in gate-all-around silicon nanowire MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 2864–2871, Nov. 2010.
[26] J.-S. Yoon, T. Rim, J. Kim, K. Kim, C.-K. Baek, and Y.-H. Jeong, "Statistical variability study of random dopant fluctuation on gate-all-around inversion-mode silicon nanowire field-effect transistors," *Appl. Phys. Lett.*, vol. 106, no. 10, p. 103507, 2015.
[27] H. Carrillo-Nuñez, M. M. Mirza, D. J. Paul, D. A. MacLaren, A. Asenov, and V. P. Georgiev, "Impact of randomly distributed dopants on *Omega*-gate junctionless silicon nanowire transistors," *IEEE Trans. Electron Devices*, vol. 65, no. 5, pp. 1692–1698, May 2018.
[28] L. Wang *et al.*, "Impact of self-heating on the statistical variability in bulk and SOI FinFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2106–2112, Jul. 2015.
[29] S. Bangsaruntip *et al.*, "Density scaling with gate-all-around silicon nanowire MOSFETs for the 10 nm node and beyond," in *IEDM Tech. Dig.*, Dec. 2013, pp. 20.2.1–20.2.4.
[30] M. A. Elmessary *et al.*, "Scaling/LER study of Si GAA nanowire FET using 3D finite element Monte Carlo simulations," *Solid-State Electron.*, vol. 128, pp. 17–24, Feb. 2017.
[31] N. Seoane, G. Indalecio, D. Nagy, K. Kalna, and A. J. García-Loureiro, "Impact of cross-sectional shape on 10-nm gate length InGaAs FinFET performance and variability," *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 456–462, Feb. 2018.
[32] M. A. Elmessary *et al.*, "Anisotropic quantum corrections for 3-D finite-element Monte Carlo simulations of nanoscale multigate transistors," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 933–939, Mar. 2016.
[33] D. Nagy, G. Indalecio, A. J. García-Loureiro, M. A. Elmessary, K. Kalna, and N. Seoane, "FinFET versus gate-all-around nanowire FET: Performance, scaling, and variability," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 332–340, Feb. 2018.
[34] M. Stadele *et al.*, "A comprehensive study of corner effects in tri-gate transistors," in *Proc. Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2004, pp. 165–168.
[35] R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 55, no. 12, pp. 2192–2193, Dec. 1967.
[36] K. Yamaguchi, "Field-dependent mobility model for two-dimensional numerical analysis of MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-26, no. 7, pp. 1068–1074, Jul. 1979.
[37] K. Tomizawa, *Numerical Simulation of Submicron Semiconductor Devices* (Artech House Materials Science Library). Norwood, MA, USA: Artech House, 1993.
[38] C. Jacoboni and P. Lugli, *The Monte Carlo Method for Semiconductor Device Simulation* (Computational Microelectronics). Vienna, Austria: Springer, 2012.
[39] B. K. Ridley, "Reconciliation of the Conwell–Weisskopf and Brooks-Herring formulae for charged-impurity scattering in semiconductors: Third-body interference," *J. Phys. C, Solid State Phys.*, vol. 10, no. 10, p. 1589, 1977.
[40] T. G. Van de Roer and F. P. Widdershoven, "Ionized impurity scattering in Monte Carlo calculations," *J. Appl. Phys.*, vol. 59, no. 3, pp. 813–815, 1986.
[41] D. Ferry, *Semiconductor Transport*. London, U.K.: Taylor & Francis, 2000.
[42] A. Islam and K. Kalna, "Monte Carlo simulations of mobility in doped GaAs using self-consistent Fermi–Dirac statistics," *Semicond. Sci. Technol.*, vol. 26, no. 5, p. 039501, 2011.
[43] G. Indalecio, A. J. García-Loureiro, M. A. Elmessary, K. Kalna, and N. Seoane, "Spatial sensitivity of silicon GAA nanowire FETs under line edge roughness variations," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 601–610, Apr. 2018.
[44] A. J. García-Loureiro *et al.*, "Implementation of the density gradient quantum corrections for 3-D simulations of multigate nanoscaled transistors," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 30, no. 6, pp. 841–851, Jun. 2011.
[45] M. Aldegunde, A. J. García-Loureiro, and K. Kalna, "3D finite element Monte Carlo simulations of multigate nanoscale transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1561–1567, May 2013.
[46] M. Aldegunde, N. Seoane, A. J. García-Loureiro, and K. Kalna, "Reduction of the self-forces in Monte Carlo simulations of semiconductor devices on unstructured meshes," *Comput. Phys. Commun.*, vol. 181, no. 1, pp. 24–34, Jan. 2010.
[47] J. Lindberg *et al.*, "Quantum corrections based on the 2-D Schrödinger equation for 3-D finite element Monte Carlo simulations of nanoscaled FinFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 423–429, Feb. 2014.
[48] G. Indalecio, A. J. García-Loureiro, N. S. Iglesias, and K. Kalna, "Study of metal-gate work-function variation using Voronoi cells: Comparison of Rayleigh and Gamma distributions," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2625–2628, Jun. 2016.
[49] X. Wang, A. R. Brown, N. Idris, S. Markov, G. Roy, and A. Asenov, "Statistical threshold-voltage variability in scaled decananometer bulk HKMG MOSFETs: A full-scale 3-D simulation scaling study," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2293–2301, Aug. 2011.
[50] H. Nam and C. Shin, "Comparative study in work-function variation: Gaussian vs. Rayleigh distribution for grain size," *IEICE Electron. Express*, vol. 10, no. 9, p. 20130109, 2013.
[51] T. Kamei *et al.*, "Experimental study of physical-vapor-deposited titanium nitride gate with an n+-polycrystalline silicon capping layer and its application to 20 nm fin-type double-gate metal–oxide–semiconductor field-effect transistors," *Jpn. J. Appl. Phys.*, vol. 50, no. 4S, p. 04DC14, 2011.
[52] H. F. Dadgour, K. Endo, V. K. De, and K. Banerjee, "Grain-orientation induced work function variation in nanoscale metal-gate transistors—Part I: Modeling, analysis, and experimental validation," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2504–2514, Oct. 2010.
[53] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1254–1260, May 2003.
[54] ITRS. (2016). *International Technology Roadmap for Semiconductors*. [Online]. Available: http://www.itrs2.net/
[55] V. P. Georgiev *et al.*, "Experimental and simulation study of a high current 1D silicon nanowire transistor using heavily doped channels," in *Proc. IEEE Nanotechnol. Mater. Devices Conf. (NMDC)*, Oct. 2016, pp. 1–3.
[56] G. Indalecio, N. Seoane, K. Kalna, and A. J. García-Loureiro, "Fluctuation sensitivity map: A novel technique to characterise and predict device behaviour under metal grain work-function variability effects," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1695–1701, Apr. 2017.

DANIEL NAGY received the M.Res. degree in nanoscience to nanotechnology and the Ph.D. degree in electronic and electrical engineering from Swansea University, Swansea, U.K., in 2013 and 2016, respectively.

He currently holds a Postdoctoral position with the Centro Singular de Investigación en Tecnoloxías da Información, University of Santiago de Compostela, Santiago de Compostela, Spain

GUILLERMO INDALECIO received the B.S. degree in physics and the Ph.D. degree in semiconductor device simulation from the University of Santiago de Compostela, Santiago de Compostela, Spain, in 2010 and 2016, respectively.

He was a Visiting Researcher with the University of Swansea, Swansea, U.K., in 2015. His current research interests include electronic devices simulation with a focus on computational techniques and novel techniques to understand variability sources.

ANTONIO J. GARCÍA-LOUREIRO received the Ph.D. degree from the University of Santiago de Compostela, Santiago de Compostela, Spain, in 1999.

He is currently an Associate Professor with the Department of Electronics and Computer Science, University of Santiago de Compostela. His current research interests include the multidimensional simulations of nanoscale transistors and solar cells.

GABRIEL ESPIÑEIRA received the B.S. degree in physics from the University of Santiago de Compostela, Santiago de Compostela, Spain, in 2018, where he is currently pursuing the M.Res. degree in HPC and also with the Centro Singular de Investigación en Tecnoloxías da Información.

MUHAMMAD A. ELMESSARY received the B.Sc. degree (Hons.) in computer and systems engineering and the M.Sc. degree in engineering physics from Mansoura University, Mansoura, Egypt, in 2004 and 2010, respectively, and the Ph.D. degree in semiconductor device simulation from Swansea University, Swansea, U.K., in 2017.

He is currently a Research Assistant with Swansea University.

KAROL KALNA received the M.Sc. (Hons.) and Ph.D. degrees from Comenius University, Bratislava, Czechoslovakia, in 1990 and 1998, respectively.

He is currently an Associate Professor leading the Nanoelectronic Devices Computational Group, Swansea University, Swansea, U.K. He has held the EPSRC Advanced Research Fellowship and has pioneered III–V MOSFETs, since 2002. He has published 93 peer-review papers and has given over 20 invited talks.

NATALIA SEOANE received the Ph.D. degree from the University of Santiago de Compostela, Santiago de Compostela, Spain, in 2007.

She was a Visiting Postdoctoral Researcher with the University of Glasgow, Glasgow, U.K., from 2007 to 2009, The University of Edinburgh, Edinburgh, U.K., in 2011, and Swansea University, Swansea, U.K., from 2013 to 2015. She is currently with the University of Santiago de Compostela.