

DC Busbar Protection for HVDC Substations Incorporating Power Restoration Control Based on Dyadic Sub-Band Tree Structures

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ABSTRACT In this paper, a new direct current (dc) busbar protection for high voltage dc (HVdc) substations is proposed. The proposed scheme relies on the instantaneous current measurements obtained from the elements (lines and converters) connected to a dc busbar. Such current measurements are analyzed through dyadic sub-band tree structures that are used to extract the specific features, such as polarity, wavelet energy, and wavelet energy ratios. The performance of the scheme is assessed through the transient simulation using the verified PSCAD models. The simulation results revealed that the scheme can: 1) discriminate, effectively and within a very short period of time, between the internal and external faults; 2) detect pole-to-pole and pole-to-ground faults (both solid and highly resistive); 3) switch to healthy busbars (if available) to allow continuous operation; 4) re-energize the converter and restore the power to pre-fault conditions; and 5) remain stable during disturbances and external faults.

INDEX TERMS Multi-terminal direct current grids, dyadic sub-band tree structures, HVDC transmission, HVDC circuit breakers.

I. INTRODUCTION

Efficient and flexible power transmission over long distances is expected to be realized by the deployment of Voltage-Source Converters (VSCs) and High Voltage Direct Current (HVDC) grids. The VSC technology is advantageous due to its contribution to the controllability, power quality and services support (e.g. reactive power, black start capability) of the existing and future power networks [1]. Apart from the existing point-to-point HVDC links, additional technological benefits are anticipated to arise with the realization and deployment of Multi Terminal Direct Current (MTDC) systems [2]–[5]. However, in order to enable a broad deployment of MTDC grids, a number of potential challenges should be mitigated in order to establish a reliable, efficient, and secure operation. A vast amount of the challenges of MTDC grids are associated with DC-side faults accounting for detection, control, protection and isolation [6], [7].

DC-side faults on High Voltage Direct Current (HVDC) networks are characterized by large inrush currents escalating over a short period of time [8]. After the occurrence of a DC-side fault, protection systems are expected to minimize its onerous effects, by initiating clearing actions such as

selective tripping of Circuit Breakers (CBs). Consequently, there is a need for fast and discriminative protection systems to enable fast detection and isolation of fault currents [9].

Recent advancements in relay algorithms have enabled discriminative and fast detection of DC-side faults. This has been achieved by utilizing unit or non-unit protection structures. For example, non-unit protection schemes based on transient post-fault voltage signatures have been proposed in [10] and [11]. A few other non-unit schemes depending on current measurements (and also on voltage) can be also found in [6], [12], and [13]. There are also a number of differential type schemes proposed in technical literature [14], [15].

Most of the above-reviewed methods focus mainly on detection and discrimination methods for faults occurring on feeders (i.e. transmission lines and cables). Research on busbar faults has been mainly conducted to illustrate the stability of the proposed schemes to external faults. As such, the research still needs to be enhanced for protection strategies (detection and isolation) focusing on faults occurring on HVDC substations (i.e. busbar faults). Busbar faults are quite more detrimental when compared to feeder faults due to the fact that the impedance is significantly lower (i.e. due

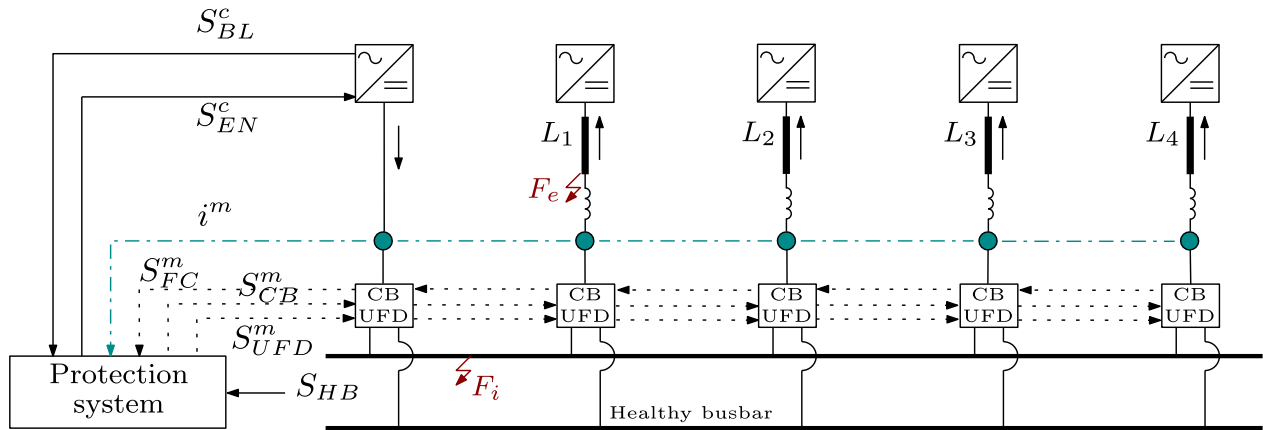


FIGURE 1. Typical representation of an HVDC substation incorporating double busbar configuration.

to the lack of any line impedance to the fault). Consequently, the sources connected to the faulted busbars are subjected to severe electrical and mechanical stresses. Moreover, when busbar faults occur, a larger portion of the network is disconnected leading to longer and more significant power outage and reduced availability and stability of the network [16].

The available protection methods to detect busbars faults in HVDC networks can be found in [13], [15], and [17]. In these methods, busbar protection is achieved by the well-known principle of instantaneous differential current and its comparison with a near-zero threshold value. Such protection schemes are not developed as standalone research objects but they are rather a part of a wider protection system, focusing on feeder protection. As such, their performance has not been scrutinized under severe scenarios and consequently the design is not very sophisticated. Specifically, even though Instantaneous Current Differential Protection (ICDP) can be fast, its performance might be compromised during wide or local disturbances and external faults.

Another significant research gap found in the relevant technical literature (both for busbar and feeder protection schemes) is that after the detection and disconnection of the faulted parts, there is no information exchange for power restoration. For example, usually after faults, local (and possibly remote) converters will shut-down for self-protection purposes. Therefore, information could be exchanged between the local relays and converters to enable smooth and faster power restoration. Taking all the above into account, a novel busbar protection scheme is proposed in this paper. In order to further demonstrate the technical merits of the proposed scheme, its performance has been compared with conventional ICDP.

II. PROPOSED BUSBAR PROTECTION

A high-level structure of the proposed scheme can be seen in Fig. 1 where a double busbar configuration is adopted. The substation comprises of Voltage Source Converters (VSCs), CBs, Ultra Fast Disconnectors (UFDs) and

transmission lines. The proposed protection scheme utilizes the following signal exchange:

- i^m : Instantaneous current measurements from each feeder connected to the busbar (input).
- S^m_{CB} : Tripping signal to CBs (output).
- S^m_{FC} : Fault clearance signal from CBs (input).
- S^m_{UFD} : Switching signal to UFDs (output).
- S^c_{ST} : Status signal from local converters (input).
- S^c_{EN} : Enable signal to local converters (output).
- S_{HB} : Signal for healthy busbar availability (input).

The superscript m denotes the index number of each connected feeder incorporating the protection elements (i.e. current sensors, CBs and UFDs), and superscript c denotes the index of the locally-connected converters connected to the DC busbar.

As illustrated in Fig. 2, the proposed scheme consists of four modules: i) Signal Acquisition Module (SAM), ii) Fault Detection and Discrimination Module (FDDM), iii) Stability of Protection Module (SOPM) and iv) Power Restoration Module (PRM). The protection algorithm is explained in detail in the following subsections.

A. SIGNAL ACQUISITION MODULE

The purpose of SAM is to receive the current measurements i^m and sample them to the desired frequency in conjunction with low-pass filtering.

Following filtering, current traces are analyzed using dyadic sub-band tree structures. Such sub-band structures are a multi-resolution powerful tool for signal processing. The characteristic feature of multi-resolution sub-band structures is that they split the frequency band of the signal into two bands at each level of the tree, and then decompose only one of these bands at the next level [18]. For the needs of the proposed protection and control scheme, Wavelet Transform (WT) has been put forward as a dyadic sub-band tree. Initially, WT-based processing is achieved by selecting the

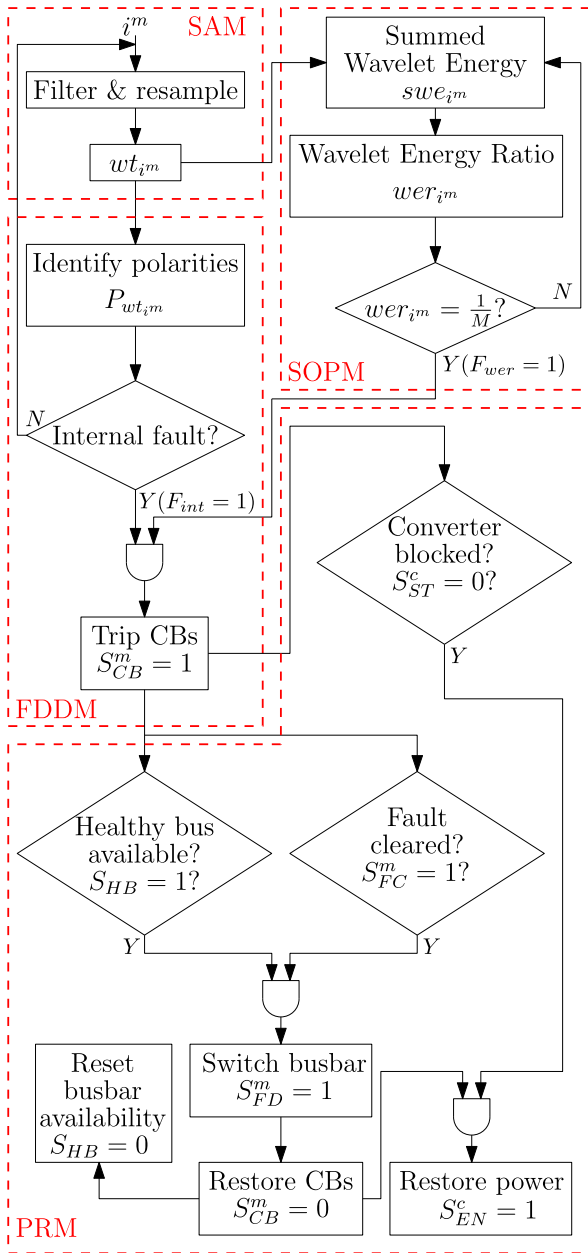


FIGURE 2. Algorithm of proposed protection scheme.

base wavelet $\psi(t)$ which satisfies the following condition:

$$\int_{\mathbb{R}} \psi(t)dt = 0 \quad (1)$$

where \mathbb{R} is a set of real numbers.

The family wavelet $\psi_{\alpha,b}(t)$ is composed via dilation and translation which are driven by parameters α and b respectively:

$$\psi_{\alpha,b}(t) = \frac{1}{\sqrt{\alpha}} \psi\left(\frac{t-b}{\alpha}\right), \quad \alpha, b \in \mathbb{R}, \alpha \neq 0 \quad (2)$$

Therefore, the WT of each current measurement i^m can be achieved by:

$$wt_{i^m} = \frac{1}{\sqrt{\alpha}} \int_{-\infty}^{\infty} i^m(t) \psi\left(\frac{t-b}{\alpha}\right) dt \quad (3)$$

Even though equation (3) provides the basis for WT, the fact that it needs to be realized by digital systems in conjunction with discrete signals, strengthens the requirement for discretization.

When a discrete dyadic wavelet transform is applied to a discrete signal $i^m(n)$, the signal can be decomposed into discrete wavelet approximations A and discrete wavelet details W :

$$A_{\alpha} i^m(n) = \sum_k h_k A_{2^{j-1}} i^m(n - 2^{j-1} - k) \quad (4)$$

$$W_{\alpha} i^m(n) = \sum_k g_k A_{2^{j-1}} i^m(n - 2^{j-1} - k) \quad (5)$$

where h_k and g_k are the wavelet coefficients determined by the wavelet function, which correspond to high-pass and low-pass coefficients respectively. The dilation parameter α can only be a power-of-two series 2^j , where j is the level of decomposition.

This decomposition is repeated at each level to further increase the frequency resolution. The discrete wavelet approximations A and discrete wavelet details W are decomposed with high and low pass filters and then down-sampled by a factor of 2 as depicted in Fig. 3.

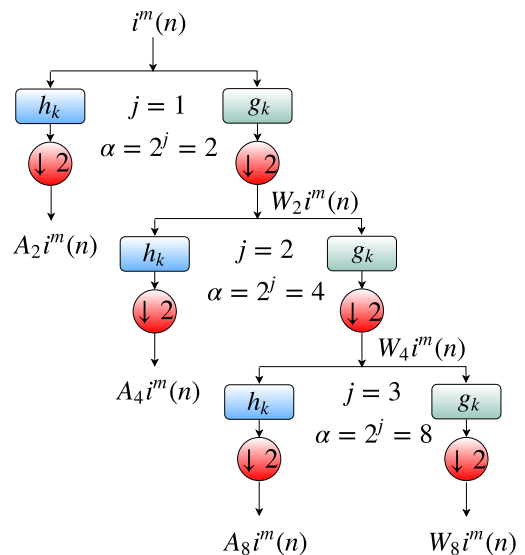


FIGURE 3. Typical representation of a dyadic sub-band tree structure.

This procedure is practically expressed as a binary tree with nodes reflecting a sub-band with a different time-frequency localization (also known as filter banks). At each level in the above diagram the signal is decomposed into low and high frequencies.

Consequently it can be understood that WT can be obtained by iterating a low-pass filter at each level, within a dyadic tree structure. It should be noted that historically, Wavelet-based busbar protection has been proposed for AC systems [19], [20] to mitigate issues arising from CT saturation, transformer energization and magnitude mismatch. In this paper, a Wavelet-based protection scheme for HVDC substations is proposed to further improve the performance of conventional ICDP.

B. FAULT DETECTION & DISCRIMINATION MODULE

After the WT of current measurements i^m has been obtained, a potential fault case is detected and characterized either as internal or external. This is achieved by identifying the polarities $P_{wt_i^m}$ of WT, using the notation depicted in Fig. 4.

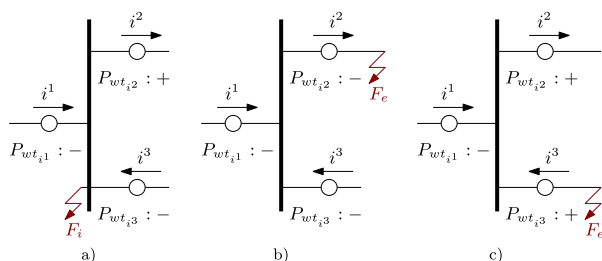


FIGURE 4. DC busbar fault illustrating the polarity $P_{wt_i^m}$ of travelling waves on measuring points with different current direction and measuring notation: a) internal fault (F_i) on DC busbar, b) external fault (F_e) on element 2, c) external fault (F_e) on element 3.

When a fault occurs (either internal or external), travelling waves (TWs) initiated from the fault point travel towards the connected element until they meet a point of measurement. At this point, the initial wave-fronts will appear either positive or negative, depending on the assumed current measurement convention i^m (i.e. i^1, i^2, i^3) and the location of the fault (i.e. inside or outside the busbar). Thus, a decision can be made whether the fault is internal or external.

The Modulus Maxima (MM) of WT (WTMM) is used to extract the polarities of TWs which corresponds to the local maxima of the detail coefficients of WT. MM is a good indicator for the extraction of wave-fronts and polarities of TWs (which are practically discontinuity points), due to the fact they occur at the same time instant as the discontinuity points [21].

WTMM is a strictly local maximum of the modulus either on the left or right side of instant t at scale α . Therefore, WTMM is true if the following conditions are met [22], [23]:

$$\forall \epsilon > 0, \exists |t - t_0| < \epsilon, t \neq t_0 \rightarrow |w(\alpha, t_0)| < |w(\alpha, t)| \quad (6)$$

If the fault is classified as internal the algorithm will generate a flag $F_{int} = 1$. Considering the transient is an actual fault (and not a disturbance) as identified by the SOPM, the algorithm will initiate a tripping signal ($S_{CB}^M = 1$) to the corresponding CBs.

C. STABILITY OF PROTECTION MODULE

The purpose of SOPM is to provide stability to external disturbances, faults and other possible transients (e.g. short spikes in current measurements) which could jeopardise the performance of the proposed scheme. The stability of protection is achieved by extracting the wavelet energy we_{i^m} , the summed wavelet energy swe_{i^m} of the WT of all current measurements over a moving window Z , and the wavelet energy ratios wer_{i^m} of each current measurement individually. The wavelet energy we_{i^m} and wavelet energy ratio wer_{i^m} are given by equations (7) and (8) respectively.

$$we_{i^m} = \sum_{z=1}^Z [wt_{i^m}(z)]^2 \quad (7)$$

$$wer_{i^m} = \frac{we_{i^m}}{k_w + swe_{i^m}} = \frac{\sum_{z=1}^Z [wt_{i^m}(z)]^2}{k_w + \underbrace{\sum_{m=1}^M \left(\sum_{z=1}^Z [wt_{i^m}(z)]^2 \right)}_{\text{summed wavelet energy } swe_{i^m}}} \quad (8)$$

where Z is the length of moving time window, and M the number of each connected feeder. A factor k_w is added to the calculation of wer_{i^m} to prevent division with zero at normal operation or during zero-crossing transients.

When an internal fault occurs, TWs are generated from the fault point travel until they meet a measuring point (refer to Fig. 4). At the very first instant of TWs arrival at measuring points, the detection and contribution from the connected elements is expected to be fairly equal. As such, the calculated wavelet energy ratio for each element m will theoretically be $wer_{i^m} = \frac{1}{M}$. Even though during external disturbances (or other type of transients) the wavelet energy ratios can reach higher values (even higher than $\frac{1}{M}$) this will not be reflected equally for all the connected elements. For example, a disturbance on one line or one measurement point, will not induce equal wavelet energy (and hence the same wavelet energy ratio) to all the current measurements. When the condition $wer_{i^m} = \frac{1}{M}$ is true, the SOPM will confirm that the transient is an actual internal fault and will generate a flag $F_{wer} = 1$. It should be noted that for stability-related reasons, the criterion for wavelet energy ratios has been extended to include a margin of $\pm 5\%$. Practically, a flag $F_{wer} = 1$ will be generated if $wer_{i^m} = \frac{1}{M} \pm 5\%$.

D. POWER RESTORATION MODULE

The PRM is included in the algorithm to implement two basic operations: i) switch to healthy busbars (if available) in case of internal faults and ii) re-energize the converters connected locally to the busbars in the case they are switched-off (during over-current conditions such as DC-side faults, converters usually shut-down to protect the power electronic components from damage).

When the FDDM has initiated a tripping signal to the CBs, the algorithm will examine the availability for a healthy

busbar (i.e. if $S_{HB} = 1$). It is worth noting that busbar redundancy is a common practice for AC transmission systems and hence it could be adopted for HVDC substations [24], allowing continuous operation and reduced downtime. The switching is achieved by triggering the UFDs ($S_{UFD}^m = 1$) taking also into account that the fault is cleared (i.e. $S_{FC}^m = 1$). This is achieved by monitoring the status of the CBs. For example, in most of the CB designs there is a residual switch which opens when the fault is cleared. When the switching is achieved, the algorithm will restore the CBs ($S_{CB}^m = 0$) and will also change the availability of the healthy busbar ($S_{HB} = 0$). When these actions are executed, the algorithm will monitor if the local converters are switched off (i.e. if $S_{ST}^c = 0$). If this statement is true, the algorithm will initiate a re-energizing signal ($S_{EN}^c = 1$) to the locally-connected converters.

III. INFRASTRUCTURES OF HVDC SUBSTATION

A. DC BREAKERS SWITCHGEAR

Recent research on DC breakers for HVDC grids has revealed of few possible solutions towards DC fault current interruption and current re-routing.

Several switchgear concepts have been proposed which include solid state [25], hybrid [26], [27], super conducting [28], resonant [29], DC/DC converters [30], [31], integrated CBs with current flow control capability [2], [32], multi-port/hybrid solutions [33] and DC/DC current flow controllers [34], [35]. All the architectures for DC breakers and UFDs have their own advantages and disadvantages. However the selection of a proper solution is subjected to desired speed of operation, controllability, operational losses, required components, investment and operational cost, applicability and expected fault current signatures [36], [37].

For the studies presented in this paper, hybrid circuit breakers and ultra fast disconnectors have been utilized. Their speed of operation is dictated by the speed of operation of fast mechanical disconnectors, which is 2 ms [11]. Faster fault current interruption and switching could be achieved by utilizing a solid state approach, but this solution would impose larger conduction losses during steady state operation.

B. SIGNAL EXCHANGE

Due to the fast-acting response required by the proposed protection system, it is important to consider the practical impact of time delays for signal exchange involved in an actual implementation. It is assumed that the current measurements have been obtained at a sampling frequency of 96 kHz which conforms to IEC 61869-9 [38]. It should be noted that even though the IEC 61869-9 standard has recommended the sampling frequency of 96 kHz for DC instrument transformer applications, the research investigating its performance and suitability for DC protection is very limited in the open literature [17]. As such, another important contribution of the present work is the investigation and utilization of IEC 61869-9 for protection of HVDC grids.

All of the measurements required for the protection system are local within the substation and therefore there is no latency associated with wide-area communications. If the current sensors are directly wired to a centralized protection system, then the maximum measurement delay (assuming that a fault occurs immediately after a sample is digitized) is the reciprocal of the sampling rate (i.e. $1/96\text{ kHz} = 10.4\ \mu\text{s}$). However, a more practical approach for modern digital substations is to locally digitize and time-stamp the current samples at each current sensor, and use a communications network to transmit signals to the protection system. A benefit of using a communications network is that standards-based methods for network redundancy [39] can be used to improve reliability. The method given in [17] can be used to calculate the maximum measurement and communications delay, which would be $37.22\ \mu\text{s}$ for the arrangement given in Fig. 1. In either case, the impact of measurement and communications is relatively small compared to the overall trip times (refer to Section IV-D) and will not unduly affect real-time operation of the proposed protection system. Regarding the sensor technology any modern current sensors could be adopted including distributed optical sensors [14].

IV. SIMULATION-BASED PERFORMANCE ANALYSIS

A. HVDC SUBSTATION TEST MODEL

An HVDC substation test model as shown in Fig. 1, with double busbar configuration has been developed in PSCADTM/EMTDCTM. At the HVDC substation depicted in Fig. 1 there is one converter connected locally to the busbar and four which are remotely connected through transmission lines. All the converters are modelled as modular multi-level converters (MMCs) operating at $\pm 400\text{ kV}$ (in symmetric monopole configuration). It should be noted that the proposed protection scheme operates independently for each pole. This enables its adoption to HVDC grids with different converter architectures (e.g. monopole, bipole, etc.). The representation of the transmission lines utilize the frequency dependent model. The parameters of the network are described in Table 1.

TABLE 1. Test model parameters.

Parameter	Value
DC voltage [kV]	800
AC voltage [kV]	400
AC short-circuit level [GVA]	40
AC frequency [Hz]	50
Lengths of lines 1 to 4 [km]	300, 200, 600, 180
Power rating of converters 1 to 5 [MVA]	500, 100, 100, 100, V_{dc} ctrl.

The notation for each current measurement of each feeder connected to the busbar is shown with black arrows in Fig. 1. Based on this notation, the polarities of TWs for internal F_i and external F_e faults are illustrated in Table 2.

For the tuning of the dyadic tree, the coefficients presented in Table 3 have been used.

TABLE 2. Travelling wave polarities for internal and external faults.

	F_i	$F_{e(L1)}$	$F_{e(L2)}$	$F_{e(L3)}$	$F_{e(L4)}$
Converter	-	-	-	-	-
Line 1	+	-	+	+	+
Line 2	+	+	-	+	+
Line 3	+	+	+	-	+
Line 4	+	+	+	+	-

TABLE 3. Dyadic sub-band tree coefficients.

h_k	g_k
-0.2304, 0.7148, -0.6309, -0.0280,	-0.0106, 0.0329, 0.0308, -0.1870,
0.1870, 0.0308, -0.0329, -0.0106	-0.0280, 0.6309, 0.7148, 0.2304

B. FAULT SCENARIOS

In order to test the sensitivity and stability of the proposed scheme, the case scenarios included in Table 4 have been generated and presented graphically in the following subsection. The faults for these scenarios include solid pole-to-pole faults and disturbances triggered at $t = 2\text{ ms}$.

TABLE 4. Description of case scenarios.

Scenario	Description
I	Internal fault (no healthy busbar available for switching)
II	Internal fault (healthy busbar available for switching)
III	External fault at Line 1
IV	Internal busbar disturbance

The performance of the proposed scheme under highly resistive faults and other types of faults are presented later in Section IV-D.

C. SIMULATION RESULTS

1) FAULT SCENARIO I

The response of the protection system to Fault Scenario I is presented in Fig. 5.

After the fault is triggered at $t = 2\text{ ms}$, there is a rapid increase in the current from the converter and connected lines (refer to Fig. 5(a)).

Based on the WTMM of DC currents, the polarities of TWs are extracted (refer to Fig. 5(b)), which verify that the fault is internal, setting the flag $F_{int} = 1$ (refer to Fig. 5(d)). It should be noted that the table inside Fig. 5(b) illustrates the polarities of TWs which are consistent with the notation of internal faults as described in Table 2.

The algorithm will proceed to the calculation of wavelet energy ratios wer_{i^m} to verify the actual presence of a fault. The contribution of TWs from all the connected elements at this case is fairly equal (refer to Fig. 5(c)) and satisfy the condition $wer_{i^m} = \frac{1}{M} \pm 5\%$, setting the flag $F_{wer} = 1$. Therefore, the algorithm will initiate a tripping command ($S_{CB}^m = 1$) to the CBs connected to the faulted busbar. Since there is no healthy busbar available ($S_{HB} = 0$), there is no further action for power restoration or switching.

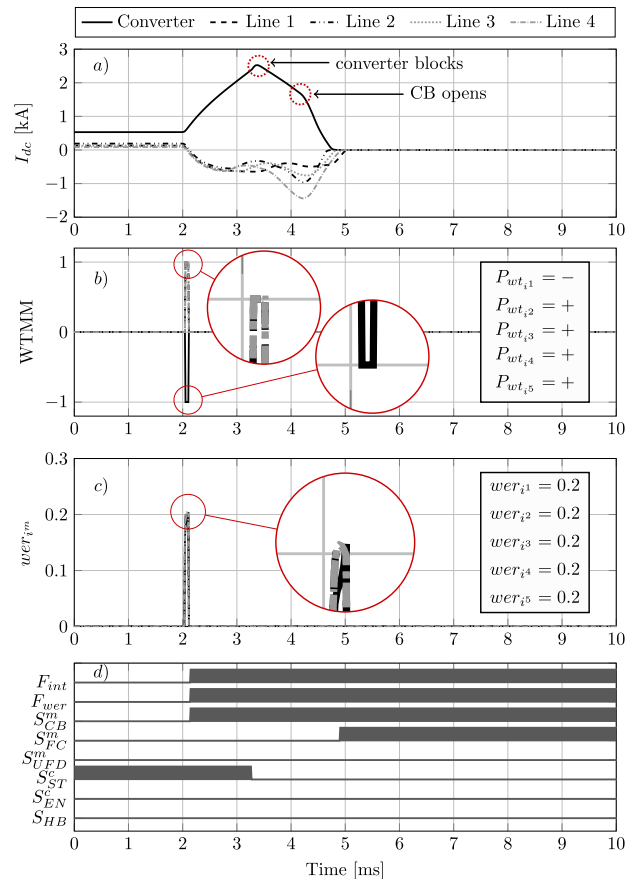


FIGURE 5. Response of protection system to internal fault (no healthy busbar available): a) DC currents, b) WTMM of DC currents, c) wer of DC currents, d) Control and tripping signals.

2) FAULT SCENARIO II

The response of the protection system to Fault Scenario II is presented in Fig. 6.

From the detection point of view, it can be seen from Fig. 6(b) and Fig. 6(c) that an internal fault is successfully identified (also refer to F_{int} and F_{wer} in Fig. 6(d)). This leads to the tripping of CBs ($S_{CB}^m = 1$). During the fault, the converter is also blocked ($S_{ST}^m = 0$) due to over-current conditions. After the fault is cleared ($S_{FC}^m = 1$), and since there is a healthy busbar available ($S_{HB} = 1$), a switching command is sent to the UFDs ($S_{UFD}^m = 1$).

However, after approximately $t = 2\text{ ms}$ of the UFD switching command (this corresponds to the operational time delay of UFDs), the protection system sends an enabling pulse for 1 ms ($S_{EN}^c = 1$) to the converter. This results to the converter being re-energized ($S_{ST}^m = 1$) to pre-fault conditions after approximately 80 ms (refer to the zoomed-out window inside Fig. 6(a)). Moreover, the availability of busbar is set to zero ($S_{HB} = 0$) to prohibit any switching operation in case of a sequential internal busbar fault. Finally, the remaining operating flags and signals are reset to pre-fault conditions (refer to Fig. 6(d)).

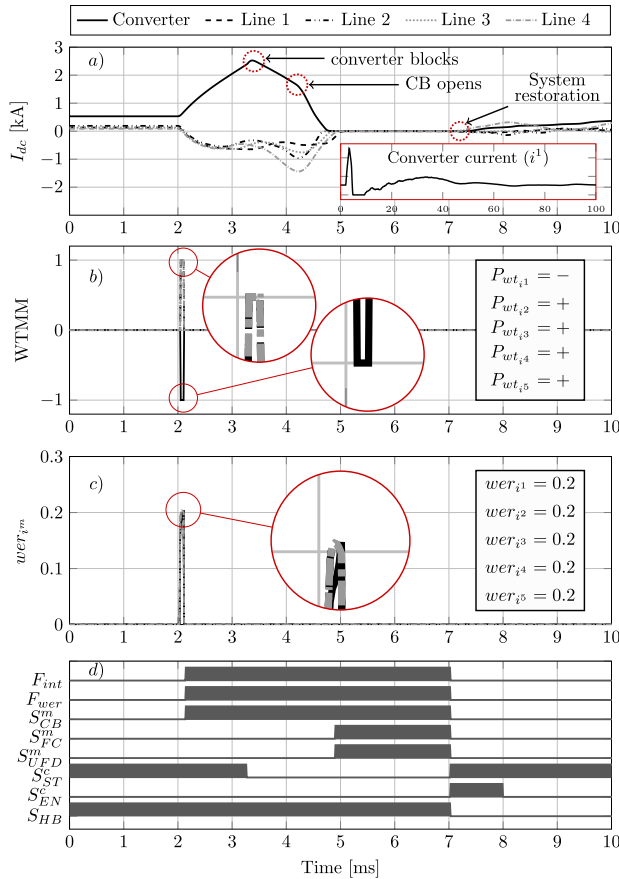


FIGURE 6. Response of protection system to internal fault considering a healthy busbar available: a) DC currents, b) WTMM of DC currents, c) wer of DC currents, d) Control and tripping signals.

3) FAULT SCENARIO III

An external fault F_e is triggered at the beginning of Line 1, as illustrated in Fig. 1.

The response of the protection system for this fault scenario is depicted in Fig. 7. After the fault is triggered at $t = 2\text{ ms}$, the polarities of TWs suggest that the fault is external, since the values of the table inside Fig. 7(b) are consistent with the notation of external faults explained in Table 2. It is also interesting to observe the resulting values of wavelet energy ratios in Fig. 7(c). As also explained in Section II-C, the wavelet energy ratios during external faults (or other type of transients) will not be approximately equal for all the connected elements (as opposed for internal faults). This is also verified from Fig. 7(c), where the wer_{i1} reaches higher values of $\frac{1}{M} = 0.2 \pm 5\%$ criterion, while the other wavelet energy ratio values (i.e. wer_{i2} to wer_{i5}) stay below $\frac{1}{M} = 0.2 \pm 5\%$. As depicted in Fig. 7(d), the response of the protection system is restrained as no control or tripping signal is initiated.

It can be only observed that the converter is blocked ($S_{ST}^c = 0$) at some point due to over-current conditions.

4) FAULT SCENARIO IV

This scenario is described by an internal disturbance at DC busbar. Internal disturbances can occur due to several

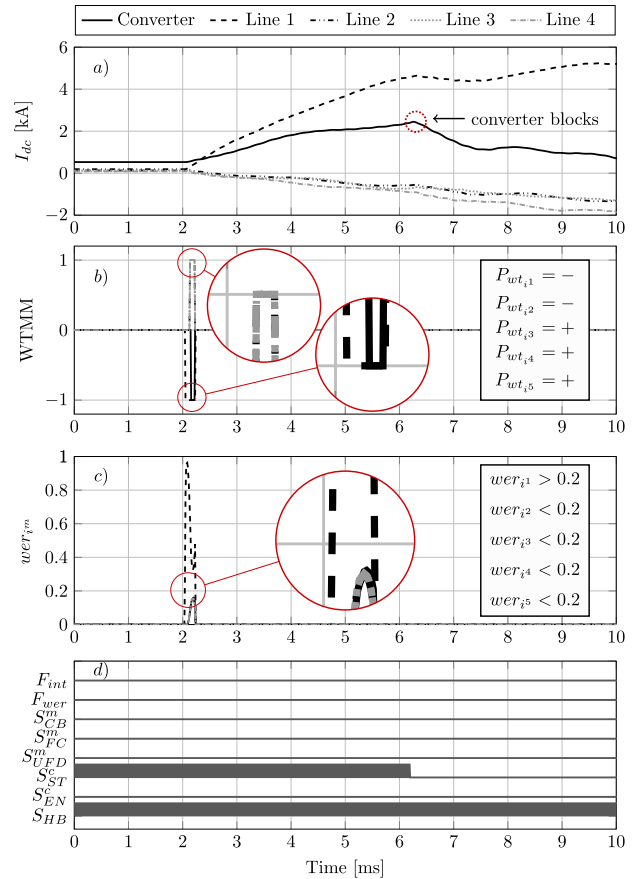


FIGURE 7. Response of protection system during external fault at Line 1: a) DC currents, b) WTMM of DC currents, c) wer of DC currents, d) Control and tripping signals.

reasons such as measurement uncertainties, increased noise levels or actual step changes in current arising from active shunt DC filters [40], [41] or other transients. Disturbances due to noise are expected to be mitigated by low-pass filters and properly-tuning and selecting the wavelet functions.

As such, an active shunt DC filter has been put forward to generate steep changes in DC currents. The response of the protection system for this disturbance is depicted in Fig. 8. The filter is activated at $t = 2\text{ ms}$, creating abrupt changes in DC currents (refer to Fig. 8(a)). The resulting polarities of TWs suggest that the fault is internal (refer also to flag $F_{int} = 1$ in Fig. 8(d)), since the values of the table inside Fig. 8(b) are consistent with the notation of internal faults indicated by Table 2.

At this case, the stability of protection is achieved by the corresponding values of wavelet energy ratios in Fig. 8(c). It can be seen that all values of wer_{im} deviate significantly from $\frac{1}{M} = 0.2 \pm 5\%$ criterion, forcing the protection system to remain stable (refer to flag $F_{wer} = 0$ in Fig. 8(d)). Ultimately, there is no command initiated for breakers or switching as indicated by signals S_{CB}^m and S_{UFD}^m which are held to zero (refer to Fig. 8(d)).

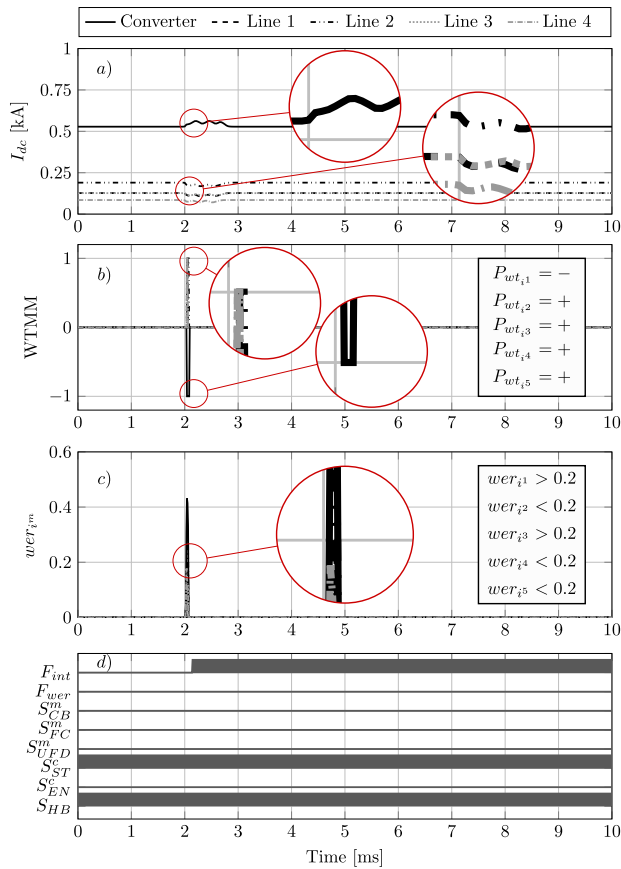


FIGURE 8. Response of protection system internal disturbance: a) DC currents, b) WTMM of DC currents, c) wer of DC currents, d) Control and tripping signals.

D. IMPACT OF FAULT TYPE AND FAULT RESISTANCE

In order to assess the impact of fault type and fault resistance R_f to the performance of the proposed scheme, different internal faults have been applied. These include Pole-to-Pole Faults (PPF), Positive pole-to-Ground Faults (PGF) and Negative pole-to-Ground Faults (NGF) with fault resistances up to 500 Ω . For these cases, it was assumed that there is no healthy busbar available for switching. The trip time of the protection system has been calculated and is depicted in Fig. 9.

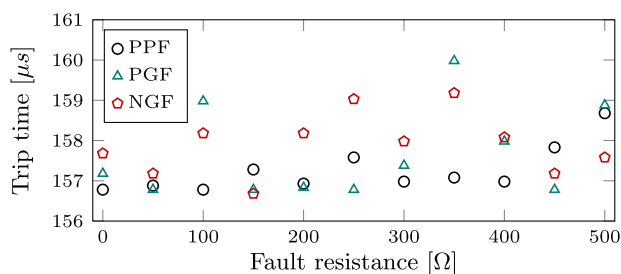


FIGURE 9. Trip time for different fault types and fault resistance values.

By observing Fig. 9 it can be seen that the values of trip time vary insignificantly within a range of 4 μs (i.e. between

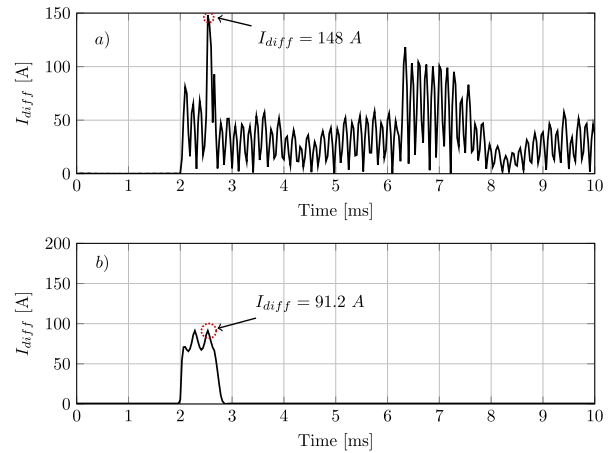


FIGURE 10. Response of Instantaneous Current Differential Protection: a) External Fault, b) Disturbance.

156 μs and 160 μs). This is actually anticipated as the proposed protection scheme does not depend on magnitudes of fault current signatures but rather in ‘binary’ characteristics of TWs (e.g. polarity). This confirms that the proposed scheme is robust against fault current levels which is extremely important in the case of highly-resistive faults. It should be noted the protection scheme has operated correctly at 100 % of the cases.

E. COMPARISON WITH INSTANTANEOUS CURRENT DIFFERENTIAL PROTECTION

In this section, the response of ICDP to the external fault at Line 1 (Scenario III) and to the internal busbar disturbance (Scenario IV) is assessed. For these scenarios the instantaneous differential current is calculated according to equation (9) and the corresponding results are illustrated in Fig. 10.

$$I_{diff}(t) = \sum_{m=1}^M i^m(t) \tag{9}$$

where M the total number of feeders connected to a busbar and i^m the instantaneous current measurements from each feeder.

It can be seen in Fig. 10(a) that during the external fault a non-zero differential current is present. This is expected due to the discharge of any transient/parasitic capacitance included inside substations and converters, in conjunction with post-fault voltage variations. In the case of internal busbar disturbance, it can be seen in Fig. 10(b) that a non-zero value is also present for the entire operation time of the filter.

To avoid spurious operation of the ICDP scheme for those two cases, an increased threshold and/or possibly a time delay would have to be introduced which would compromise the sensitivity and speed of operation. In this context, the proposed scheme can be considered advantageous in terms of stability to external faults internal disturbances.

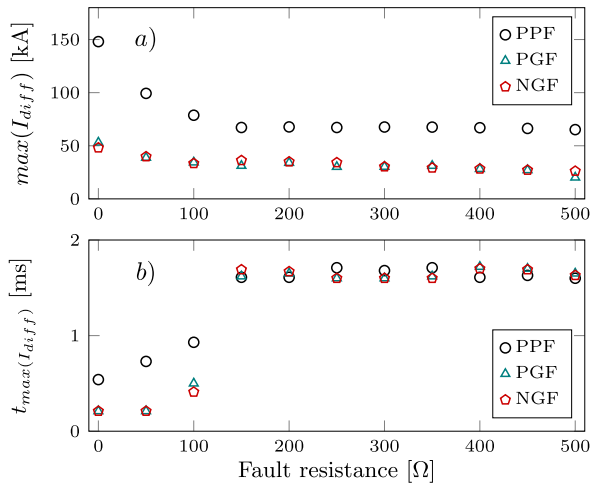


FIGURE 11. ICDP response for external faults: a) Maximum current reached, b) Time to reach maximum current.

To further demonstrate the technical merits of the proposed scheme when compared to ICDP, different external faults to Line 1 have been applied. The studies consider PPF, PGFs and NGFs with fault resistances up to 500 Ω. For these cases, the maximum differential current $\max(I_{diff})$ and the $t_{\max}(I_{diff})$ (time to reach $\max(I_{diff})$) have been calculated. These are depicted in Fig. 11(a) and Fig. 11(b) respectively.

These figures clearly demonstrate that in order to avoid operation during external faults, ICDP threshold should be set above the values presented in Fig. 11(a) and/or to apply additional time delay longer than those included Fig. 11(b). By doing so, the sensitivity and speed of operation would be compromised. It should be noted that during the external faults the proposed scheme remained stable for 100 % of the cases.

V. CONCLUSIONS

A new DC-busbar protection scheme for HVDC substations has been proposed in this paper. The scheme relies on current measurements (sampled at 96 kHz) obtained from lines and converters connected to a DC busbar. Dyadic sub-band tree structures are adopted to extract the polarities of travelling waves to discriminate between internal and external faults. Further analysis based on wavelet energy and wavelet energy ratios is utilized to verify the presence of disturbances and prohibit spurious tripping. The proposed scheme has been found to provide discriminative, sensitive and fast protection covering both pole-to-pole and pole-to-ground faults (solid and highly resistive), while remaining stable during disturbances and external faults. It has been also demonstrated that the proposed protection scheme does not depend on magnitudes of fault current signatures but rather in binary characteristics of travelling waves. In the case of internal faults, the proposed scheme allows continuous operation of HVDC substation by switching to healthy busbars (if available). Moreover by continuously monitoring the status of

locally-connected converters, the proposed scheme is able to re-energize the converters and restore the power to pre-fault conditions, enabling smooth and faster power restoration. The performance of the scheme has been also compared with conventional instantaneous current differential protection, and its technical advantages in terms of stability, sensitivity and speed have been highlighted. The requirements and options with regards to DC switchgear and communication infrastructures have been also discussed in the paper.

REFERENCES

- [1] T. Joseph, C. E. Ugalde-Loo, J. Liang, and P. F. Coventry, "Asset management strategies for power electronic converters in transmission networks: Application to HVDC and FACTS devices," *IEEE Access*, vol. 6, pp. 21084–21102, 2018.
- [2] K. Rouzbehi, S. S. H. Yazdi, and N. S. Moghadam, "Power flow control in multi-terminal HVDC grids using a serial-parallel DC power flow controller," *IEEE Access*, vol. 6, pp. 56934–56944, 2018.
- [3] A. Raza et al., "Power dispatch and voltage control in multiterminal HVDC systems: A flexible approach," *IEEE Access*, vol. 5, pp. 24608–24616, 2017.
- [4] R. H. Renner and D. Van Hertem, "Ancillary services in electric power systems with HVDC grids," *IET Gener., Transmiss. Distrib.*, vol. 9, no. 11, pp. 1179–1185, 2015.
- [5] S. S. Torbaghan, M. Gibescu, B. G. Rawn, H. Müller, M. Roggenkamp, and M. van der Meijden, "Investigating the impact of unanticipated market and construction delays on the development of a meshed HVDC grid using dynamic transmission planning," *IET Gener., Transmiss. Distrib.*, vol. 9, no. 15, pp. 2224–2233, 2015.
- [6] A. Raza et al., "A protection scheme for multi-terminal VSC-HVDC transmission systems," *IEEE Access*, vol. 6, pp. 3159–3166, 2018.
- [7] A. Hossam-Eldin, A. Lotfy, M. Elgamel, and M. Ebeed, "Artificial intelligence-based short-circuit fault identifier for MT-HVDC systems," *IET Gener., Transmiss. Distrib.*, vol. 12, no. 10, pp. 2436–2443, 2018.
- [8] J. Yang, J. E. Fletcher, and J. O'Reilly, "Short-circuit and ground fault analyses and location in VSC-based DC network cables," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3827–3837, Oct. 2012.
- [9] P. T. Lewis, B. M. Grainger, H. A. A. Hassan, A. Barchowsky, and G. F. Reed, "Fault section identification protection algorithm for modular multilevel converter-based high voltage DC with a hybrid transmission corridor," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5652–5662, Sep. 2016.
- [10] J. Liu, N. Tai, and C. Fan, "Transient-voltage-based protection scheme for DC line faults in the multiterminal VSC-HVDC system," *IEEE Trans. Power Del.*, vol. 32, no. 3, pp. 1483–1494, Jun. 2017.
- [11] C. Li, A. M. Gole, and C. Zhao, "A fast DC fault detection method using DC reactor voltages in HVDC grids," *IEEE Trans. Power Del.*, vol. 33, no. 5, pp. 2254–2264, Oct. 2018.
- [12] R. Dantas, J. Liang, C. E. Ugalde-Loo, A. Adamczyk, C. Barker, and R. Whitehouse, "Progressive fault isolation and grid restoration strategy for MTDC networks," *IEEE Trans. Power Del.*, vol. 33, no. 2, pp. 909–918, Apr. 2018.
- [13] S. P. Azad and D. Van Hertem, "A fast local bus current-based primary relaying algorithm for HVDC grids," *IEEE Trans. Power Del.*, vol. 32, no. 1, pp. 193–202, Feb. 2017.
- [14] D. Tzelepis et al., "Single-ended differential protection in MTDC networks using optical sensors," *IEEE Trans. Power Del.*, vol. 32, no. 3, pp. 1605–1615, Jun. 2017.
- [15] M. Hajian, L. Zhang, and D. Jovcic, "DC transmission grid with low-speed protection using mechanical DC circuit breakers," *IEEE Trans. Power Del.*, vol. 30, no. 3, pp. 1383–1391, Jun. 2015.
- [16] H. Dong, Z. Xu, P. Song, G. Tang, Q. Xu, and L. Sun, "Optimized power redistribution of offshore wind farms integrated VSC-MTDC transmissions after onshore converter outage," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8948–8958, Nov. 2017.
- [17] D. Tzelepis et al., "Centralised busbar differential and wavelet-based line protection system for multi-terminal direct current grids, with practical iec-61869-compliant measurements," *IET Gener., Transmiss. Distrib.*, vol. 12, no. 14, pp. 3578–3586, 2018.

- [18] G. Choi and R. A. Haddad, "Theory and design of dyadic subband tree structures with embedded PDF-optimized quantizers," *IEEE Trans. Signal Process.*, vol. 46, no. 5, pp. 1260–1274, May 1998.
- [19] R. P. Medeiros and F. B. Costa, "A wavelet-based transformer differential protection with differential current transformer saturation and cross-country fault detection," *IEEE Trans. Power Del.*, vol. 33, no. 2, pp. 789–799, Apr. 2018.
- [20] K. M. Silva, A. M. P. Escudero, F. V. Lopes, and F. B. Costa, "A wavelet-based busbar differential protection," *IEEE Trans. Power Del.*, vol. 33, no. 3, pp. 1194–1203, Jun. 2018.
- [21] L. Tang, X. Dong, S. Luo, S. Shi, and B. Wang, "A new differential protection of transmission line based on equivalent travelling wave," *IEEE Trans. Power Del.*, vol. 32, no. 3, pp. 1359–1369, Jun. 2017.
- [22] X. Dong, W. Kong, and T. Cui, "Fault classification and faulted-phase selection based on the initial current traveling wave," *IEEE Trans. Power Del.*, vol. 24, no. 2, pp. 552–559, Apr. 2009.
- [23] S. Mallat and W. L. Hwang, "Singularity detection and processing with wavelets," *IEEE Trans. Inf. Theory*, vol. 38, no. 2, pp. 617–643, Mar. 1992.
- [24] D. V. Hertem, O. Gomis-Bellmunt, and J. Liang, *HVDC Grids: For Off-shore and Supergrid of The Future*. Hoboken, NJ, USA: Wiley, 2016, ch. 8.5.
- [25] K. Sano and M. Takasaki, "A surgeless solid-state DC circuit breaker for voltage-source-converter-based HVDC systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2690–2699, Jul. 2014.
- [26] Z. Chen *et al.*, "Analysis and experiments for IGBT, IEGT, and IGCT in hybrid DC circuit breaker," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 2883–2892, Apr. 2018.
- [27] C. Li, J. Liang, and S. Wang, "Interlink hybrid DC circuit breaker," *IEEE Trans. Ind. Electron.*, vol. 65, no. 11, pp. 8677–8686, Nov. 2018.
- [28] B. Xiang *et al.*, "DC interrupting with self-excited oscillation based on the superconducting current-limiting technology," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 529–536, Feb. 2018.
- [29] L. Angquist, S. Norrga, and T. Mod er, "A new DC breaker with reduced need for semiconductors," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, Sep. 2016, pp. 1–9.
- [30] B. Zhao, Q. Song, J. Li, and W. Liu, "A modular multilevel DC-link front-to-front DC solid-state transformer based on high-frequency dual active phase shift for HVDC grid integration," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8919–8927, Nov. 2017.
- [31] H. You and X. Cai, "Stepped 2-level operation of three-port modular DC/DC converter applied in HVDC application," *IEEE Access*, vol. 6, pp. 53822–53832, 2018.
- [32] O. Cwikowski *et al.*, "Integrated HVDC circuit breakers with current flow control capability," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 371–380, Feb. 2018.
- [33] A. Mokherdorran, D. van Hertem, N. Silva, H. Leite, and A. Carvalho, "Multiport hybrid HVDC circuit breaker," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 309–320, Jan. 2018.
- [34] J. Sau-Bassols, E. Prieto-Araujo, O. Gomis-Bellmunt, and F. Hassan, "Series interline DC/DC current flow controller for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 33, no. 2, pp. 881–891, Apr. 2018.
- [35] D. Jovcic and L. Zhang, "LCL DC/DC converter for DC grids," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2071–2079, Oct. 2013.
- [36] N. A. Belda, C. A. Plet, and R. P. P. Smeets, "Analysis of faults in multiterminal HVDC grid for definition of test requirements of HVDC circuit breakers," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 403–411, Feb. 2018.
- [37] M. Hajian, D. Jovcic, and B. Wu, "Evaluation of semiconductor based methods for fault isolation on high voltage DC grids," *IEEE Trans. Smart Grid*, vol. 4, no. 2, pp. 1171–1179, Jun. 2013.
- [38] *Instrument Transformers—Part 9: Digital Interface for Instrument Transformers*, Standard IEC 61869-9: ED 1.0, BSI, 2013.
- [39] *Industrial Communication Networks—High Availability Automation Networks—Part 3: Parallel Redundancy Protocol (PRP) and High-Availability Seamless Redundancy (HSR)*, Standard IEC 62439-3, BSI, 2018.
- [40] S. Aali, "Shunt active DC filter based on intelligence controller for HVDC link," *High Voltage*, vol. 2, no. 4, pp. 274–279, 2017.
- [41] P. Hao, W. Zanji, and C. Jianye, "Study on the control of shunt active DC filter for HVDC systems," *IEEE Trans. Power Del.*, vol. 23, no. 1, pp. 396–401, Jan. 2008.



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