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Performance Investigation of Three-Phase Three-Switch Direct PWM AC/AC Voltage Converters

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ABSTRACT Reducing the number of active switches is substantial for obtaining a simple, reliable, high-efficiency, and cost-effective AC/AC voltage converter. In this paper, two topologies of three-phase direct PWM AC/AC voltage converter are proposed. The first is for the buck converter and the other is for the boost one. Each converter has no DC energy storage elements and employs only three IGBTs. The proposed converters do not use lossy snubber circuits and have not commutation problems. A simple, reliable, and cost-effective control strategy, which employs only one voltage sensor, is also proposed. Using a closed-loop voltage control technique, two complementary PWM gate signals are generated to drive the three active switches of each converter. Adjusting the duty ratio of PWM gate signals regulates the output voltage of the AC/AC converters. Operating principle and mathematical analysis of the converters are presented. Voltage stresses across active and passive semiconductor switches of the proposed converters are derived. Small signal analysis based on complex DQ transformed equivalent circuits of the converter is introduced. Voltage controller design using frequency response analysis is provided. The converters are simulated using MATLAB/SIMULINK and laboratory prototypes are implemented in real-time using DSP-DS1104 control board. The converters are tested under different operating conditions and their performances are investigated and compared. The symmetry of the output voltage/current is examined by the theory of symmetrical components. The simulation and experimental results are in a close agreement. This confirms the validity of the theoretical analysis, the effectiveness of the control strategy, and the feasibility of the proposed converters.

INDEX TERMS AC-AC voltage converters, control design, small signal analysis, stability analysis, symmetrical components, voltage stress.

I. INTRODUCTION

Recently, AC/AC voltage converters have been gained more and more attention in industrial applications. They are utilized in different applications such as induction heating, voltage restorers, power transmission control, reactive power compensation, lighting intensity control, voltage sag/swell compensators, soft starters for AC motors, and speed controllers for blowers and fans [1]–[5]. Direct AC/AC voltage controllers convert fixed AC input voltage to controlled AC output voltage at constant frequency without the need for DC-link stage. Therefore, they offer numerous advantages such as no need for the bulk DC storage element, small size, low weight and minimum cost [6]–[9].

Several direct AC/AC voltage regulation approaches have been explored in the literature. Transformers with tap changing have been utilized as AC/AC voltage regulators in power distribution networks. However, the dynamic response speed of this technique is slow and hence it has limited applications. To increase the response speed, electronic tap changer transformers are proposed [10], [11]. However, numerous power switches and large size of the electronic tap changers transformers increase their cost and limit their use. In addition, fine control of the output voltage cannot be achieved.

Line-commutated silicon-controlled rectifier (SCR) AC/AC voltage regulators are presented [12]. In these regulators, the voltage regulation process is traditionally carried

out using phase angle control technique. Therefore, it is necessary to synchronize the gate signals of thyristors with the input voltage signal of the converter. Although these kinds of voltage regulators are robust, commutation problems of SCRs, limited control range, high voltage/current harmonics and low input power factor (PF) of these regulators are the main drawbacks. In addition, zero crossing detectors (ZCDs) that require numerous voltage sensors increase the complexity and the cost of these converters. Further, SCR AC/AC voltage regulators operate in buck mode only and they do not have the voltage boosting ability.

Development of high-switching self-commutating semiconductor devices, such as insulated gate bipolar transistor (IGBT), and introduction of pulse width modulation (PWM) control method overcome these drawbacks and improve the AC/AC voltage converter performance in terms of harmonics reduction, input PF improvement, needless of ZCDs and wide control range. In addition, PWM AC/AC voltage converters can operate in buck and/or boost mode of operations, similarly to DC/DC voltage converters. However, Direct PWM AC/AC voltage converters require additional components such as inductors and capacitors in order to filter the harmonics generated due to switching action of the PWM converters. Size of the filter components depends on the switching frequency. As switching frequency increases, the filter size and the total harmonics distortion (THD) are decreased and the input PF is improved. Unfortunately increasing the switching frequency increases the switching losses, and hence decreases the converter efficiency. Therefore, innovation of simple topologies for direct PWM converters with minimal number of active switches has a great importance, especially with their applications increase in the industry. Four-switch [13], [14], three-switch [15] and two-switch [16], [17] topologies for single-phase PWM AC/AC converters are presented in the literature. While, a three-phase converter that employs six active switches is presented in [18] and [19]. A four-switch topology for three-phase PWM AC chopper is proposed in [20]. Several structures of three-phase PWM AC/AC buck converter are presented in [21].

In this article, two circuits of three-phase direct PWM AC/AC voltage converter for buck and boost operations are proposed. The aim of the proposed converters is to reduce the number of active switches. So, each converter employs only three active switches; three IGBTs, and has no DC-link stage. Switch count reduction minimizes the system cost, reduces the system volume and simplifies the system control. Furthermore, the proposed converters have a safe commutation without using the lossy RC snubber circuits. Moreover, only one voltage sensor is used for the closed loop voltage control. This structure simplifies the control strategy, reduces complexity of the control algorithm and increases the reliability. Mathematical analysis and schematic diagrams for the individual operation stages of the proposed converters are introduced. Then, state space models and transfer functions of the proposed converters are derived. The proposed PI voltage controller gains based on stability analysis using frequency

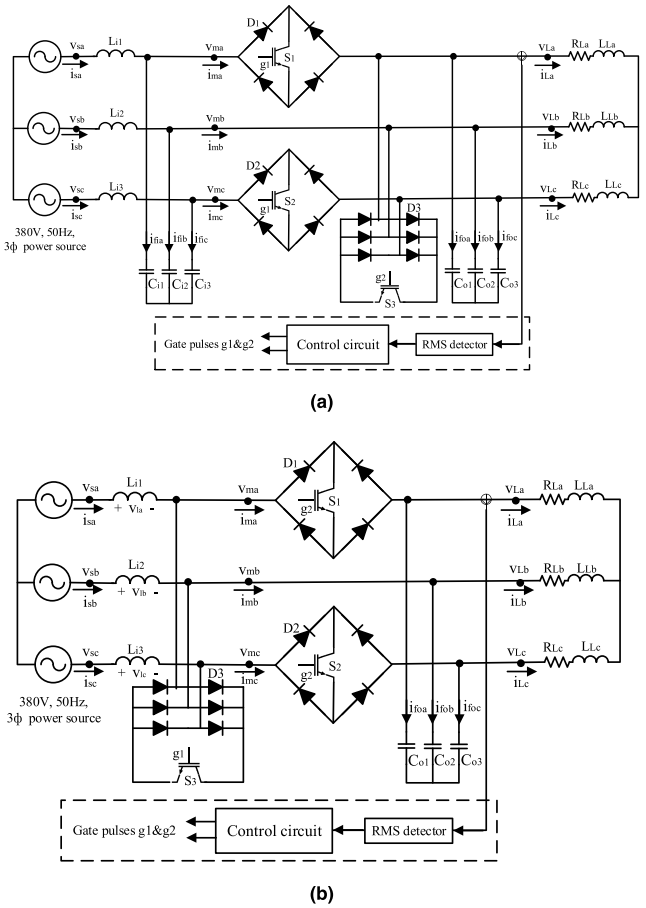

FIGURE 1. Power circuit of the proposed three-phase three-switch AC/AC voltage converter. (a) Buck-type. (b) Boost-type.

response are designed. The proposed AC/AC voltage converters are simulated using MATLAB/SIMULINK software program. Laboratory prototypes of the experimental systems are implemented in real-time using DSP-DS1104 control board. Extensive dynamic and steady state simulation and experimental results under different operating conditions are investigated and compared to validate the effectiveness of the proposed converters.

II. TOPOLOGY DESCRIPTION

Fig. 1(a) and Fig. 1(b) display the power circuits of the proposed three-switch buck and boost voltage converters, respectively. Each converter has no DC energy storage elements and employs three active switches (S_1, S_2, and S_3). One of the proposed configurations advantages is that any base/gate self-commutating switch such as BJT, FET, MOSFET or IGBT can be utilized. This feature facilitates and widens the use of the proposed converters in practical applications. In the proposed arrangements, the insulated gate bipolar transistor (IGBT) is selected as an active switch because of its high power, high switching frequency and self-commutating features.

The proposed buck AC/AC converter is powered from 380 V, 50 Hz, three-phase source. Inductors (L_{i1}, L_{i2}, and L_{i3})

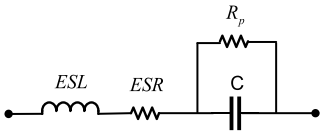

FIGURE 2. Equivalent circuit of a practical capacitor.

and capacitors (C_{i1}, C_{i2}, and C_{i3}) construct the input LC filter, which is utilized to absorb the source current harmonics. Output capacitors (C_{o1}, C_{o2}, and C_{o3}) construct the output filter, which is used to absorb output voltage harmonics. In addition, they provide a snubber operation that suppresses the high voltage spikes resulted from the converter switching. Therefore, in the proposed buck converter topology, the traditional lossy RC snubber circuits across the semiconductor switches are not mandatory. The bidirectional switches S_1 and S_2 are used to control the power delivered to the three-phase load through periodically connection/disconnection only two terminals of the load to/from the source. While, the active switch S_3 is connected across a three-phase diode bridge rectifier for freewheeling purpose during the off intervals of S_1 and S_2 switches. In the proposed buck topology, the output filter is only capacitor in order to reduce the system components as much as possible. However, self-inductances of the wires that connect between capacitors of the input and output filters through switches as well as the parasitic components of the practical capacitors, i.e. equivalent series resistance (ESR) and equivalent series inductance (ESL) of the capacitor, limit the inrush current between input and output capacitors in the switching transition period. Fig. 2 shows the equivalent circuit of a practical capacitor, which consists of four components: capacitance (C), insulation resistance (R_P), ESR and ESL. The parasitic components of the capacitor affect its transient response as they reduce the overshoot and undershoot and improve the damping [22], [23]. Therefore, they prevent the capacitors from the instantaneous charge and discharge and hence limit the high-voltage and high-current spikes. Moreover, as the discharge path of the output filter capacitors is through the load circuit, the stored energy of the load inductance helps to substantially prevent the instantaneous discharge of the capacitors and in turn the high-current spikes can be avoided. Typical values of ESR are from 50 to 200 mΩ, whereas ESL values are from 1 to 5 nH. Self-inductance of the wire is 1.32 μH/phase and calculated as in [24]:

$$L_{wire} = 0.002l\left\{\log_e\left(\frac{2l}{\rho}\right) - 1 + \frac{\mu}{4}\right\} \quad (1)$$

where L_{wire} is the self-inductance of the wire (μH), ρ is the radius of the wire (cm), l is the length of the wire (cm), and μ is the permeability of the wire material. Since ESR and ESL of the capacitors and self-inductance of the wires are small, so they can be neglected for simplicity of the analysis.

In the proposed boost converter, inductors (L_{i1}, L_{i2}, and L_{i3}) are used for voltage step-up purpose. The power switch S_3 is periodically used to connect and disconnect the boosting inductors (L_{i1}, L_{i2}, and L_{i3}) to the power source. Adjusting the duty ratio of S_3 controls the power delivered to the boosting inductors. While the bidirectional power switches S_1 and S_2 are used to control the power transferred to the load. Output capacitors (C_{o1}, C_{o2}, and C_{o3}) represent the output filter of the boost converter. As compared to other structures of the bidirectional switch, the proposed structure of the bidirectional switch uses only one IGBT, as shown in Fig. 1. Therefore, it offers lower cost, simpler control algorithm and simpler driver circuit. But, the drawback of one-active-switch structure is that the current stress of the active switch will increase.

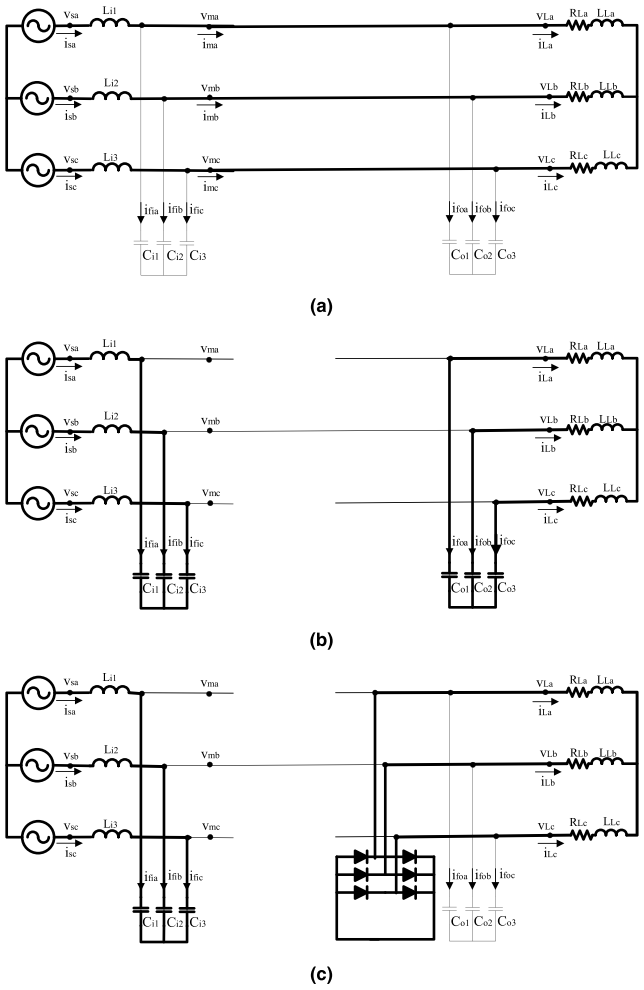

FIGURE 3. Schematic diagrams for the operation stages of the proposed buck converter. (a) Active. (b) Dead-time. (c) Freewheeling.

III. OPERATION PRINCIPLE

Operation of the proposed buck AC/AC converter is divided into three modes: 1) active mode, 2) freewheeling mode and 3) dead-time mode. Schematic diagrams for the operation stages of the proposed buck converter are shown in Fig. 3. The current path is expressed by the bolded line in each circuit. During the active mode; i.e. S_1&S_2 are on, S_3 is off, and the power source is connected to the load as shown in

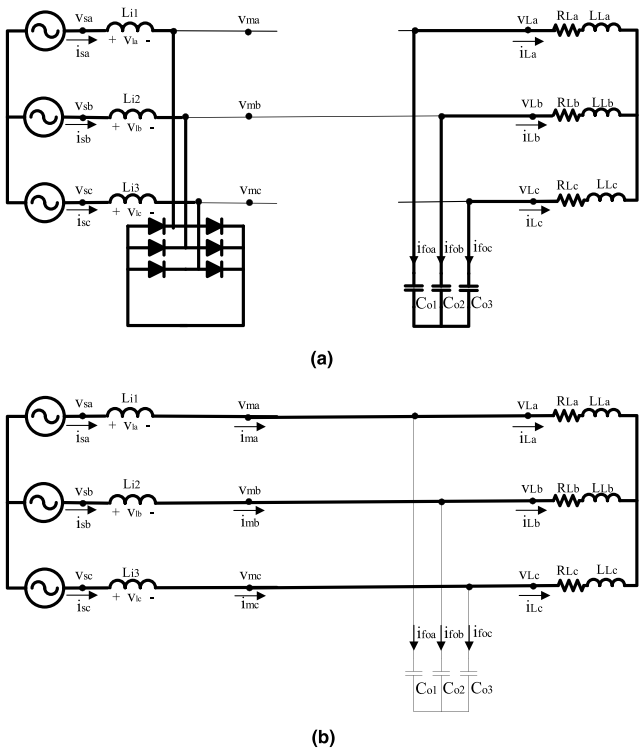

FIGURE 4. Schematic diagrams for the operation stages of the proposed boost converter. (a) Active. (b) Freewheeling.

Fig. 3(a). The energy is transferred from the source and stored in the load. In the freewheeling mode; i.e. S_1&S_2 are off, S_3 is on, and the stored energy in the load is discharged in the freewheeling path as shown in Fig. 3(c). Since the regulating power switches; i.e. S_1&S_2, and the freewheeling switch S_3 work in an alternative way, a dead-time mode is required for safe commutation. In dead-time period, the three switches S_1, S_2, and S_3 are off as shown in Fig. 3(b). During the turn-off transition interval of switches S_1 and S_2, the capacitors of the output filter provide snubber operation by forming a bypass across the load and drain the inductive load current. Therefore, the stored energy of the inductive load can be discharged more safely and quietly. Consequently, the turn-off high voltage spikes due to the converter switching can be avoided. In addition, since there is no need for the lossy RC snubber circuits across the active switches, the converter performance is improved. Like the load current, the input side current is also continuously conducted through the LC input filter during the dead-time period. Using PWM control technique, the output voltage of the buck converter is adjusted.

Operation of the proposed boost converter is divided into two modes: 1) active mode and 2) freewheeling mode. Operation stages of the proposed boost converter are schematically displayed in Fig. 4. During the active mode; S_1&S_2 are off, S_3 is on, and the current of boosting inductors (L_{i1}, L_{i2}, and L_{i3}) rises and the energy is stored as shown in Fig. 4(a). During the freewheeling mode; S_1&S_2 are on, S_3 is off, and the stored energy in the boosting inductors is transferred to the load as shown in Fig. 4(b). Therefore, the boosting inductors are

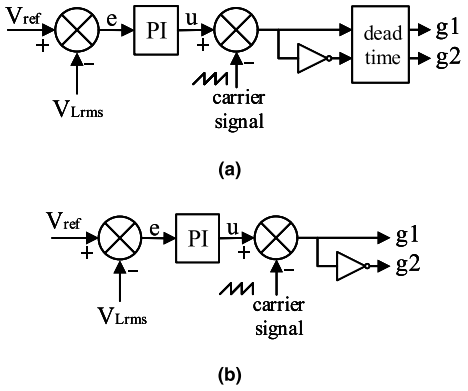

FIGURE 5. Schematic diagrams of the proposed control circuit. (a) Buck converter. (b) Boost converter.

utilized to store the energy and thereafter transfer it to the load circuit. The boost converter switches are controlled using PWM gate signals. Adjusting the duty ratio controls the boost converter output voltage and hence the energy transferred to the load. In the boost converter, there is no need to a dead-time period. Hence, it is expected to have lower harmonics compared to the buck converter and hence has a higher input PF and higher efficiency.

In the proposed converters, the commutation strategy does not require synchronization circuits with the input voltage. Thus, this feature simplifies the hardware design, avoids the ZCDs errors and reduces the size and cost.

IV. VOLTAGE CONTROL STRATEGY

Using PWM technique, the voltage of the proposed converters is regulated. Fig. 5(a) and Fig. 5(b) display the schematic diagrams of the control circuits of the proposed buck and boost voltage converters, respectively. A simple control strategy that uses two complementary PWM signals (g_1 and g_2) is adopted for both buck and boost converters. The load voltage is measured, and the sampled voltages of the measured signal are squared and averaged over a window with one-cycle duration to estimate its RMS value.

The discrete RMS calculation for the sliding window of the load voltage (V_{Lrms}) is given as follows [25]:

$$V_{Lrms}(k) = \sqrt{\frac{\sum_{i=k-N+1}^{k} v_i^2}{N}} \tag{2}$$

where N is the number of samples per cycle, v_i is the sampled voltage waveform, and $k = 1, 2, 3, \ldots$etc. The RMS value of the measured signal is compared with the reference signal (V_{ref}). The error signal; $e(t)$, is passed through a PI controller. Output of the PI controller; $u(t)$, can be given as:

$$u(t) = K_P e(t) + K_I \int e(t)dt \tag{3}$$

where K_P and K_I are the proportional and the integral gains of the controller, respectively. The controller output is compared with a sawtooth signal to generate the gate pulse g_1. The gate pulse g_2 is complementary with g_1. The frequency of

the sawtooth signal is maintained constant at 4.5 kHz. This low value of the switching frequency is chosen in order to investigate the proposed converters applicability in medium and high-power applications. The dead-time block is added in the control circuit of the buck converter in order to provide a very small time period, which is taken as 2 μs, between active and freewheeling modes for sake of the safe commutation.

V. MATHEMATICAL ANALYSIS

A. BUCK-TYPE CONVERTER

Assume the phase voltages v_{sa}, v_{sb} and v_{sc} of the three-phase source are sinusoidal and symmetrical and are given as:

$$\begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} = V_{sp} \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - 120^\circ) \\ \sin(\omega t + 120^\circ) \end{bmatrix} \tag{4}$$

where V_{sp} is the peak value of the input phase voltage, and ω is the angular frequency of the source ($\omega = 2\pi F$). The intermediate voltages v_{ma}, v_{mb} and v_{mc}, which are the converter input voltages, can be given as:

$$\begin{aligned} \begin{bmatrix} v_{ma} \\ v_{mb} \\ v_{mc} \end{bmatrix} &= \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} - \begin{bmatrix} L_{i1} & 0 & 0 \\ 0 & L_{i2} & 0 \\ 0 & 0 & L_{i3} \end{bmatrix} \begin{bmatrix} \frac{di_{sa}}{dt} \\ \frac{di_{sb}}{dt} \\ \frac{di_{sc}}{dt} \end{bmatrix} \\ &= V_{mp} \begin{bmatrix} \sin(\omega t + \varphi_{Li}) \\ \sin(\omega t + \varphi_{Li} - 120^\circ) \\ \sin(\omega t + \varphi_{Li} + 120^\circ) \end{bmatrix} \end{aligned} \tag{5}$$

where L_{i1}, L_{i2} and L_{i3} are the inductances of the input filter, i_{sa}, i_{sb} and i_{sc} are the three phase supply currents, V_{mp} is the peak value of the intermediate phase voltage, and φ_{Li} is the phase angle of the voltage drop across the filter input inductor. The currents of the input filter capacitors i_{fia}, i_{fib} and i_{fic} can be given as:

$$\begin{bmatrix} i_{fia} \\ i_{fib} \\ i_{fic} \end{bmatrix} = \begin{bmatrix} C_{i1} & 0 & 0 \\ 0 & C_{i2} & 0 \\ 0 & 0 & C_{i3} \end{bmatrix} \begin{bmatrix} \frac{dv_{ma}}{dt} \\ \frac{dv_{mb}}{dt} \\ \frac{dv_{mc}}{dt} \end{bmatrix} \tag{6}$$

The currents i_{ma}, i_{mb} and i_{mc} can be given as:

$$\begin{bmatrix} i_{ma} \\ i_{mb} \\ i_{mc} \end{bmatrix} = \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} - \begin{bmatrix} i_{fia} \\ i_{fib} \\ i_{fic} \end{bmatrix} \tag{7}$$

The phase voltages of the load circuit v_{La}, v_{Lb} and v_{Lc} which are the output voltages of the converter can be expressed as:

$$\begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix}$$

$$\begin{aligned} &= DV_{mp} \begin{bmatrix} \sin(\omega t + \varphi_{Li}) \\ \sin(\omega t + \varphi_{Li} - 120^\circ) \\ \sin(\omega t + \varphi_{Li} + 120^\circ) \end{bmatrix} \\ &+ \begin{bmatrix} \sum_{k=1}^{\infty} \frac{V_{mp} \sin(kD\pi)}{K\pi} \sin\{(\omega \pm k\omega_{sw})\, t + \varphi_{Li}\} \\ \sum_{k=1}^{\infty} \frac{V_{mp} \sin(kD\pi)}{K\pi} \sin\{(\omega \pm k\omega_{sw})\, t + \varphi_{Li} - 120^\circ\} \\ \sum_{k=1}^{\infty} \frac{V_{mp} \sin(kD\pi)}{K\pi} \sin\{(\omega \pm k\omega_{sw})\, t + \varphi_{Li} + 120^\circ\} \end{bmatrix} \end{aligned} \tag{8}$$

where ω_{sw} is the angular switching frequency of the converter and D is the duty ratio of the converter; $0 \leq D \leq 1$, and it can be given as:

$$D = \frac{T_{on}}{T_{sw}} = \frac{T_{on}}{T_{on} + T_{off}} \tag{9}$$

where T_{on}, T_{off} and T_{sw} are the converter on time, off time and switching time, respectively. Switching frequency (F_{sw}) of the converter can be given as:

$$F_{sw} = \frac{1}{T_{sw}} \tag{10}$$

The currents of the output filter capacitors i_{foa}, i_{fob} and i_{foc} can be given as:

$$\begin{bmatrix} i_{foa} \\ i_{fob} \\ i_{foc} \end{bmatrix} = \begin{bmatrix} C_{o1} & 0 & 0 \\ 0 & C_{o2} & 0 \\ 0 & 0 & C_{o3} \end{bmatrix} \begin{bmatrix} \frac{dv_{La}}{dt} \\ \frac{dv_{Lb}}{dt} \\ \frac{dv_{Lc}}{dt} \end{bmatrix} \tag{11}$$

The load equation can be given as:

$$\begin{aligned} \begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix} &= \begin{bmatrix} R_{La} & 0 & 0 \\ 0 & R_{Lb} & 0 \\ 0 & 0 & R_{Lc} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \\ &+ \begin{bmatrix} L_{La} & 0 & 0 \\ 0 & L_{Lb} & 0 \\ 0 & 0 & L_{Lc} \end{bmatrix} \begin{bmatrix} \frac{di_{La}}{dt} \\ \frac{di_{Lb}}{dt} \\ \frac{di_{Lc}}{dt} \end{bmatrix} \end{aligned} \tag{12}$$

where (R_{La}, R_{Lb} and R_{Lc}), (L_{La}, L_{Lb} and L_{Lc}) and (i_{La}, i_{Lb} and i_{Lc}) are resistances, inductances and currents of the three-phase load circuit.

The right-hand side of (8) has two terms. The first term is the fundamental component of the buck-type converter output voltage, which is proportional to the duty ratio. While, the second term represents the harmonic components that are resulted from the converter switching. The harmonic components can be absorbed using the output filter. The size of input and output filter components; inductors and capacitors, is inversely proportional to the switching frequency of the converter (F_{sw}). Whereas the converter losses are directly proportional to F_{sw}. Therefore, a suitable value of F_{sw} should be specified. Several computer simulations under different operating conditions were carried out in order to choose F_{sw}.

The output filter is utilized to minimize the harmonics of the converter output voltage; and hence the second term of (8) can be ignored. Therefore, with ignoring the voltage drop across the input filter inductor, the voltage across the load circuit can be approximately given as:

$$\begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix} \cong D \begin{bmatrix} v_{ma} \\ v_{mb} \\ v_{mc} \end{bmatrix} \cong D \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{13}$$

Hence, the load voltage can be adjusted by varying the duty ratio (D) of the converter. Since the duty ratio is always less than 1, the load voltages are lower than the input voltages in the buck-type converter.

B. BOOST-TYPE CONVERTER

As the duty cycle of the boost converter is D, the complementary of the duty cycle (1-D) can be given as:

$$(1 - D) = \frac{T_{off}}{T_{sw}} \tag{14}$$

During one switching period of the boost converter, the average values of the voltages v_{la}, v_{lb} and v_{lc} across the boost inductors (L_{i1}, L_{i2} and L_{i3}) can be given as:

$$\begin{bmatrix} v_{la} \\ v_{lb} \\ v_{lc} \end{bmatrix} = D \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} + (1 - D) \left\{ \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} - \begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix} \right\} \tag{15}$$

Since the switching cycle time (T_{sw}) is very small compared with the cycle time of the power source, therefore the inductor voltages are approximately equal zero.

$$\begin{bmatrix} v_{la} \\ v_{lb} \\ v_{lc} \end{bmatrix} \cong 0 \tag{16}$$

From (15) and (16), the load voltages can be given as:

$$\begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix} \cong \frac{1}{(1 - D)} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{17}$$

Therefore, the load voltage can be adjusted by varying the duty ratio (D) of the converter. Since the duty ratio is always less than 1, the load voltages are higher than the input voltages in the boost-type converter. Fig. 6 shows the voltage gain of the proposed buck and boost converters versus duty ratio.

C. VOLTAGE STRESSES OF SEMICONDUCTOR SWITCHES

The voltage stresses V_{S1} and V_{S2} across the buck converter switches S_1 and S_2, respectively, are equal. Each voltage stress equals the difference between the source and load line-line voltages, i.e. $V_{s,LL}$ and $V_{L,LL}$ respectively. It can be given as:

$$V_{S1} = V_{S2} = V_{s,LL} - V_{L,LL} \tag{18}$$

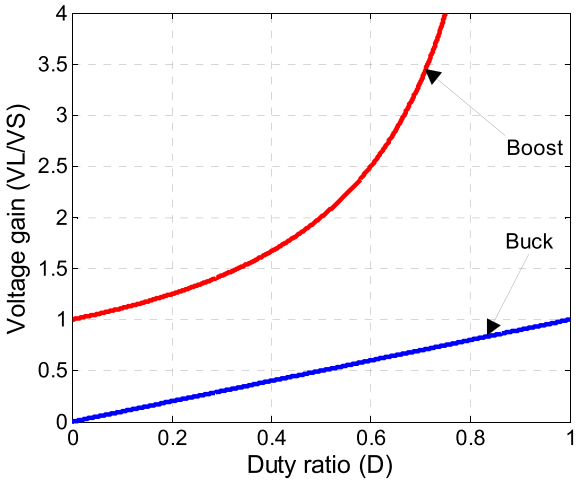

FIGURE 6. Voltage gain (V_L/V_S) of the proposed converters versus duty ratio (D).

The voltage stresses across S_1 and S_2 are normalized to the line-line load voltage and can be given as:

$$\left.\frac{V_{S1}}{V_{L,LL}}\right|_{rms} = \left.\frac{V_{S2}}{V_{L,LL}}\right|_{rms} = \sqrt{\frac{1 - D}{D}} \tag{19}$$

The normalized voltage stresses across passive switches D_1 and D_2, one diode of single-phase bridge rectifier connected to S_1 and S_2 respectively, can be given as:

$$\left.\frac{V_{D1}}{V_{L,LL}}\right|_{rms} = \left.\frac{V_{D2}}{V_{L,LL}}\right|_{rms} = \sqrt{\frac{1 - D}{2D}} \tag{20}$$

The normalized voltage stress V_{S3} across the active switch S_3 that connected across DC side of the three-phase bridge rectifier can be given as:

$$\left.\frac{V_{S3}}{V_{L,LL}}\right|_{rms} = \sqrt{1 + \frac{3\sqrt{3}}{2\pi}} \tag{21}$$

Whereas the normalized voltage stress V_{D3} across passive switch D_3, one diode of the three-phase bridge rectifier connected to S_3, can be given as:

$$\left.\frac{V_{D3}}{V_{L,LL}}\right|_{rms} = \sqrt{\frac{4}{9} + \frac{2}{\sqrt{3}\pi}} \tag{22}$$

The normalized voltage stresses of the active and passive switches of the buck converter are displayed versus the voltage gain ($V_L/V_S = D$) in Fig. 7. As shown from the figure, the normalized voltage stresses V_{S1}, V_{S2}, V_{D1} and V_{D2} increase when the voltage gain decreases, and vice versa. Therefore, the switches S_1, S_2, D_1 and D_2 have maximum voltage stresses when D is minimum. Whereas the normalized V_{S3} and V_{D3} remain constant against D variations.

Similarly, the normalized voltage stresses of the active and passive switches of the boost converter are derived and displayed versus the voltage gain ($V_L/V_S = 1/(1\text{-}D)$) as shown

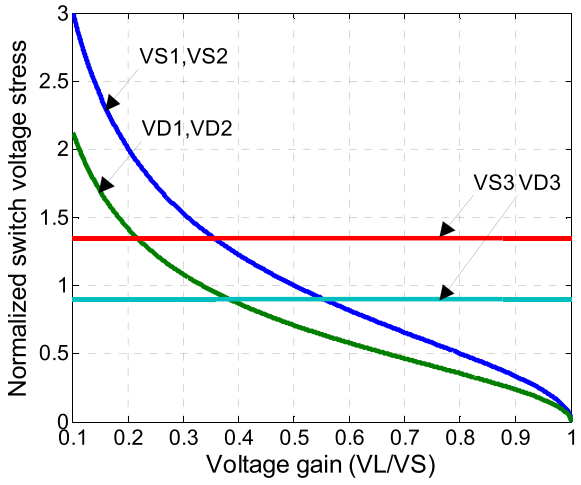

FIGURE 7. Voltage stresses across active and passive switches of the proposed buck converter.

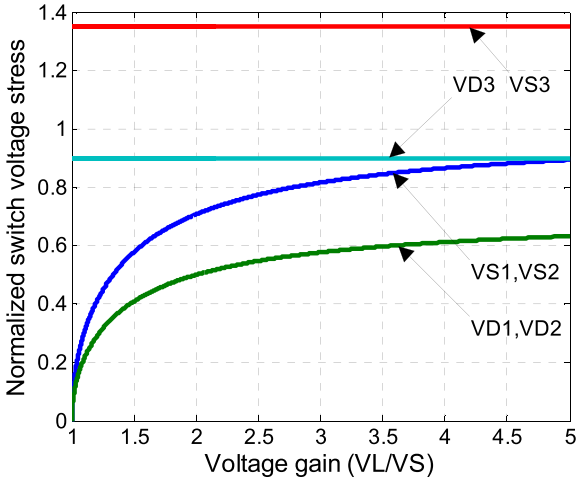

FIGURE 8. Voltage stresses across active and passive switches of the proposed boost converter.

in Fig. 8. These voltage stresses can be given as follows:

$$\begin{cases} \left.\dfrac{V_{S1}}{V_{L,LL}}\right|_{rms} = \left.\dfrac{V_{S2}}{V_{L,LL}}\right|_{rms} = \sqrt{D} \\ \left.\dfrac{V_{D1}}{V_{L,LL}}\right|_{rms} = \left.\dfrac{V_{D2}}{V_{L,LL}}\right|_{rms} = \sqrt{\dfrac{D}{2}} \\ \left.\dfrac{V_{S3}}{V_{L,LL}}\right|_{rms} = \sqrt{1+\frac{3\sqrt{3}}{2\pi}} \\ \left.\dfrac{V_{D3}}{V_{L,LL}}\right|_{rms} = \sqrt{\dfrac{4}{9}+\dfrac{2}{\sqrt{3}\pi}} \end{cases} \tag{23}$$

As shown in Fig. 8, the normalized voltage stresses V_{S1}, V_{S2}, V_{D1} and V_{D2} increase when the voltage gain increases, and vice versa. Therefore, the switches S_1, S_2, D_1 and D_2 have maximum voltage stresses when the voltage gain is maximum. Whereas the normalized V_{S3} and V_{D3} remain constant against voltage gain variations.

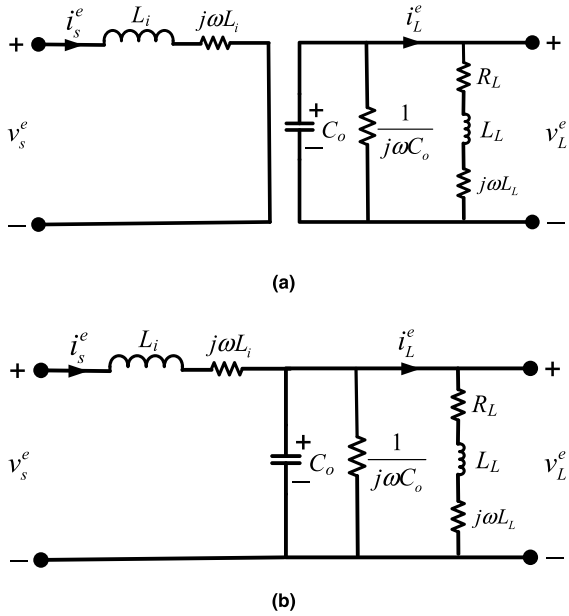

FIGURE 9. Complex DQ transformed equivalent circuits of the proposed three-phase AC/AC boost converter at synchronously rotating reference frame. (a) Active mode ($t \in [0, DT_{SW}]$). (b) Freewheeling mode ($t \in [0, (1-D)T_{SW}]$).

D. DESIGN AND STABILITY ANALYSIS OF THE PROPOSED VOLTAGE CONTROLLER

Space vector representation is an effective analytical tool to analyze three-phase systems. Since the variables in synchronously rotating reference frame are dc values, this reference frame is suitable for driving the linearized model of the converter for the purpose of small signal analysis [26], [27]. The gains of the voltage PI controller for the proposed three-phase AC/AC boost converter are designed, as an example, in this section. By applying the vector DQ transform on the three-phase AC/AC boost converter, the complex DQ transformed equivalent circuits of the boost converter are obtained and illustrated by Fig. 9.

The mathematical equations of the boost converter during the active mode of Fig. 9(a) are derived and given as follows:

$$\begin{cases} L_i \dfrac{di_s^e}{dt} = v_s^e - j\omega L_i i_s^e \\ L_L \dfrac{di_L^e}{dt} = v_L^e - i_L^e R_L - i_L^e j\omega L_L \\ C_o \dfrac{dv_L^e}{dt} = -i_L^e - v_L^e j\omega C_o \end{cases} \tag{24}$$

where

$$\begin{cases} i_s^e = i_{sd}^e + j i_{sq}^e \\ v_s^e = v_{sd}^e + j v_{sq}^e \\ i_L^e = i_{Ld}^e + j i_{Lq}^e \\ v_L^e = v_{Ld}^e + j v_{Lq}^e \end{cases} \tag{25}$$

In (24), the terms $j\omega L_i$, $j\omega L_L$ and $(1/j\omega c_o)$ do not refer to conventional impedances but they represent the relationship of d and q components.

For freewheeling mode, equations of Fig. 9(b) are obtained as follows:

$$\begin{cases} L_i \dfrac{di_s^e}{dt} = v_s^e - v_L^e - j\omega L_i i_s^e \\ L_L \dfrac{di_L^e}{dt} = v_L^e - i_L^e R_L - i_L^e j\omega L_L \\ C_o \dfrac{dv_L^e}{dt} = i_s^e - i_L^e - v_L^e j\omega C_o \end{cases} \tag{26}$$

Hence, the state-space equations for the two modes of the boost converter operation can be given, respectively, as follows:

$$\begin{bmatrix} \frac{di_s^e}{dt} \\ \frac{di_L^e}{dt} \\ \frac{dv_L^e}{dt} \end{bmatrix} = \begin{bmatrix} -j\omega & 0 & 0 \\ 0 & -\left(\frac{R_L}{L_L} + j\omega\right) & \frac{1}{L_L} \\ 0 & \frac{-1}{C_o} & -j\omega \end{bmatrix} \begin{bmatrix} i_s^e \\ i_L^e \\ v_L^e \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \end{bmatrix} v_s^e \tag{27}$$

$$\begin{bmatrix} \frac{di_s^e}{dt} \\ \frac{di_L^e}{dt} \\ \frac{dv_L^e}{dt} \end{bmatrix} = \begin{bmatrix} -j\omega & 0 & \frac{-1}{L_i} \\ 0 & -\left(\frac{R_L}{L_L} + j\omega\right) & \frac{1}{L_L} \\ \frac{1}{C_o} & \frac{-1}{C_o} & -j\omega \end{bmatrix} \begin{bmatrix} i_s^e \\ i_L^e \\ v_L^e \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \end{bmatrix} v_s^e \tag{28}$$

Therefore, from (27) and (28), the average state-space model of the boost converter can be derived as:

$$\begin{bmatrix} \frac{di_s^e}{dt} \\ \frac{di_L^e}{dt} \\ \frac{dv_L^e}{dt} \end{bmatrix} = \begin{bmatrix} -j\omega & 0 & \frac{-(1-d)}{L_i} \\ 0 & -\left(\frac{R_L}{L_L} + j\omega\right) & \frac{1}{L_L} \\ \frac{(1-d)}{C_o} & \frac{-1}{C_o} & -j\omega \end{bmatrix} \times \begin{bmatrix} i_s^e \\ i_L^e \\ v_L^e \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \end{bmatrix} v_s^e \tag{29}$$

The average model can be rewritten as follows:

$$\begin{cases} \dfrac{di_s^e}{dt} = -j\omega i_s^e - \dfrac{(1-d)}{L_i} v_L^e + \dfrac{1}{L_i} v_s^e \\ \dfrac{di_L^e}{dt} = -\left(\dfrac{R_L}{L_L} + j\omega\right) i_L^e + \dfrac{1}{L_L} v_L^e \\ \dfrac{dv_L^e}{dt} = \dfrac{(1-d)}{C_o} i_s^e - \dfrac{1}{C_o} i_L^e - j\omega v_L^e \end{cases} \tag{30}$$

The AC analysis of the boost converter is carried out by introducing small AC variations in all variables of (30) as:

$$\begin{cases} v_s^e = V_s^e + \hat{v}_s^e \\ v_L^e = V_L^e + \hat{v}_L^e \\ d = D + \hat{d} \\ i_s^e = I_s^e + \hat{i}_s^e \\ i_L^e = I_L^e + \hat{i}_L^e \end{cases} \tag{31}$$

where the parameters denoted by capital letters refer to steady state operating point, while the perturbed components are denoted by the mark '^'. Therefore, the small-signal equations of the boost converter can be derived as follows:

$$\begin{cases} \dfrac{d\hat{i}_s^e}{dt} = -j\omega \hat{i}_s^e - \dfrac{D'}{L_i} \hat{v}_L^e + \dfrac{V_L^e}{L_i} \hat{d} + \dfrac{1}{L_i} \hat{v}_s^e \\ \dfrac{d\hat{i}_L^e}{dt} = -\left(\dfrac{R_L}{L_L} + j\omega\right) \hat{i}_L^e + \dfrac{1}{L_L} \hat{v}_L^e \\ \dfrac{d\hat{v}_L^e}{dt} = \dfrac{D'}{C_o} \hat{i}_s^e - \dfrac{I_s^e}{C_o} \hat{d} - \dfrac{1}{C_o} \hat{i}_L^e - j\omega \hat{v}_L^e \end{cases} \tag{32}$$

where $D' = 1 - D$. Using Laplace transform, the small-signal model can be given as:

$$\begin{cases} s\hat{i}_s^e(s) = -j\omega \hat{i}_s^e(s) - \dfrac{D'}{L_i} \hat{v}_L^e(s) + \dfrac{V_L^e}{L_i} \hat{d}(s) + \dfrac{1}{L_i} \hat{v}_s^e(s) \\ s\hat{i}_L^e(s) = -\left(\dfrac{R_L}{L_L} + j\omega\right) \hat{i}_L^e(s) + \dfrac{1}{L_L} \hat{v}_L^e(s) \\ s\hat{v}_L^e(s) = \dfrac{D'}{C_o} \hat{i}_s^e(s) - \dfrac{I_s^e}{C_o} \hat{d}(s) - \dfrac{1}{C_o} \hat{i}_L^e(s) - j\omega \hat{v}_L^e(s) \end{cases} \tag{33}$$

From (33), there are three independent input variations: control ($\hat{d}(s)$), input voltage ($\hat{v}_s^e$) and load current ($\hat{i}_L^e(s)$) variations. Therefore, the output voltage ($\hat{v}_L^e(s)$) variation can be given as a linear combination of these three inputs as follows:

$$\hat{v}_L^e(s) = G_{vd}(s)\,\hat{d}(s) + G_{vg}(s)\,\hat{v}_s^e(s) - Z_L(s)\,\hat{i}_L^e(s) \tag{34}$$

where: $G_{vd}(s)$ is the control-to-output transfer function, which is derived as follows:

$$G_{vd}(s) = \left.\frac{\hat{v}_L^e(s)}{\hat{d}(s)}\right|_{\hat{v}_s^e(s)=0} \tag{35}$$

and $G_{vg}(s)$ is the input-to-output transfer function, which is derived as follows:

$$G_{vg}(s) = \left.\frac{\hat{v}_L^e(s)}{\hat{v}_s^e(s)}\right|_{\hat{d}(s)=0} \tag{36}$$

and $Z_L(s)$ is load impedance, which can be given as follows:

$$Z_L(s) = \frac{\hat{v}_L^e(s)}{\hat{i}_L^e(s)} \tag{37}$$

In order to obtain $G_{vd}(s)$, the perturbed voltage source is set to zero ($\hat{v}_s^e(s) = 0$) in (33) and rewrite it in state-space form as:

$$\dot{X} = A_{vd}x + B_{vd}u \tag{38}$$

$$Y = C_{vd}x + D_{vd}u \tag{39}$$

where

$$x = \begin{bmatrix} \hat{i}_s^e & \hat{i}_L^e & \hat{v}_L^e \end{bmatrix}^T \tag{40}$$

$$u = \begin{bmatrix} \hat{d} \end{bmatrix} \tag{41}$$

$$A_{vd} = \begin{bmatrix} -j\omega & 0 & \frac{-D'}{L_i} \\ 0 & -\left(\frac{R_L}{L_L} + j\omega\right) & \frac{1}{L_L} \\ \frac{D'}{C_o} & \frac{-1}{C_o} & -j\omega \end{bmatrix} \tag{42}$$

$$B_{vd} = \begin{bmatrix} \frac{v_L^e}{L_i} & 0 & \frac{I_s^e}{C_o} \end{bmatrix}^T \quad (43)$$

$$C_{vd} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \quad (44)$$

$$D_{vd} = [0] \quad (45)$$

Therefore, $G_{vd}(s)$ can be given as:

$$G_{vd}(s) = C_{vd}(sI - A_{vd})^{-1} B_{vd} + D_{vd} \quad (46)$$

Fig. 10(a) shows block diagram for voltage control strategy of the proposed three-phase AC/AC boost converter. The open-loop transfer function $T(s)$ of the voltage control loop is the product of the controller transfer function $G_C(s)$, the transfer function of the PWM stage $G_{PWM}(s)$ and the control-to-output transfer function $G_{vd}(s)$. It can be given as follows:

$$T(s) = G_C(s) G_{PWM}(s) G_{vd}(s) \quad (47)$$

Since $G_{PWM}(s) = 1/V_M$, where V_M is the maximum value of the sawtooth waveform of PWM. Therefore, $T(s)$ can be rewritten as:

$$T(s) = \frac{(k_p s + k_i)}{s} \left(\frac{1}{V_M}\right) G_{vd}(s) \quad (48)$$

The open-loop transfer function $T(s)$ is employed to design the gains of the PI voltage controller. To guarantee the desired dynamic performance and the stability, the gain and phase margins give a proper indication of the system performance and stability. Fig. 10(b) shows the bode diagrams of the open-loop control system in uncompensated ($T(s) = G_{vd}(s)$) and compensated ($T(s) = G_C(s)G_{PWM}(s)G_{vd}(s)$) conditions. This figure clarifies the adjustment of frequency response of the open-loop system using PI controller to attain the desired control objectives. The open-loop system in an uncompensated condition has gain margin (G_m) $= -54.5$ dB at phase crossover frequency (W_{cp}) $=$ 1380 rad/s and phase margin (P_m) $= -45.5°$ at gain crossover frequency (W_{cg}) $=$ 506000 rad/s, which is considered unstable. Dynamic performance and stability of the system is improved by increasing the phase and gain margins using the PI controller. The gains (K_p and K_i) of the PI controller are designed to attain $G_m =$ 7.03dB at $W_{cp} =$ 1050 rad/s and $P_m = 156°$ at $W_{cg} =$ 38.1 rad/s which achieve the desired control objectives.

E. DESIGN OF PASSIVE ELEMENTS

The inductor L_i design depends on its maximum current handling capability and allowable current ripple [28]. It can be determined for boost converter, as an example, as follows:

$$L_i \geq \frac{V_o}{\Delta_{iL}} D(1 - D) T_{sw} \quad (49)$$

The current ripple Δ_{iL} is a percentage of maximum load current $I_{L,max}$ and it can be given as:

$$\Delta_{iL} = x\% I_{L,max} \quad (50)$$

whereas, the output capacitor C_o is designed such as the output filtering capacitance's current is less than 5% maximum load [29]. Therefore, it can be determined for buck and boost converters as follows:

$$C_o \leq \frac{5\% P_{out,max}}{V_o^2 (2\pi F)} \quad (51)$$

where $P_{out,max}$ is the maximum output power, V_o is the RMS value of the output voltage and F is the supply frequency.

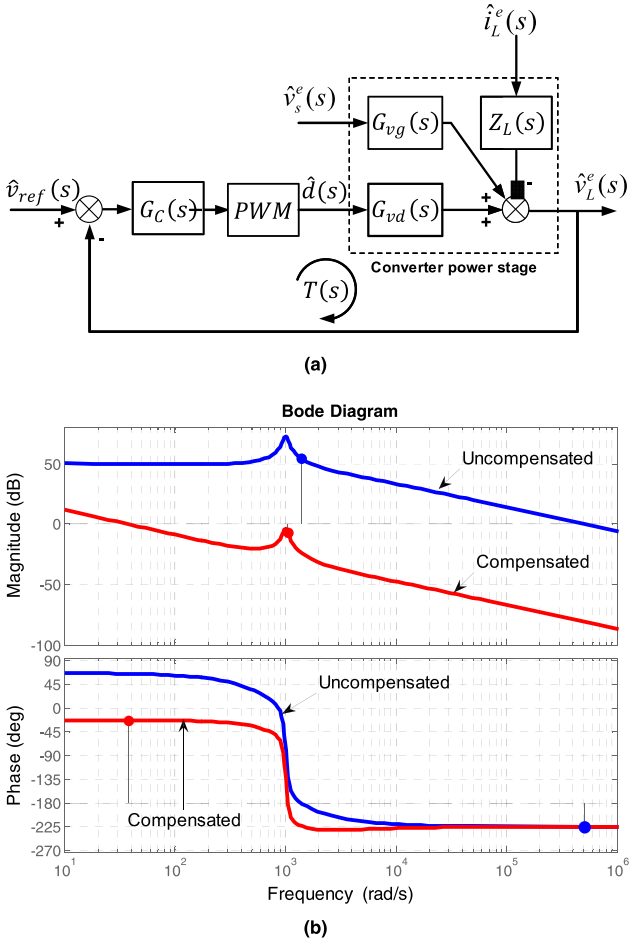

FIGURE 10. Voltage control strategy of the proposed three-phase AC/AC boost converter. (a) Block diagram. (b) Bode diagram of the open-loop control system.

F. Efficiency analysis

The efficiency of the AC/AC converter, either buck-type or boost-type is mainly related to the losses in semiconductor devices. The losses of semiconductor devices depend on their characteristics and the operating conditions such as voltage, current and switching frequency. The efficiency (η) can be estimated as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \quad (52)$$

where P_{in}, P_{out} and P_{loss} refer to the input power, output power and power loss of the converter, respectively. The converter loss is the sum of the losses of its semiconductor components. Power losses of any semiconductor component, IGBT or the antiparallel diode, of the converter are

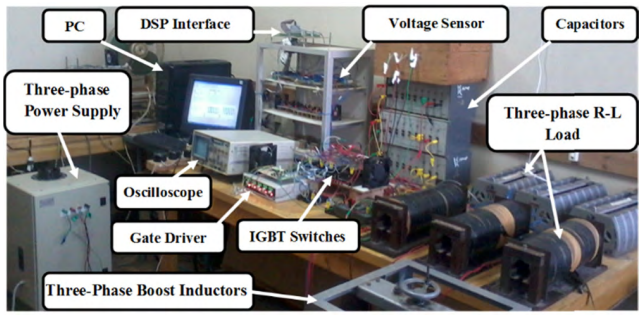

FIGURE 11. Photo of the real experimental system.

divided mainly into two categorifies: conduction losses and switching losses. The average conduction losses in the IGBT ($P_{conIGBT,avg}$), which occur during the conduction period, can be given as:

$$P_{conIGBT,avg} = V_{CE0} \cdot I_{C,avg} + R_C \cdot I_{C,rms}^2 \tag{53}$$

where V_{CE0} is the on-state zero-current collector-emitter voltage; R_c is the on-state forward collector-emitter resistance; $I_{C,avg}$ is the average collector and $I_{C,rms}$ is the effective collector current of the IGBT. As the same, the average conduction losses in the diode can be given as:

$$P_{conD,avg} = V_{D0} \cdot I_{D,avg} + R_D \cdot I_{D,rms}^2 \tag{54}$$

where V_{D0} denotes for the on-state zero-current voltage; R_D is the on-state forward resistance; $I_{D,avg}$ is the average current and $I_{D,rms}$ is the RMS current of the antiparallel diode.

The switching losses in the IGBT ($P_{sw,IGBT}$), which occur as a result of energy losses during the transition periods, can be given as:

$$P_{sw,IGBT} = \left(E_{on,IGBT} + E_{off,IGBT}\right) \cdot F_{sw} \tag{55}$$

where $E_{on.IGBT}$ and $E_{off,IGBT}$ are the dissipated energies of the IGBT during turn-on and turn-off instants, respectively. As the same, the switching losses in the antiparallel diode ($P_{sw,D}$) can be given as:

$$P_{sw,D} = \left(E_{on,D} + E_{off,D}\right) \cdot F_{sw} \tag{56}$$

where $E_{on,D}$ and $E_{off,D}$ are the dissipated energies of the diode during turn-on and turn-off time periods, respectively.

VI. RESULTS AND DISCUSSION

The performance of the proposed three-switch buck and boost converters are simulated in the MATLAB/Simulink environment to investigate their behaviors under different operating conditions.

To validate the simulation results and confirm the feasibility of proposed converters, laboratory prototypes of the buck-type and boost-type converters were built based on the dSPACE DS1104 control board. Fig. 11 shows a photo of the real experimental system. The experimental setup consists of three-phase autotransformer, three-switch PWM AC/AC converter using three IGBTs each 50A/1200V (CM50DY-24H MITSUBISHI Module), three-phase resistive-inductive (R-L) load, a dSPACE (DS1104), IGBTs gate driver and a voltage sensor (LV25-P). The parameters of the proposed circuits are listed in Table 1.

TABLE 1. Parameters of the proposed circuits.

Symbol	Parameter	Value
V_s	supply voltage	220 V/ph
F	supply frequency	50 Hz
R_L	load resistor	40 Ω/ph
L_L	load inductor	130 mH/ph
L_{i_buck}	input filter inductance for buck converter	5 mH/ph
$C_{i\ buck}$	input filter capacitance for buck converter	8 μ/ph
C_{o_buck}	output filter capacitance for buck converter	14 μ/ph
P_{o_buck}	output power of buck converter	1500 W
L_{i_boost}	inductance of boost inductor	25 mH/ph
C_{o_boost}	output filter capacitance for boost converter	15.5 μ/ph
P_{o_boost}	output power of boost converter	5000 W
F_{sw}	switching frequency	4.5 kHz
$K_{p\ buck}$	proportional gain for buck PI controller	0.0052
K_{i_buck}	integral gain for buck PI controller	0.182
K_{p_boost}	proportional gain for boost PI controller	0.0043
K_{i_boost}	integral gain for boost PI controller	0.117

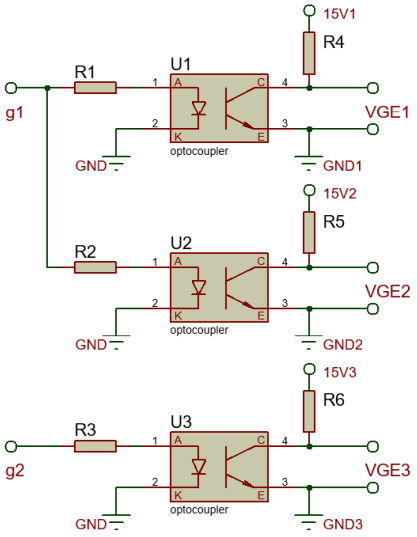

FIGURE 12. Gate driver circuit.

The load voltage is measured using voltage sensor (LV25-P) to generate the feedback signal and then this signal is sent to the dSPACE control board via the A/D converter ports. The required pulses (g_1 and g_2) are generated by using a dSPACE board (DS1104) synchronized with MATLAB/SIMULINK. The output signals ($g1$ and $g2$) of the dSPACE board are not sufficient to drive the IGBTs. For this reason, a gate interface board circuit is used between the dSPACE board and the IGBTs to increase the signals power and achieve pulses of approximately 15 V to achieve an effective IGBT switching; and to introduce an isolation between the dSPACE board and the converter power circuit.

Fig. 12 shows the gate driver circuit which employs three isolated gate 15V power supplies and three optocouplers. The

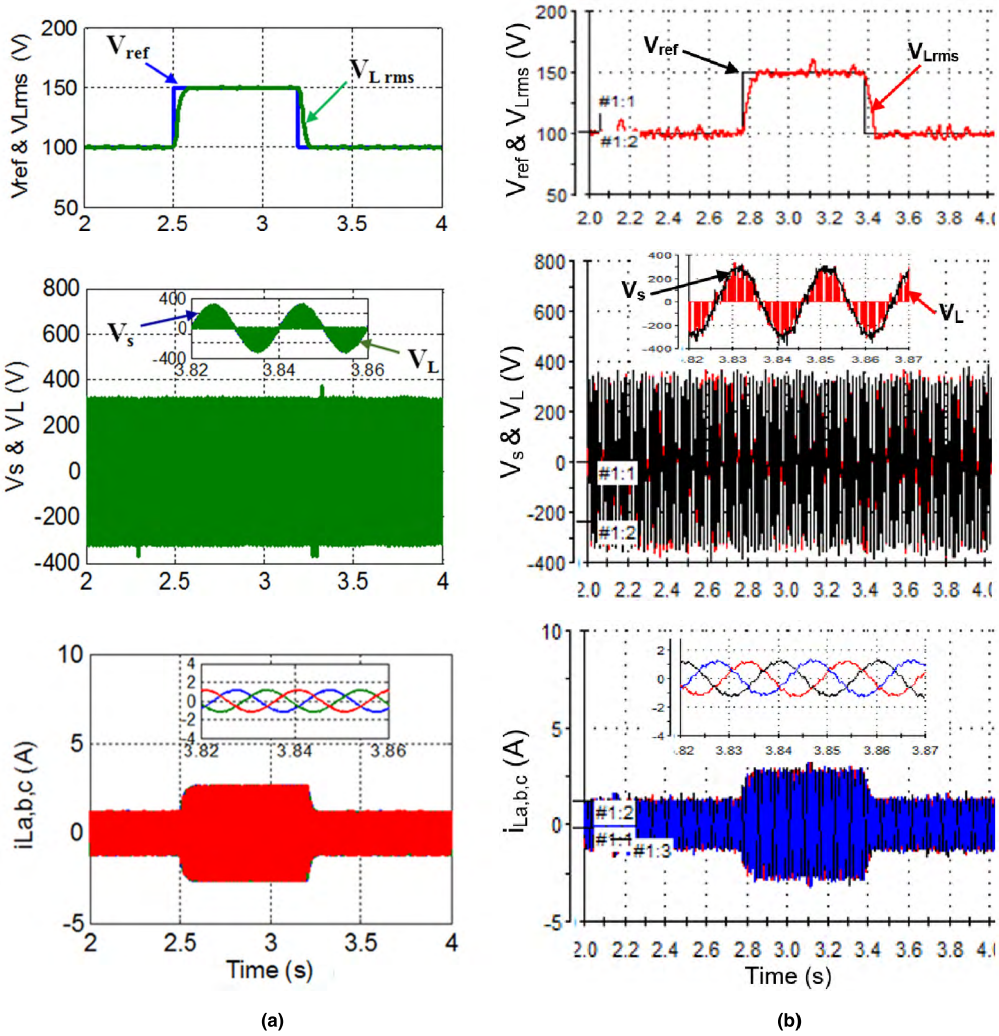

FIGURE 13. Simulation and experimental responses of the buck converter at ±50% step change in the reference voltage. (a) Simulation. (b) Experimental.

gate signal g_1, which is the output of DSP control board, is used to generate the gate-emitter voltages V_{GE1} and V_{GE2} that drive the IGBT switches S_1 and S_2, respectively. As a result, V_{GE1} and V_{GE2} signals have the same driving singal with two different grounds. Consequently, the two switches are synchronized to operate simultaneously which ensures the symmetry of the output voltage/current of the converter. Also, the synchronization of the switches ensures that there is no circulating current between any two phases of the load. Whereas, the gate signal g_2 is used to generate the gate-emitter voltage V_{GE3} that drives the IGBT switch S_3.

A. DYNAMIC PERFORMANCE INVESTIGATION OF BUCK CONVERTER

The following tests are carried out to examine the performance of the proposed three-switch buck converter:

1) CHANGE IN THE REFERENCE VOLTAGE

The effective value and frequency of the supply phase voltage are 220 V and 50 Hz, respectively. The reference voltage is firstly set at 100 V, then sudden changes in the reference voltage (from 100V to 160V and vice versa) are occurred and the converter performance is examined. Fig. 13 shows the simulation and experimentation results of the steady-state and dynamic response of the proposed buck converter at ±50% step changes in the reference voltage (V_{ref}). This figure has three subplots: the upper subplot shows the reference and actual load RMS voltages, the middle one displays the instantaneous source and load voltages waveforms, and the lower one demonstrates the three phase load currents. It is noted that at the actual load voltage (V_{Lrms}) has a good tracking behavior during the step changes of the reference voltage. The middle subplot shows that the instantaneous load voltage (V_L) is a chopped voltage due to switching action of the buck converter. The three phase load currents have nearly sinusoidal waveforms as shown in the lower subplot.

The symmetry of load voltage and load currents are examined using the theory of symmetrical components. This theory resolves any set of unbalanced voltages or currents into three sets of symmetrical balanced phasors (positive, negative and

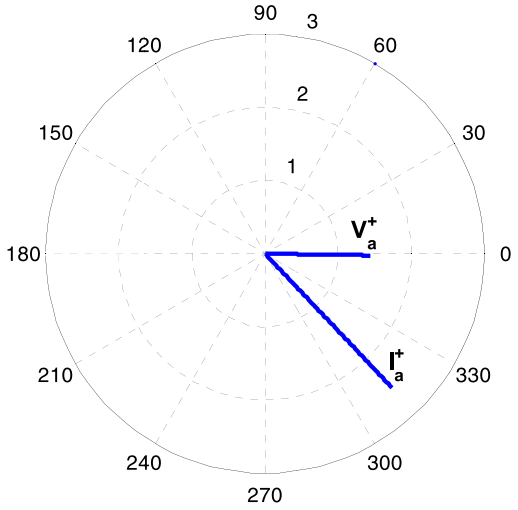

FIGURE 14. Sequence components of phase *a* [100V/div, 1A/div].

zero sequence components) which can be calculated as:

$$\begin{bmatrix} \vec{X}_a^+ \\ \vec{X}_a^- \\ \vec{X}_a^\circ \end{bmatrix} = \begin{bmatrix} 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \vec{X}_a \\ \vec{X}_b \\ \vec{X}_c \end{bmatrix} \tag{57}$$

where X refers to voltage or current, $\vec{X}_a^+, \vec{X}_a^-, \vec{X}_a^\circ$ refer to the positive, negative and zero sequence components of phase a, and $\alpha = e^{j2\pi/3} = 1\angle 120°$ is known as the Fortescue operator. The phasors representing the sequence components for phases b and c are given by:

$$\begin{cases} \vec{X}_b^+ = \alpha^2 \vec{X}_a^+; X_b^- = \alpha \vec{X}_a^-; \quad \vec{X}_b^\circ = \vec{X}_a^\circ \\ \vec{X}_c^+ = \alpha \vec{X}_a^+; \vec{X}_c^- = \alpha^2 \vec{X}_a^-; \quad \vec{X}_c^\circ = \vec{X}_a^\circ \end{cases} \tag{58}$$

Applying the symmetrical component method to the load voltage and load current responses, the sequence components for phase a are depicted in Fig. 14 and are given respectively as:

$$\begin{bmatrix} \vec{V}_a^+ \\ \vec{V}_a^- \\ \vec{V}_a^\circ \end{bmatrix} = \begin{bmatrix} 144.4\angle -0.96° \\ 3.521 \times 10^{-2}\angle 0° \\ 2.348 \times 10^{-8}\angle 0° \end{bmatrix} \tag{59}$$

$$\begin{bmatrix} \vec{I}_a^+ \\ \vec{I}_a^- \\ \vec{I}_a^\circ \end{bmatrix} = \begin{bmatrix} 2.527\angle -46.5° \\ 6.848 \times 10^{-4}\angle 0° \\ 1.412 \times 10^{-12}\angle 0° \end{bmatrix} \tag{60}$$

It is clear from the results that the negative and zero sequence components of phase-a voltage and current are very low and can be neglected which proves the symmetry of the load voltages and currents. Also. this ensures that there is no circulating current between the load phases which shows the effectiveness of the proposed control strategy. It is observed that the load currents follow the variations in the load voltage, i.e. increase in the load voltages increases the load currents at constant load impedance.

2) SUPPLY VOLTAGE CHANGE

The robustness of the proposed three-switch AC/AC buck converter is examined at ±20% step changes in the supply voltage (V_s) as illustrated in Fig. 15. This figure has two subplots: the upper subplot shows the reference and actual load RMS voltages, and the lower one displays the instantaneous source and load voltages. As shown, the proposed buck converter achieves a small voltage variation in the load voltage (V_{Lrms}) and a fast recovery time; approximately 0.06 s, to its reference voltage (V_{ref}). This figure shows that the system has a good dynamic response against sudden variations in the supply voltage.

3) LOAD CHANGE

Performance of the proposed buck converter is also examined under sudden load changes to prove its robustness against load variations. Fig. 16 demonstrates the simulation and experimental responses of the buck converter at ±33.33% step changes in the load at time 6 s and time 6.7 s, respectively. This figure has two subplots: the upper subplot shows the reference and actual load RMS voltages, and the lower one displays the instantaneous three phase load currents. As shown from the upper subplot, the load voltage (V_{Lrms}) has a fast response recovery to its reference voltage (V_{ref}) value against load change with small voltage perturbations.

B. DYNAMIC PERFORMANCE INVESTIGATION OF BOOST CONVERTER

The following tests are carried out to examine the performance of the proposed three-switch boost converter:

1) CHANGE IN THE REFERENCE VOLTAGE

Fig. 17 displays the simulation and experimentation results of the dynamic response of the proposed boost converter at ±20% step changes in the reference voltage. The reference voltage is set first at 250V which is higher than the rated 220V supply voltage to ensure the step-up voltage ability of the proposed boost converter. During the step changes in the reference voltage (from 250V to 300V and vice versa), as shown from the results, the load voltage (V_{Lrms}) follows the reference voltage (V_{ref}) with a good tracking behavior as shown in the upper subplot of this figure. The proposed boost converter ensures balanced and symmetrical three-phase load voltages and currents with a low harmonic distortion and nearly sinusoidal waveforms as seen in the zoomed voltages and currents waveforms of the middle and lower subplots of this figure. It is obvious that the harmonic contents of the proposed boost converter are lower compared with the proposed buck converter. Therefore, the input power factor PF and hence the efficiency of the proposed boost converter is higher as compared to the proposed buck converter.

2) SUPPLY VOLTAGE CHANGE

Fig. 18 demonstrates the simulation and experimental responses of boost converter at ±20% step changes in the

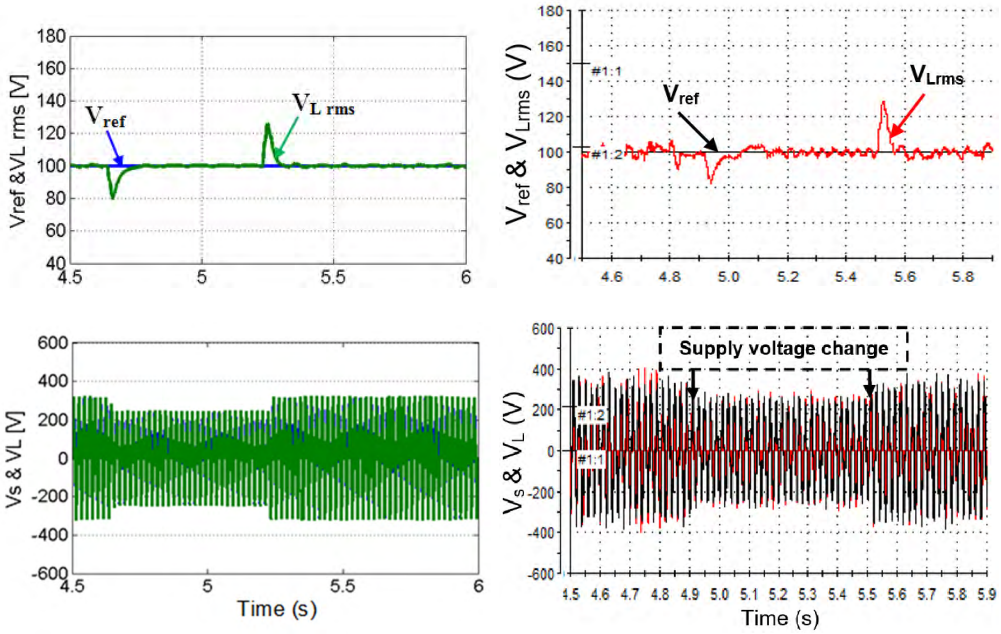

FIGURE 15. Simulation and experimental responses of the buck converter at ±20% step change in the supply voltage. (a) Simulation. (b) Experimental.

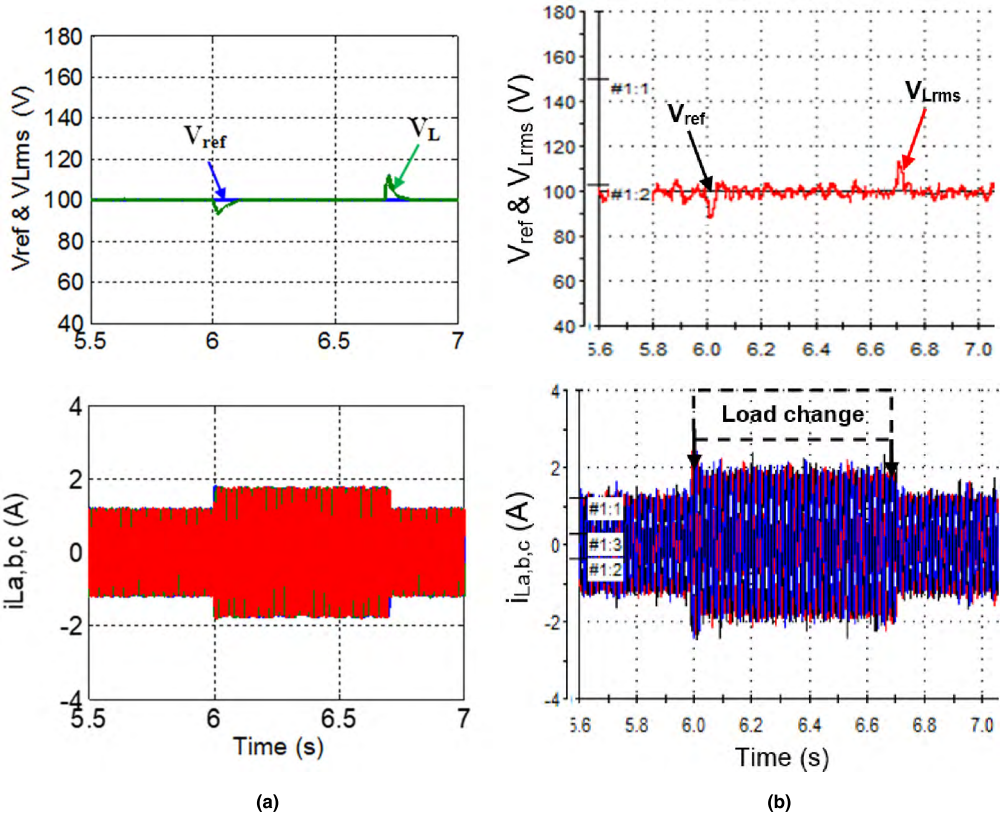

FIGURE 16. Simulation and experimental responses of the buck converter at ±33.33 % step change in the load. (a) Simulation. (b) Experimental.

supply voltage. This figure has two subplots: the upper subplot shows the waveforms of load voltage together with the reference voltage in rms values, whereas instantaneous load voltage together with supply voltage is shown in the lower one. As shown, the load voltage maintains its value under sudden changes in the supply voltage. The results prove that

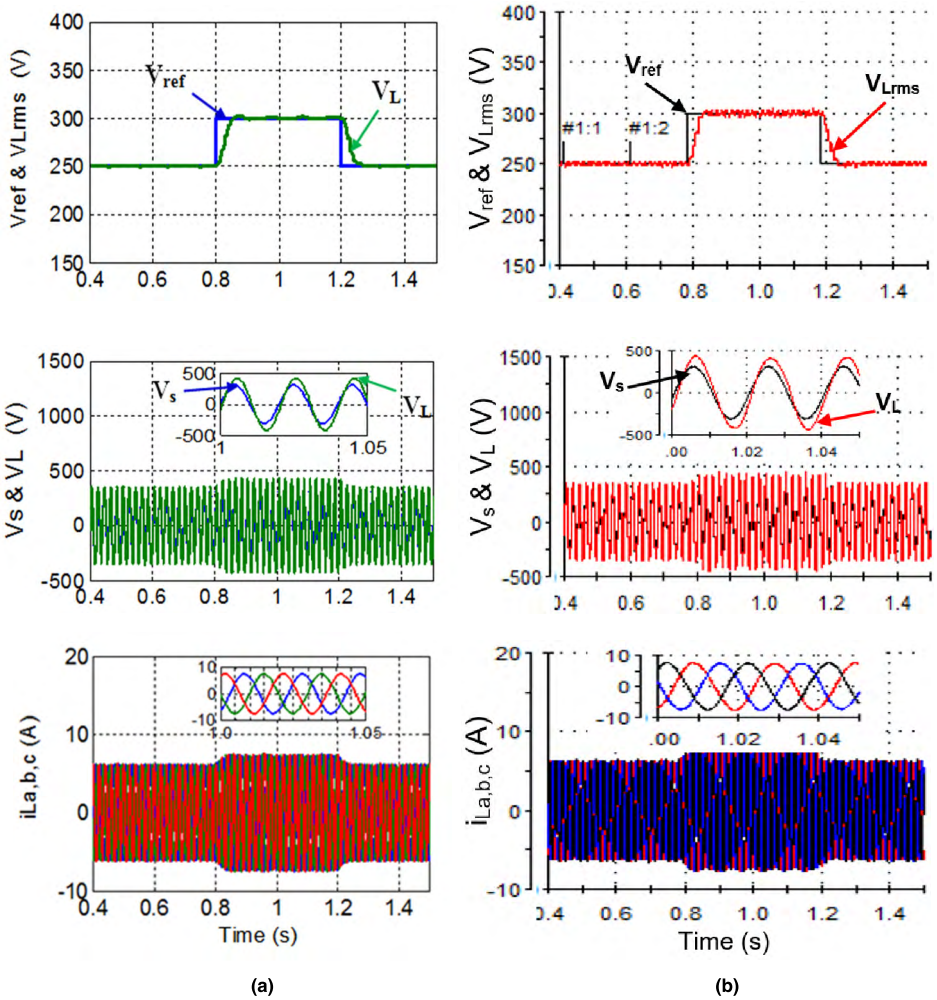

FIGURE 17. Simulation and experimental responses of the boost converter at ±20% step change in the reference voltage. (a) Simulation. (b) Experimental.

TABLE 2. Comparison between the proposed converters and the previous works.

	Buck			Boost	
	[30]	[31]	Proposed	[32]	Proposed
Active switch count	6 SCRs	6 IGBTs	3 IGBTs	6 IGBTs	3 IGBTs
Control	angle	PWM	PWM	PWM	PWM
ZCDs	yes	no	no	no	No
Gate Drivers	6	8	3	6	3
Complexity	high	moderate	low	moderate	low
Cost	moderate	high	low	high	low
Efficiency	80.51%	87.18%	94.23%	90.51%	96.43%
THD	16.61%	6.57%	6.54%	7.21%	3.21%
PF	0.673	0.943	0.9538	0.71	0.99949

boost converter offers good output voltage regulation versus the supply voltage variations.

3) LOAD CHANGE

Fig. 19 illustrates the simulation and experimental waveforms of the boost converter to examine its operation under step changes in the load. The figure has two subplots. The upper subplot displays that the load voltage keeps its value against ±33.33% sudden changes of the load, which are depicted in the lower subplot. Also, the load voltage has a fast response recovery to its reference voltage value with small voltage perturbations. The results ensure that the proposed boost converter circuit gives an excellent dynamic response versus load variations.

C. PERFORMANCE COMPARISON WITH THE PREVIOUS WORKS

Table 2 shows the performance comparison of the proposed circuits for buck and boost AC/AC converters with the similar topologies of previous works in terms of switch count, control strategy, the need for ZCDs, number of gate driver circuits, complexity, cost, efficiency, THD and input PF. For fair comparison, all compared converters are tested at the same loading conditions, same supply and same switching frequency. The proposed buck converter is compared with the previous works in [30] and [31]. Whereas, the proposed boost converter is compared with the previous work in [32].

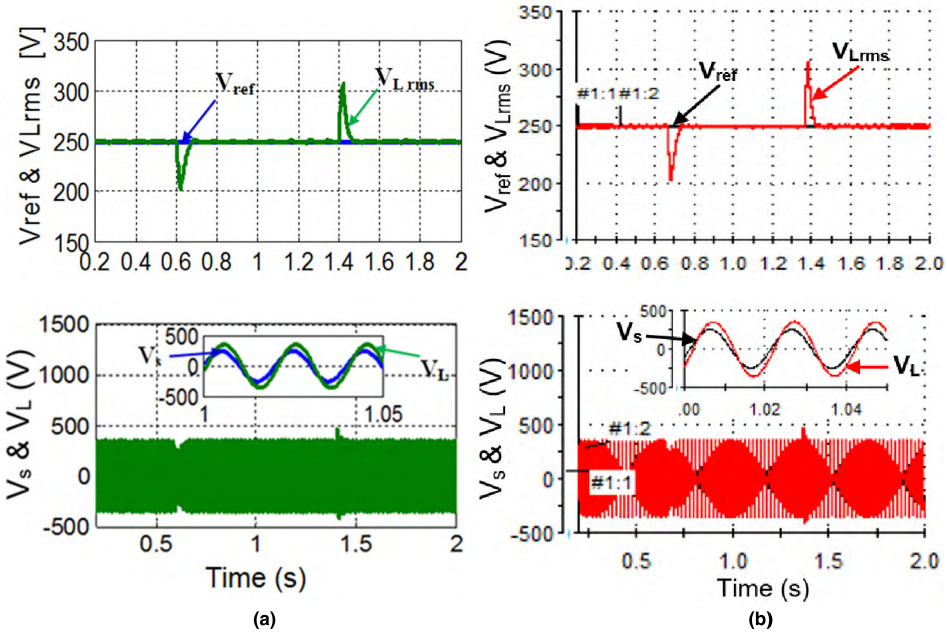

FIGURE 18. Simulation and experimental responses of the boost converter at ±20% step change in the supply voltage. (a) Simulation. (b) Experimental.

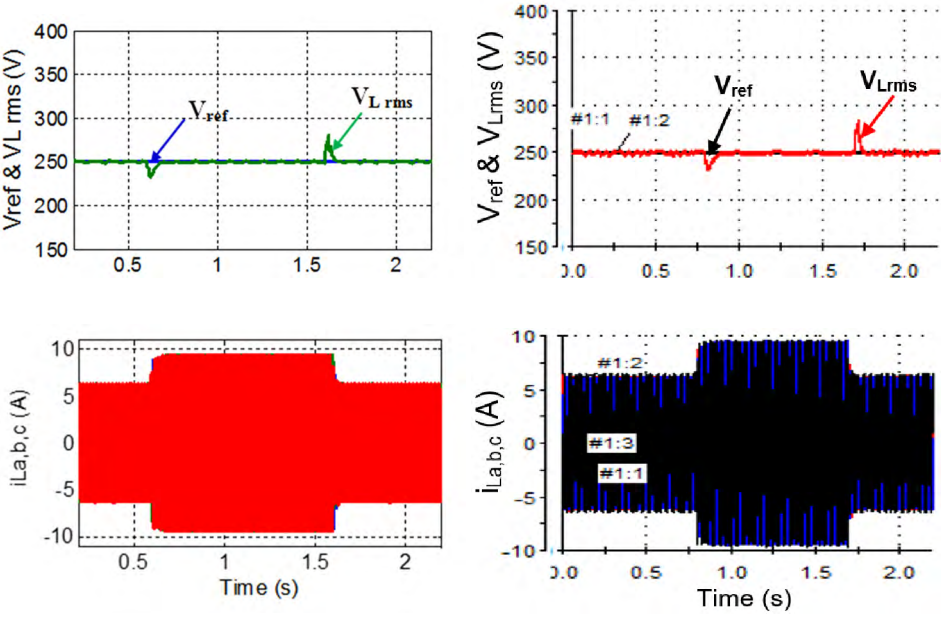

FIGURE 19. Simulation and experimental responses of the boost converter at ±33.33 % step change in the load. (a) Simulation. (b) Experimental.

It is highly observed that the proposed converters avoid the commutation problems of SCRs and the need of ZCDs in [30] by adopting PWM control strategy, as well as they have lesser number of IGBT switches and gate drive circuits than [31] and [32]. This ensures a low complexity and a low cost. Furthermore, efficiency, THD and PF of the proposed converters are improved compared with the previous works in [30]–[32]. This performance comparison indicates that the proposed converters are designed to be low cost, high efficiency, low THD and high PF.

VII. CONCLUSIONS

Two topologies of three-phase three-switch direct PWM AC/AC voltage converters were proposed; one for the buck-type converter and the other for the boost-type. Each topology has not DC link stage and has only three IGBTS. In addition, two simple control circuits were proposed; each control circuit employs only one voltage sensor. Operating principles of the proposed converters were elaborated; modulation schemes were discussed and mathematical expressions were derived. Computer simulations using MATLAB/SIMULINK

software program were performed. The experimental prototypes were built and the experimental results were obtained and compared with the corresponding simulation results in order to examine the performance of the proposed converters, under various operating conditions. It has been found that less number of the semiconductor switches offers lower switching and conduction losses, higher efficiency, smaller size and lower manufacturing cost of the proposed converters, as compared to the existing converters. In addition, the proposed closed-loop voltage control circuits provide excellent voltage regulation against variations in the reference voltage, the supply voltage and the load. Each control circuit has one sensor with a simple control algorithm, which results in a lower computational burden and hence a low-cost processor that can be used in the system implementation. Further, the proposed converters were examined with low switching frequency that ensured their applicability for medium and high-power applications. The experimental and simulation results are in a close agreement and verify the feasibility of the proposed converters.

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