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When Less Is More. . . Few Bit ADCs in RF Systems

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ABSTRACT Digitizing RF signals using few bit ADCs can provide system advantages in terms of reduced power dissipation, wider sampling bandwidth, and decreased demand for digital throughput. The diversity of established applications based on few bit ADCs, together with the recent surge of interest in the topic for 5G wireless communications and millimeter-wave radar, has created a need for practical design guidance governing their use in general RF systems. This paper, therefore, summarizes the state-of-the-art in few bit ADCs, comparing the dynamic range considerations involved with those of conventional RF receiver design. A simple analytic model for the monobit ADC is extended to multiple bits. Parametric analysis, independent of sampling considerations and system-specific signal processing, is used to illustrate the variation in the ADC output signal-to-noise-and-distortion ratio (SNDR) versus both the number of quantization bits and the input signal-to-noise ratio (SNR). At low and negative input SNR, increasing ADC resolution beyond 3–4 bits yields little advantage in output SNDR. Experiment confirms analytic predictions for the specific conditions under which the loss of signal fidelity due to quantization can be made negligible. In addition, parametric analysis of two-tone intermodulation distortion shows clear disadvantages to quantizing with <4 bits in the presence of strong blockers. The results reported in this paper, which are general and independent of system application, can be used to customize the number of ADC bits in an RF system based on system-specific performance requirements for receiver dynamic range.

INDEX TERMS Analog-to-digital converters (ADCs), 5G, low resolution ADCs, quantization, coherent receivers, radiofrequency integrated circuits, wireless communications, radar.

I. INTRODUCTION

The ADC is a key component in virtually all RF receivers. Whether digitizing a received signal at RF, baseband, or some intermediate frequency (IF), the system designer's ADC selection process typically involves a compromise between three factors: sample rate (which is proportional to input signal bandwidth), dynamic range, and power dissipation. The conventional approach to this tradeoff is to pick the ADC with the highest available dynamic range that can comply with system constraints on sample rate, power dissipation, and cost. This emphasis on dynamic range is reflected in Fig. 1, which tracks all ADCs reported over the 1997-2018 period at three IEEE conferences [1], [2]; the majority of research focuses on ADCs with >60 dB of SNDR dynamic range from a single sample.

The "dynamic range first" approach is so common that many engineers are, in fact, surprised to learn about entire application spaces that operate using only a few – or even just one – ADC bit. Examples of specialized wireless systems based on few bit ADCs include global positioning system (GPS) receivers [3]–[6]; radio astronomy [7], [8]; pulse Doppler radar [9]–[14], noise radar [15], [16], and next generation automotive radar [17]; low power [18]–[22], ultrawideband [23], [24], and impulse [25]–[29] communi-

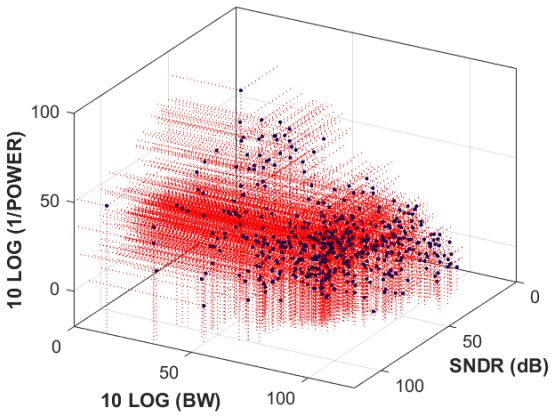

FIGURE 1. Illustration of available ADC performance in terms of power consumption, sampling bandwidth (BW), and SNDR dynamic range for all ADCs published in [1] and [2] from 1997-2018. The majority of research focuses on designs achieving >60 dB SNDR from a single ADC sample.

cations; ultrawideband spectrum monitoring [30] and channel estimation [31], [32]; digital RF memory (DRFM) and electronic warfare (EW) receivers [33]–[39]; and even biological sensing and computation [40]–[43]. The motivations for restricting a receiver design to only a few bits can vary widely to include: maximizing sample rate [38], minimizing power dissipation [25], achieving insensitivity to clock jitter over long coherent integration times [9], [10], [44] and, perhaps most importantly, dramatically reducing digital processing throughput requirements in large scale systems [18], [45]–[77].

Most recently, interest in few bit receivers for 5G communications has exploded [46], [76], both for millimeter wave phased arrays and for massive MIMO architectures. Fig. 2 illustrates the trend in phased array receiver design that drives this surge of interest. In Fig. 2a, classical element-level RF beamforming uses analog phase shifting and variable gain at each antenna element to generate a single scannable beam in a predetermined direction. The contributions from the individual elements are summed, optionally downconverted to IF, and digitized by an ADC. The chief disadvantage of this approach is that each additional independently scannable beam can only be generated by multiplexing another RF beamforming network to the same antenna aperture [78]. Conversely, in Fig. 2b, element-level digital beamforming digitizes the signal received at each antenna element, making it possible to form numerous simultaneous beams by applying variable gain and phase in the digital domain. Digital beamforming, as shown is this example, is well established in large scale L and S band radars [79], [80] and millimeter automotive radar [81]. For 5G applications, hybrid RF/digital approaches combining element level RF beamforming with subarray level digital beamforming have been proposed, and the required number of ADC bits is currently a subject of intense discussion, both for millimeter wave and massive MIMO systems [18], [46]–[76]. At a fundamental level, this debate is motivated by a key difference between RF and digital beamforming: the signal to noise ratio (SNR) at the input to the ADC. In Fig. 2a, beamforming based on RF combining

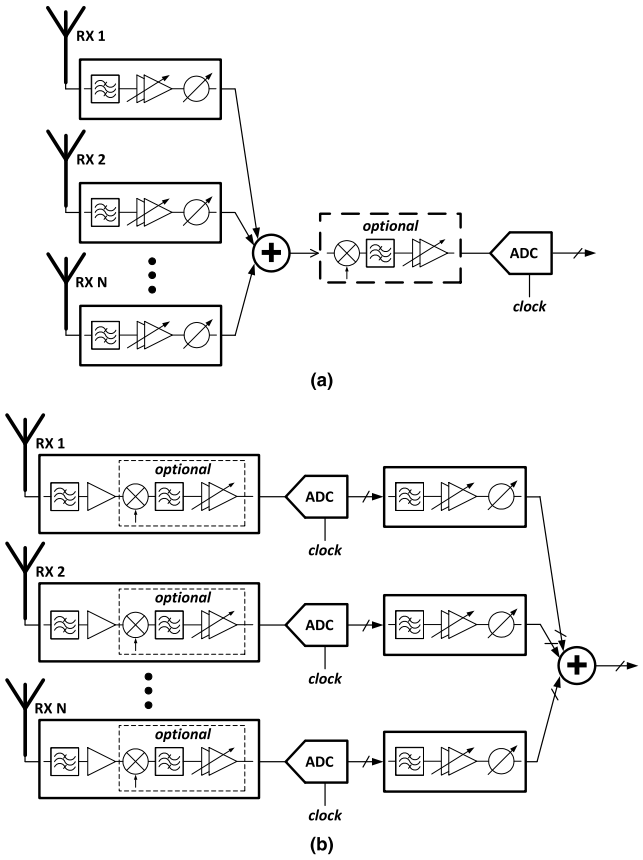

FIGURE 2. Two example beamforming architectures: (a) RF beamforming in which element level phase shift, amplitude scaling, and coherent summation take place before digitization and (b) digital beamforming in which the same processes take place after digitization. For (b), the SNR at the input to the ADC can be negative, which is exactly the case in which few bit ADCs become attractive.

increases SNR by a factor of N prior to digitization whereas digital beamforming increases SNR by N after digitization. Thus, if N is large, the useful range of input SNR at the ADC can easily extend to negative values for digitally beamformed phased arrays. As this paper will show, low and negative SNR is exactly the situation in which few bit ADCs can become attractive.

Unfortunately, in many development teams, ADC design trades tend to straddle the boundary between signal processing and RF engineering. As a result, programs frequently miss opportunities to apply few bit techniques in situations where they could significantly benefit overall size, weight, power, or performance. Making matters worse, existing literature surrounding few bit RF receivers is deeply enmeshed with application-specific considerations on waveform design and processing [18], [46]–[76]. Likewise, considerable analytical work on multilevel quantization of noisy waveforms [15], [82]–[96], is computationally challenging for parametric trade studies and lacks application to practical RF system design considerations.

To correct this deficit, this article provides broadly relevant design guidance for the use of few bit ADCs in RF receivers. The conventional multibit receiver is reviewed

and contrasted with the well-established monobit receiver. These design principles are then extended to an arbitrary number of bits, demonstrating how, under the simple assumption of sinusoidal excitation in Gaussian noise, the asymptotic behavior of few bit quantizers is separable from signal processing considerations. Parametric analysis and a variety of case studies illustrate the application of these results to RF systems.

II. DYNAMIC RANGE OF MANY BIT ADCS IN RF RECEIVERS

Digitization in RF systems can be conceptually distilled into two time domain processes, sampling and quantization, as illustrated in Fig. 3. The sampler captures discrete samples of the continuous input signal $v_{in}(t)$ at a rate $1/T_s$. This sampling action is a purely linear process given the appropriate selection of sample rate for the input waveform [97]. Although sampling impacts important RF design issues (e.g., frequency planning, oscillator specifications, filtering, etc.), the sampling process is conceptually the same whether an ADC has 1 bit or 16 [98].

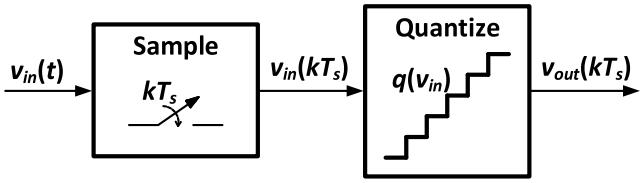

FIGURE 3. Conceptual block diagram for an ADC, illustrating the sampling and quantization operations.

In contrast, quantization applies a nonlinear transfer function $q(v_{in})$ to the input signal that digitizes each sample to one of 2^B levels, where B is the number of quantization bits. Quantization introduces an error that looks noise-like in the frequency domain, hence the term "quantization noise". For a many bit ADC, it is common to approximate the quantization noise power [97] for a sinusoidal input as

$$N_Q = \frac{\delta^2}{12} = \frac{1}{12}\left(\frac{V_{FS}}{2^B}\right)^2 \tag{1}$$

where δ is the least significant bit (LSB) size and V_{FS} is the peak to peak full scale range at the ADC input. The ADC output reference impedance is assumed to be 1 without loss of generality. If the input signal is a full scale sinusoid, the ideal output signal power is $V_{FS}^2/8$, making the quantizer's output signal to noise ratio

$$SNR_{OUT} = \frac{V_{FS}^2/8}{N_Q} = 1.5 \cdot 2^{2B} = (6.02 \cdot B + 1.76) \ \text{dB} \tag{2}$$

A more common ADC figure of merit is the signal to noise and distortion ratio (SNDR or SINAD), which includes the power contribution of all nonlinear distortion at the ADC output. Substituting $SNDR_{OUT}$ for SNR_{OUT} in the preceding expression to account for both quantization and other noise components yields the definition of the "effective number" of ADC bits (ENOB) [99]:

$$ENOB = \frac{SNDR_{OUT} - 1.76}{6.02} \tag{3}$$

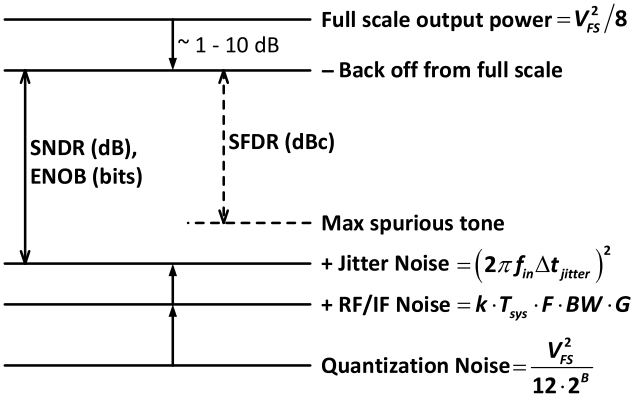

FIGURE 4. Illustration of RF system receiver dynamic range considerations. Realized SNDR is limited by the ADC backoff from full scale as well as by contributions from RF/IF noise, jitter noise, and quantization noise. The presence of spurious tones within the band of interest also limits dynamic range. The accepted expressions for RF/IF noise and jitter noise used in this illustration can be found in [100] and [101], respectively.

ADC performance is tightly linked to the most fundamental metrics in RF receiver design: sensitivity and dynamic range. Fig. 4 illustrates the considerations involved. The ADC's full scale output power and quantization noise floor set the outer bounds of the receiver dynamic range. Total gain from the RF and IF components should be chosen so that the maximum input signal to the ADC is backed off between 1 to 10 dB from full scale to avoid distortion. 6 dB is a typical back off. The RF gain should also be sufficiently large so that the receiver's thermal noise is dominated by the noise figure and noise bandwidth of the RF front end rather than by thermal noise contributions from gain or loss in the IF section or ADC input stages. The thermal noise power adds linearly to the quantization noise floor. For receiver designs with sufficient margin, it is often desirable to design the thermal noise to be roughly 10 dB higher than the quantization noise power to ensure sufficient noise power to dither the LSB and preclude any hysteretic effects. Jitter noise from the sample clock and RF waveform can further degrade the noise floor at the output of the ADC [100]. The resulting SNDR, or ENOB, describes the useful dynamic range of the receiver prior to any application of digital signal processing (DSP) gain. The maximum power of any spurious tone within the full Nyquist bandwidth then defines the spur free dynamic range (SFDR). Spurious tones and/or intermodulation distortion (IMD) from the RF and IF sections or from the ADC are especially undesirable because these distortion terms are correlated with the signal of interest and thus do not decrease with the application of DSP gain.

Although ADC data sheets provide detailed information on performance under a limited set of specific conditions, more detailed characterization can be highly beneficial for

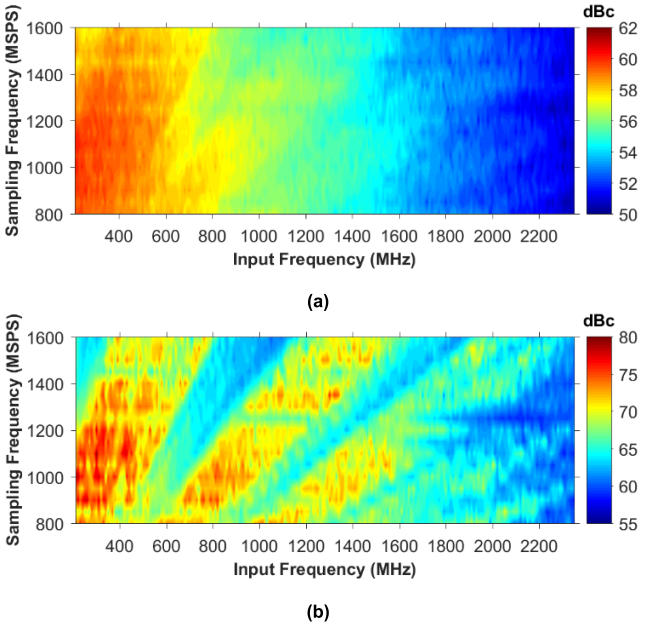

FIGURE 5. Measured dynamic range of the Texas Instruments ADC12D1600RF while varying sampling frequency and input frequency: (a) SNDR and (b) SFDR.

selecting the correct ADC and receiver frequency plan. The Texas Instruments ADC12D1600RF is an example of a part evaluated by the authors. This device is a 12 bit, 1.6 GSPS ADC capable of digitizing RF signals at frequencies >2.3 GHz using second and third Nyquist zone techniques [102]. Fig. 5a shows parametric tests characterizing this ADC in terms of its SNDR for a sinusoidal input at 1 dB backoff from full scale. A Rohde & Schwarz SMA100A generates the input signal; the sample clock is provided by the digital-to-analog converter (DAC) output of a Rohde & Schwartz FSV spectrum analyzer, with appropriate external filtering. Fig. 5b illustrates the SFDR for the same test. In this case, SFDR exceeds the SNDR, indicating that the ADC spurs are below the ADC's noise floor and only appear with the application of processing gain. The results in these plots are useful for determining the sample rate and the center frequency at the input to the ADC to achieve optimum receiver dynamic range for a given receiver bandwidth.

As indicated by (1)-(3), the available dynamic range from a *single* ADC sample becomes limited as the number of bits decreases. Fortunately, in coherent RF systems, digital processing of numerous samples is widely used to extend an ADC's useful dynamic range to levels below the noise floor. However, as described in the following sections, an ADC's input/output transfer function changes in the negative SNR regime, creating tradeoffs that have not previously been examined systematically for the case of general RF receiver design.

III. MONOBIT ADCS

The principles described in the preceding section can be inaccurate for few bit receivers. For example, the accepted

TABLE 1. Full scale SNDR vs. number of ADC bits.

Number of Bits	*Full Scale SNDR (dB)*	$(6.02 \times B + 1.76)$ dB
1	6.31	7.78
2	13.28	13.8
3	19.52	19.82
4	25.55	25.84
5	31.61	31.86
6	37.67	37.88
7	43.81	43.9
8	50.07	49.92

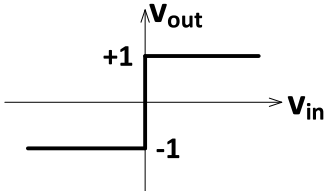

FIGURE 6. Input/output relationship for a monobit ADC.

expression given in (2) is only an approximation as ADC resolution decreases below 4 bits, as shown in Table 1, which compares (2) with DSP simulation of the quantization of a sinusoid. More importantly, however, the limited dynamic range of few bit ADCs implies that they will typically process low SNR waveforms, and the analysis used to develop (2) is invalid for the quantization of noise.

Alternative design guidance is thus required for few bit RF systems. Fortunately, as described in the introduction, 1-bit or "monobit" techniques are already mature in a variety of RF receiver applications, and provide a useful starting point for describing general few bit systems.

As shown in Fig. 6, the transfer function of a monobit quantizer clamps all positive input voltage samples to "+1" and all negative input voltage samples to "−1". (The actual choice of values for the ADC digital output levels is arbitrary, with no bearing on the result.) From [10], the exact solution for the output SNDR resulting from a sinusoid in Gaussian noise at the input to the monobit ADC is

$$SNDR_{OUT} = \left[\left(\frac{2\sqrt{2}}{\pi} \int_0^\infty J_1\left(u\sqrt{2 \cdot \rho_s}\right) \frac{e^{-u^2/2}}{u} du \right)^{-2} - 1 \right]^{-1} \quad (4)$$

where ρ_s is the input SNR. This result, which is independent of sample rate, sample frequency, noise bandwidth, etc., is plotted in Fig. 7. At low input SNR, the ADC acts as a unity gain amplifier with 1.96 dB noise figure. At high input SNR, output SNDR saturates at the maximum value from Table 1. Although correlation between MIMO / phased array channels can reduce this loss to less than 1.96 dB [67], such noise advantages are typically conservatively neglected in RF system design.

The two primary mechanisms for performance degradation in monobit ADCs are clock jitter and DC offset.

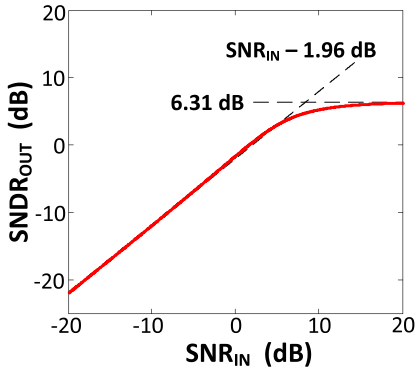

FIGURE 7. Output SNDR vs. input SNR for an ideal monobit ADC. At low input SNR, output SNDR increases linearly with an effective 1.96 dB noise figure. At high input SNR, SNDR saturates at the maximum value from Table 1.

Importantly, the impact of jitter is typically negligible at the low and negative input SNR levels where monobit ADCs achieve most of their dynamic range [10]. DC offset, on the other hand, can be a significant issue at low input SNR. Qualitatively, if the input noise is too small compared to a monobit ADC's total input-referred DC offset, only high input SNR can overcome the DC offset in order to reliably toggle the 1-bit quantization step. Fortunately, recent results have demonstrated robust cancellation approaches [9] mitigating the impact of DC offset in order to increase the practical applications and versatility of few bit RF receivers.

IV. FEW BIT ADCS

The rigorous closed form analysis presented in the previous section provides useful results for modeling and benchmarking monobit RF receivers. Unfortunately, the exact solution for ADC quantization noise becomes quite computationally demanding for multiple quantization levels, even in the simple case of a sinusoid in Gaussian noise [15], [82]–[96]. The range of convergence can be limited, and numerical evaluation of the functions involved over the regions of interest for RF applications is actually an ongoing topic of mathematical research [107]. As an alternative suitable for parametric analysis, this section presents a highly simplified model for multibit quantization that agrees well with time domain simulation and laboratory testing. This model provides the practicing engineer with an understanding of the asymptotic behavior of few bit ADCs in RF receivers, as well as useful guidance on strategy for more detailed simulations.

Fig. 8 illustrates the transfer function $q(\cdot)$ of an arbitrary M level quantizer. This input/output relationship can be written as

$$v_{out} = q(v_{in}) = \begin{cases} q_1 & \text{if } v_{in} \le V_1 \\ q_2 & \text{if } V_1 < v_{in} \le V_2 \\ q_3 & \text{if } V_2 < v_{in} \le V_3 \\ \vdots & \\ q_{M-1} & \text{if } V_{M-2} < v_{in} \le V_{M-1} \\ q_M & \text{if } V_{M-1} < v_{in} \end{cases} \tag{5}$$

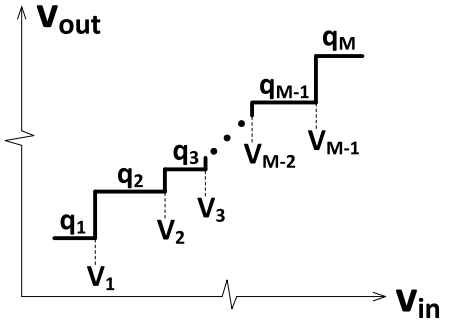

FIGURE 8. The input/output relationship for a quantizer with arbitrary transition points $V_1, V_2 \ldots V_M$ and quantization levels $q_1, q_2 \ldots q_M$.

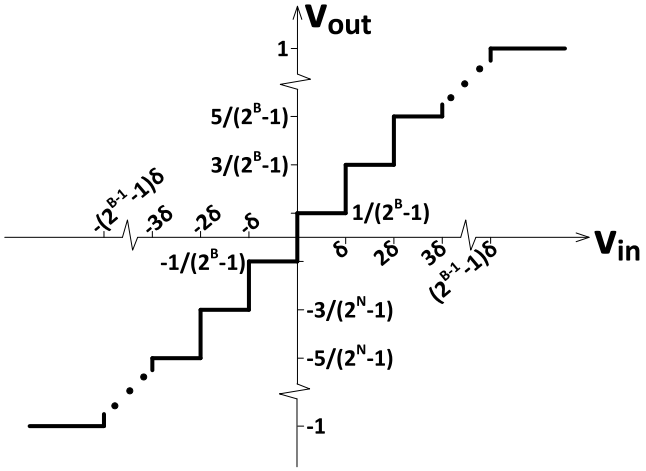

FIGURE 9. The input/output relationship for an ideal B bit quantizer with LSB size δ.

For reference, Fig. 9 illustrates an ideal B-bit quantizer with least significant bit (LSB) size δ. Comparing Figs. 8 and 9, it is easy to show that, for an ideal quantizer,

$$M = 2^B, \quad V_m = \left(\frac{m}{M} - \frac{1}{2}\right) V_{FS}, \quad q_m = -1 + 2\left(\frac{m-1}{M-1}\right) \tag{6}$$

where $m = 1, 2 \ldots M$ and setting $V_{FS} = M\delta$ effectively includes bits at the top and bottom rails.

Using elementary probability analysis, the expected voltage at the quantizer output is:

$$\begin{aligned} \overline{v_{out}} &= \int_{-\infty}^{\infty} q(v_{in}) f(v_{in})\, dv_{in} \\ &= q_1 \int_{-\infty}^{V_1} f(v_{in})\, dv_{in} + \sum_{m=2}^{M-1} q_m \int_{V_{m-1}}^{V_m} f(v_{in})\, dv_{in} \\ &\quad + q_M \int_{V_{M-1}}^{\infty} f(v_{in})\, dv_{in} \end{aligned} \tag{7}$$

Or, alternatively,

$$\overline{v_{out}} = q_1 P\left(v_{in} \le V_1\right) + \sum_{m=2}^{M-1} q_m P\left(V_{m-1} < v_{in} \le V_m\right) + q_M P\left(V_{M-1} < v_{in}\right) \quad (8)$$

where $P\left(V_{m-1} < v_{in} \le V_m\right)$ is the probability that v_{in} falls within the given interval. The expected total power at the quantizer output is likewise

$$\overline{v_{out}^2} = q_1^2 P\left(v_{in} \le V_1\right) + \sum_{m=2}^{M-1} q_m^2 P\left(V_{m-1} < v_{in} \le V_m\right) + q_M^2 P\left(V_{M-1} < v_{in}\right) \quad (9)$$

For the specific case in which the input voltage v_{in} consists of a discrete sample of a desired signal v_s and Gaussian input noise of power N_{in}, then $f\left(v_{in}\right)$ is Gaussian and the probability intervals are easily calculated using error functions:

$$\begin{aligned} P\left(v_{in} \le V_1\right) &= \frac{1}{2} + \frac{1}{2} erf\left(\frac{V_1 - v_s}{\sqrt{2N_{in}}}\right) \\ P\left(V_{m-1} < v_{in} \le V_m\right) &= \frac{1}{2} erf\left(\frac{V_m - v_s}{\sqrt{2N_{in}}}\right) - \frac{1}{2} erf\left(\frac{V_{m-1} - v_s}{\sqrt{2N_{in}}}\right) \\ P\left(V_{M-1} < v_{in}\right) &= \frac{1}{2} - \frac{1}{2} erf\left(\frac{V_{M-1} - v_s}{\sqrt{2N_{in}}}\right) \end{aligned} \quad (10)$$

The output SNDR is then simply the ratio of the expected output signal power $\overline{v_{out}}^2$ and the expected noise and distortion power $\overline{v_{out}^2} - \overline{v_{out}}^2$:

$$SNDR_{out} = \frac{\gamma \overline{v_{out}}^2}{\overline{v_{out}^2} - \gamma \overline{v_{out}}^2} \quad (11)$$

where a "clipping factor" γ is added to enforce saturation with

$$\gamma = \frac{SNDR_{noiseless}}{1 + SNDR_{noiseless}} \quad (12)$$

and $SNDR_{noiseless}$ is the SNDR achievable under noiseless conditions. Table 1, for example, provides the SNDR achievable for a full scale sinusoid (i.e., 0 dB back off from full scale) under noiseless conditions.

For parametric analysis, it is convenient to define the input SNR as $\rho_s = \gamma v_s^2 / N_{in}$. For a monobit ADC, (11) then simplifies to:

$$SNDR_{out} = \left[\frac{1}{\gamma} erf\left(\sqrt{\frac{\rho_s}{2\gamma}}\right)^{-2} - 1\right]^{-1} \quad (13)$$

Fig. 10 shows that this simple approximate expression compares well with the rigorous result of (4), with error less than 0.001 dB in the asymptotic limits at high and low SNR.

For higher numbers of bits, Fig. 11 compares the approximate technique of (11) with an exhaustive time domain simulation, showing excellent agreement in the asymptotic limits

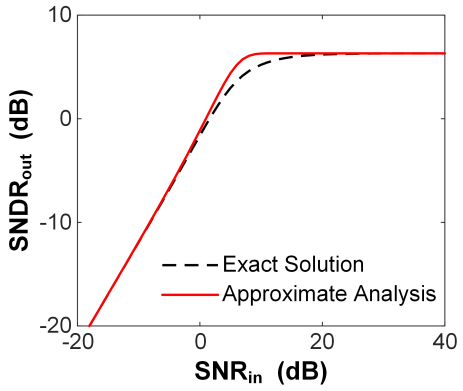

FIGURE 10. Comparison of the output SNDR of a monobit quantizer operating on a sinusoid in Gaussian white noise. The results compare the exact solution of (4) with the approximate result of (13). Error is <0.001 dB in the asymptotic limits at low and high SNR.

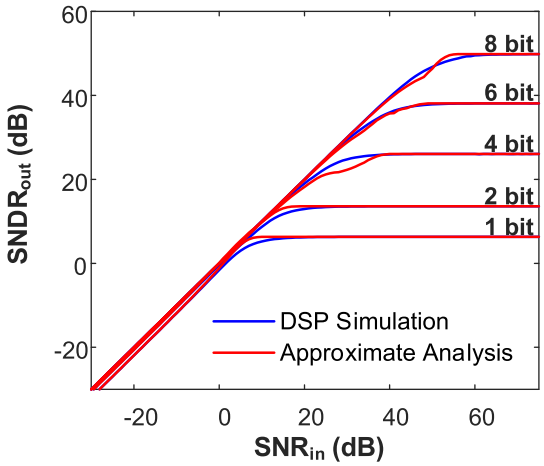

FIGURE 11. Comparison of output SNDR calculated using the approximate result of (13) with results from exhaustive DSP simulation. At low input SNR, the output SNDR increases linearly with input SNR.

where input SNR is either low or high. The simulation generates 10^8 data points from a single sinusoidal tone oversampled at 250 times the Nyquist rate. Gaussian noise is added to the signal to achieve the desired SNR and then quantized to 1, 2, 4, 6, and 8 bit resolution. Output SNDR of the quantized signal is calculated using Welsh's method [97]. The simulation takes 302 minutes to complete using MATLAB running on a workstation with dual 2.7 GHz Intel® Xeon® processors (24 total physical cores) and 256 GB of RAM. For both the approximate analysis and time domain simulation, the quantizer's input full scale range is scaled as input SNR changes to maintain 0 dB back off of the input waveform. The input range scaling used follows a common rule of thumb for optimal quantization [108]. These multibit transfer function curves show similar behavior to the monobit ADC result in Fig. 10. At low input SNR, the input/output relationship is log-log linear with an inherent SNR loss that varies depending on the number of bits. As input SNR increases, output SNDR saturates at the full scale maximum level. Note that the approximate analysis is general and includes no information on sampling considerations, so that the results in Fig. 11 are

likewise general for the quantization of any input sinusoid in Gaussian noise.

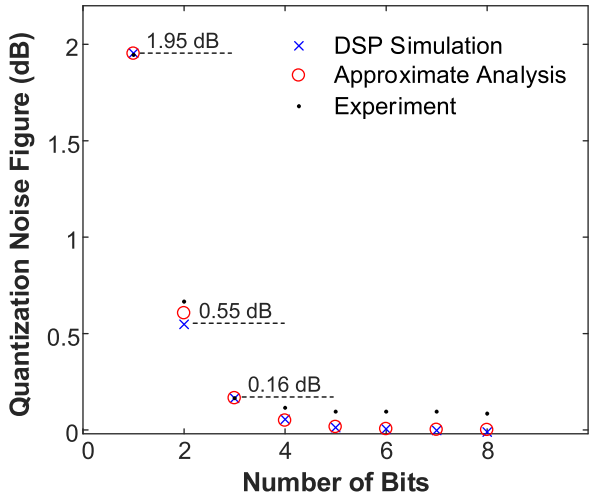

FIGURE 12. Degradation in output SNDR due to quantization. The input signal is a sinusoid at −20 dB SNR. "Quantization noise figure" refers to the difference between input SNR and output SNDR. Results are calculated using DSP simulation, the approximate analysis of (11), and experimental data. As the number of bits increases beyond 3, signal degradation due to quantization is negligible.

The behavior at low input SNR is of special interest for few bit receiver applications. Fig. 12 illustrates the degradation of an ADC's output noise floor (i.e., the difference between input SNR and output SNDR), or "quantization noise figure", for 1 to 8 quantization bits. The DSP simulation and approximate analysis data points are calculated using the approach and simulation settings used in Fig. 11 but at a fixed input SNR of −20 dB. The experimental results are achieved using a Tektronix AFG3102C arbitrary function generator to generate a tone at 100 MHz with −20 dB SNR in wideband noise having a mean power spectral density of $64.3 \cdot 10^{-12} \mathrm{V}_{\mathrm{rms}}^2/\mathrm{Hz}$. A Spectrum Netbox DN2.225-08 digitizer captures 2^{14} coherent samples over a ±0.5 V full scale range at a 312.5 MHz rate that are then deresolved to 1-8 bits in the time domain before performing a 20,000 point FFT to evaluate output SNDR in the frequency domain. Referring to the figure, monobit quantization of a low SNR signal degrades receiver sensitivity by ∼2 dB, as described analytically in the prior section. This is effectively a 2 dB drop in receiver noise figure, which can be significant for many RF systems, especially in wide band or high frequency applications. As the number of bits increases, the degradation drops effectively to 0 dB in simulation and analysis, and to <0.1 dB in measurement, with little to no improvement to be gained by increasing beyond 3 or 4 bits.

The above parametric analysis demonstrates how the classical relationship in (2) for ADC dynamic range, which states that output SNDR increases by about 6 dB/bit for sinusoidal input, is invalid for the quantization of low SNR input signals. This fact can thus be used as a powerful tool to reduce ADC power dissipation and/or data throughput requirements in noise dominated scenarios where additional ADC resolution provides no advantage.

V. TWO TONE DISTORTION

Two tone intermodulation distortion is an important consideration in RF [101] and other general sensor systems [109]. The standard two tone test procedure quantifies the third order intermodulation products (IM3) resulting from two tones presented at a component's input [99]. The results of this test are cascadable across multiple components in an RF receiver chain and prove useful for estimating the overall spurious IM3 levels resulting from two equal – or unequal – tones at the receiver input [110], [111]. In a well designed, high performance RF receiver, the final nonlinear component (i.e., the ADC) should dominate the IM3 response [101]. Detailed results of two tone distortion tests in the absence of noise are commonly provided in the data sheets of ADCs intended for RF applications.

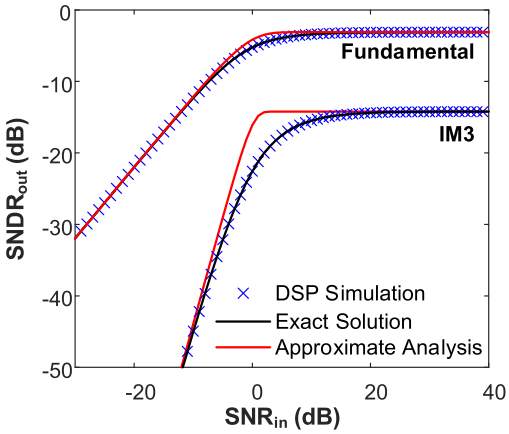

FIGURE 13. Output SNDR for the fundamental and third order intermodulation (IM3) products resulting from two equal amplitude sinusoidal tones presented to the input of a monobit ADC. Input SNR with respect to one of the two tones is varied from −30 to +40 dB. The exact solution from [10] agrees closely with DSP simulation; the approximate model shows close agreement at the asymptotic limits.

For monobit ADCs, an exact analytic model describing two tone distortion of sinusoids in Gaussian white noise is available and shows good agreement with measurement results [10]. In addition, the simple but approximate approach of (11) can be extended to IM3 products by substituting v_s^3 for v_s in (10) and introducing a second clipping factor γ_{IM3}. Likewise, the time domain DSP simulation of the prior section can be extended to two tones by adding an equal-amplitude second tone that is not a harmonic of the first signal. Fundamental tone SNDR is then evaluated considering one of the two tones as the desired signal and all other output power as noise and distortion; the same definition can be used for calculating the SNDR of an IM3 product. As shown in Fig. 13, the comparison between DSP simulation and the exact solution is excellent, and the approximate model shows close agreement at the asymptotic limits. At low input SNR, output SNDR increases at a 1:1 slope for a fundamental tone,

and at a 3:1 slope for an IM3 product, before saturating at the values corresponding to a two tone test under noiseless conditions.

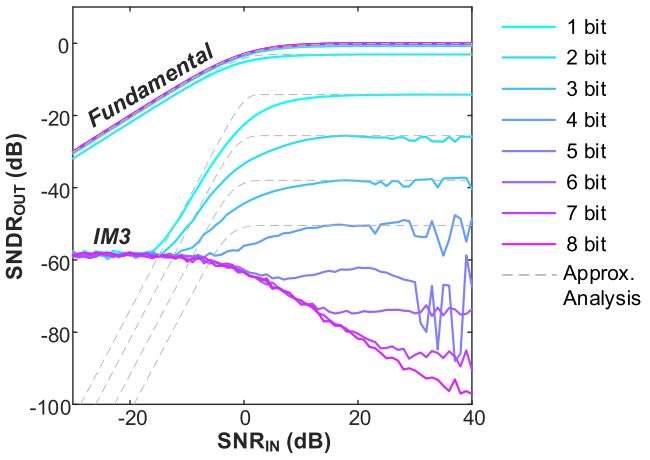

FIGURE 14. DSP simulated results for the output SNDR for the fundamental and IM3 products resulting from two equal amplitude sinusoidal tones presented to the input of a 1-8 bit ADC. For clarity, comparison with the approximate analysis is shown for 1-4 bits only. The spectral density estimate for IM3 terms below −60 dB is limited by simulation resources at low input SNR.

The simulation and approximate analysis used to generate the monobit results in Fig. 13 are repeated for 1-8 bits in Fig. 14. The two tone time domain simulation is performed in MATLAB using the same approach and computational resources as in Section IV, for a total run time of 401 minutes. The spectral density estimate is limited by the processing gain of the FFT and is unable to resolve IM3 less than −60 dB when input SNR is low. For clarity, the approximate analysis is only shown for 1-4 bits. In general, the two tone distortion curves follow the same trends seen in Fig. 13 for monobit quantization, in which the fundamental tone shows a 1:1 slope at low input SNR while IM3 trends toward a 3:1 slope. For complex, many bit designs, it is well known that practical ADC IM3 at low input levels can be dominated by other design-specific effects [112], [113] that may not follow a 3:1 slope; these results must therefore be taken as a lower limit for ADC IM3 distortion.

For the dynamic range requirements in many RF applications, the curves in Fig. 14 indicate little IM3 advantage to increasing the number of bits beyond 4 or 5. In fact, because ADC architectures that push the limits of both resolution and sampling bandwidth tend to have practical disadvantages in terms of spurious performance and power dissipation [114], there can be a net disadvantage to needlessly increasing the number of ADC bits used in a wideband digital receiver.

On the other hand, Fig. 14 does show a significant performance disadvantage for <4 bit ADCs at high input SNR. The experimental results shown in Fig. 15 illustrate the issue. Two Tektronix AFG3102C arbitrary function generators are used to produce a pair of phase locked, equal amplitude tones at 60 and 70 MHz in Gaussian white noise, each tone individually having 20 dB input SNR. The resulting

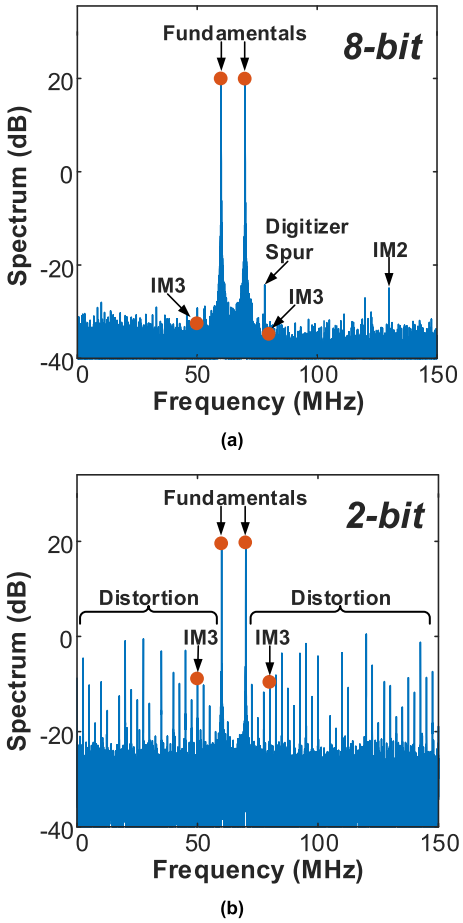

FIGURE 15. Measured two tone distortion test in which fundamental tones at 60 and 70 MHz in Gaussian white noise with 20 dB input SNR are digitized, resulting in IM3 products at 50 and 80 MHz. (a) At 8-bit resolution, the IM3 products are below the noise floor; a digitizer spur and IM2 term are visible. (b) At 2-bit resolution, IM3 and numerous correlated distortion products are observed above the noise floor; the digitizer spur is below the noise floor.

waveform is digitized at −15 dBFS using the same digitizer settings described for the measurements in Section IV. Fig. 15 shows the 20,000 point FFT of the received data at 8 bit and 2 bit resolution. For the 8 bit case, although the expected IM3 products at 50 and 80 MHz are below the noise floor, a digitizer spur is visible at 78 MHz as well as a second order intermodulation product (IM2) at the sum of the fundamental frequencies. At 2 bit resolution, strong IM3 products appear as well as numerous related distortion products at a 2.5 MHz spacing; the digitizer spur is below the quantization noise floor.

Fig. 15 thus underscores the need to consider the impact of in-band blockers on the dynamic range of few bit ADCs. Before selecting a few bit ADC for use in an RF receiver, two tone intermodulation distortion must be simulated for the case of the maximum anticipated blocker level, a scenario examined infrequently in recent literature [23], [24], [18], [46]–[56], [56]–[76]. For well regulated applications such as GPS and radio astronomy [3]–[8], or for deep space communications [22], blockers may not be

a driving concern, but in many other scenarios, ADC intermodulation distortion should be carefully considered.

VI. CONCLUSIONS

This paper has developed practical guidance for the use of few bit ADCs in general RF systems. An approximate analytic model was developed to describe the SNDR of a multibit ADC using the simplifying assumption of a sinusoid in Gaussian white noise. This model was compared with the exact analytic model for a monobit ADC and with measurement and exhaustive time domain simulation for multibit ADCs. Parametric analysis independent of sampling considerations has demonstrated several key findings:

1. Although the classical relationship for ADC dynamic range states that output SNDR increases by about 6.02 dB/bit for sinusoidal input, this rule of thumb is only approximate for <4 bits and largely invalid for the quantization of low SNR input signals.
2. At low input SNR, ADC output SNDR varies linearly with input SNR.
3. At low input SNR, the degradation due to quantization noise (i.e., the difference between input SNR and output SNDR) decreases from about 2 dB when using 1 quantization bit to approximately 0 dB for >3 bits.
4. Two tone intermodulation distortion is a significant issue for ADCs with <4 bits operating in the presence of strong in band blockers, and should be evaluated for the case of the maximum anticipated blocker level.

These results, which are independent of system-specific signal processing considerations, are useful for optimizing the number of bits in RF receiver applications and should facilitate cross disciplinary dialog within development teams encompassing both RF and digital designers.

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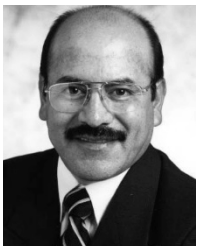

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