

# Minimax and WLS Designs of Digital FIR Filters Using SOCP for Aliasing Errors Reduction in BI-DAC

XING YANG<sup>ID</sup>, HOUJUN WANG, KE LIU<sup>ID</sup>, AND YINDONG XIAO

School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China

Corresponding author: Ke Liu (liuke@uestc.edu.cn)

This work was supported by the National Natural Science Foundation of China under Grant 61671114 and Grant 61871089.

**ABSTRACT** This paper presented the optimal minimax and weighted least squares (WLS) methods for designing digital finite impulse response (FIR) filters to reduce the aliasing errors generated by the non-ideality of analog filters and mixers in bandwidth interleaving digital-to-analog converter (BI-DAC). To satisfy the given expected spurious free dynamic range (SFDR), we formulated these optimal designs of digital FIR filters in BI-DAC as a convex optimization problem—second-order cone programming (SOCP) that allowed the linear equality and convex quadratic inequality constraints including the magnitude flatness and the peak aliasing errors constraints to be merged. Furthermore, we derived the computational complexity of our presented optimal design. Several design examples were given to evaluate the performance of our presented unconstrained and constrained minimax and WLS designs using SOCP including their effectiveness and computational complexity. The simulation results showed that, in our presented unconstrained minimax and WLS designs using SOCP, the maximum distortion errors were all around 0.02 dB. The maximum aliasing errors were  $-73.9$  and  $-80.5$  dB, which satisfied the expected SFDR of a 12-bit BI-DAC system. In addition, we analyzed the influence of different values of the nonnegative weighting function on our presented unconstrained minimax and WLS designs using SOCP, and we found that there was a tradeoff among the nonnegative weighting function's value, and the distortion and aliasing errors. Moreover, when the constraints were imposed in our presented constrained minimax and WLS designs using SOCP in the selected frequency bands, the distortion errors were equal to zero and the aliasing errors were reduced below  $-110$  dB, but the expense was that the larger distortion and aliasing errors achieved out of these selected frequency bands. Finally, we gave the computational complexity comparisons among our presented unconstrained and constrained minimax and WLS design using SOCP, we also compared the influence of the digital FIR filters' length on our presented designs' worst-case passband ripple and stopband roll-off, and we found that there was a tradeoff among the digital FIR filters' length, the passband ripple, the stopband roll-off, the computational complexity, and the actual hardware cost.

**INDEX TERMS** Minimax and weighted least squares (WLS) designs, digital FIR filter, second-order cone programming (SOCP), aliasing errors reduction, linear equality and convex quadratic inequality constraints.

## I. INTRODUCTION

Digital-to-analog converter (DAC) [1] is the key component of software defined radio (SDR) such as communication and radar systems [2]. As one of important specifications of DAC, the output bandwidth of DAC limits that of the SDR system. To achieve high bandwidth output in the SDR system, Time interleaving (TI) method [3], [4], with paralleling multiple sub-DACs, was proposed to increase the sampling rate for achieve high output bandwidth in TI-DAC, but the output

bandwidth of TI-DAC was still limited by the zero-hold (ZOH) characteristic of each sub-DAC.

Bandwidth interleaving (BI) DAC [5]–[11], not affected by the ZOH characteristic of each sub-DAC, could be also used as the other method to break through the DAC output bandwidth limitation such that the available signal bandwidth can be increased. Fig. 1 shows an architecture of BI-DAC with  $M$  sub-DACs, the bandwidth of the BI-DAC analog wide-band output  $y(t)$  is increased  $M$  times each sub-DAC output

bandwidth. Nevertheless, various different errors existed in BI-DAC including time delay error because of the length difference between different sub-channels, phase offset caused by the local oscillator signal nonzero initial phase, and all aliasing errors generated from the non-ideality of analog filters and mixers. The BI-DAC analog output  $y(t)$  can be deteriorated because of these errors. Therefore, it is very important for BI-DAC to reduce these errors. In [5], time delay error and phase offset were simultaneously estimated based on the auto-power spectrum of the wideband output of BI-DAC, and then these two errors were simultaneously reduced using digital predistortion (DPD) technique. In [6], the aliasing errors generated from the non-ideality of analog mixers in BI-DAC, were reduced by DPD technique. However, how to reduce the aliasing errors generated from the non-ideality of analog filters in BI-DAC did not be described in [6]. The calibration matrix [7] and the additional digital filters [8] were, respectively, used to reduce the aliasing errors generated from the non-ideality of analog filters in BI-DAC, but the computational demands and the realization complexity were all increased.

We can know from [11], in a BI-DAC with  $M$  sub-DACs shown in Fig.1, digital finite impulse response (FIR) filters  $F_m(z)$ ,  $m = 1, \dots, M$  can be designed using different optimal methods for reducing the aliasing errors generated from the non-ideality of analog mixers and filters. In [11], all aliasing errors reduction were achieved by the optimal design of digital FIR filters in minimax sense utilizing linear programming (LP) in BI-DAC. As the contrary structure of BI-DAC, in BI analog-to-digital converter (ADC), biconjugate gradient stabilized algorithm was used to design digital FIR filters to reduce the aliasing errors generated from the non-ideality of analog mixers and filters [12]. It is common knowledge that, whether in BI-DAC or BI-ADC, if we fix and design one of the digital and analog filters bank at first, the other filters bank can be designed using different optimization methods. Consequently, the optimal design in BI-ADC, which was proposed in [12], is suitable for BI-DAC as well. Whereas we can know from [11] that, comparing with the optimal minimax design proposed in [11], the optimal design in [12] achieved worse aliasing errors reduction and larger computational complexity.

Except in BI-DAC or BI-ADC, the optimal design of digital infinite impulse response (IIR) and FIR filters had been made active research in other research areas [13]–[20]. In [15], a complicated-guided weighted least squares (WLS) method was presented to design the variable fractional-delay (VFD) FIR filters. In [17], all pass digital VFD filters were designed for minimizing the largest absolute phase error by utilizing an iterative WLS method. In [20], a high-accuracy low-complexity digital VFD filters were designed for minimizing the largest absolute error of the digital VFD filter's variable frequency response (VFR) in minimax sense utilizing a simple LP technique. The former WLS design could achieve a lower total error energy of VFR, while the latter minimax design had lower computational complexity.

In comparison with LP which is a conventional optimization problem [20], [21], second-order cone programming (SOCP) [22]–[26], which is a convex optimization problem, can allow some different constraints to be merged. Therefore, SOCP has been widely used for the optimal designs of digital IIR and FIR filters. In [25], an optimal minimax design of digital IIR filters was proposed by utilizing an iterative SOCP. Additionally, in [26], a minimax design of even-order digital FIR VFD filters was presented for minimizing the VFR's peak error utilizing SOCP. In these different papers, all of their authors did not be taken into count for the realization of the optimal design of digital FIR filters in BI-DAC. While these paper still had their own advantages so that they were of reference significance for the research about different optimal designs in BI-DAC.

The principle objective of this paper was to present efficient minimax and WLS methods for designing the digital FIR filters such that all aliasing errors could be reduced in BI-DAC. We firstly opted Butterworth filters as the analog low pass and bandpass filters that were utilized to eliminate the images of each sub-DAC's output and the unwanted sidebands generated from an analog up-conversion, respectively. And then we opted digital FIR filters to split the digital broadband input signal of BI-DAC into multiple digital sub-band signals. The optimal design of digital FIR filters in minimax sense and WLS error sense, were formulated as an SOCP problem that could be effectively utilized to calculate the optimum coefficients vector of these digital FIR filters. Further, SOCP allows the linear equality and convex quadratic inequality constraints to be incorporated in our presented minimax and WLS designs. Therefore, our presented optimal design using SOCP can provide greater flexibility in design goals including these design constraints such as the magnitude flatness on the BI-DAC output and the peak restrictions on the aliasing errors constraints. The minimax and WLS designs using SOCP with or without constraints are of much importance for the optimal design of digital FIR filters since the aliasing errors can be reduced lower than a given level such that the accuracy of BI-DAC in terms of spurious free dynamic range (SFDR) can be easily controlled. It can be known from [11] that, SFDR is defined as the ratio of the root mean square (RMS) amplitude of the largest signal component to the RMS value of the next-largest distortion component, and it is an important measurement of the DAC accuracy [27].

In summary, our main contributions are listed as follows:

- (1) In the particular context of BI-DAC, the optimal minimax and WLS designs of digital FIR filters using SOCP were presented to reduce all aliasing errors generated from the non-ideality of analog mixers and filters.
- (2) The description of minimax and WLS designs using SOCP with or without the linear equality and convex quadratic inequality constraints was presented in detail. Additionally, we deduced the computational complexity of our presented minimax and WLS designs using

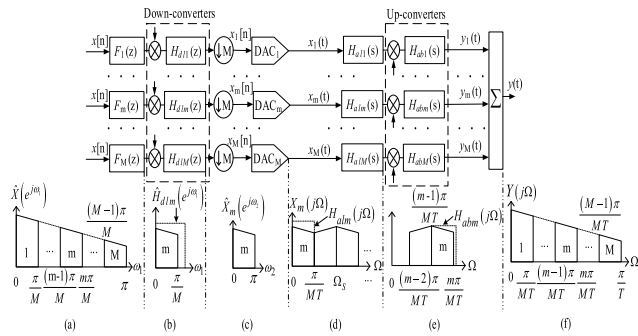


FIGURE 1. Architecture of a BI-DAC with  $M$  sub-DACs.

SOCP with or without the linear equality and convex quadratic inequality constraints.

- (3) Multiple design examples were, respectively, used to verify the performance of our presented optimal design such as the effectiveness of the unconstrained and constrained minimax and WLS designs using SOCP, and the influence of different values of the nonnegative weighting function on our presented unconstrained minimax and WLS design using SOCP. Further, we compared the computational complexity among our presented unconstrained and constrained minimax and WLS design using SOCP, the optimal designs in [11] and [12]. Finally, we verified the influence of the digital FIR length on the worst-case passband ripple and stopband roll-off of our presented unconstrained minimax and WLS design using SOCP, the optimal designs in [11] and [12]. The simulation results showed that, our presented optimal designs were more effective for the aliasing errors reduction than the optimal designs in [11] and [12], and there was a trade-off among the nonnegative weighting function's value, the distortion and aliasing errors or among the digital FIR filters' length, the passband ripple, the stopband roll-off, the computational complexity and the actual hardware cost.

**II. ACTUAL TRANSFER FUNCTION OF BANDWIDTH INTERLEAVING DIGITAL-TO-ANALOG CONVERTER**

The idea of BI-DAC is to digitally split a digital broadband input into several digital sub-band signals and complete the digital down-conversion, and then perform the digital-to-analog conversion in different lower-bandwidth sub-DACs. These sub-DACs' outputs are then up-converted and yielded together to obtain an analog wideband output signal. Fig.1 shows an architecture of a BI-DAC with  $M$  sub-DACs, where the bandwidth and the sampling rate of the BI-DAC system are, respectively, assumed to be  $\frac{\pi}{T}$  and  $\frac{1}{T}$ . The sampling rate of each sub-DAC is  $\frac{1}{MT}$ .

From Fig.1 and the principle of a BI-DAC with  $M$  sub-DACs illustrated in [11], we can get the frequency

response of the  $m$ th sub-DAC's output  $x_m(t)$  as

$$\begin{aligned}
 X_m(j\Omega) &= \frac{1}{MT} \sum_{k=-\infty}^{+\infty} \hat{X}_m \left( e^{j(\Omega MT - 2\pi k)} \right) H(j\Omega) \\
 &= \frac{1}{MT} \sum_{k=-\infty}^{+\infty} \hat{X} \left( e^{j\left(\Omega T - \frac{2\pi k}{M}\right) + \frac{(m-1)\pi}{M}} \right) H(j\Omega) \\
 &\quad \times \hat{F}_m \left( e^{j\left(\Omega T - \frac{2\pi k}{M}\right) + \frac{(m-1)\pi}{M}} \right) \hat{H}_{dlm} \left( e^{j\left(\Omega T - \frac{2\pi k}{M}\right)} \right)
 \end{aligned} \tag{1}$$

where  $\Omega = \frac{\omega_1}{T} = \frac{\omega_2}{MT}$ . Further,  $\hat{X}(e^{j\omega_1})$ ,  $\hat{X}_m(e^{j\omega_2})$ ,  $H(j\Omega)$ ,  $\hat{F}_m(e^{j\omega_1})$  and  $\hat{H}_{dlm}(e^{j\omega_1})$  are, respectively, the frequency responses of the digital wideband input signal  $x[n]$ , the  $m$ th sub-DAC input  $x_m[n]$ , the  $m$ th sub-DAC preserving function, the  $m$ th digital FIR filter  $F_m(z)$  and the  $m$ th digital low pass filter (LPF)  $H_{dlm}(z)$ . Then, the images in  $x_m(t)$  and the unwanted sidebands introduced by the analog up-conversion are, respectively, eliminated using the  $m$ th analog LPF  $H_{alm}(s)$  and the  $m$ th analog bandpass filter (BPF)  $H_{abm}(s)$ . So the frequency response of the  $m$ th sub-channel analog output  $y_m(t)$  can be written as

$$\begin{aligned}
 Y_m(j\Omega) &= \frac{1}{MT} \sum_{k=-\infty}^{+\infty} \hat{X} \left( e^{j\left(\Omega T - \frac{2\pi k}{M}\right)} \right) \\
 &\quad \times \hat{F}_m \left( e^{j\left(\Omega T - \frac{2\pi k}{M}\right)} \right) \hat{H}_{dlm} \left( e^{j\left(\Omega T - \frac{2\pi k}{M}\right) - \frac{(m-1)\pi}{M}} \right) \\
 &\quad \times H \left( j \left( \Omega - \frac{(m-1)\pi}{MT} \right) \right) \\
 &\quad \times H_{alm} \left( j \left( \Omega - \frac{(m-1)\pi}{MT} \right) \right) H_{abm}(j\Omega), \tag{2}
 \end{aligned}$$

where  $H_{alm}(j\Omega)$  and  $H_{abm}(j\Omega)$  are the frequency response of  $H_{alm}(s)$  and  $H_{abm}(s)$ . As mentioned in [11], the analog wideband signal  $y(t)$  can be yielded by summing all of the sub-channel output  $y_m(t)$ ,  $m = 1, \dots, M$ , that is described in the frequency domain as

$$\begin{aligned}
 Y(j\Omega) &= \sum_{m=1}^M Y_m(j\Omega) \\
 &= \frac{1}{MT} \sum_{m=1}^M \sum_{k=-\infty}^{+\infty} \hat{X} \left( e^{j\left(\Omega T - \frac{2\pi k}{M}\right)} \right) \\
 &\quad \times \hat{F}_m \left( e^{j\left(\Omega T - \frac{2\pi k}{M}\right)} \right) \hat{H}_{dlm} \left( e^{j\left(\Omega T - \frac{2\pi k}{M}\right) - \frac{(m-1)\pi}{M}} \right) \\
 &\quad \times H \left( j \left( \Omega - \frac{(m-1)\pi}{MT} \right) \right) \\
 &\quad \times H_{alm} \left( j \left( \Omega - \frac{(m-1)\pi}{MT} \right) \right) H_{abm}(j\Omega) \\
 &= \sum_{k=-\infty}^{+\infty} \hat{X} \left( e^{j\left(\Omega T - \frac{2\pi k}{M}\right)} \right) T_k(j\Omega), \tag{3}
 \end{aligned}$$

where  $Y(j\Omega)$  denotes the frequency response of  $y(t)$ , and  $\Omega \in [0, \frac{\pi}{T}]$ .  $T_k(j\Omega)$  is the actual transfer function of this

BI-DAC with  $M$  sub-DACs, which can be written as follow

$$T_k(j\Omega) = \frac{1}{MT} \sum_{m=1}^M \hat{F}_m \left( e^{j(\Omega T - \frac{2\pi k}{M})} \right) \times \hat{H}_{dlm} \left( e^{j(\Omega T - \frac{2\pi k}{M}) - \frac{(m-1)}{M}\pi} \right) \times H \left( j \left( \Omega - \frac{(m-1)}{MT} \pi \right) \right) \times H_{alm} \left( j \left( \Omega - \frac{(m-1)}{MT} \pi \right) \right) H_{abm}(j\Omega). \quad (4)$$

### III. MINIMAX AND WLS DESIGN OF DIGITAL FIR FILTER USING SOCP

In this section, we firstly decompose the optimal design of digital FIR filters into a pair of separate optimal designs (minimax and WLS designs) that can be easily solved using SOCP. Then, the linear equality and convex quadratic inequality constraints are merged into the minimax and WLS designs using SOCP to meet some requirements. Ultimately, we deduce the computational complexity of our presented minimax and WLS designs using SOCP.

#### A. MINIMAX AND WLS DESIGNS USING SOCP

Due to the advantages of Butterworth filters as described in [11], we also opt second-order Butterworth filters as analog LPFs and BPFs which are, respectively, utilized to eliminate the images of each sub-DAC output and the unwanted sidebands generated from an analog up-conversion.

For easy understanding of the optimal design formulation, we begin from the ideal and actual transfer functions of this BI-DAC with  $M$  sub-DACs with the terms  $k = 0, \dots, M-1$ . Where,  $T_0(j\Omega)$  represents the distortion function denoting the magnitude gain and group delay of this BI-DAC with  $M$  sub-DACs,  $T_k(j\Omega)$ ,  $k = 1, \dots, M-1$  represents the aliasing functions denoting the shifted and unwanted editions of digital wideband input which must perfectly be eliminated, and (3) can be rewritten as

$$Y(j\Omega) = \sum_{k=0}^{M-1} \hat{X} \left( e^{j(\Omega T - \frac{2\pi k}{M})} \right) T_k(j\Omega) = \sum_{k=0}^{M-1} \hat{X} \left( e^{j(\Omega T - \frac{2\pi k}{M})} \right) \frac{1}{MT} \sum_{m=1}^M \hat{F}_m \left( e^{j(\Omega T - \frac{2\pi k}{M})} \right) \times \hat{H}_{dlm} \left( e^{j(\Omega T - \frac{2\pi k}{M}) - \frac{(m-1)}{M}\pi} \right) \times H \left( j \left( \Omega - \frac{(m-1)}{MT} \pi \right) \right) \times H_{alm} \left( j \left( \Omega - \frac{(m-1)}{MT} \pi \right) \right) H_{abm}(j\Omega). \quad (5)$$

Consequently, the analog wideband output signal  $Y(j\Omega)$  is a hybrid of the frequency-shifting editions of the digital broadband input signal  $\hat{X}(e^{j\omega_1})$ . Additionally, we can know from [11] that, when all of analog filters and mixers are ideal

in BI-DAC, the ideal transfer function of this  $M$ -channel BI-DAC can be written as

$$D_k(j\Omega) = \begin{cases} ce^{-j\Omega T d}, & k = 0 \\ 0, & k = 1, \dots, M-1, \end{cases} \quad \Omega \in \left[ 0, \frac{\pi}{T} \right] \quad (6)$$

where  $c$  and  $d$  are, respectively, a nonzero constant and the delay parameter of this BI-DAC with  $M$  sub-DACs. As a result, the approximation error can be obtained from the difference between (4) and (6) as

$$e_k(\Omega) = T_k(j\Omega) - D_k(j\Omega) \quad (7)$$

In this BI-DAC with  $M$  sub-DACs, if all of analog mixers, analog LPFs and BPFs are ideal, an ideal analog wideband output signal  $Y(j\Omega)$  without the aliasing errors will be obtained, namely,  $e_k(\Omega) = 0$  for  $k = 1, \dots, M-1$ . Otherwise the aliasing errors will be generated from the non-ideality of analog mixers, analog LPFs and BPFs. To reduce these aliasing errors, we should minimize the approximation error  $e_k(\Omega)$  by using the optimal design of digital FIR filters.

The  $m$ th digital FIR filter  $F_m(z)$  is assumed to be an  $N$ -tap FIR filter, its  $z$ -transform is shown as [11]

$$F_m(z) = \sum_{n=0}^{N-1} f_m(n) z^{-n}, \quad (8)$$

such that we obtain

$$\hat{F}_m \left( e^{j(\Omega T - \frac{2\pi k}{M})} \right) = \sum_{n=0}^{N-1} f_m(n) e^{-j(\Omega T - \frac{2\pi k}{M})n} = f_m^T [c_k(\Omega) - j s_k(\Omega)], \quad (9)$$

where  $f_m(n)$ ,  $n = 0, \dots, N-1$  are the coefficients of the  $m$ th digital FIR filter which should be computed, and

$$f_m = [f_m(0), f_m(1), \dots, f_m(N-1)]^T \quad (10a)$$

$$c_k(\Omega) = \left[ 1, \cos \left( \Omega T - \frac{2\pi k}{M} \right), \dots, \cos(N-1) \left( \Omega T - \frac{2\pi k}{M} \right) \right]^T \quad (10b)$$

$$s_k(\Omega) = \left[ 0, \sin \left( \Omega T - \frac{2\pi k}{M} \right), \dots, \sin(N-1) \left( \Omega T - \frac{2\pi k}{M} \right) \right]^T \quad (10c)$$

Using this digital FIR filter, the actual transfer function of this BI-DAC with  $M$  sub-DACs can be rewritten as

$$T_k(j\Omega) = \sum_{m=1}^M f_m^T r_{k,m}(\Omega) - j \sum_{m=1}^M f_m^T i_{k,m}(\Omega) = r_k^T(\Omega) f - j i_k^T(\Omega) f = \text{Re}\{T_k(j\Omega)\} - j \text{Im}\{T_k(j\Omega)\}, \quad (11)$$

where

$$f = [f_1^T, f_2^T, \dots, f_M^T]^T \quad (12a)$$

$$Re \{T_k(j\Omega)\} = r_k^T(\Omega)f \quad (12b)$$

$$Im \{T_k(j\Omega)\} = i_k^T(\Omega)f \quad (12c)$$

$$r_k(\Omega) = [r_{k,1}^T(\Omega), r_{k,2}^T(\Omega), \dots, r_{k,M}^T(\Omega)]^T \quad (12d)$$

$$i_k(\Omega) = [i_{k,1}^T(\Omega), i_{k,2}^T(\Omega), \dots, i_{k,M}^T(\Omega)]^T \quad (12e)$$

$$r_{k,m}(\Omega) = \frac{1}{MT} c_k(\Omega) \hat{H}_{dlm} \left( e^{j(\Omega T - \frac{2\pi k}{M}) - \frac{(m-1)\pi}{M}} \right) \times H_{abm}(j\Omega) H \left( j \left( \Omega - \frac{(m-1)\pi}{MT} \right) \right) \times H_{alm} \left( j \left( \Omega - \frac{(m-1)\pi}{MT} \right) \right) \quad (12f)$$

$$i_{k,m}(\Omega) = \frac{1}{MT} s_k(\Omega) \hat{H}_{dlm} \left( e^{j(\Omega T - \frac{2\pi k}{M}) - \frac{(m-1)\pi}{M}} \right) \times H_{abm}(j\Omega) H \left( j \left( \Omega - \frac{(m-1)\pi}{MT} \right) \right) \times H_{alm} \left( j \left( \Omega - \frac{(m-1)\pi}{MT} \right) \right). \quad (12g)$$

Here,  $Re \{\bullet\}$  and  $Im \{\bullet\}$  can be, respectively, used to return the real and imaginary components of a complex number or a vector.

According to the aforementioned derivations, the approximation error can be rewritten as

$$e_k(\Omega) = [r_k^T(\Omega)f - R_k^D(\Omega)] - j [i_k^T(\Omega)f - I_k^D(\Omega)] = Re \{e_k(\Omega)\} - j Im \{e_k(\Omega)\} \quad (13)$$

where

$$R_k^D(\Omega) = Re \{D_k(\Omega)\} \quad (14a)$$

$$I_k^D(\Omega) = Im \{D_k(\Omega)\} \quad (14b)$$

### 1) MINIMAX DESIGN USING SOCP

To reduce all aliasing errors generated from the non-ideality of analog mixers and filters, we should make the approximation error  $e_k(\Omega)$ ,  $k = 0, \dots, M - 1$  approximate zero in minimax sense, and the minimax problem is solved as follow

$$\arg \min \{ \max (W_k(\Omega) |e_k(\Omega)|) \}, \quad \Omega \in \Omega_I, \quad k = 0, \dots, M - 1f \quad (15)$$

where  $W_k(\Omega)$  is a nonnegative weighting function that is used to specify the relative significance between the distortion error and the aliasing errors,  $\Omega_I$  is the largest output bandwidth of this BI-DAC with  $M$  sub-DACs and  $\Omega_I = [0, \frac{\pi}{T}]$ . The objective in (15) can be written as follows

$$\begin{aligned} & W_k(\Omega) |e_k(\Omega)| \\ &= W_k(\Omega) |T_k(j\Omega) - D_k(j\Omega)| \\ &= W_k(\Omega) \left\| \begin{bmatrix} r_k^T(\Omega)f - R_k^D(\Omega) \\ i_k^T(\Omega)f - I_k^D(\Omega) \end{bmatrix} \right\|_2 \\ &= W_k(\Omega) \sqrt{(r_k^T(\Omega)f - R_k^D(\Omega))^2 + (i_k^T(\Omega)f - I_k^D(\Omega))^2} \\ &= \sqrt{(R_k^W(\Omega))^2 + (I_k^W(\Omega))^2}, \end{aligned} \quad (16)$$

where  $\|\bullet\|_2$  denotes the two-or Euclidean norm of a vector, and

$$R_k^W(\Omega) = W_k(\Omega) (r_k^T(\Omega)f - R_k^D(\Omega)) \quad (17a)$$

$$I_k^W(\Omega) = W_k(\Omega) (i_k^T(\Omega)f - I_k^D(\Omega)) \quad (17b)$$

Consequently, the minimax problem in (15) can be reformulated as

$$\begin{aligned} & \min_{\delta} f \\ & \text{subject to } \delta \geq \sqrt{(R_k^W(\Omega))^2 + (I_k^W(\Omega))^2} \end{aligned} \quad (18)$$

Here,  $\delta$  is used to calculate the optimum coefficients in  $f$  according to the constraint condition. In  $\Omega_I = [0, \frac{\pi}{T}]$ , we discretize the continuous frequency variable  $\Omega$  into a serried cluster of frequency points  $\{\Omega_i, 1 \leq i \leq P_L\}$ .  $P_L$  is the number of the discretized frequency point  $\Omega_i$ .  $\Omega_i$  is uniformly distributes in the frequency band  $\Omega_I$ . Therefore, the constraints in (18) become  $\delta \geq [(R_k^W(\Omega_i))^2 + (I_k^W(\Omega_i))^2]^{\frac{1}{2}}$

Assuming that  $c = [1, O_{NM}]^T$ ,  $O_{NM}$  represents a  $l$ -by- $NM$  matrix of zeros.  $x = [\delta, f^T]^T$ ,  $F_{k,i} = W_k(\Omega_i) \begin{bmatrix} 0, r_k^T(\Omega_i) \\ 0, i_k^T(\Omega_i) \end{bmatrix}$ ,  $g_{k,i} = W_k(\Omega_i) \begin{bmatrix} R_k^D(\Omega_i) \\ I_k^D(\Omega_i) \end{bmatrix}$ . Then, (18) is recast as a SOCP problem, which can be solved using a standard SOCP solver as follows

$$\begin{aligned} & \min_x c^T x \\ & \text{subject to } c^T x \geq \|F_{k,i}x - g_{k,i}\|_2 \end{aligned} \quad (19)$$

### 2) WLS DESIGN USING SOCP

In addition to the minimax design, the optimum coefficients vector  $f$  can be found by minimizing the sum of all weighted squared approximation errors' integrals

$$J(f) = \sum_{k=0}^{M-1} \int_{\Omega_I} W_k(\Omega) |e_k(\Omega)|^2 d\Omega \quad (20)$$

Expanding (20), we obtain

$$\begin{aligned} J(f) &= \sum_{k=0}^{M-1} \int_{\Omega_I} W_k(\Omega) e_k(\Omega) e_k^*(\Omega) d\Omega \\ &= \sum_{k=0}^{M-1} \int_{\Omega_I} W_k(\Omega) (Re \{e_k(\Omega)\} - j Im \{e_k(\Omega)\}) \times (Re \{e_k(\Omega)\} + j Im \{e_k(\Omega)\}) d\Omega \\ &= \sum_{k=0}^{M-1} \int_{\Omega_I} W_k(\Omega) \left[ (r_k^T(\Omega)f - R_k^D(\Omega))^2 + (i_k^T(\Omega)f - I_k^D(\Omega))^2 \right] d\Omega \\ &= \sum_{k=0}^{M-1} \int_{\Omega_I} W_k(\Omega) \{f^T [r_k(\Omega) r_k^T(\Omega) + i_k(\Omega) i_k^T(\Omega)] f\} \end{aligned}$$

$$-2f^T \left[ r_k(\Omega) R_k^D(\Omega) + i_k(\Omega) I_k^D(\Omega) \right] + \left[ \left( R_k^D(\Omega) \right)^2 + \left( I_k^D(\Omega) \right)^2 \right] d\Omega, \quad (21)$$

and then (21) can also be rewritten as

$$J(f) = f^T S f - 2f^T v + p = \left\| S^{\frac{1}{2}} f - S^{-\frac{1}{2}} v \right\|_2^2 - \left( v^T S^{-1} v - p \right), \quad (22)$$

where

$$S = \sum_{k=0}^{M-1} \int_{\Omega_l} W_k(\Omega) \left[ r_k(\Omega) r_k^T(\Omega) + i_k(\Omega) i_k^T(\Omega) \right] d\Omega \quad (23a)$$

$$v = \sum_{k=0}^{M-1} \int_{\Omega_l} W_k(\Omega) \left[ r_k(\Omega) R_k^D(\Omega) + i_k(\Omega) I_k^D(\Omega) \right] d\Omega \quad (23b)$$

$$p = \sum_{k=0}^{M-1} \int_{\Omega_l} W_k(\Omega) \left[ \left( R_k^D(\Omega) \right)^2 + \left( I_k^D(\Omega) \right)^2 \right] d\Omega \quad (23c)$$

The WLS design (22) becomes the SOCP problem as follows

$$\begin{aligned} \min_x \quad & c^T x \\ \text{subject to} \quad & c^T x \geq \left\| \tilde{S}x - \tilde{v} \right\|_2 \end{aligned} \quad (24)$$

where  $\tilde{S} = \left[ O_{NM}^T, S^{\frac{1}{2}} \right]$  and  $\tilde{v} = S^{-\frac{1}{2}} v$ .

It well known that, the effective software *SeDuMi* [28] can be used to solve (19) and (24), which utilizes a primal-dual interior-point algorithm called centering-predictor-corrector method.

As mentioned in Section I, SFDR is used to evaluate the performance of each sub-DAC in BI-DAC, and the expected SFDR can be computed as [11]

$$SFDR \text{ (dB)} = 6.02 \times SFDR_{bits} \quad (25)$$

where  $SFDR_{bits}$  is the resolution of BI-DAC. For a given  $SFDR_{bits}$  in BI-DAC, our presented minimax and WLS design using SOCP is used to reduce the distortion error to 0 dB and the aliasing errors lower than the expected SFDR.

## B. PRESENTED OPTIMAL DESIGN WITH CONSTRAINTS

### 1) LINEAR EQUALITY CONSTRAINTS

At certain frequency points of a low-frequency band, the magnitude flatness of the distortion function is sometimes desirable, which can be formulated as a linear equality constraint in our presented minimax and WLS designs using SOCP. The relationship between the derivatives of the frequency response of our presented minimax and WLS design using SOCP and its ideal counterparts is considered as follows

$$\left. \frac{d^i T_o(j\Omega)}{dz^i} \right|_{\Omega=\hat{\Omega}} = \left. \frac{d^i D_o(j\Omega)}{dz^i} \right|_{\Omega=\hat{\Omega}}, \quad i = 0, \dots, P_L - 1 \quad (26)$$

It can be known from (18) that the digital FIR filters in BI-DAC must be designed for approximating the expected frequency response at  $\Omega = \hat{\Omega}$  up to the  $(P_L - 1)$ th order. To merge the magnitude flatness with the  $(P_{\hat{\Omega}} - 1)$ th order

into  $T_0(j\Omega)$  at frequency  $\hat{\Omega}d$ , we obtain the equation as

$$\begin{aligned} & \frac{1}{MT} \sum_{m=1}^M \sum_{n=0}^{N-1} \hat{H}_{dlm} \left( e^{j \left( \hat{\Omega}d T - \frac{2\pi k}{M} \right) - \frac{(m-1)}{M} \pi} \right) \\ & \times H \left( j \left( \hat{\Omega}d - \frac{(m-1)}{MT} \pi \right) \right) H_{alm} \\ & \times \left( j \left( \hat{\Omega}d - \frac{(m-1)}{MT} \pi \right) \right) \\ & \times H_{abm} \left( j \hat{\Omega}d \right) (n-d)^q f_m(n) e^{-j \left( \hat{\Omega}d T - \frac{2\pi k}{M} \right) (n-d)} \\ & = \begin{cases} c, & q = 0 \\ 0, & q = 1, \dots, P_{\hat{\Omega}d} - 1. \end{cases} \end{aligned} \quad (27)$$

which can be also rewritten as

$$L_{\hat{\Omega}d} f = d_{\hat{\Omega}d} \quad (28)$$

where

$$\begin{aligned} l_{\hat{\Omega}d, q}^m = & \left[ \frac{1}{MT} \hat{H}_{dlm} \left( e^{j \left( \hat{\Omega}d T - \frac{2\pi k}{M} \right) - \frac{(m-1)}{M} \pi} \right) \right. \\ & \times H \left( j \left( \hat{\Omega}d - \frac{(m-1)}{MT} \pi \right) \right) \\ & \times H_{alm} \left( j \left( \hat{\Omega}d - \frac{(m-1)}{MT} \pi \right) \right) \\ & \times H_{abm} \left( j \hat{\Omega}d \right) (0-d)^q e^{-j \left( \hat{\Omega}d T - \frac{2\pi k}{M} \right) (0-d)} \\ & , \dots, \frac{1}{MT} \hat{H}_{dlm} \left( e^{j \left( \hat{\Omega}d T - \frac{2\pi k}{M} \right) - \frac{(m-1)}{M} \pi} \right) \\ & \times H \left( j \left( \hat{\Omega}d - \frac{(m-1)}{MT} \pi \right) \right) \\ & \times H_{alm} \left( j \left( \hat{\Omega}d - \frac{(m-1)}{MT} \pi \right) \right) \\ & \left. \times H_{abm} \left( j \hat{\Omega}d \right) (N-1-d)^q e^{-j \left( \hat{\Omega}d T - \frac{2\pi k}{M} \right) (N-1-d)} \right] \end{aligned} \quad (29a)$$

$$L_{\hat{\Omega}d} = \left[ l_{\hat{\Omega}d, 0}^T, \dots, l_{\hat{\Omega}d, P_{\hat{\Omega}d}-1}^T \right]^T \quad (29b)$$

$$l_{\hat{\Omega}d, q}^m = \left[ l_{\hat{\Omega}d, q}^0, \dots, l_{\hat{\Omega}d, q}^{M-1} \right] \quad (29c)$$

$$d_{\hat{\Omega}d} = \left[ 1, O_{P_{\hat{\Omega}d}-1} \right] \quad (29d)$$

It can be known that, the linear equality constraints described in (28), can be easily merged in our presented minimax and WLS design using SOCP such that the desirable magnitude flatness is achieved in the low-frequency band. However, comparing with the minimax and WLS design without these constraints, a larger distortion error may be obtained out of this low-frequency band.

## 2) CONVEX QUADRATIC INEQUALITY CONSTRAINTS

Except for the constraints described in Section III-B-1), the convex quadratic inequality constraints can also be readily incorporated in our presented minimax and WLS designs using SOCP.

To illustrate the convex quadratic inequality constraints, a specified aliasing error constraint is imposed for satisfying a expected SFDR which can be obtained from (25). Assuming that the expected peaking aliasing error  $A_{peak}$  is imposing in the frequency band  $\Omega \in [\Omega_{s1}, \Omega_{s2}]$ , the peak aliasing error constraint is written as

$$|T_k(j\Omega)| \leq A_{peak}, k = 1, \dots, M-1, \Omega \in [\Omega_{s1}, \Omega_{s2}] \quad (30)$$

Similar to the minimax design using SOCP, this constraint can be rewritten as

$$A_{peak} \geq \|R_k x\|_2 \quad (31)$$

where  $R_k = \begin{bmatrix} 0, r_k^T(\Omega) \\ 0, i_k^T(\Omega) \end{bmatrix}$ . The constraints on the peak ripples which is obtained from discretizing (30), are extended to the actual constraints in (19) and (24) for our presented minimax and WLS designs using SOCP as a cluster of SOCP constraints, respectively. Imposing the convex quadratic inequality constraints in the frequency band  $[\Omega_{s1}, \Omega_{s2}]$ , the aliasing errors can be lower than a expected SFDR. However, a larger aliasing errors may be obtained out of the frequency band  $[\Omega_{s1}, \Omega_{s2}]$ .

## C. COMPUTATIONAL COMPLEXITY

It is well known that, the computational complexity of the addition and subtraction between two  $N \times N$  matrices can be regarded as a linear parallel operation with  $O(N)$ , the multiplication of the  $L \times M$  and  $M \times N$  matrices is  $O(LMN)$ , the inverse of a  $M \times M$  matrix is  $O(M^3)$ . According these above knowledge, the computational complexity of the optimal designs in [11] and [12], respectively,  $O(4P_L \times N_{D1}(NM+1))$  and  $O(N_{D2}(NM(MP_L)^3 + (1+MP_L)(NM)^2))$ , where  $N_{D1}$  and  $N_{D2}$  are, respectively, the iterations times of the optimal designs in [11] and [12].

In contrast to the optimal designs in [11] and [12], the computational complexity of our presented minimax and WLS designs using SOCP with or without the linear equality and convex quadratic inequality constraints, are deduced as list below

- (1) The minimax and WLS designs using SOCP without the linear equality and convex quadratic inequality constraints equal, respectively,  $O(MP_L N_{D3}(2NM+3))$  and  $O(N_{D4}(3M(NM)^3 + 2(NM)^2))$ , where  $N_{D3}$  and

$N_{D4}$  denote, respectively, the number of iterations of the minimax and WLS design using SOCP without these constraints.

- (2) The minimax and WLS designs using SOCP with the linear equality and convex quadratic inequality constraints are, respectively,  $O(N_{D5}(MP_L(2NM+3) + MP_{\Omega d} N_{\Omega d} + N_{\Omega}(2NM+1)))$  and  $O(N_{D6}(3M \times (NM)^3 + 2(NM)^2 + MP_{\Omega d} + (2NM+1)))$ , where  $N_{D5}$  and  $N_{D6}$  denote the iterations times of the minimax and WLS design using SOCP with these constraints, respectively.  $N_{\Omega d}$  and  $N_{\Omega}$  denote, respectively, the number of all discretized frequency points in the selected frequency band used by the minimax and WLS designs using SOCP with the linear equality and convex quadratic inequality constraints.

According to the aforementioned computational complexity, we think that the computational complexity of our presented minimax and WLS designs using SOCP are lower than that of the optimal design in [12], but larger than that of the optimal design in [11], and whether with or without constraints, our presented minimax design using SOCP has lower computational complexity than our presented WLS design using SOCP. Further, the computational complexity of our presented unconstrained minimax design using SOCP are lower than this design with constraints, as same as the comparison between our presented unconstrained and constrained WLS designs using SOCP.

$N$  - the length of digital FIR filters in BI-DAC, is an important parameter which is used to determine the performance of BI-DAC. It is common knowledge that, with  $N$  increasing, a lower distortion error deviation and a larger aliasing errors attenuation can be achieved, but at an expense of larger computational complexity and higher actual hardware cost.

## IV. DESIGN PERFORMANCE VERIFICATION AND ANALYSIS

In this section, several design examples of BI-DAC are given for verifying the performance of our presented unconstrained and constrained minimax and WLS designs using SOCP. The minimax and WLS designs using SOCP without constraints, the unconstrained minimax and WLS designs using SOCP with different values of the nonnegative weighting function, the minimax and WLS design using SOCP with the linear equality and convex quadratic inequality constraints, are both considered. Except as otherwise noted, in all of our presented BI-DAC design examples, the number of the discretized frequency points  $P_L$ , the length of digital FIR filter  $N$ , the delay parameter  $d$ , and the scale factor  $c$ , are set to 100, 60, 25 and 1, respectively.

### A. EFFECTIVENESS ANALYSIS

#### 1) EXAMPLE 1: MINIMAX AND WLS DESIGNS USING SOCP WITHOUT CONSTRAINTS

In this design example of BI-DAC, the sub-channel number  $M$ , the resolution  $SFDR_{bits}$  and the sampling rate  $f_s$  are,

respectively, set to 4, 12-bit and  $\frac{1}{T}$ .  $SFDR_{bits}$  is only used for calculating the expected SFDR of BI-DAC such that it can be set to any value and do not have any influence on the simulation results.

According to (25), the expected SFDR of BI-DAC in this design example, is  $12 \times 6.02 = 72.24dB$ . As a result, the aliasing errors must be reduced lower than  $-72.24$  dB. Then, the minimax and WLS designs using SOCP without constraints were all considered, and we opted second-order Butterworth filters as analog LPFs and BPFs in this design example. Further, the nonnegative weighting function  $W_k(\Omega)$  were set as follows

$$W_k(\Omega) = 1, \quad k = 0, 1, 2, 3, \Omega \in [0, \frac{\pi}{T}] \quad (32)$$

To evaluate the effectiveness of our presented minimax and WLS designs using SOCP without constraints, the optimal designs in [11] and [12] were carried for comparison.

Fig.2 shows the frequency responses of these four different optimal design in this design example of BI-DAC. As shown in Fig.2(a), in  $\Omega \in [0, \frac{\pi}{T}]$ , the maximum distortion error of our presented minimax and WLS designs using SOCP without constraints, and the optimal design in [11] were all approximately 0.02 dB, but the optimal design in [12] achieved a larger distortion error that was approximately 0.05 dB. As shown in Fig.2(b), the aliasing errors of our presented minimax and WLS designs using SOCP without constraints ranged, respectively, from  $-73.9$  dB to  $-108.8$  dB and from  $-80.5$  dB to  $-120.1$  dB. These aliasing errors were suppressed lower than  $-72.24$  dB in  $\Omega \in [0, \frac{\pi}{T}]$  such that they all satisfied the expected SFDR. In contrast, in  $\Omega \in [0, \frac{\pi}{T}]$ , the maximum aliasing errors of the optimal designs in [11] and [12] were  $-62.9$  dB and  $-50.6$  dB, respectively. They all could not satisfy the expected SFDR. Therefore, the relationship among the effectiveness of these four optimal designs for the aliasing errors reduction, could be sorted from the best to the worst as

$$\begin{aligned} \text{Unconstrained WLS} &> \text{Unconstrained minimax} \\ &> [11] \\ &> [12] \end{aligned} \quad (33)$$

Namely, our presented minimax and WLS designs using SOCP without constraints can achieve better aliasing errors reduction than the optimal designs in [11] and [12]. Additionally, the WLS design using SOCP without constraints has a better aliasing errors reduction than the minimax design using SOCP without constraints.

## 2) EXAMPLE 2: UNCONSTRAINED MINIMAX AND WLS DESIGNS USING SOCP WITH DIFFERENT VALUES OF NONNEGATIVE WEIGHTING FUNCTIONS

To evaluate the influence of the nonnegative weighting functions  $W_k(\Omega)$ ,  $k = 0, 1, 2, 3$  on our presented optimal designs, the unconstrained minimax and WLS designs using SOCP with different values of  $W_k(\Omega)$ ,  $k = 0, 1, 2, 3$  are all

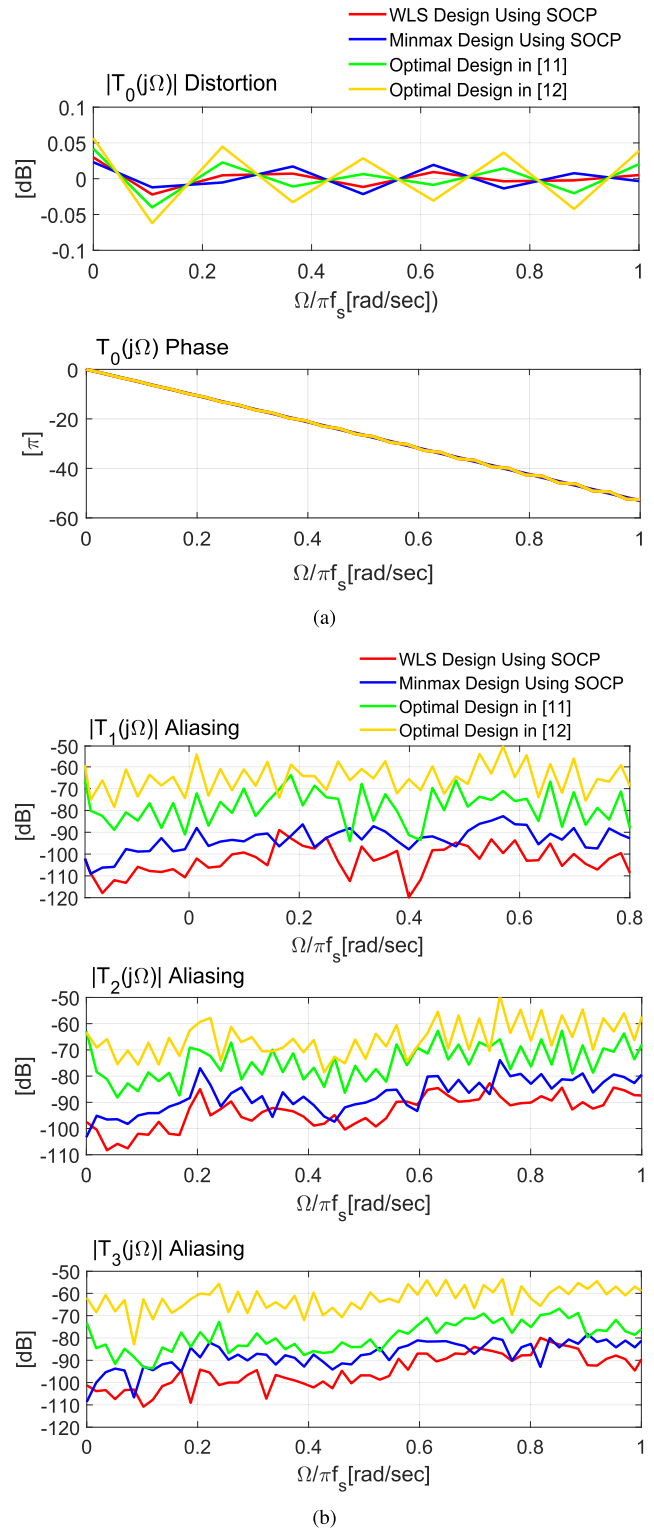


FIGURE 2. Frequency responses of minimax and WLS designs using SOCP without constraints, optimal designs in [11] and [12]: (a) Distortion function. (b) Aliasing functions.

considered in a four-channel 12-bit BI-DAC system, where

$$W_k(\Omega) = \begin{cases} 1 \\ 10^2 \\ 10^4 \end{cases} \quad k = 0, 1, 2, 3 \quad (34)$$



TABLE 1. Summary of maximum distortion and aliasing errors.

$W_k (\Omega)$	$T_0 (j\Omega)$		$T_1 (j\Omega)$		$T_2 (j\Omega)$		$T_3 (j\Omega)$	
	Unconstrained Minimax Design	Unconstrained WLS Design	Unconstrained Minimax Design	Unconstrained WLS Design	Unconstrained Minimax Design	Unconstrained WLS Design	Unconstrained Minimax Design	Unconstrained WLS Design
$10^0$	0.022 dB	0.021 dB	-82.1 dB	-88.7 dB	-73.9 dB	-83.8 dB	-78.1 dB	-80.5 dB
$10^1$	0.024 dB	0.022 dB	-85.7 dB	-95.9 dB	-76.3 dB	-85.4 dB	-81.3 dB	-85.3 dB
$10^2$	0.023 dB	0.023 dB	-88.9 dB	-100.6 dB	-79.1 dB	-88.1 dB	-83.8 dB	-91.7 dB
$10^3$	0.022 dB	0.020 dB	-92.0 dB	-103.2 dB	-82.6 dB	-92.5 dB	-85.5 dB	-93.2 dB
$10^4$	0.041 dB	0.022 dB	-95.3 dB	-106.4 dB	-86.2 dB	-95.7 dB	-88.2 dB	-98.4 dB
$10^5$	0.073 dB	0.043 dB	-96.1 dB	-107.2 dB	-87.1 dB	-96.4 dB	-88.9 dB	-99.3 dB
$10^6$	0.112 dB	0.076 dB	-96.8 dB	-107.7 dB	-87.8 dB	-97.0 dB	-89.5 dB	-100.1 dB
$10^7$	0.165 dB	0.117 dB	-97.3 dB	-108.1 dB	-88.2 dB	-97.4 dB	-90.1 dB	-100.7 dB
$10^8$	0.231 dB	0.170 dB	-97.6 dB	-108.3 dB	-88.7 dB	-97.7 dB	-90.4 dB	-101.0 dB

Further, the other configurations in Example 2 are identical with these in Example 1.

The frequency responses of the unconstrained minimax and WLS designs using SOCP with different values of the nonnegative weighting functions are, respectively, shown in Fig.3 and Fig.4. It could be seen from Fig.3(a) and Fig.4(a), except in the unconstrained minimax design using SOCP with  $W_k (\Omega) = 10^4, k = 0, 1, 2, 3$ , the maximum distortion errors were almost unchanged when the value of  $W_k (\Omega), k = 0, 1, 2, 3$  increased in the unconstrained minimax and WLS designs using SOCP and they were all approximately 0.02 dB. Further, when  $W_k (\Omega), k = 0, 1, 2, 3$  increased to  $10^4$  in the unconstrained minimax design using SOCP, the maximum distortion error also increased to 0.04 dB. We could know from Fig.3(b) and Fig.4(b) that, the aliasing errors could be, respectively, reduced below  $-73$  dB and  $-80$  dB in the unconstrained minimax and WLS designs using SOCP. Additionally, in these designs, the aliasing errors became lower and lower when the value of  $W_k (\Omega), k = 0, 1, 2, 3$  increased. However, from Table 1 which shows the maximum distortion and aliasing errors in the unconstrained minimax and WLS designs using SOCP, we found that, the distortion errors kept almost unchanged when  $W_k (\Omega), k = 0, 1, 2, 3$  in the unconstrained minimax and WLS designs using SOCP increased from 1 to  $10^3$  and from 1 to  $10^4$ , respectively. When  $W_k (\Omega), k = 0, 1, 2, 3$  were, respectively, larger than  $10^3$  and  $10^4$  in the unconstrained minimax and WLS designs using SOCP, all of the maximum distortion errors became larger and larger with the value of  $W_k (\Omega), k = 0, 1, 2, 3$  increasing, and the difference between two adjacent maximum distortion errors also became larger. Moreover, the aliasing errors in these two designs still became lower and lower with the value of  $W_k (\Omega), k = 0, 1, 2, 3$  increasing, while unlike the situation about the maximum distortion errors, the difference between two adjacent maximum aliasing errors was becoming smaller and smaller.

In conclusion, there is a tradeoff among the value of  $W_k (\Omega), k = 0, 1, 2, 3$ , the distortion error and the aliasing errors. Additionally, it can be known from Fig.3, Fig.4 and Table 1 that, no matter what value  $W_k (\Omega), k = 0, 1, 2, 3$  increased to, the unconstrained WLS design using SOCP

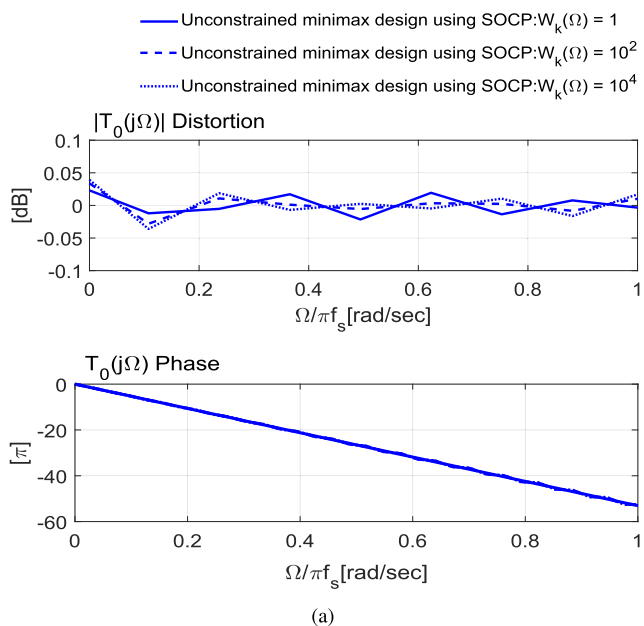
could still achieve better aliasing errors reduction than the unconstrained minimax design using SOCP.

### 3) EXAMPLE 3: MINIMAX AND WLS DESIGNS USING SOCP WITH LINEAR EQUALITY AND CONVEX QUADRATIC INEQUALITY CONSTRAINTS

In this design example of BI-DAC, the configurations are identical with these in Example 1. Further, the linear equality and convex quadratic inequality constraints are incorporated in our presented minimax and WLS designs using SOCP, which can be described as follows

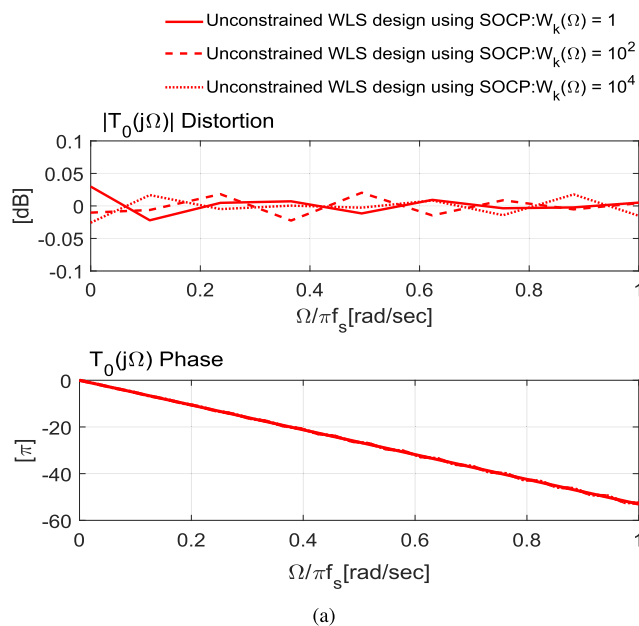
- (1) To obtain a low distortion error in a low-frequency band, a first-order ( $P_{\Omega_d} = 1$ ) magnitude flatness constraint is imposed at the frequency points in  $[0, \frac{0.1}{T}\pi]$ .
- (2) To reduce the aliasing errors lower than  $-110$  dB such that satisfied the expected SFDR of a 16-bit BI-DAC system, the convex quadratic inequality constraints were, respectively, imposed in these two frequency bands  $[0, \frac{0.6}{T}\pi]$  and  $[0, \frac{0.8}{T}\pi]$ .

The simulation results were shown in Fig.5. It could be seen from Fig.5(a) that the distortion errors of our presented constrained minimax and WLS designs using SOCP with the linear equality constraints were all equal to zero in the selected frequency band  $[0, \frac{0.1}{T}\pi]$ . Nevertheless, comparing with the unconstrained minimax and WLS designs using SOCP in Example 1, the linear equality constraints in these two designs was satisfied, while the expense was that larger maximum distortion errors were achieved out of the selected frequency band  $[0, \frac{0.1}{T}\pi]$ , which was the same as the description in Section III-B-1). From Fig.5(b), we could see that, in the minimax and WLS designs using SOCP with the convex quadratic inequality constraints, all of the aliasing errors were reduced below  $-110$  dB in the selected frequency bands  $[0, \frac{0.6}{T}\pi]$  and  $[0, \frac{0.8}{T}\pi]$ , but the expense was that larger aliasing errors were achieved in these frequency bands  $[\frac{0.6}{T}\pi, \frac{\pi}{T}]$  and  $[\frac{0.8}{T}\pi, \frac{\pi}{T}]$ . These simulation results were the same as the description in Section III-B-2). Further, in the same selected frequency band, the constrained minimax and WLS designs using SOCP with the convex quadratic inequality constraints almost obtained the identical aliasing errors. However, out of



**FIGURE 3.** Frequency responses of unconstrained minimax designs using SOCP with different values of nonnegative weighting functions: (a) Distortion function. (b) Aliasing functions.

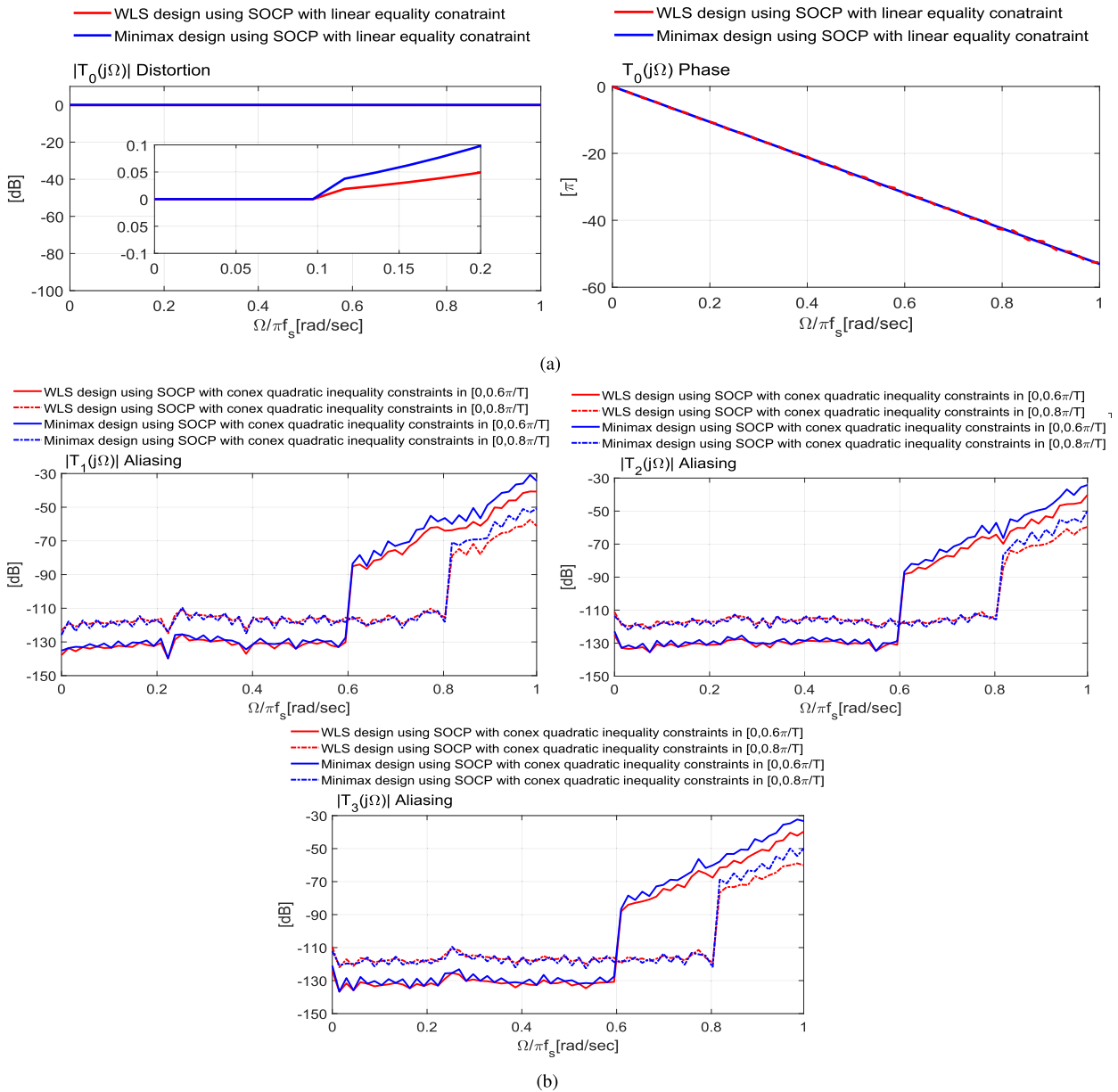
this selected frequency band, the constrained minimax design using SOCP had larger aliasing errors than the constrained WLS design using SOCP. Additionally, in the constrained minimax and WLS designs using SOCP, lower aliasing errors were achieved with the bandwidth of the selected frequency



**FIGURE 4.** Frequency responses of unconstrained WLS designs using SOCP with different values of nonnegative weighting function: (a) Distortion function. (b) Aliasing functions.

band decreasing, but larger aliasing errors were obtained out of this selected frequency band.

From this design example, we know that, there is a trade-off between the bandwidth of the selected frequency band, the peak aliasing errors and the aliasing errors reduction. In addition, it demonstrates that our presented minimax and



**FIGURE 5.** Frequency responses of minimax and WLS designs using SOCP with linear equality and convex quadratic inequality constraints: (a) Distortion function. (b) Aliasing functions.

WLS designs using SOCP offer more flexibility in aliasing errors reduction than the optimal designs in [11] and [12].

**B. COMPUTATIONAL COMPLEXITY ANALYSIS**

Computational complexity, as one of the important specifications of the optimal design of digital FIR filters, is usually used to evaluate the performance of the optimal design. In this section, we compared the computational complexity among our presented unconstrained and constrained minimax and WLS designs using SOCP, the optimal designs in [11] and [12] using the following parameters:  $N_{D1} = N_{D3} = N_{D4} = 5$ ,  $N_{D2} = 8$ ,  $N_{D5} = N_{D6} = 6$ ,  $P_L = 100$ ,  $P_{\Omega_d} = 1$ , the linear equality and convex quadratic inequality constraints were, respectively, imposed in the selected frequency bands  $[0, \frac{0.1}{T}\pi]$  and  $[0, \frac{0.8}{T}\pi]$  so that  $N_{\Omega_d} = 10$  and  $N_{\Omega} = 80$ .

Fig.6 shows the comparisons among the computational complexity of these six optimal designs with different number of sub-channels when  $N = 60$  and with different length of digital FIR filters when  $M = 4$ . It can be seen from Fig.6(a) that, the relationship among the computational complexity of these six optimal designs was sorted from the largest to the lowest as

$$\begin{aligned}
 [12] &> \text{Constrained WLS} \\
 &> \text{Unconstrained WLS} \\
 &> \text{Constrained minimax} \\
 &> \text{Unconstrained minimax} \\
 &> [11]
 \end{aligned} \tag{35}$$

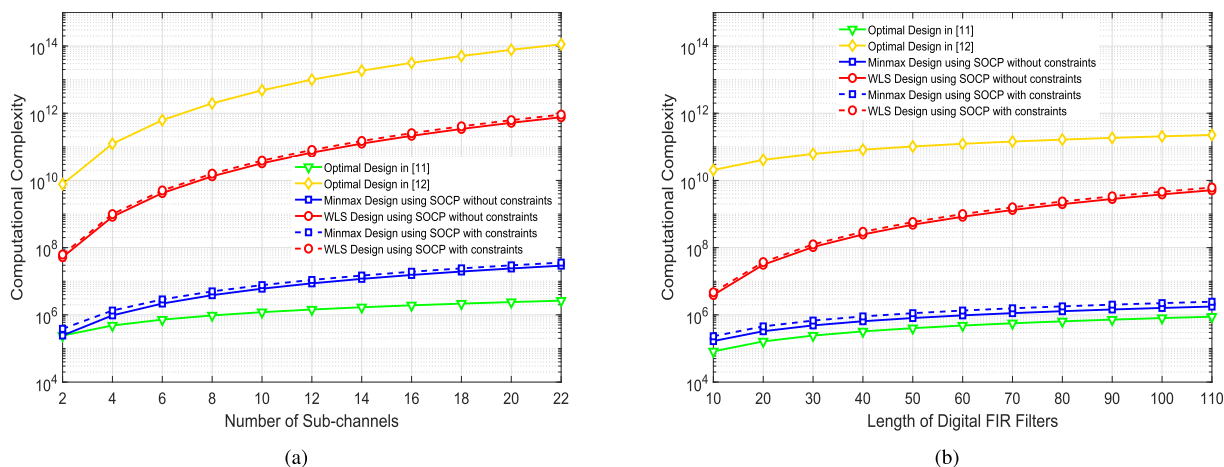


FIGURE 6. Computational complexity comparisons among different optimal designs: (a) Computational complexity with different number of sub-channels when  $N = 60$ . (b) Computational complexity with different length of digital FIR filters when  $M = 4$ .

TABLE 2. Summary of worst-case passband ripple  $\epsilon_d$  and stopband roll-off  $\epsilon_a$ .

N	$\epsilon_d$						$\epsilon_a$					
	Unconstrained Minimax Design	Constrained Minimax Design	Unconstrained WLS Design	Constrained WLS Design	Optimal Design in [11]	Optimal Design in [12]	Unconstrained Minimax Design	Constrained Minimax Design	Unconstrained WLS Design	Constrained WLS Design	Optimal Design in [11]	Optimal Design in [12]
10	0.198 dB	0.360dB	0.196 dB	0.258dB	0.215 dB	0.312 dB	-69.2 dB	-44.6 dB	-75.2 dB	-52.8 dB	-56.2 dB	-45.5 dB
20	0.146 dB	0.307dB	0.147 dB	0.206dB	0.163 dB	0.263 dB	-70.8 dB	-46.2 dB	-77.3 dB	-55.1 dB	-58.3 dB	-47.0 dB
30	0.102 dB	0.275dB	0.102 dB	0.164dB	0.114 dB	0.221 dB	-72.1 dB	-47.7 dB	-78.4 dB	-57.2 dB	-59.7 dB	-48.2 dB
40	0.079 dB	0.242dB	0.076 dB	0.139dB	0.082 dB	0.193 dB	-72.8 dB	-48.9dB	-79.1 dB	-58.8 dB	-60.6 dB	-49.2 dB
50	0.059 dB	0.224dB	0.054 dB	0.118dB	0.061 dB	0.171 dB	-73.3 dB	-49.8 dB	-79.8 dB	-60.1 dB	-61.2 dB	-50.0 dB
60	0.042 dB	0.202dB	0.042 dB	0.105dB	0.048 dB	0.152 dB	-73.9 dB	-50.5 dB	-80.5 dB	-61.8 dB	-62.9 dB	-50.6 dB
70	0.034 dB	0.181dB	0.032 dB	0.094dB	0.036 dB	0.135 dB	-74.5 dB	-51.1 dB	-81.1 dB	-63.3 dB	-63.5 dB	-56.1 dB
80	0.026 dB	0.161dB	0.026 dB	0.085dB	0.026 dB	0.124 dB	-75.0 dB	-51.5 dB	-81.5 dB	-64.5 dB	-64.1 dB	-56.5 dB
90	0.020 dB	0.143dB	0.019 dB	0.077dB	0.023 dB	0.115 dB	-76.1 dB	-51.9 dB	-81.8 dB	-65.4 dB	-64.4 dB	-57.2 dB
100	0.016 dB	0.126dB	0.015 dB	0.071dB	0.020 dB	0.107 dB	-76.7 dB	-52.1 dB	-82.4 dB	-66.1 dB	-65.4 dB	-57.4 dB
110	0.014 dB	0.121dB	0.013 dB	0.066dB	0.019 dB	0.010 dB	-78.1 dB	-52.2dB	-83.1 dB	-66.6 dB	-65.9 dB	-59.1 dB

Additionally, the computational complexity of these six optimal designs raised as number of sub-channels increased, and the computational complexity of the optimal design in [12], our presented unconstrained and constrained minimax and WLS designs using SOCP, were rising faster than the optimal design in [11].

From Fig.6(b), one could be seen that the relationship among these six optimal designs could also be described as same as that in (35). Further, the computational complexity of these six optimal designs raised with the length of digital FIR filters increasing. Specially, the computational complexity of the unconstrained and constrained WLS designs using SOCP, were rising faster than that of another five optimal designs.

Above all, the computational complexity comparisons among these six optimal designs, shown in Fig.6(a) and (b), were the same as the description in Section III-C.

### C. DIGITAL FIR FILTER LENGTH ANALYSIS

From Section III-C, we know that,  $N$ -the length of digital FIR filters in BI-DAC, is an important parameter which determines the performance of BI-DAC. In order to illustrate the influence of the digital FIR length  $N$  on our presented optimal designs, the constrained and unconstrained minimax and WLS designs using SOCP are all considered, where the

digital FIR length  $N$  gradually increases from 10 to 110 at an interval of 10. Further, the selected frequency bands used in these constrained designs are  $[0, \frac{0.1}{T}\pi]$  and  $[0, \frac{0.8}{T}\pi]$ , respectively.

Table 2 summarizes the worst-case passband ripple  $\epsilon_d$  and stopband roll-off  $\epsilon_a$  of our presented constrained and unconstrained minimax and WLS designs using SOCP and the optimal designs in [11] and [12], respectively. It could be seen from Table 2 that, with the digital FIR length  $N$  increasing,  $\epsilon_d$  and  $\epsilon_a$  of these six optimal designs became lower and lower. However, a longer digital FIR filter length  $N$  required much higher actual hardware cost. Moreover, it can be known from Section IV-C, the computational complexity of these four optimal designs became larger and larger with the digital FIR filter's length  $N$  increasing. These simulation results were identical with the description in Section III-C. Therefore, there is a tradeoff among the digital FIR filters' length  $N$ , the passband ripple, the stopband roll-off, the computational complexity and the actual hardware cost.

### V. CONCLUSION

In this paper, we presented the optimal minimax and WLS designs of digital FIR filters using SOCP for the aliasing errors reduction in BI-DAC. The SOCP formulation is a

convex optimization problem, which allows the linear equality and convex quadratic inequality constraints such as the magnitude flatness and the peaking aliasing error constraints to be incorporated in the distortion function and the aliasing functions, respectively. Several design examples had been used to illustrate the performance of our presented unconstrained and constrained minimax and WLS designs of digital FIR filters using SOCP. The simulation results showed that, our presented unconstrained minimax and WLS designs using SOCP could achieve satisfactory results which satisfied the expected SFDR in a 12-bit BI-DAC, and there was a tradeoff among the distortion error, the aliasing errors and the value of the nonnegative weighting function. At an expense of larger computational complexity, in the selected frequency band, our presented constrained minimax design using SOCP almost has the same distortion and aliasing errors as the constrained WLS design using SOCP, but out of this selected frequency band, this constrained minimax design has larger distortion and aliasing errors than the constrained WLS design using SOCP. Moreover, our presented constrained and unconstrained minimax design using SOCP had lower computational complexity than our presented constrained and unconstrained WLS design using SOCP, and our presented unconstrained optimal design also had lower computational complexity than our presented constrained optimal design. Ultimately, there was a tradeoff among the digital FIR length, the distortion and aliasing errors, the computational complexity and the actual hardware cost. In a word, our presented unconstrained and constrained WLS designs using SOCP is more suitable for the situation with lower aliasing errors at an expense of larger computational complexity, while our presented unconstrained and constrained minimax designs using SOCP is more suitable for the situation with lower computational complexity at an expense of larger aliasing errors.

In our future research, the next important exploration will be that how to control the finite word length such that a expected SFDR will still be satisfied after determining the optimum coefficients of digital FIR filters in BI-DAC. Moreover, we will explore the design of hardware circuit and the accomplishment of the parameterized digital FIR filters based on field programmable gate array(FPGA), and we will also evaluate and consider the hardware circuit cost.

## REFERENCES

- [1] Y. Xing, X. Yindong, W. Houjun, G. Guangkun, and Y. Linglong, "Synchronization method of multiple multiplexed DACs," in *Proc. 13th IEEE Int. Conf. Electron. Meas. Instrum.*, Oct. 2017, pp. 17–23.
- [2] Y. Zhao, Y. H. Hu, and J. Liu, "Random triggering-based sub-Nyquist sampling system for sparse multiband signal," *IEEE Trans. Instrum. Meas.*, vol. 66, no. 7, pp. 1789–1797, Jul. 2017.
- [3] Y. Park and K. A. Remley, "Two-stage correction for wideband wireless signal generators with time-interleaved digital-to-analog-converters," in *Proc. 83rd ARFTG Microw. Meas. Conf.*, Jun. 2014, pp. 1–4.
- [4] C. Krall, C. Vogel, and K. Witrals, "Time-interleaved digital-to-analog converters for UWB signal generation," in *Proc. IEEE Int. Conf. Ultra-Wideband*, Sep. 2007, pp. 366–371.
- [5] X. Yang, H. Wang, and K. Liu, "Estimation and compensation methods of time delay and phase offset in hybrid filter bank DACs," *Electron. Lett.*, vol. 54, no. 13, pp. 806–808, 2018.
- [6] X. Chen et al., "All-electronic 100-GHz bandwidth digital-to-analog converter generating pam signals up to 190 gbaud," *J. Lightw. Technol.*, vol. 35, no. 3, pp. 411–417, Feb. 1, 2017.
- [7] C. Schmidt, C. Kottke, V. Jungnickel, and R. Freund, "Enhancing the bandwidth of DACs by analog bandwidth interleaving," in *Proc. Broadband Coverage Germany ITG-Symp.*, Apr. 2016, pp. 1–8.
- [8] M. Sichma, S. Bieder, and A. Czylwik, "A 40 GHz arbitrary waveform generator by frequency multiplexing," in *Proc. 19th Int. Conf. OFDM Freq. Domain Techn.*, Aug. 2016, pp. 1–7.
- [9] C. Schmidt, V. H. Tanzil, C. Kottke, R. Freund, and V. Jungnickel, "Digital signal splitting among multiple DACs for analog bandwidth interleaving (ABD)," in *Proc. IEEE Int. Conf. Electron., Circuits Syst.*, Dec. 2016, pp. 245–248.
- [10] P. J. Pupalaiakis, "High speed arbitrary waveform generator," U.S. Patent 7 535 394 B2, May 19, 2009.
- [11] X. Yang, H. Wang, K. Liu, Y. Xiao, Z. Fu, and G. Guo, "Minimax design of digital FIR filters using linear programming in bandwidth interleaving digital-to-analog converter," *IEICE Electron. Express*, vol. 15, no. 13, p. 20180565, 2018.
- [12] J. Song, S. Tian, L. Guo, and K. Yang, "Digital correction of frequency-response errors in bandwidth-interleaved ADCs," *Electron. Lett.*, vol. 52, no. 19, pp. 1596–1598, Sep. 2016.
- [13] C.-C. Tseng, "Design of 1-D and 2-D variable fractional delay all-pass filters using weighted least-squares method," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 49, no. 10, pp. 1413–1422, Oct. 2002.
- [14] J.-C. Liu and S.-J. You, "Weighted least squares near-equiripple approximation of variable fractional delay FIR filters," *IET Signal Process.*, vol. 1, no. 2, pp. 66–72, Jun. 2007.
- [15] J.-J. Shyu and S.-C. Pei, "A generalized approach to the design of variable fractional-delay FIR digital filters," *Signal Process.*, vol. 88, no. 6, pp. 1428–1435, 2008.
- [16] T.-B. Deng, "Generalized WLS method for designing all-pass variable fractional-delay digital filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 10, pp. 2207–2220, Oct. 2009.
- [17] J.-J. Shyu, S.-C. Pei, and C.-H. Chan, "Minimax phase error design of all-pass variable fractional-delay digital filters by iterative weighted least-squares method," *Signal Process.*, vol. 89, no. 9, pp. 1774–1781, 2009.
- [18] T. B. Deng, "Hybrid structures for low-complexity variable fractional-delay FIR filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 4, pp. 897–910, Apr. 2010.
- [19] J.-J. Shyu, S.-C. Pei, and Y.-D. Huang, "Two-dimensional farrow structure and the design of variable fractional-delay 2-D FIR digital filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 2, pp. 395–404, Feb. 2009.
- [20] T.-B. Deng, "Decoupling minimax design of low-complexity variable fractional-delay fir digital filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 10, pp. 2398–2408, Oct. 2011.
- [21] A. Chottera and G. Jullien, "A linear programming approach to recursive digital filter design with linear phase," *IEEE Trans. Circuits Syst.*, vol. 29, no. 3, pp. 139–149, Mar. 1982.
- [22] J. O. Coleman and D. P. Scholnik, "Design of nonlinear-phase FIR filters with second-order cone programming," in *Proc. 42nd Midwest Symp. Circuits Syst.*, vol. 1, Aug. 1999, pp. 409–412. 1.
- [23] W.-S. Lu and T. Hinamoto, "Optimal design of IIR frequency-response-masking filters using second-order cone programming," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 50, no. 11, pp. 1401–1412, Nov. 2003.
- [24] S. Boyd and L. Vandenberghe, *Convex Optimization*. Cambridge, U.K.: Cambridge Univ. Press, 2004.
- [25] A. Jiang and H. K. Kwan, "Minimax design of IIR digital filters using iterative SOCP," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 6, pp. 1326–1337, Jun. 2010.
- [26] T.-B. Deng, "Minimax design of low-complexity even-order variable fractional-delay filters using second-order cone programming," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 10, pp. 692–696, Oct. 2011.
- [27] K. Liu, S. Tian, G. Guo, and Y. Xiao, "Precisely synchronous and cascaded multi-channel arbitrary waveform generator," *Rev. Sci. Instrum.*, vol. 88, no. 3, p. 035110, 2017.
- [28] J. F. Sturm, "Using SeDuMi 1.02, A Matlab toolbox for optimization over symmetric cones," *Optim. Methods Softw.*, vol. 11, nos. 1–4, pp. 625–653, 1999.



**XING YANG** was born in 1992. He received the B.S. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2014, where he is currently pursuing the Ph.D. degree with the School of Automation Engineering. His research interests include instrument science and technology, circuits and systems, and signal processing.



**KE LIU** was born in Sichuan, China, in 1978. He received the M.S. and Ph.D. degrees from the University of Electronic Science and Technology of China, China, in 2003 and 2010, respectively, where he is currently a Professor with the School of Automation Engineering. His research interests include frequency synthesis, measurements and instruments, and signal processing.



**HOUJUN WANG** received the M.Sc. and Ph.D. degrees in information and signal processing from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 1985 and 1992, respectively.

He is currently a Professor, and he has been the Vice President of UESTC, since 2005. His current research interests include time domain measurement and signal processing, design for testability of complex systems, architecture of auto test systems, and signal processing.



**YINDONG XIAO** was born in 1982. He received the B.S., M.Sc., and Ph.D. degrees from the University of Electronic Science and Technology of China, Chengdu, China, in 2004, 2007, and 2013, respectively, where he is currently an Associate Professor. His research interests include the computer network test technology and the arbitrary waveform generation technology.

...