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A Family of Scalable Non-Isolated Interleaved DC-DC Boost Converters With Voltage Multiplier Cells

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ABSTRACT In this paper, a family of non-isolated interleaved high-voltage-gain DC–DC converters is presented. This family can be used in a wide variety of applications, such as in a photovoltaic systems interface to a high voltage DC distribution bus in a microgrid and an X-ray system power supply. The general structure of this family is illustrated and consists of two stages: an interleaved boost stage and a voltage multiplier stage. The interleaved boost stage is a two-phase boost converter, and it converts the input DC voltage to an AC square waveform. Moreover, using the interleaved boost stage increases the frequency of the AC components so that it can be easily filtered with smaller capacitors and, therefore, makes the input current smoother than the one from the conventional boost converter. The voltage multiplier cell (VMC) can be a Dickson cell, Cockcroft–Walton (CW), or a combination of the two. The VMC stage rectifies the square-shaped voltage waveform coming from the interleaved boost stage and converts it to a high DC voltage. Several combinations of VMCs and how they can be extended are illustrated, and the difference between them is summarized so that designers can be able to select the appropriate topology for their applications. An example of this converter family is illustrated with detailed modes of operation, a steady-state analysis, and an efficiency analysis. The example converter was simulated to convert 20 V_{DC} to 400 V_{DC}, and a 200 W hardware prototype was implemented to verify the analysis and simulation. The results show that the example has a peak efficiency of 97% of this family of converters and can be very suitable for interfacing renewable energy sources to a 400 V_{DC} DC distribution system.

INDEX TERMS Interleaved, boost, step-up, high-gain, DC-DC, renewable, microgrid, PV, DC distribution, VMC, modular.

I. INTRODUCTION

The total power generation from renewable energy sources has been increasing rapidly and is predicted to increase threefold in the near future [1], [2]. The transition from using conventional and depletable energy sources in electricity generation to renewable and sustainable sources requires adaptable power infrastructure and high-efficiency power electronic converters. The power electronics play an indispensable role in renewable energy sources' integration to the main electric grid. Using highly efficient power converters could help customers save energy and therefore increase the economic benefits [3], [4]. The renewable energy market necessitates not only efficient, but also versatile and multi-purpose, converters. Recently, the idea of integrating a low voltage PV panel to a 400 V DC distribution bus became a research interest due to the advantage of the DC distribution bus over AC. The DC distribution system has less conversion units and better efficiency, power quality, and performance than the AC distribution systems [5]–[9]. Integration of a single PV panel to a 400 V DC distribution system requires a high-gain DC-DC converter [10].

Several topologies found in the literature can be used as high-gain DC-DC converters [11]–[22]. However, there is no superior solution for all applications. The most common topology used to step up the input voltage is the conventional boost converter, which is the most straightforward step-up converter [23]. However, the conventional boost converter would not have enough voltage gain for integrating renewable energy sources to a 400 V, but if it were to have enough voltage gain, it would be only when operating at a higher

duty cycle, which might lead to the appearance of reverse recovery phenomena and low overall efficiency, especially if the inductor DC equivalent resistance is high. Moreover, the required inductance to stay in the continuous conduction mode is very large, and therefore, the converter requires large and bulky magnetics [24], [25].

Cascaded boost converters were introduced to replace the conventional boost converter. Such solutions increase the overall voltage gain and allow each converter to operate at a lower duty cycle [26]. However, cascading two or more converters at least doubles the power being processed, and that might compromise the efficiency as well. Moreover, controlling cascaded converters requires that the output impedance of a converter be lower than the input impedance of the following converter to ensure stability [27]. That might lead to complications in the design and control. Stacking two or more converters helps by sharing the power among different converters and allows the use of lower current rating devices [28]. However, the overall voltage gain is still the same as the voltage gain of the conventional boost converter.

Several converters can achieve higher voltage by incorporating either coupled inductors or transformers [29], [30]. Such topologies increase the voltage gain by increasing the turn ratio. However, several issues can arise. First, the leakage inductance can cause some voltage spikes across switching devices, and that might require some voltage clamp circuits. Second, incorporating such devices reduces the power density of the converter and increases the weight. Furthermore, the semiconductor materials will improve rapidly, while magnetic materials will not. Therefore, with the increase of switching frequency, the magnetic-based components might become the most significant culprits for power loss inside the converter. Thus, this paper introduces a family of converters that can have a high-voltage-gain ratio, continuous current, low stress across both active and passive devices, and high power density. The proposed family consists of two stages: an interleaved boost stage and voltage multiplier cells. The interleaved boost stage reduces the variation of the input current so that it is easy to obtain more accurate measurements of the PV current to track the maximum power. The voltage multiplier cells increase the voltage gain and reduce the voltage stresses across switching devices. Moreover, the converter can achieve a high-voltage-gain ratio while operating at a lower duty cycle. The proposed family requires the lower value of critical inductance to keep the converter operating in the continuous conduction mode (CCM). The rest of the paper is structured as follows: Section II provides the theory of operation and the general structure of the proposed family. Section III presents different variations of the converter belonging to the proposed family. In Section IV, an example of the proposed converter is given and analyzed. In Section V and VI, the simulation and experimental results of the example converter are provided, respectively. Finally, conclusions and future work are described in Section VII.

II. THEORY OF OPERATION AND GENERAL STRUCTURE OF THE PROPOSED FAMILY

The general structure of the proposed family is shown in Fig. 1, which consists of an interleaved boost stage followed by a voltage multiplier cell, and then it is either filtered using an output diode and capacitor capacitor as in Fig. 1(a) or using an LC filter as shown in Fig. 1(b). By using an output diode and a capacitor filter, the output of VMC is further increased by $\frac{1}{1-d}$ but the output current is discontinuous. On the contrary, when using an LC filter, the output voltage of the VMC is not increased, but the output current is continuous if the inductor is large enough to operate in the CCM mode. Several papers present members belonging to the proposed family [31]–[37]. However, no information about extending the VMC cells or the interleaved boost phases has been reported. The following sections present details about each stage of the proposed family.

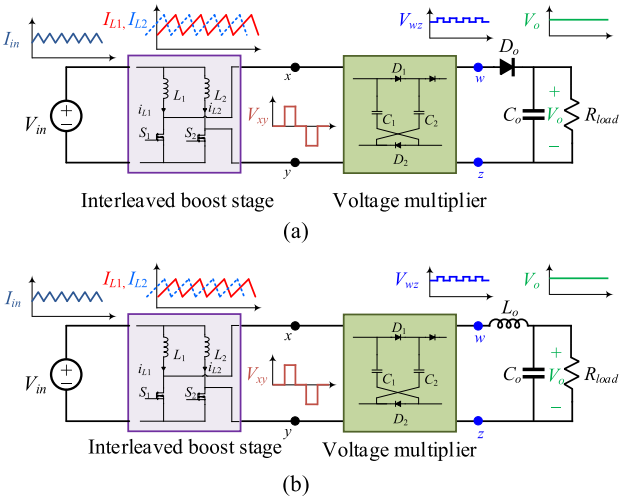

FIGURE 1. General structure of the proposed family: (a) with output diode and capacitor (b) with LC filter output.

A. INTERLEAVED BOOST STAGE

The IBC stage consists of two or more phases. Each phase consists of an inductor and a low-side active switch. Since the IBC stage is a current source, the active switches can be closed simultaneously with no need for a dead time insertion circuit as in the voltage-fed converters. A phase shift between the active switches is vital to reduce the current ripples from the input current and therefore reduce the size of the input filter. A recommended phase shift between active switches can be given by

$$Shift \geq \frac{360^\circ}{\phi} \tag{1}$$

where ϕ is the number of interleaved phases, which is a positive integer greater than or equal to two. To ensure the continuity of the input current and to prevent a voltage-second imbalance in the inductors, the minimum duty cycle

is given by

$$D \geq \frac{\phi - 1}{\phi}. \tag{2}$$

Besides reducing the current ripples, the interleaved boost stage reduces the magnetic storage. In the case of two-phase, and assuming the inductors share the input current equally, the reduction in the magnetic element is half as follows:

$$\frac{E_2}{E_1} = \frac{\frac{1}{2}L\left(\frac{I}{2}\right)^2 + \frac{1}{2}L\left(\frac{I}{2}\right)^2}{\frac{1}{2}LI^2} \times 100 = 50\%. \tag{3}$$

The reduction for E_ϕ is given by κ as

$$\kappa(\%) = (1 - \frac{1}{\phi}) \times 100. \tag{4}$$

Figure 2 shows the percentage of the reduction of a different number of phases. The reduction becomes insignificant as the number of phases increases. The reduction of the magnetic volume ζ does not follow (4) as illustrated in [38]. Instead, one should compare the volume reduction as follows:

$$\zeta = \frac{Volume_{n=1} - \phi Volume_{n=\phi}}{Volume_{n=1}} \times 100 \tag{5}$$

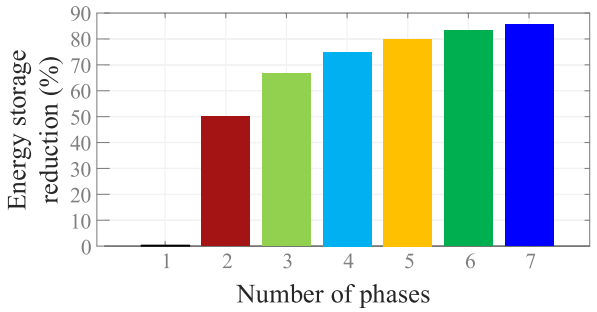

FIGURE 2. Reduction of energy storage at multiple phases. In case of two phases, the required energy storage is reduced by 50%.

where $Volume_{n=1}$ is the volume of the magnetic element in a single phase converter and $Volume_{n=\phi}$ is the volume of the magnetic element of a multiphase converter with ϕ phases. Another advantage of interleaving is that the total conduction loss in the inductors and the active switching devices is reduced if the current is shared equally between the phases as follows:

$$P_{L_{total}} = \frac{I_L^2 \times R_{DC}}{\phi}, \tag{6}$$

$$P_{S,cond_{total}} = \frac{I_{S,rms}^2 \times R_{ON}}{\phi}. \tag{7}$$

The input current ripples depend on the number of interleaved phases and the duty cycle. Figure 3 shows the relationship between the number of stages and the normalized input ripples. Increasing the number of phases reduces the ripples and allows ripple cancellation to occur at multiple duty cycle values. Two phases can have one point of ripple cancellation

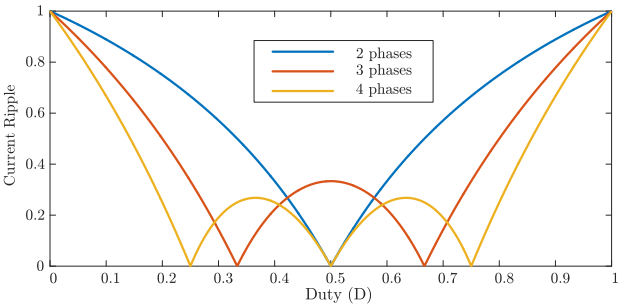

FIGURE 3. The normalized current ripples with respect to a single phase boost converter.

at the 0.5 duty cycle; while in three phases the ripple cancellation occurs at two points: the 0.25 and 0.75 duty cycles. For more phases, the duty cycle values where ripple cancellation can occur are given by

$$d_{\Delta v=0} = [\frac{1}{\phi}, \frac{2}{\phi}, ..., \frac{\phi - 1}{\phi}] \tag{8}$$

Figures 4(a) and (b) show the schematic and output waveforms of the interleaved boost stage for two and three phases, respectively. The switching waveforms and modes of operations are shown in Fig. 5 for two phases and Fig. 6 for three phases. More phases can be used, such as in [39], but three or more phases will not have a uniform pattern of connections to the VMC, and the permutation of variation of the topologies is large. Therefore, the number of phases is limited to two in this paper.

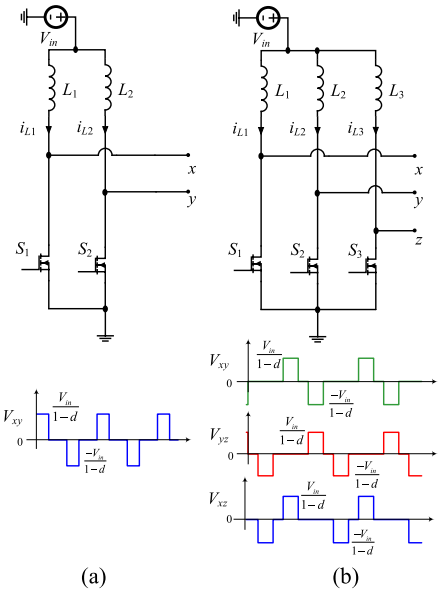

FIGURE 4. Interleaved boost stage with output waveforms: (a) two phases (b) three phases.

B. VOLTAGE MULTIPLIER STAGE

The voltage multiplier stage rectifies the modified squared waveform that comes from the interleaved boost stage and

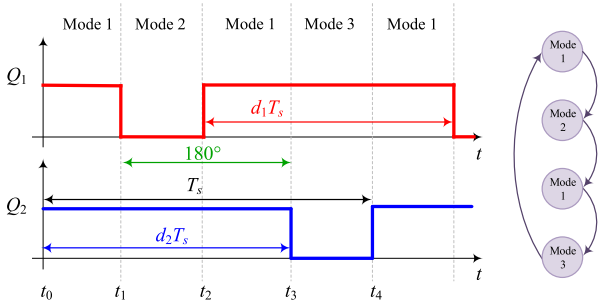

FIGURE 5. The switching pattern for the two-phase interleaved boost converter. The active switches are driven by two out of phase signals, and the converter operates in three modes of operation in the CCM.

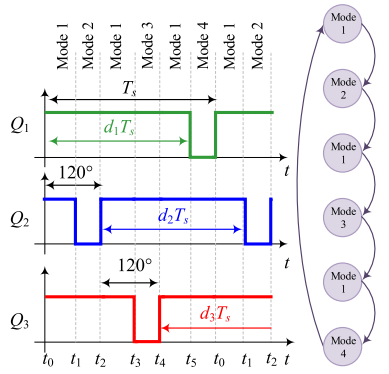

FIGURE 6. The switching pattern for a three-phase interleaved boost converter. The converter is driven by three signals with a phase shift of 120°, and the converter operates at four modes of operation in the CCM.

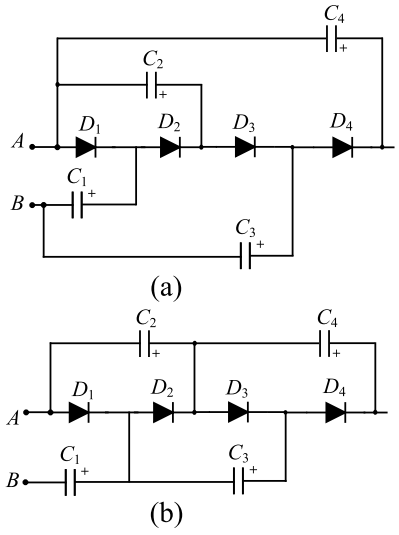

FIGURE 7. Two main voltage multiplier cells: (a) Dickson VMC (b) Cockcroft-Walton VMC.

boosts the voltage to a higher level. The VMC stage consists of capacitors and diodes. The two main extendable VMCs are the Dickson VMC and Cockcroft-Walton VMC, as shown in Fig. 7. The main difference between these VMCs is the way capacitors are connected. In the Dickson VMC, all negative sides of the even capacitors are connected to phase a, and all negative sides of the odd capacitors are connected to phase b. In the Cockcroft-Walton VMC, each negative side of the odd capacitor is connected to the positive side of the previous odd capacitor, and each negative side of the even capacitor is connected to the positive side of the previous even capacitor. Various combinations are derived out of these two VMCs, as in [40]–[45] .

C. TOPOLOGIES OF A TWO-PHASE INTERLEAVED BOOST CONVERTER WITH VMCS

Figures 8 and 9 show different interleaved boost converters with different VMCs and a diode capacitor filter. Figure 10 shows the same groups, but with an LC output filter instead of a diode-capacitor filter. Group A uses cross capacitor VMC cells. This group is analyzed in [46]. Group B and C have cross diode VMC cells, and similar work is presented in [47]. The cells can start in the inverting cells, as in group B, or non-inverting VMC stage, as in group C. To extend the VMC in these two groups, each cell must be followed by a cell with the opposite polarity. For example, the first stage in group B is positive (the diodes are upward), so it must be followed by a negative cell (diodes are downward), and vice versa. The polarity of the output voltage depends on the polarity of the last cell. Group D has Dickson VMC [10], and group E consists of Cockcroft-Walton [48]. Group F contains the example converter and will be analyzed in this paper. Group G has two CW chains, and it can have either the same or a different number of cells on each chain. Finally, Group H uses Dickson cells on one phase and Cockcroft-walton VMC on the other phase with either the same or a different number VMC stages. Several interleaved boost converters with VMCs belonging to this family can be found in the literature such as [49], where the Dickson VMC is modified to have lower voltage stress across capacitors without changing the overall voltage gain.

The main difference between these groups is how internal capacitors are charged and discharged. Some other differences including the load connection type (floating, inverted, or grounded), the stress on the capacitors and diodes, and the number of components in each VMC stage. The VMC structure affects the sharing of the input current between phases in the interleaved boost stage. That is, in converters that have an output diode, if there is a single diode in each stage, then the current sharing can be equal if the number of stages is even. However, if there is an output diode and each stage of the VMC has two diodes, then there will never be equal current sharing between the inductors. In converters where an LC filter is used, there will not be equal current sharing between phases. Table 2 summarizes the differences between the VMCs and illustrates this.

D. POSSIBLE MODIFICATIONS TO THE TOPOLOGIES

The presented family can be modified to obtain specific features such as isolation, where a transformer can be inserted between the interleaved boost stage and the VMC stage, or to convert a topology with a floating output to a grounded output.

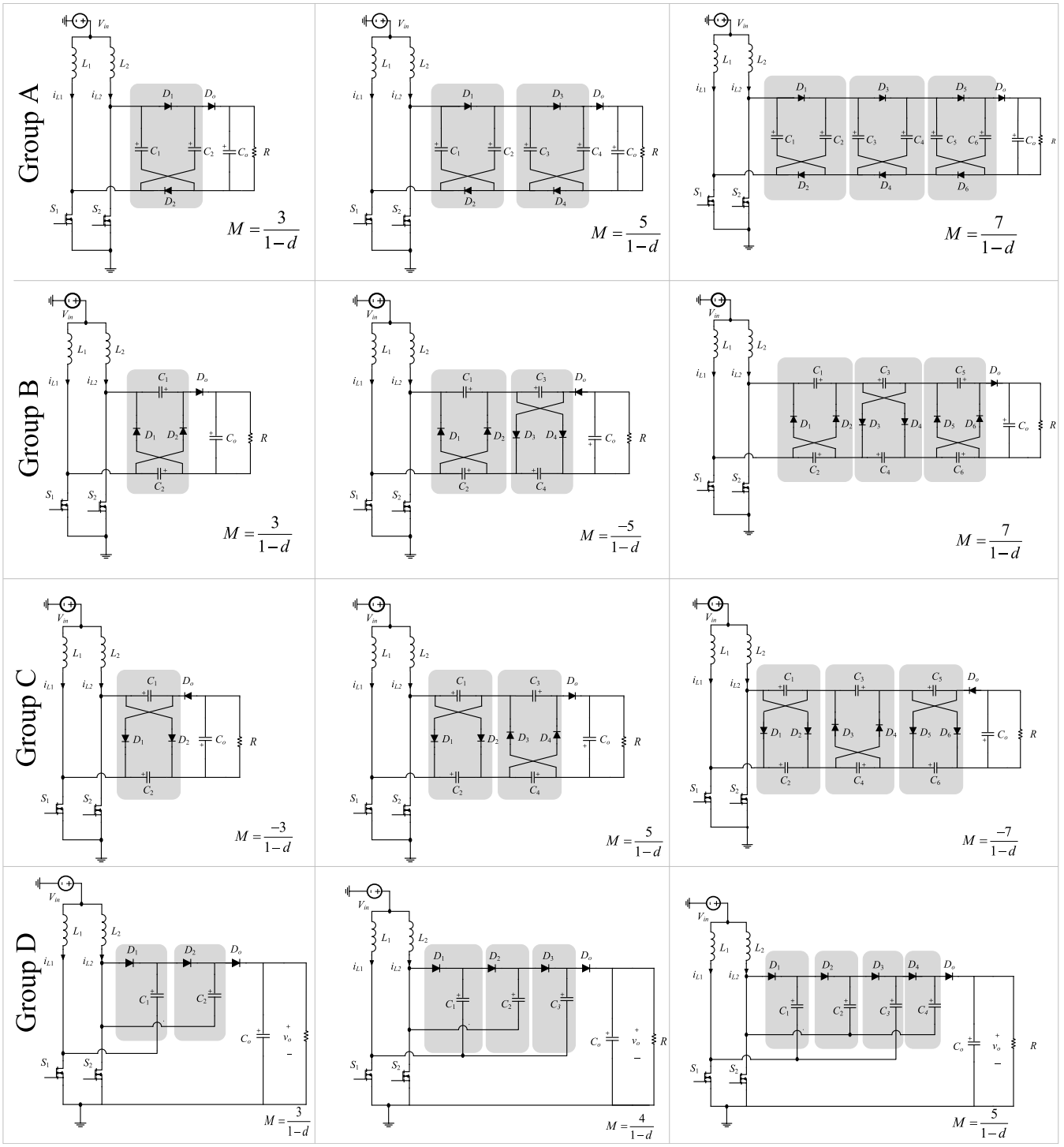

FIGURE 8. Various topologies belong to the interleaved boost converter with voltage multiplier cells (group A-D). The output is filtered using an output diode and a capacitor filter.

1) CONVERT A FLOATING OUTPUT CONVERTER TO GROUNDED OUTPUT

Groups A and F have a floating output, where the output has a different reference point than the input. In voltage control mode, a differential sensor is required for the feedback loop. Designers can convert floating outputs to grounded outputs by adding a diode to the VMC, and connecting the output to the ground, as shown in Fig. 11. Although the voltage stress across the components in the grounded output converter are still the same as the ones in the floating output converter, the voltage gain is significantly reduced. Figure 12 shows group A and F with the grounded output.

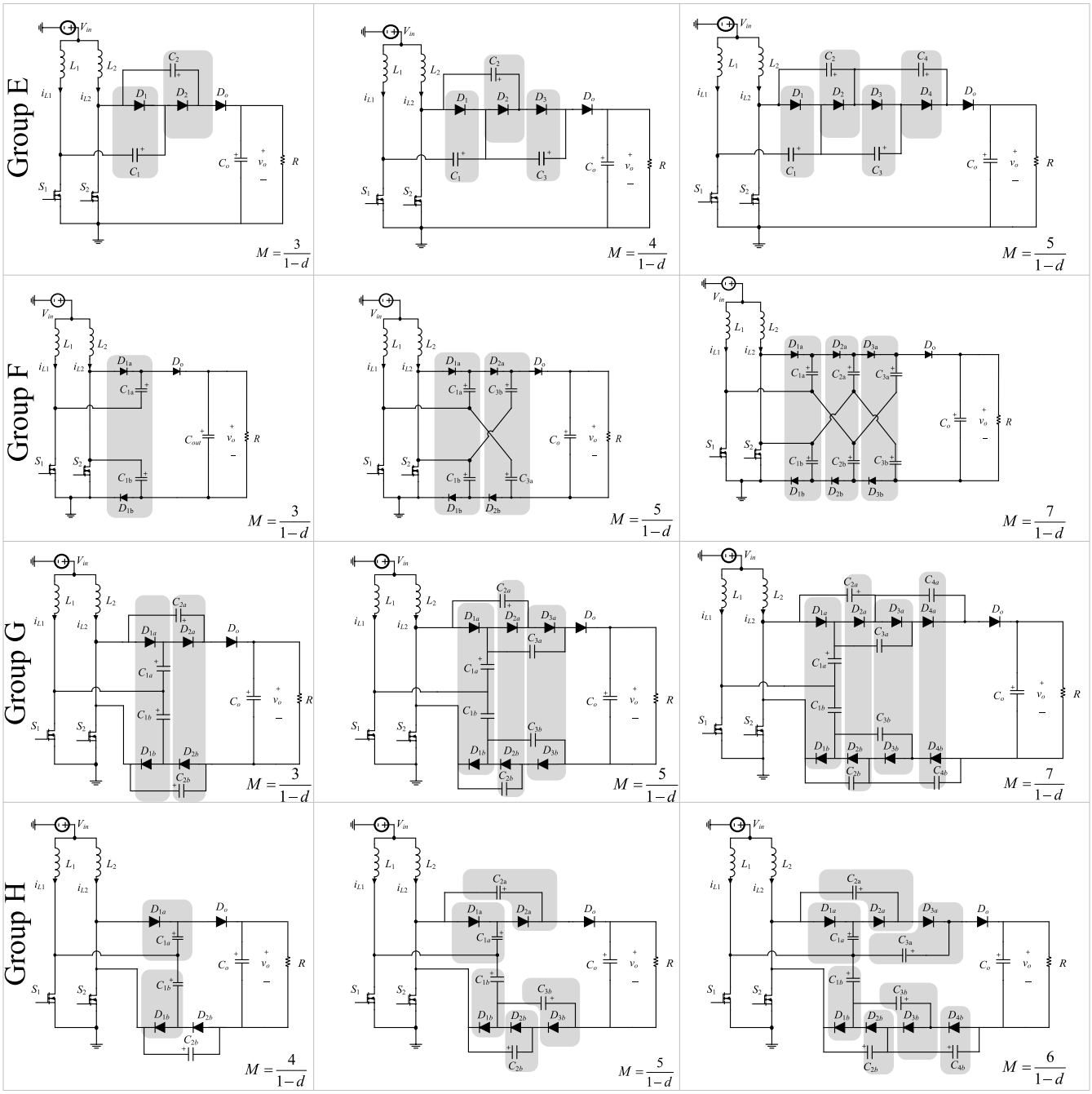

FIGURE 9. Various topologies belong to the interleaved boost converter with voltage multiplier cells (group A-H): with an output diode and a capacitor filter.

2) MODIFICATION TO MAKE THE CONVERTER ISOLATED.

This family can easily be a family of isolated converters by adding a transformer or coupled inductors between the interleaved boost stage and the VMC stage, as shown in Fig. 13. After adding the isolation device with an $N_1 : N_2$ turns ratio, the voltage gain can be calculated as

$$M_{isolated} = M_{nonisolated} \times \frac{N_2}{N_1} \tag{9}$$

3) CONNECTING TWO DIFFERENT VMCS TO OBTAIN THE OVERALL NONUNIFORM CONVERTER.

Extra possible combinations of different voltage multiplier cells can be derived, e.g., but will be unable to expand one or both VMCs. The analysis of nonuniform converters is performed on a case by case basis. Figure 14 shows an example of nonuniform combinations. The converter consists of one cell from group F followed by Cockcroft-Walton cells.

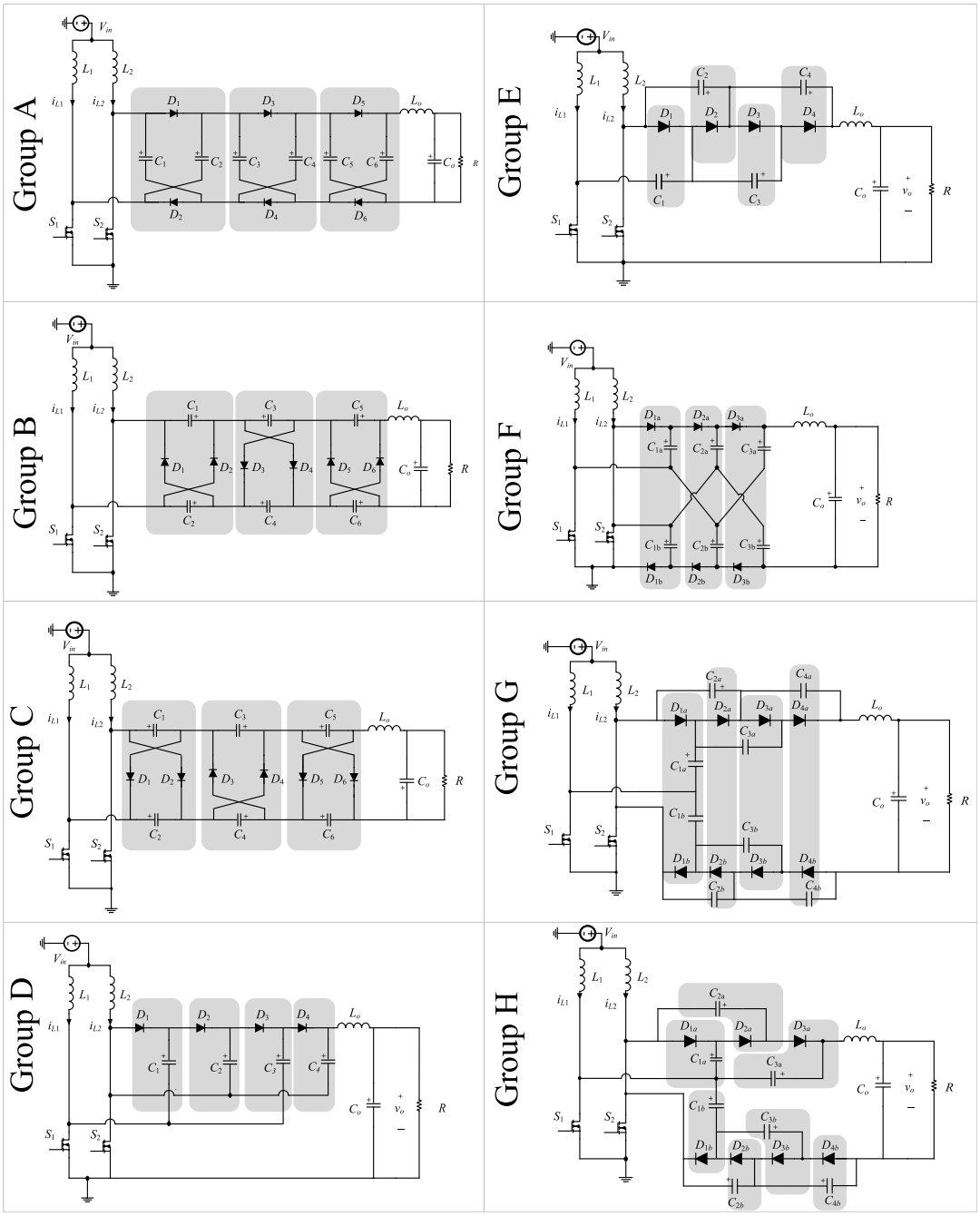

FIGURE 10. Using an output LC filter instead of a diode-capacitor for the same groups aforementioned.

III. MODES OF OPERATION AND STEADY-STATE ANALYSIS OF AN EXAMPLE CONVERTER

This section presents a detailed analysis of the circuit, shown in Fig. 15. The converter is driven by two 180° out phase signals, as shown in Fig. 6. The equivalent circuit of the three modes is shown in Fig. 16 (a-c). The analysis was performed with several assumptions: 1) All components are ideal; 2) The capacitors are large enough that ripples can be neglected; 3) The converter is operating in the steady-state condition; 4) The duty cycles of the active switches are symmetrical; and 5) The converter is fed by a single voltage source.

A. MODE 1: BOTH MOSFETS ARE ON

In this mode, both inductors draw energy from the source, and all diodes are in reverse biased mode. The voltage across the inductors is given by

$$v_{L_1} = v_{L_2} = V_{in}. \tag{10}$$

B. MODE 2: S_1 IS ON AND S_2 IS OFF

In this mode L_1 still draws energy from the source, L_2 discharges into the VMC capacitors, and all diodes are in reverse biased mode. The voltage across the inductors is

TABLE 1. Comparison of different interleaved DC-DC converters.

Group	Output	Diodes/stage	Caps/stage	With output diode and capacitor filter (Figs. 8 and 9)		With LC filter (Fig. 10)	
				Ideal voltage gain	$\frac{\langle I_{L_1}\rangle}{\langle I_{L_2}\rangle}$	Ideal voltage gain	$\frac{\langle I_{L_1}\rangle}{\langle I_{L_2}\rangle}$
A	Floating	2	2	$\frac{2N+1}{1-d}$	$\frac{N}{N+1}$	$\frac{2N}{1-d}$	$\begin{cases}\frac{N-1+d}{N+1-d} & N\ even\\ \frac{N-d}{N+d} & N\ odd\end{cases}$
B	Floating/ inverting	2	2	$\begin{cases}\frac{-(2N+1)}{1-d} & N\ even\\ \frac{2N+1}{1-d} & N\ odd\end{cases}$	$\frac{N+1}{N}$	$\begin{cases}\frac{-(2N)}{1-d} & N\ even\\ \frac{2N}{1-d} & N\ odd\end{cases}$	$\begin{cases}\frac{N+1-d}{N-1+d} & N\ even\\ \frac{N+d}{N-d} & N\ odd\end{cases}$
C	Floating/ inverting	2	2	$\begin{cases}\frac{-(2N+1)}{1-d} & N\ odd\\ \frac{2N+1}{1-d} & N\ even\end{cases}$	$\frac{N}{N+1}$	$\begin{cases}\frac{-(2N)}{1-d} & N\ odd\\ \frac{2N}{1-d} & N\ even\end{cases}$	$\begin{cases}\frac{N-d}{N+d} & N\ odd\\ \frac{N+d-1}{N+1-d} & N\ even\end{cases}$
D	Grounded	1	1	$\frac{N+1}{1-d}$	$\begin{cases}\frac{N}{N+2} & N\ even\\ 1 & N\ odd\end{cases}$	$\frac{N+1-d}{1-d}$	$\begin{cases}\frac{N+1-2d}{N+1} & N\ odd\\ \frac{N}{N+2(1-d)} & N\ even\end{cases}$
E	Grounded	1	1	$\frac{N+1}{1-d}$	$\begin{cases}\frac{N}{N+2} & N\ even\\ 1 & N\ odd\end{cases}$	$\frac{N+1-d}{1-d}$	$\begin{cases}\frac{N+1-2d}{N+1} & N\ odd\\ \frac{N}{N+2(1-d)} & N\ even\end{cases}$
F	Floating	2	2	$\frac{2N+1}{1-d}$	$\frac{N}{N+1}$	$\frac{2N}{1-d}$	$\frac{N+d}{N-d}$
G	Floating	2	2	$\frac{2N+1}{1-d}$	$\frac{N}{N+1}$	$\frac{2N}{1-d}$	$\frac{N+d}{N-d}$
H	Floating	$1/VMC_{dn}$ $1/VMC_{dn}$	$1/VMC_{dn}$ $1/VMC_{dn}$	$\begin{cases}\frac{2\ max(N_{up},N_{dn})}{1-d} & N_{up}+N_{dn}\ odd\\ \frac{N_{up}+N_{dn}}{1-d} & N_{up}+N_{dn}\ even\end{cases}$	1	$\frac{N_{up}+N_{dn}}{1-d}$	$\begin{cases}1 & N_{up}+N_{dn}\ even\\ \begin{cases}\frac{N_{up}-(1-d)}{N_{dn}+(1-d)} & N_{up}>N_{dn}\\ \frac{N_{up}+(1-d)}{N_{dn}-(1-d)} & N_{up}<N_{dn}\end{cases} & N_{up}+N_{dn}\ odd\end{cases}$

TABLE 2. Output voltage at different cases of the input current and duty cycles.

Case	the output voltage
$d_1 \neq d_2$ and $V_{in_1} \neq V_{in_2}$	$\frac{NV_{in_1}}{1-d_1} + \frac{(N+1)V_{in_2}}{1-d_2}$
$d_1 \neq d_2$ and $V_{in_1} = V_{in_2}$	$V_{in}(\frac{N}{1-d_1} + \frac{(N+1)}{1-d_2})$
$d_1 = d_2$ and $V_{in_1} \neq V_{in_2}$	$\frac{1}{1-d}(NV_{in_1} + (N+1)V_{in_2})$
$d_1 = d_2$ and $V_{in_1} = V_{in_2}$	$\frac{(2N+1)V_{in}}{1-d}$

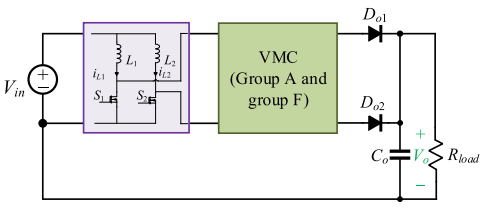

FIGURE 11. Modification to convert a floating output converter to a grounded output converter.

given by

$$v_{L_1} = V_{in}, \tag{11}$$

$$v_{L_2} = V_{in} - V_{C_{1a}} = V_{in} - V_{C_{1b}} = V_{in} + V_{C_{2a}} - V_{C_{3a}} = V_{in} + V_{C_{2b}} - V_{C_{3b}}. \tag{12}$$

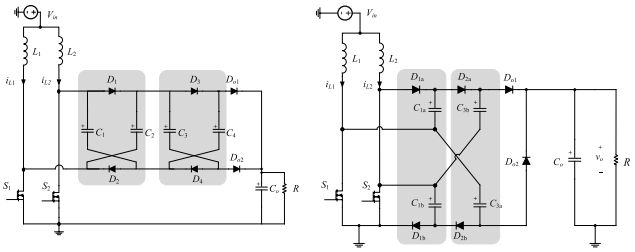

FIGURE 12. Group A and F can be converted to have a grounded output. Both have an ideal voltage gain of $M = \frac{N+1}{1-d}$, which is $\frac{N}{1-d}$ less than the ones with floating outputs.

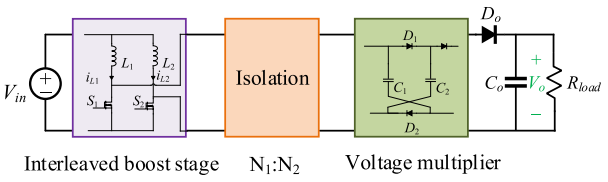

FIGURE 13. The presented family can be modified by adding an isolation device to meet the isolation requirement and improve the voltage gain.

C. MODE 3: S_1 IS OFF AND S_2 IS ON

In this mode L_1 discharges into the VMC capacitors, L_2 draws energy from the source, and all diodes are in reverse biased mode. The voltage across the inductors is given by

$$v_{L_1} = V_{in} + V_{C_{1a}} - V_{C_{2a}} = V_{in} + V_{C_{1b}} - V_{C_{2b}} = V_{in} + V_{C_{3a}} + V_{C_{3b}} - V_o, \tag{13}$$

$$v_{L_2} = V_{in}. \tag{14}$$

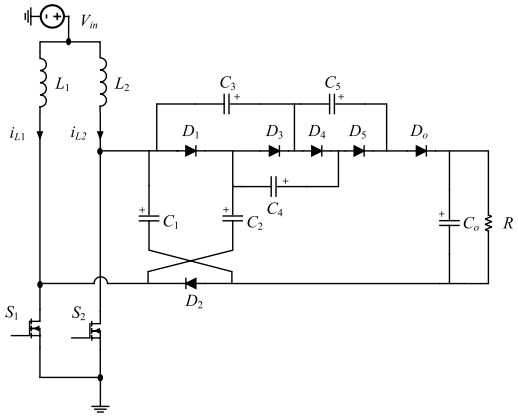

FIGURE 14. Example of nonuniform topologies. The converter features two different types of VMCs, a cell from group F and Cockcroft-Walton VMC.

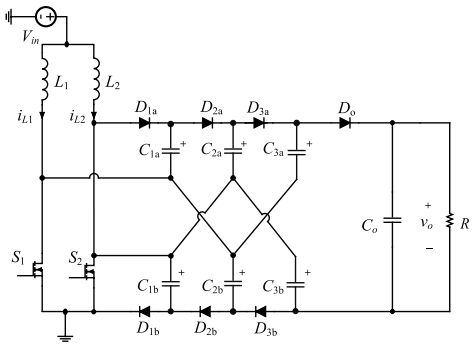

FIGURE 15. Example converter; an interleaved boost stage with a 3 level VMC.

D. STEADY-STATE VOLTAGE GAIN

Steady state equations can be derived from the state equations by a voltage-second balance on the inductors. The average voltage across the inductors is given by

$$\langle v_{L_1} \rangle = \langle v_{L_2} \rangle = 0 \tag{15}$$

The voltage across each first-stage capacitor is given by

$$V_{C_{1a}} = V_{C_{1b}} = \frac{V_{in}}{1-D}. \tag{16}$$

The voltage of each second-stage capacitor is given by

$$V_{C_{2a}} = V_{C_{2b}} = \frac{2V_{in}}{1-D}. \tag{17}$$

Each third-stage capacitor's voltage is given by

$$V_{C_{3a}} = V_{C_{3b}} = \frac{3V_{in}}{1-D}. \tag{18}$$

Therefore, the output voltage transfer function is given by

$$M = \frac{V_o}{V_{in}} = \frac{7}{1-D}. \tag{19}$$

For N number of VMC stages, the transfer function is given by

$$M = \frac{2N+1}{1-D}. \tag{20}$$

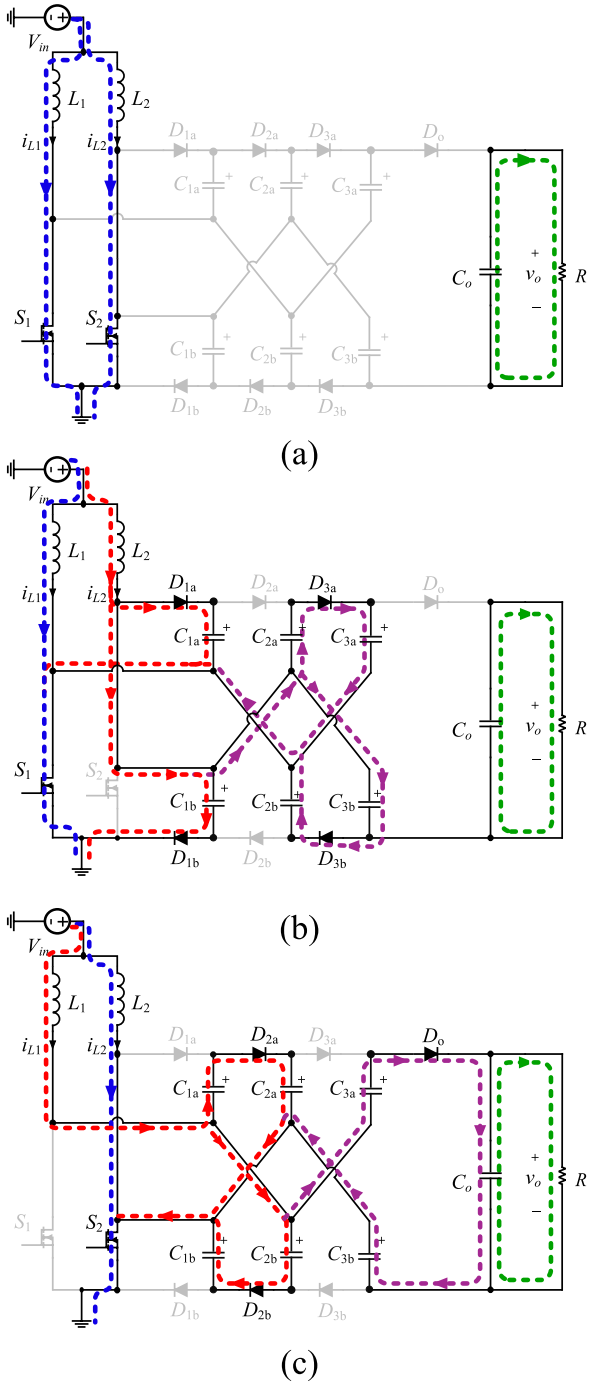

FIGURE 16. Modes of operation of the example converter; (a) mode 1 (b) mode 2 (c) mode 3.

The previous analysis was for a converter that is being fed by a single source, and equal duty cycles were assumed. The proposed converter is capable of being fed by two independent voltage sources, e.g., different PV panels, as shown in Fig. 17. Also, it can operate at different duty ratios, which is suitable for tracking the maximum power point for each PV panel. The table 2 summarizes the voltage gain in cases with two different sources and asymmetrical duty cycles.

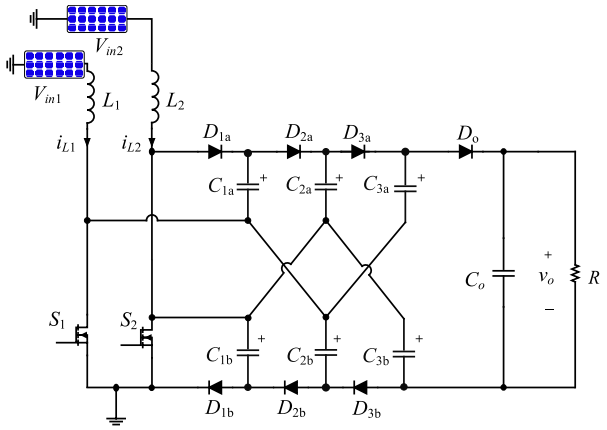

FIGURE 17. The example converter can convert the voltage from two independent power sources.

IV. COMPONENT SELECTIONS AND EFFICIENCY ANALYSIS

This section presents details about the design and component selections of the example converter.

A. INDUCTOR SELECTION

The critical inductance that ensures CCM operation is given by

$$L_{1_{crit}} = \frac{Rd(1-d)^2}{N(2N+1)f_s}, \tag{21}$$

$$L_{2_{crit}} = \frac{Rd(1-d)^2}{(N+1)(2N+1)f_s}. \tag{22}$$

However, to select an inductor based on the percentage of the ripple, one should follow

$$L_1 = \frac{V_{in}d}{\Delta i_{L_1} f_s}, \tag{23}$$

$$L_2 = \frac{V_{in}d}{\Delta i_{L_2} f_s}. \tag{24}$$

The average current passing through inductors L_1 and L_2 is as follows:

$$I_{L_{1,avg}} = \frac{V_o}{R}\frac{N}{(1-d)}, \tag{25}$$

$$I_{L_{2,avg}} = \frac{V_o}{R}\frac{N+1}{(1-d)}. \tag{26}$$

The peak currents can be calculated as follows:

$$I_{L_{1,pk}} = \frac{V_o}{R}\frac{N}{(1-d)} + \frac{dV_{in}}{Lf_s}, \tag{27}$$

$$I_{L_{2,pk}} = \frac{V_o}{R}\frac{N+1}{(1-d)} + \frac{dV_{in}}{Lf_s}. \tag{28}$$

The RMS currents are given by

$$I_{L_{1,rms}} = \sqrt{\left(\frac{V_o N}{R(1-d)}\right)^2 + \left(\frac{dV_{in}}{2\sqrt{3}Lf_s}\right)^2}, \tag{29}$$

$$I_{L_{2,rms}} = \sqrt{\left(\frac{V_o(N+1)}{R(1-d)}\right)^2 + \left(\frac{dV_{in}}{2\sqrt{3}Lf_s}\right)^2}. \tag{30}$$

B. ACTIVE SWITCHES SELECTION

The voltage stress across MOSFETs can be calculated by

$$V_{S_1} = V_{S_2} = \frac{V_{in}}{1-d} \tag{31}$$

and the average current passing through the MOSFETs is given by

$$I_{S_{1,avg}} = \frac{V_o}{R}\left(\frac{dN}{1-d} + N + 1\right), \tag{32}$$

$$I_{S_{2,avg}} = \frac{V_o}{R}\left(\frac{d(N+1)}{1-d} + N\right). \tag{33}$$

The maximum input current passing through the MOSFETs is given by

$$I_{S_{1,pk}} = I_{S_{2,pk}} = \frac{V_o(2N+1)}{R(1-d)} + \frac{V_{in}(2d-1)}{Lf_s}. \tag{34}$$

The root mean square value of the switch current is given by

$$I_{S_{1_{rms}}} = \sqrt{\left(\frac{V_o}{R}\left(\frac{dN}{1-d}+N+1\right)\right)^2 + \left(\frac{(2N+1)V_{in}(2d-1)}{2Lf_s}\right)^2}, \tag{35}$$

$$I_{S_{2,rms}} = \sqrt{\left(\frac{V_o}{R}\left(\frac{d(N+1)}{1-d}+N\right)\right)^2 + \left(\frac{(2N+1)V_{in}(2d-1)}{2Lf_s}\right)^2}. \tag{36}$$

C. DIODE SELECTION

The voltage stress across the diodes is a function of the number of stages. The voltage stress is reduced as the number of stages increases, and that comes at the cost of efficiency. The voltage stress is given by

$$V_D = \frac{2V_o}{(2N+1)}. \tag{37}$$

The average current passing through each diode can be calculated by

$$I_{D_N,avg} = I_o \tag{38}$$

and the RMS value of the diodes can be calculated as

$$I_{D,rms} = I_o\sqrt{\frac{1}{1-d}}. \tag{39}$$

D. CAPACITOR SELECTION

The capacitor is selected based on the tolerated voltage ripple, and it can be calculated using the following equation

$$C = \frac{I_o(1-d)}{f\Delta v}. \tag{40}$$

The RMS value of the current passing through the output capacitor is given by

$$I_{C_{o,rms}} = I_o\sqrt{\frac{d}{(1-d)}} \tag{41}$$

and the RMS current of the other capacitors can be calculated by

$$I_{C_{n,rms}} = I_o(1 + \sqrt{\frac{d}{(1-d)}}) \tag{42}$$

V. POWER LOSSES AND EFFICIENCY ANALYSIS

The power losses in the inductors are given by

$$P_L = I^2_{L1,rms} DCR_1 + I^2_{L2,rms} DCR_2 \tag{43}$$

where DCR_1 and DCR_2 are the DC resistance.

The power losses in the active switches can be divided into two parts: switching loss and conduction loss. The switching loss can be calculated using the following equation:

$$P_{SW} = 2(\frac{1}{2} \times I_{L,avg} \times V_S \times (t_{OFF} + t_{ON}) f_s + \frac{1}{2} \times f_s \times C_{oss} \times V_S^2). \tag{44}$$

The conduction loss part is given by

$$P_{S,conduction} = I^2_{s_{1,rms}} R_1(on) + I^2_{S_{2,rms}} R_2(on) \tag{45}$$

where $R_1(on)$ and $R_2(on)$ are the drain-source resistance of S_1 and S_2. The power loss in the diodes can be calculated by

$$P_D = \sum_{i=1}^{N} I_{D_{avg}} \times V_F + \sum_{i=1}^{N} I_{D_{rms}} \times r_f \tag{46}$$

where V_F is the forward voltage of the diode, and r_f is the bulk resisor. The power loss in the capacitors due to the equivalent series resistance (ESR) is given by

$$P_{C,total} = N I^2_{C_{n,rms}} ESR_n + I^2_{C_{o,rms}} ESR_o. \tag{47}$$

The total loss is given by

$$P_{loss} = P_{D,total} + P_{C,total} + P_{S,conduction} + P_{SW} + P_L \tag{48}$$

The overall efficiency of the converter is given by

$$\eta\% = \frac{P_o}{P_{loss} + P_o} \times 100. \tag{49}$$

VI. SIMULATION

The example converter was simulated in PLECS/MATLAB, with a maximum time step of 10^{-7} s and tolerance of 10^{-3}. The parameters used in the simulation are listed in Table 3. The major waveforms are plotted in Fig. 18. The voltage stress across the active switches is 57 V. The average current on L_1 and L_2 is 4.28 A and 5.7 A, respectively. The maximum voltage across the diodes is 114 V. The average and effective values of the current passing through each diode are 0.5 A and 0.84 A. The voltage across the capacitors is shown in Fig. 19. The currents passing through the diodes and capacitors are shown in Fig. 20 and Fig. 21, respectively. The first-stage capacitors C_{1_A} and C_{1_B} have a voltage of 57 V, the second-stage capacitors have a voltage of 114 V, and the third-stage capacitors have a voltage of 171 V. The RMS current of the output capacitor is 0.68 A, while the other capacitors have an RMS current of 1.18 A. The efficiency analysis was performed using the loss equations of the components and the rating from the datasheets of the components used for implementing the hardware prototype. The approximate loss breakdown and breakdown percentage as a function of the output load is depicted in Fig. 22. The total loss at 200 W is about 4.98 W. The major source of loss is the conduction loss in the diodes, which counts for about 68%. The conduction loss in the MOSFETs is about 13%, and the switching loss is about 7% of the total loss. The conduction loss in the inductors counts for about 11%, and the total loss caused by the ESR of the capacitors is less than 1%.

TABLE 3. List of Parameters used in simulation.

Parameter	Value
Input voltage	20 V
Output voltage	400 V
Load resistance	800 Ω
Ideal duty cycle	0.65
Switching frequency	100 kHz
Inductors	100 μH
Capacitors	10 μF

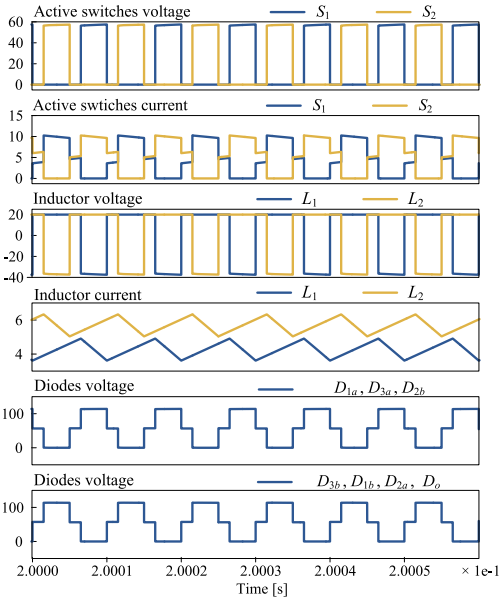

FIGURE 18. Simulation waveforms of voltages and currents across semiconductor switches and inductors.

VII. EXPERIMENTAL IMPLEMENTATION AND RESULTS

A 200 W hardware prototype was implemented and tested to further verify the operation of the example converter. The components used to construct the hardware prototype are listed in Table 4, and the experimental setup is shown in Fig. 23. The converter was designed for a nominal duty cycle of 0.65 and increased to roughly 0.657 to compensate for the gain reduction caused by the diodes' forward voltage

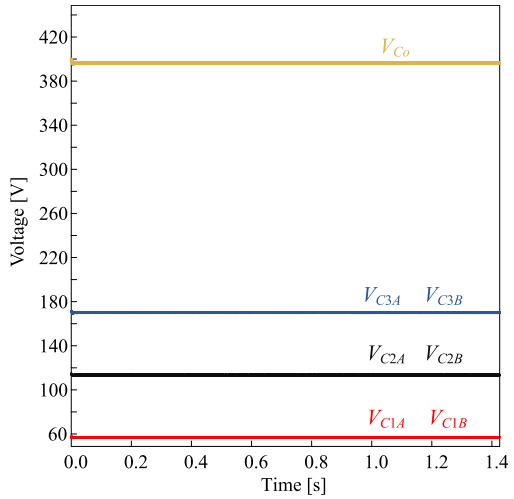

FIGURE 19. Simulation waveforms of the capacitors' voltage and the output voltage in the steady-state.

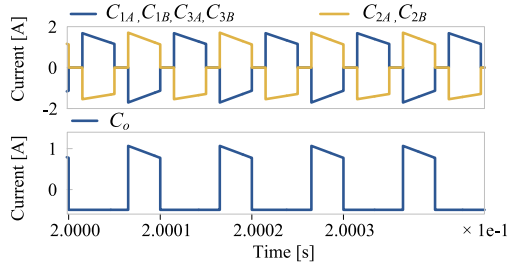

FIGURE 20. Simulation of the capacitors' currents.

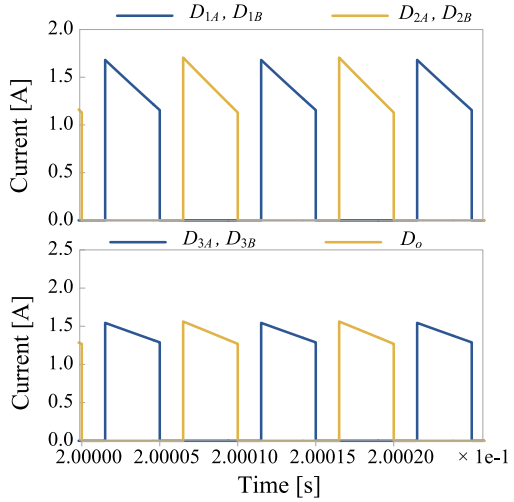

FIGURE 21. Simulation waveforms of the diodes' currents.

and losses in wires. The *AFG*3052*C* signal generator was used to generate gate signals with a switching frequency of 50 *kHz*. The converter is fed by 20 *V*, where *N*5700 power supply is used, and the output load is implemented using ceramic resistors with various values. The voltage stress across the active switches and diodes are shown in Fig. 24, which supports the simulation results as the voltage across

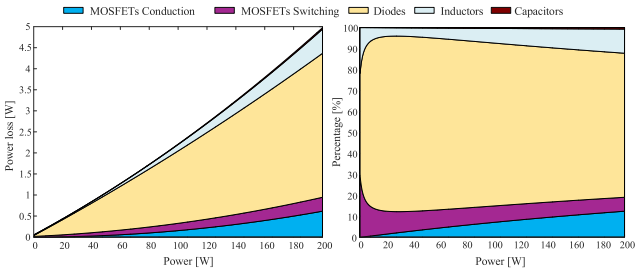

FIGURE 22. Efficiency analysis of the example converter; the actual losses (left) and the loss breakdown (right).

TABLE 4. List of Components used for the hardware prototype.

Item	Designation	Rating	Part No.
Inductor	L_1, L_2	$100\ \mu H$, $DCR = 25\ m\Omega$,	60B104C
Capacitor	C_{1A}, C_{2A} $C_{1B} C_{2B}$ $C_{3A} C_{3B}$	$10\ \mu$F	B32674D3106K
Capacitor	C_o	$22\ \mu$F	B32774D4226K000
MOSFET	Q_1, Q_2	$150\ V, 37\ A$ $R_{ds(on)} = 10.525\ m\Omega$	IPA105N15N3
Diode	D_{1A}, D_{2A} D_{1B}, D_{2B}	$250V, 40A$ $V_F = 0.86\ V, t_{rr} = 35\ ns$	MBR40250G
load	R_{load}	multiple values	L100J100E, L225J50RE L225J250E,L225J500E

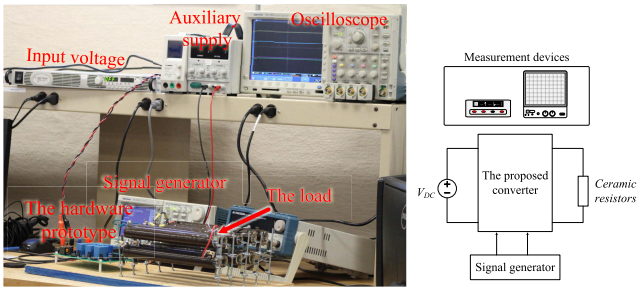

FIGURE 23. The hardware prototype and the experimental setup.

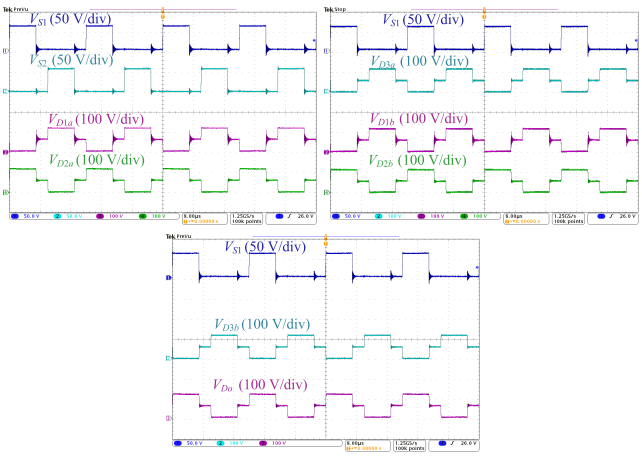

FIGURE 24. Experimental results of the voltage across the active switches and the diodes.

the active switches equals 57 *V*, and the maximum voltage stress across the diodes equals 124 *V*. The voltage across the capacitors is shown in Fig. 25. The voltage across each

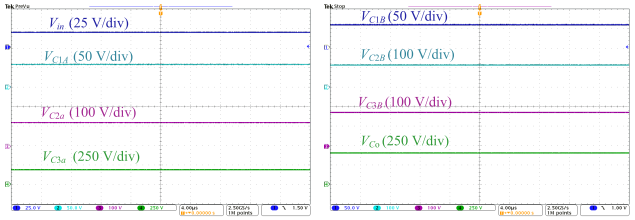

FIGURE 25. Experimental results of the voltage across the capacitors.

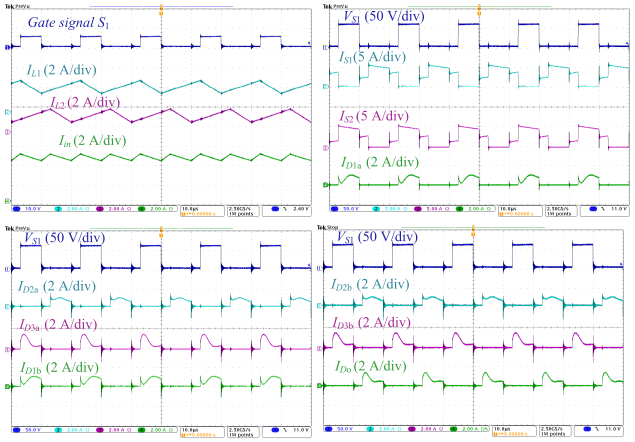

FIGURE 26. Experimental results of the input current, inductor currents, active switches and diode currents.

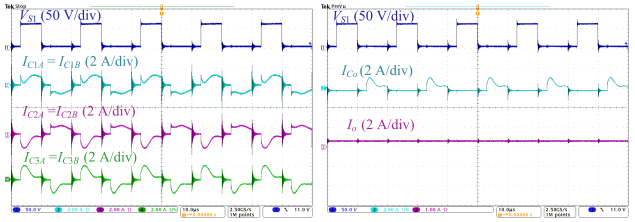

FIGURE 27. Experimental results of the capacitors' currents and the output current.

capacitor in the first stage equals 57 V, in the second stage equals 133 V, and in the third stage equals 200 V. The output voltage equals 400 V. The current waveforms of inductors and switches were acquired at $\approx$ 100 W, as shown in Fig. 27. The peak efficiency of the converter is about 97% at 160 W and about 96.3% at 200 W.

VIII. CONCLUSION

In this paper, the family of an interleaved boost converter with voltage multiplier cells was presented. The general structure of the family consists of two sections: an interleaved boost stage and voltage multiplier cells. The structure comes in two configurations. Configuration 1's output is filtered using an output diode and a capacitor filter, where configuration 2's output is filtered using an LC filter. The difference between the two configurations was explained, and a comparison between the various family members was presented. An example of this family was given with a detailed steady-state analysis and component selection, which was evinced by simulation. A 200-W hardware prototype was implemented to further verify the analysis and the simulation. The converter is capable of drawing power from both a single or dual independent input voltage and with the same or different duty cycles of the active switches. These cases were summarized and compared. The family has good features besides the high-voltage gain. The input current ripple has twice frequency of the one in the conventional boost converter, which reduces the filter requirements and increases the accuracy of the current sensing for better tracking of MPPT. Although the converter is efficient, the efficiency can be further increased by either replacing the diodes with better ones or with active switches, with a trade-off of the complexity.

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