IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received November 19, 2018, accepted December 17, 2018, date of publication January 7, 2019, date of current version January 23, 2019.

Digital Object Identifier 10.1109/ACCESS.2018.2889165

A D-Band Multiplier-Based OOK Transceiver With Supplementary Transistor Modeling in 65-nm Bulk CMOS Technology

BOHEE SUH[1], (Member, IEEE), HYUNKYU LEE[2], (Student Member, IEEE), SOOYEON KIM[2], (Student Member, IEEE), AND SANGGEUN JEON[2], (Member, IEEE)

[1]Samsung Electronics Company, Suwon 16677, Korea
[2]Schhool of Electrical Engineering, Korea University, Seoul 136-713, Korea

Corresponding author: Sanggeun Jeon (sgjeon@korea.ac.kr)

This work was supported by the Institute for Information and Communications Technology Promotion(IITP) grant funded by the Korea Government (MSIT) (No. B0717-16-0047).

ABSTRACT A D-band on–off keying (OOK) transceiver chipset is fabricated in a 65-nm bulk CMOS technology as a low-cost and highly integrative solution to short-distance wireless connectivity. Supplementary transistor modeling is performed for accurate circuit design at mm-wave frequencies. To overcome low transistor f_{max} and reduce dc power consumption, the transmitter employs a frequency-multiplier-based architecture with no power amplifier. The receiver adopts a non-coherent architecture consisting of a dc-coupled three-stage differential amplifier and an envelope detector. The OOK transmitter exhibits a measured output power of −9.8 dBm and an on–off level difference of 13.2 dB at 134.1 GHz. The receiver shows a measured average responsivity of 4.1 kV/W and a noise equivalent power of 211.4 pW/Hz$^{1/2}$ over all D-band frequencies. The dc power consumption of the transmitter and the receiver is 76 and 32.5 mW, respectively. The transceiver is tested in both on-chip loopback and air-channel configurations and demonstrates data transmission up to 10 and 2 Gb/s at a distance of 0.03 m, respectively.

INDEX TERMS D-band, low-cost bulk CMOS, OOK, transceiver, transistor modeling, wireless communication.

I. INTRODUCTION

Demand for short-distance high-speed wireless communication has continued to increase due to the explosive growth of data traffic in WPAN and IoT devices [1], [2]. Microwave frequencies have been predominantly employed for diverse commercial and military purposes. The mm-wave band is now considered an alternative frequency resource that can meet the increased demand. Several on-off keying (OOK) transceivers have been reported at mm-wave bands, especially the V-band [3]–[7]. The OOK architecture is appropriate for massive short-distance communications between chips, boards, and devices due to its simplicity, low DC consumption, and small chip size.

Recently, an upper mm-wave band beyond 100 GHz has attracted considerable attention as a promising spectrum for the OOK transceiver system. Compared to the mm-wave frequencies below 100 GHz, the upper band has several benefits. It offers a continuously available wider bandwidth and thus enables a higher data rate which is directly proportional to the bandwidth in the OOK system. Furthermore, if the carrier frequency increases, the fractional bandwidth is reduced, which enables simpler RF circuit design. This additionally reduces the chip and antenna size, thus allowing for a small form factor of the transceiver system.

Traditionally, transceivers at the upper mm-wave band have been fabricated using compound semiconductor technologies [8]–[10]. Recently, owing to rapid advancement of silicon technologies, several silicon-based OOK transceivers have been reported at the upper mm-wave band [11]–[19]. However, they primarily rely on sophisticated device technologies, such as deeply-scaled CMOS, SOI, or SiGe technologies. Consequently, they suffer from high cost and limited accessibility. It should be noted that a majority of application devices and sensors (such as for the IoT or WPAN) requiring wireless connectivity are still implemented in less-scaled bulk technologies because they do not require a high transistor speed. Therefore, it is worth developing a transceiver using the same low-cost and easily-accessible

technologies at the upper mm-wave band. This would enable seamless integration of the transceiver with the application devices and sensors and thus lower the manufacturing cost.

In this paper, a D-band OOK transmitter and receiver chip set is implemented using a 65-nm bulk CMOS technology. Compared to previous D-band transceivers that were fabricated predominantly through highly-scaled processes, such as 32-nm and 40-nm nodes, or by means of SOI technologies [14]–[17], this work demonstrates a relatively low-cost and highly-integrative solution to short-distance wireless connectivity.

Since the given bulk technology was not originally intended for upper-mm-wave circuit design, several design challenges exist, such as limited model accuracy and low transistor speed. To improve the model accuracy at upper mm-wave frequencies, a simple supplementary modeling is performed on top of the original transistor model, as described in Section II. To overcome the low transistor speed, *i.e.* a low transistor f_{max}, a multiplier-based architecture that has no power amplifier (PA) is adopted in the transmitter. The entire transceiver architecture and link budget are presented in Section III. In Section IV, the design of each circuit block comprising the D-band OOK transceiver is presented with the measurement result. Section V provides the measured performance of the integrated transmitter and receiver, followed by a demonstration of wireless data transmission using the transceiver chipset.

II. SUPPLEMENTARY EMPIRICAL TRANSISTOR MODELING

Although a transistor model is provided by the fabrication foundry, the model accuracy becomes degraded as the operating frequency increases. This is because the extrinsic RLC components distributed in the transistor pads are usually underestimated in bulk CMOS technologies. This results in a non-negligible discrepancy between simulation and measurement in the circuit design at mm-wave frequencies [20]. Therefore, supplementary modeling is performed to the original transistor model to improve the model accuracy. As shown in Fig. 1, the extrinsic distributed RLC components are simply modeled as six supplementary extrinsic components (R_g, R_d, R_s, L_g, L_d, L_s, C_{gs}, C_{gd}, and C_{ds}), and are added to the original transistor model. While not rigorously precise, the proposed empirical model enables a quick and efficient correction of the original model, thus making it suitable for mm-wave circuit design.

The supplementary extrinsic component values are empirically extracted from the measured S-parameters of transistors of various sizes. It is difficult to precisely de-embed the effect of RF probing pads and feed structures at upper mm-wave frequencies. Therefore, the supplementary modeling is fulfilled up to 50 GHz and is extrapolated toward D-band frequencies. Nonetheless, the accuracy of the extrapolated model is confirmed by V-band and D-band circuit design described in Section IV.

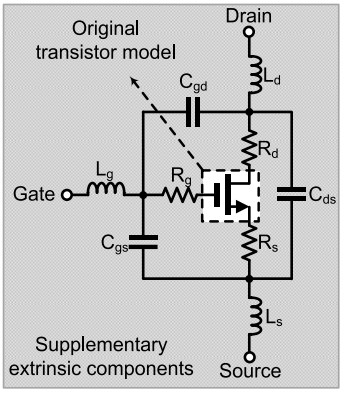


FIGURE 1. Proposed transistor model with supplementary extrinsic RLC components added to the original model.

TABLE 1. Supplementary Extrinsic Component Values Extracted In This Work.

Extrinsic component	Empirically extracted value
R_g, R_d (Ω)	$10 \times W / N_f$
R_s (Ω)	$20 \times W / N_f$
C_{gs}, C_{gd}, C_{ds} (fF)	$0.067 \times W \times N_f$
L_g, L_d, L_s (pH)	6

W: Width of gate finger, N_f: Number of gate fingers

Table 1 presents the extrinsic component values extracted for the corrected transistor model in this work. These values are scalable with the width (W) and number (N_f) of gate fingers.

III. TRANSCEIVER ARCHITECTURE AND LINK BUDGET

Fig. 2 shows the maximum available gain (MAG) or maximum stable gain (MSG) of a $2 \times 10 - \mu$m transistor of the 65-nm bulk CMOS technology employed in this work. Compared to the original model, the corrected model described in Section II predicts that the transistor f_{max} is significantly lower than 200 GHz. The low f_{max} makes it challenging to design active circuit blocks at D-band frequencies. Therefore, the D-band OOK transceiver in this work demands a new architecture that overcomes the low f_{max}.

Fig. 3(a) shows a block diagram of the proposed D-band OOK transmitter, consisting of a carrier generator and a modulator. Instead of a D-band fundamental oscillator, a V-band-oscillator-multiplier chain is employed to generate the carrier signal due to the low transistor f_{max} of the given technology. A harmonic oscillator can be considered an alternative solution to D-band carrier generation; nevertheless, it exhibits lower output power and DC-to-RF efficiency than the proposed multiplier-based carrier generator [21], [22].

The OOK modulator can be designed as either an active or passive type. The active type can yield a high gain if implemented using an advanced transistor technology, albeit at the expense of high DC power consumption [16], [17]. However, in the technology used in this work, this benefit is not available because of the limited transistor MAG.

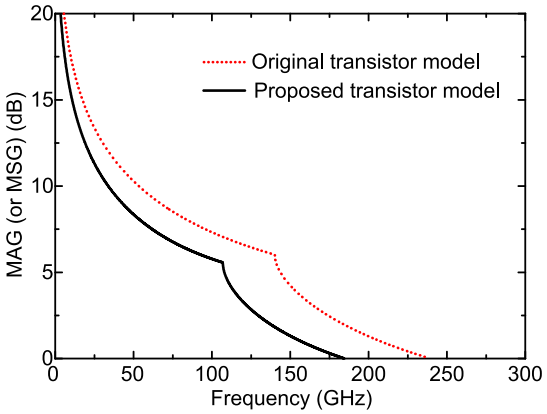


FIGURE 2. MAG (or MSG) of a 2x10-μm transistor simulated by the original and proposed transistor models.

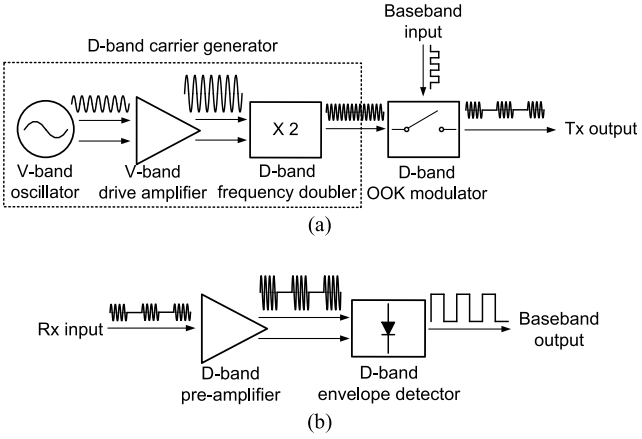


FIGURE 3. Block diagram of the proposed D-band OOK (a) transmitter and (b) receiver.

Thus, we employ a passive switched-type modulator that reduces the DC power consumption of the transmitter.

A PA design presents another challenge because a large transistor size further lowers f_{max} and MAG at the operating frequency. For example, transistor f_{max} with a large gate width of $3 \times 30\mu$m decreases to 125 GHz. Nonetheless, the OOK modulation scheme demands a lower receive SNR and thus a lower transmit power than advanced modulation schemes, such as QPSK and QAM [23]. Therefore, a PA-less architecture is employed in the transmitter in this work to target short-distance communication with low DC power consumption.

The D-band OOK receiver is shown in Fig. 3(b). It adopts a non-coherent architecture consisting of a D-band pre-amplifier and an envelope detector. Compared to a mixer-based coherent OOK receiver [13], it reduces the complexity and DC power consumption. The pre-amplifier is used to compensate the high air-channel loss and improve the noise performance of the receiver. To achieve a positive gain at the frequency close to the transistor f_{max}, an inter-stage DC-couple technique is used, as described in Section IV-E. An input balun is included in the amplifier for a single-ended antenna feed.

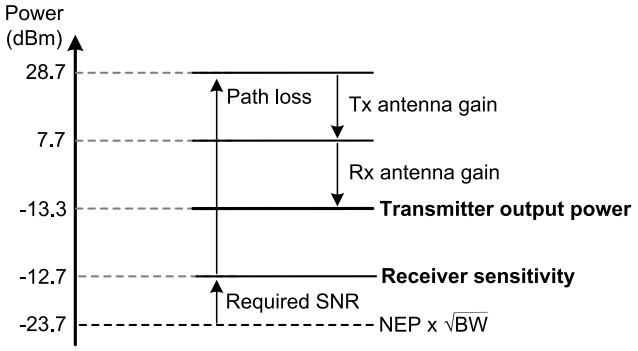


FIGURE 4. Link budget calculation for 1-Gbps OOK wireless communication at 0.02 m.

As depicted in Fig. 4, a link budget for 1-Gbps OOK wireless communication at 0.02 m is calculated to estimate the output power required from the transmitter. In non-coherent OOK architecture, the receiver sensitivity can be expressed approximately as [24]:

$$P_{sen}(dBm) = NEP(dBm/\sqrt{Hz}) + 10\log\sqrt{BW} + SNR_{\min}(dB), \quad (1)$$

where NEP is the noise equivalent power of the receiver, BW is the frequency bandwidth, and $SNR_{\min}$ is the minimum SNR required for OOK demodulation. According to the pre-simulation, receiver NEP is 95.9 pW/Hz$^{1/2}$ at 140 GHz. The $SNR_{\min}$ with a bit error rate (BER) of 10^{-3} is approximately 11 dB [25]. Considering BW of 2 GHz needed for a 1-Gbps data rate, the receiver sensitivity is calculated as -12.7 dBm. According to the Friis transmission formula [26], free-space path loss over a distance of 0.02 m is 41.4 dB at 140 GHz. The antenna gain is assumed to be 21 dBi as a typical value for commercial D-band horn antennas [27]. Then, the minimum output power demanded from the transmitter is finally calculated as -13.3 dBm.

IV. CIRCUIT BLOCK DESIGN

The complete schematics of the D-band OOK transmitter and receiver are shown in Fig. 5(a) and (b), respectively. All circuit blocks adopt a differential topology to exploit the virtual ground except the D-band modulator. The transmission lines are implemented using a microstrip line structure with a 1.2-um thick top metal used for signal and M1 for ground. The Q-factor of the microstrip line is 55.2 at 140 GHz. Each circuit block is individually designed and tested before integration into the transceiver chipset.

A. V-BAND OSCILLATOR

The V-band oscillator consists of a cross-coupled oscillation core (M_1 and M_2) and a source-following buffer (M_3 and M_4) as shown in Fig. 5(a). The gate width of M_1 and M_2 is determined with consideration of the trade-off between the oscillation startup condition and the inductance required in the LC tank. As shown in Fig. 6(a), the conductance seen looking into the oscillation core (G_{in}) has a more negative value as the gate width increases, thus facilitating oscillation

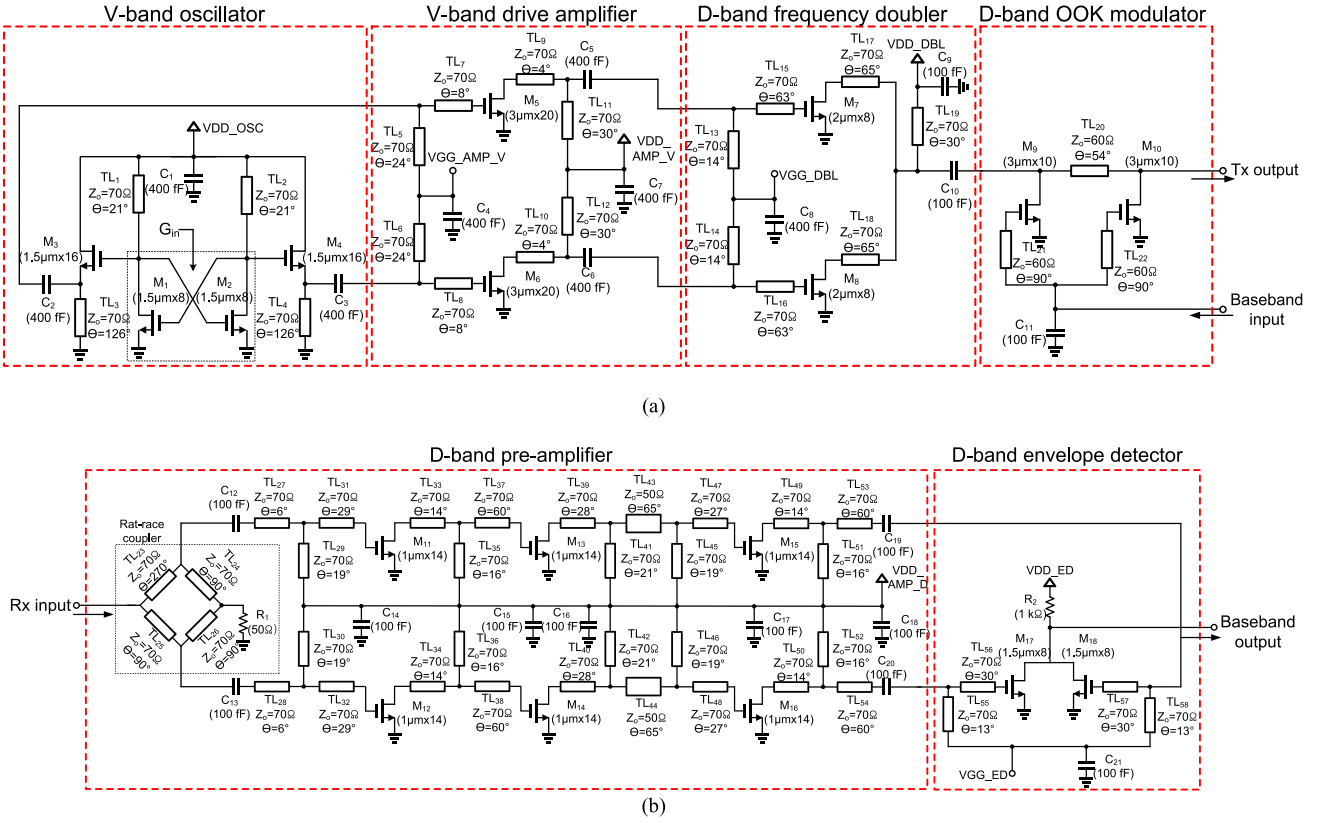


FIGURE 5. Complete schematics of the D-band OOK (a) transmitter and (b) receiver. The electrical length of transmission lines is calculated at 70 GHz for V-band circuits and at 140 GHz for D-band circuits.

startup. On the other hand, the larger gate width increases parasitic capacitance, thus dramatically reducing the inductance value required at the output LC tank. A small inductance ($<$100 pH) is typically implemented using a short transmission line. If the line is too short, it will suffer from high sensitivity to process variation, and layout difficulty. Therefore, the gate width is determined as 12 μm. The tank inductance, calculated as 122 pH, is implemented by high-impedance transmission lines (TL_1 and TL_2) with an electrical length of 21° at 70 GHz.

Fig. 6(b) and (c) show a schematic and a chip micrograph of the oscillator test cut, respectively. One of the differential output ports is terminated by an on-chip 50-Ω resistor for measurement purposes. The measured output power and spectrum are shown in Fig. 6(d). With a drain bias of 1.2 V, the oscillator exhibits a single-ended output power of 0.2 dBm at 67.8 GHz. The output power will further increase by 3 dB if the output is differentially obtained. It should be noted that the simulation based on the corrected transistor model proposed in Section II is -0.2 dBm at 69.1 GHz. This result agrees well with the measurement, and thus validates the model accuracy. The DC power consumption is 42 mW.

B. V-BAND DRIVE AMPLIFIER

The V-band drive amplifier adopts only a single stage of the common-source transistors (M_5 and M_6 in Fig. 5(a)) to reduce DC power consumption. Since the amplifier is used to provide sufficient drive power to the subsequent D-band frequency doubler, the maximum output power available from a single transistor is simulated at different gate widths, as shown in Fig. 7(a). The gate width of M_5 and M_6 is thus determined as 60 μm because a further width increase rather reduces the output power due to larger parasitic capacitance.

Fig. 7(b) and (c) show a schematic and a chip micrograph of the V-band amplifier test cut, respectively. For measurement purposes, a Marchand balun is added to both the input and output. As depicted in Fig. 7(d), the amplifier exhibits a positive gain over the entire V-band frequencies with a peak gain of 5 dB. De-embedding the back-to-back balun loss of 2 dB, the gain of the ''differential'' amplifier actually used in the transmitter will be approximately 7 dB. Consequently, the amplifier will generate output power of at least 5 dBm if driven by the previous V-band oscillator. The DC power consumption is 33.6 mW.

C. D-BAND FREQUENCY DOULBER

As shown in Fig. 5(a), the D-band frequency doubler is designed with differential common-source transistors (M_7 and M_8). At the drain of the transistors, the second-harmonic currents are added in-phase, whereas the fundamental is suppressed. Fig. 8(a) shows the second-harmonic

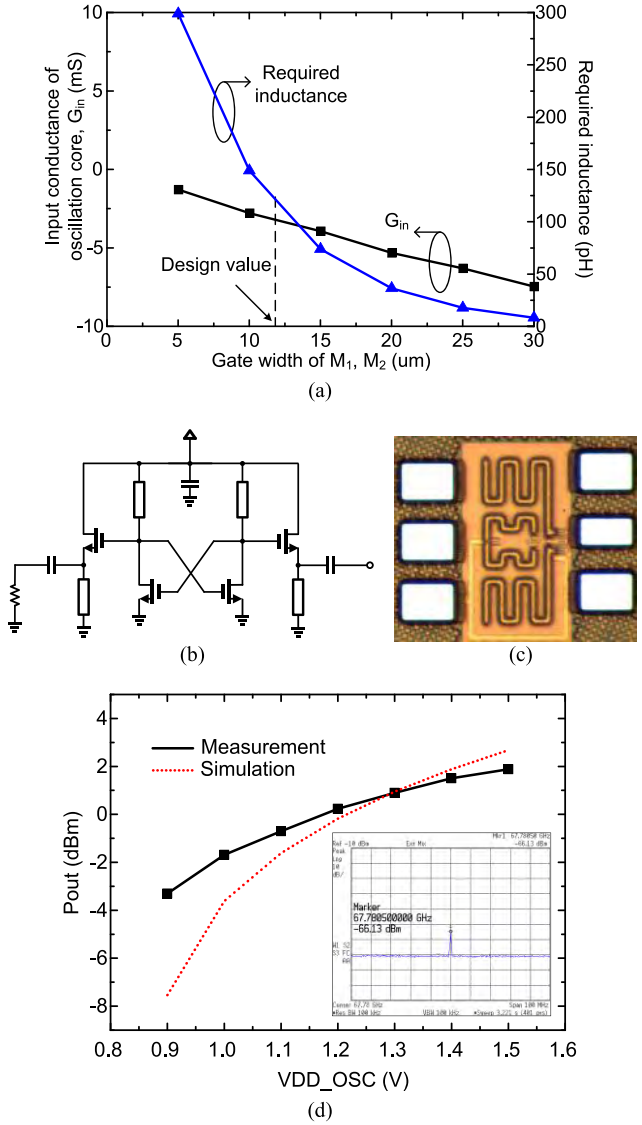


FIGURE 6. (a) Simulated conductance seen looking into the oscillation core and the inductance required at the output LC tank. (b) Schematic and (c) Chip micrograph of the V-band oscillator test cut. (d) Measured output power and spectrum.

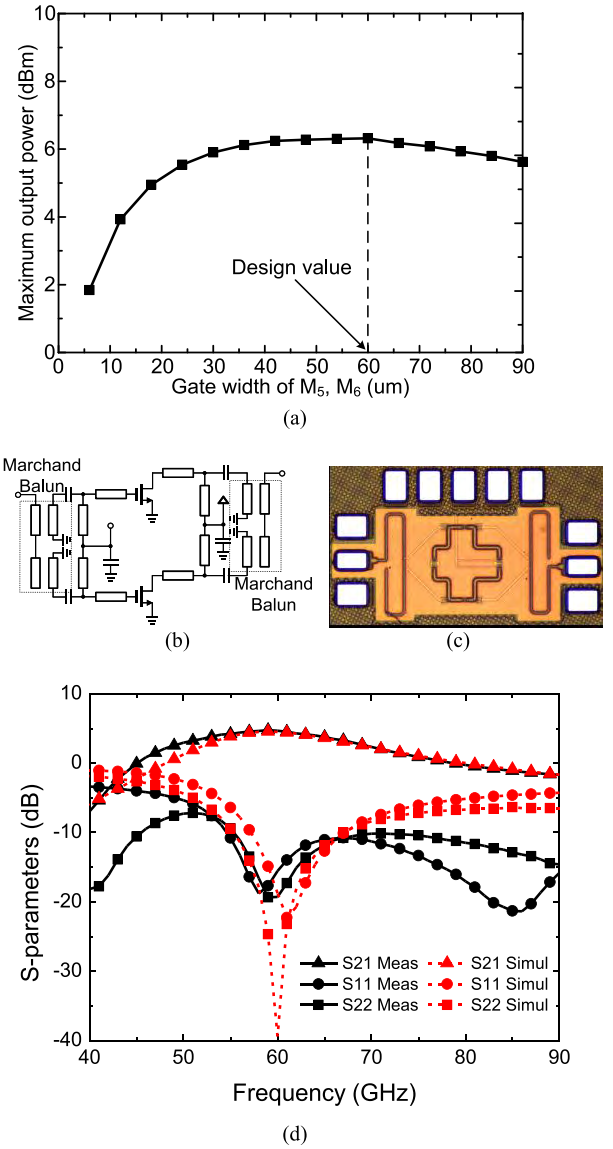


FIGURE 7. (a) Maximum output power available from a single transistor at 70 GHz. (b) Schematic and (c) Chip micrograph of the V-band amplifier test cut. (d) Measured S-parameters.

current normalized to the peak as a function of the gate bias voltage (V_{GG_DBL}). From the simulation, V_{GG_DBL} is chosen as 0.5 V to maximize the conversion gain, while consuming minimal quiescent DC power. Input and output matching are performed at the fundamental and second-harmonic frequencies, respectively, using transmission lines (TL_{13}–TL_{19}).

A schematic and a chip micrograph are shown in Fig. 8(b) and (c), respectively. A Marchand balun is added to the V-band input for measurement purposes. The measured output power and conversion gain are shown in Fig. 8(d). Assuming that the input drive power provided by the preceding stage is 5 dBm, the output power from the doubler reaches −9 dBm.

D. D-BAND OOK MODULATOR

The OOK modulator is designed with a double-shunt transistor (M_9 and M_{10} in Fig. 5(a)) that switches on or off the D-band carrier signal depending on the baseband input. In Fig. 9(a), the on-resistance (R_{on}) and off-capacitance (C_{off}) of the transistor are simulated at different gate widths. It can be seen that a large gate width results in low R_{on}, leading to high isolation of the switch. On the other hand, a small gate width is desirable for low insertion loss of the switch due to low C_{off}. Therefore, the gate width is determined as 30 μm with consideration of the trade-off.

A series transmission line (TL_{20}) is inserted between the two transistors to absorb C_{off} when the switch is in the 'on' state. Thus, the input and output impedances are matched to 50 Ω. The baseband signal is fed into the gate of each transistor through a quarter-wave transmission line (TL_{21} and TL_{22}) at the carrier frequency. Compared to conventional resistive feed methods [28], this reduces the RC time constant

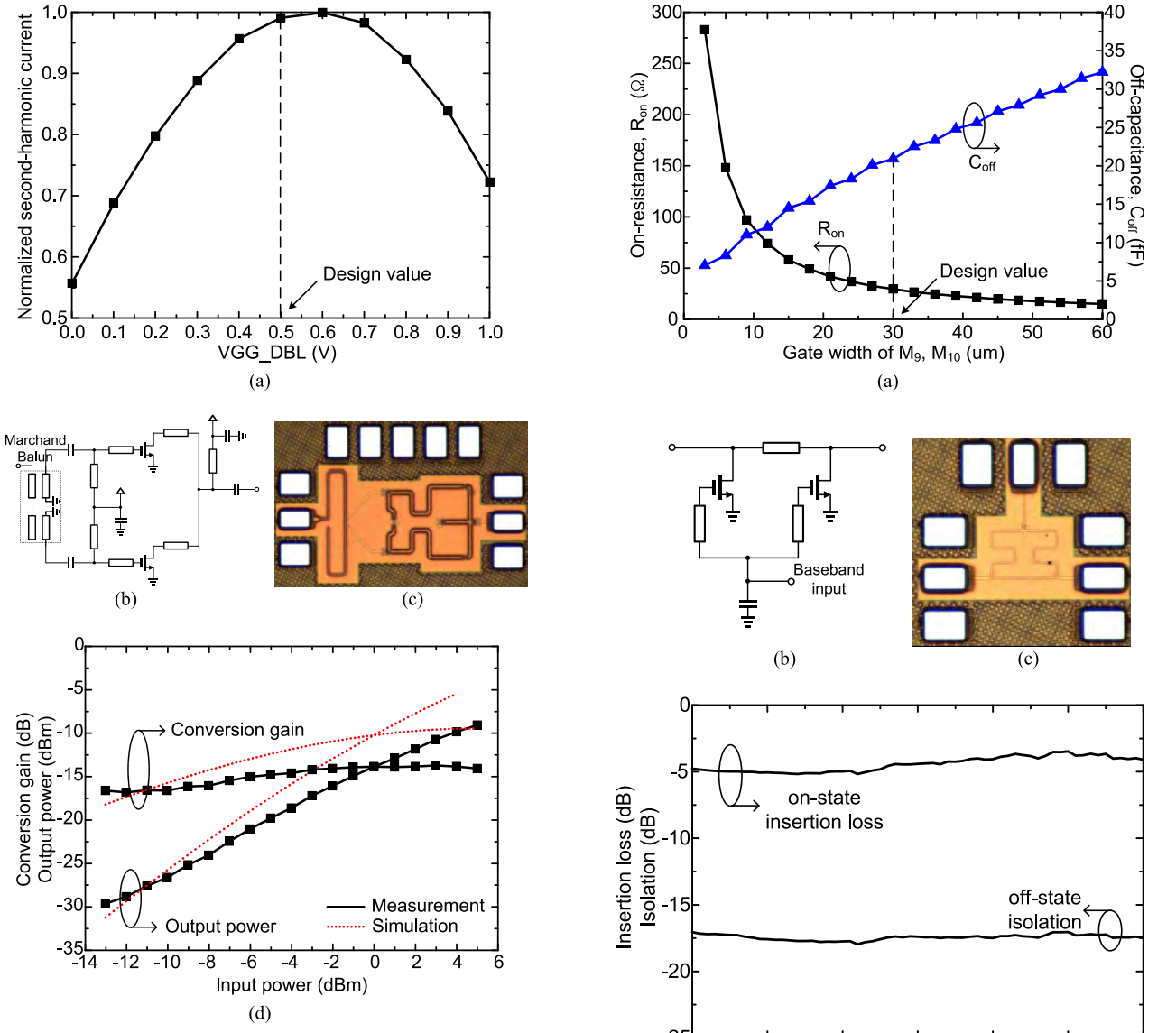


FIGURE 8. (a) Simulation of the normalized second-harmonic current versus the gate bias voltage. (b) Schematic and (c) Chip micrograph of the D-band doubler test cut. (d) Measured output power and conversion gain at 140 GHz.

FIGURE 9. (a) Simulated on-resistance and off-capacitance versus transistor gate width. (b) Schematic and (c) Chip micrograph of the D-band OOK modulator test cut. (d) Measured insertion loss and isolation.

at the baseband feed point, thus improving the modulation speed.

Fig. 9(b) and (c) show a schematic and a chip micrograph of the OOK modulator test cut, respectively. The measured result is shown in Fig. 9(d). The on-state insertion loss and the off-state isolation are 4.4 dB and 17.4 dB, respectively, at 140 GHz. Therefore, the final output power of the integrated transmitter is expected to be -13.4 dBm when the OOK modulator is driven by the preceding frequency doubler with -9 dBm. This output power meets the power budget requirement described in Fig. 4.

E. D-BAND PRE-AMPLIFIER

As shown in Fig. 2, the transistor f_{max} is lower than 200 GHz, which makes it challenging to design a D-band pre-amplifier required in the receiver. In this work, an inter-stage DC-coupled technique is employed to overcome the low f_{max} and low MAG.

A schematic of the D-band pre-amplifier is shown in Fig. 5(b). It consists of three DC-coupled differential stages (M_{11}–M_{16}) and an input balun. In conventional multi-stage amplifiers, an AC-couple capacitor is usually added between the stages to separate the DC biases. However, the capacitor suffers from a low Q-factor as the frequency increases, thus lowering the MAG of each stage. For example, the Q-factor of a 100-fF MIM capacitor decreases to 0.26 at 140 GHz according to the simulation. In Fig. 10(a), the MAG of a two-stage transistor cell is compared when the two transistors

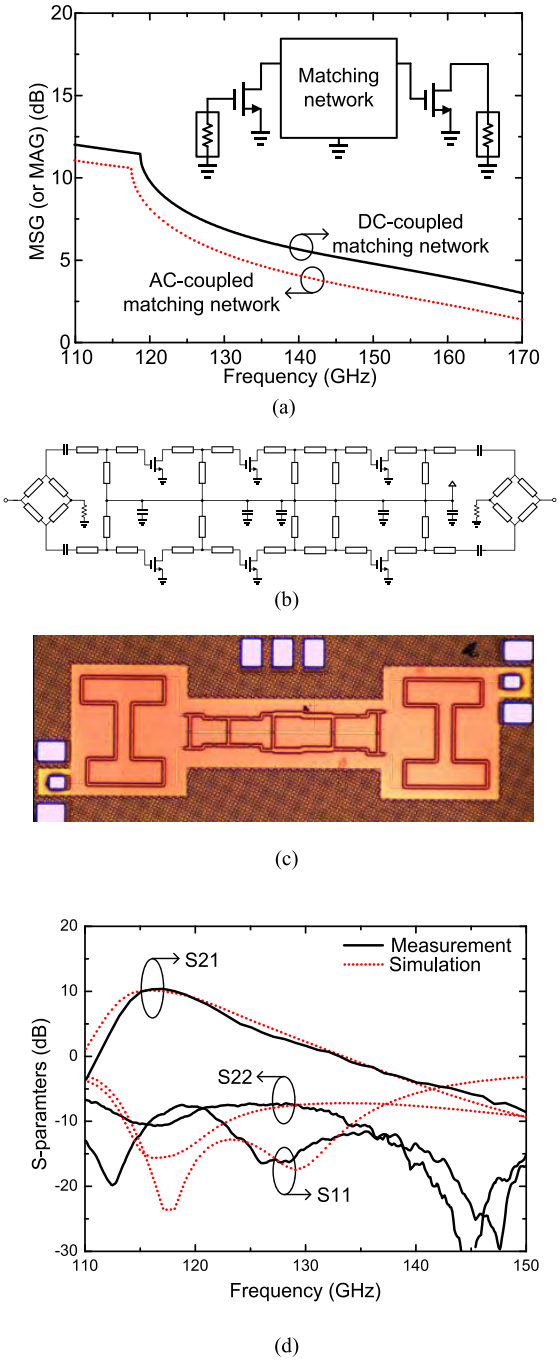


FIGURE 10. (a) Comparison of MAG between an AC-coupled two-stage transistor cell and a DC-coupled cell. (b) Schematic and (c) Chip micrograph of the D-band pre-amplifier test cut. (d) Measured S-parameters.

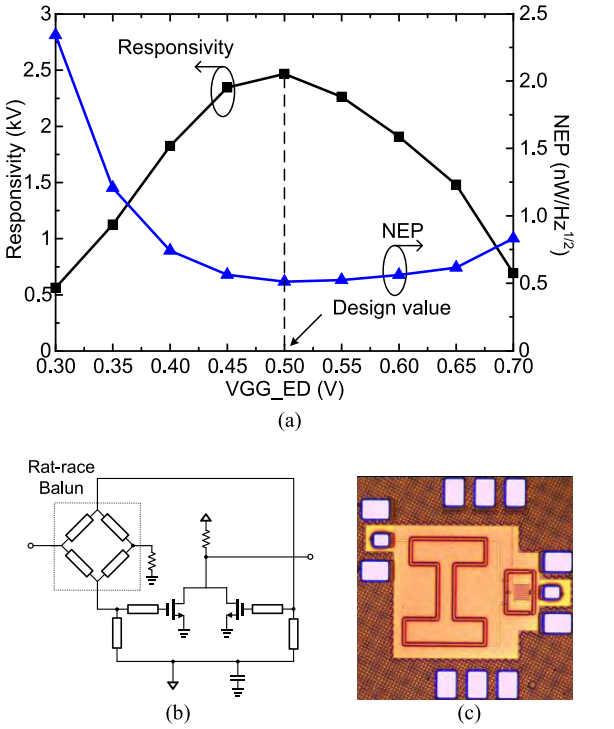


FIGURE 11. (a) Simulated responsivity and NEP at 140 GHz versus gate bias voltage. (b) Schematic and (c) Chip micrograph of the D-band envelope detector test cut.

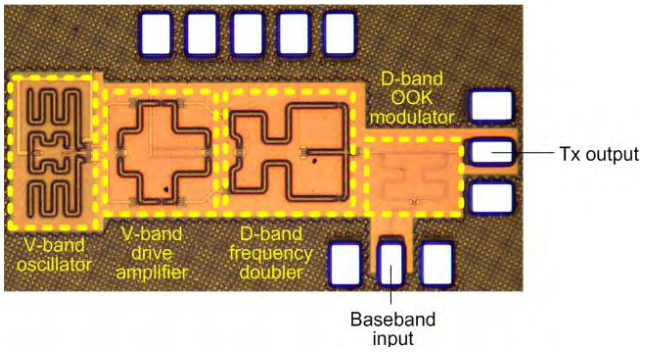


FIGURE 12. Chip micrograph of the D-band integrated OOK transmitter.

are AC-coupled with the MIM capacitor or are DC-coupled without the capacitor. The MAG of the AC-coupled cell decreases by 1.6 dB at 140 GHz. Therefore, the D-band amplifier in this work is designed without AC-couple capacitors.

Since the inter-stage is DC-coupled, the gate and drain biases are all tied into a common voltage of 1 V. The gate width is optimized to 1 $\times$ 14 μm to obtain the maximum MAG at D-band frequencies. Impedance matching is performed using transmission lines. Especially, the relatively wide transmission lines of TL_{43} and TL_{44} are employed to extend the operating bandwidth [29]. A rat-race coupler is inserted at the input for converting a single-ended signal into a differential one.

Fig. 10(b), (c), and (d) depict a schematic, a chip micrograph, and measured S-parameters of the D-band amplifier test cut, respectively. The peak gain of 10.4 dB is measured at 117 GHz. The DC power consumption is 32 mW. The simulation agrees well with the measurement even at D-band frequencies owing to the supplementary modeling proposed in Section II.

F. D-BAND ENVELOPE DETECTOR

The D-band envelope detector is designed in a differential common-source topology. According to the simulation of

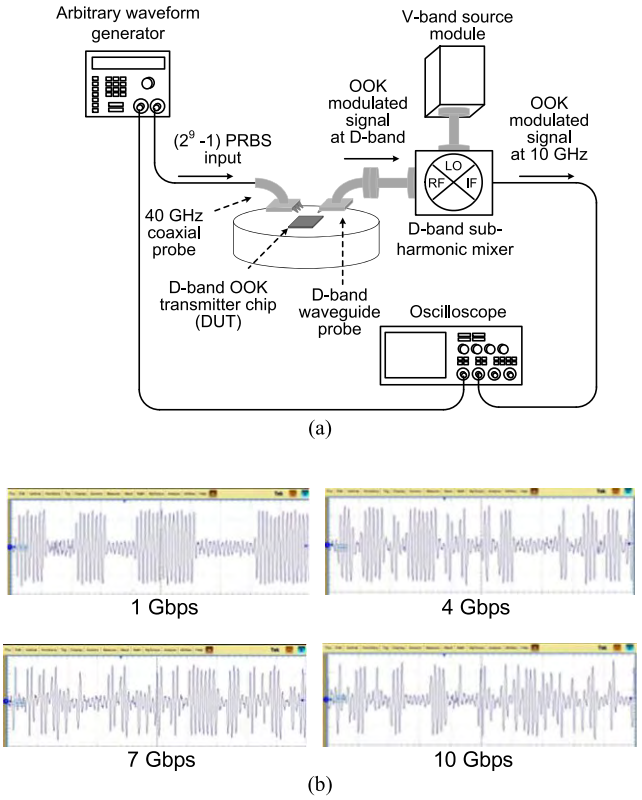


FIGURE 13. (a) Measurement setup for OOK modulation performance of the D-band transmitter, (b) Measured OOK-modulated output signals.

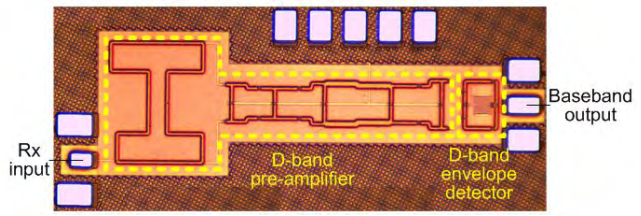


FIGURE 14. Chip micrograph of the D-band integrated OOK receiver.

the responsivity and noise-equivalent power (NEP) shown in Fig. 11(a), the gate bias voltage is chosen as 0.5 V. The input impedance is matched using transmission lines (TL_{55}–TL_{58}). The DC output is taken at the common node of the differential pair, so that the D-band carrier is suppressed by itself. The output load resistor (R_2) is chosen as 1 kΩ considering the trade-off between responsivity and voltage headroom.

Fig. 11(b) and (c) show a schematic and a chip micrograph of the envelope detector, where a D-band rat-race balun is added to the differential input for measurement purposes. The measured average responsivity and NEP from 110 to 170 GHz are 1.2 kV/W and 234 pW/Hz$^{1/2}$, respectively.

V. MEASUREMENTS OF INTEGRATED TRANSCEIVER

A. D-BAND INTEGRATED OOK TRANSMITTER

The transmitter chip, integrating the V-band oscillator, drive amplifier, D-band frequency doubler, and OOK modulator,

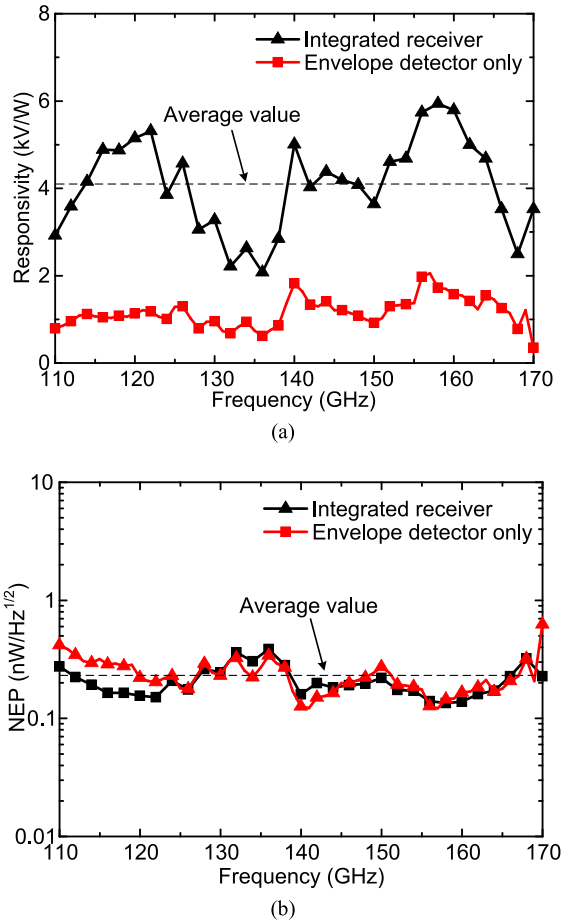


FIGURE 15. (a) Measured responsivity and (b) NEP of the D-band receiver. The responsivity and NEP of the envelope detector alone are superimposed.

is shown in Fig. 12. The chip area is 1110 μm × 634μm including probing pads. The measured output power when the baseband input is one and zero are -9.8 dBm and -23 dBm, respectively, at 134.1 GHz. The DC power consumption of the transmitter is 76 mW.

The modulation performance of the transmitter is tested using the measurement setup shown in Fig. 13(a). A $(2^9 - 1)$ PRBS from an arbitrary waveform generator modulates the transmitter. The D-band modulated output is down-converted to IF of 10 GHz by a sub-harmonic mixer and then is monitored by an oscilloscope. The modulated waveforms at 1, 4, 7, and 10 Gbps are depicted in Fig. 13(b).

B. D-BAND INTEGRATED OOK RECEIVER

The receiver chip, integrating the D-band pre-amplifier and envelope detector, is shown in Fig. 14. The chip area is 1420 μm × 620μm including probing pads. The measured responsivity and NEP of the receiver are shown in Fig. 15. The averaged responsivity and NEP over the entire D-band frequencies are 4.1 kV/W and 211.4 pW/Hz$^{1/2}$, respectively. The responsivity and NEP of the envelope detector alone are superimposed. The integrated receiver exhibits a higher responsivity than the individual envelope detector owing

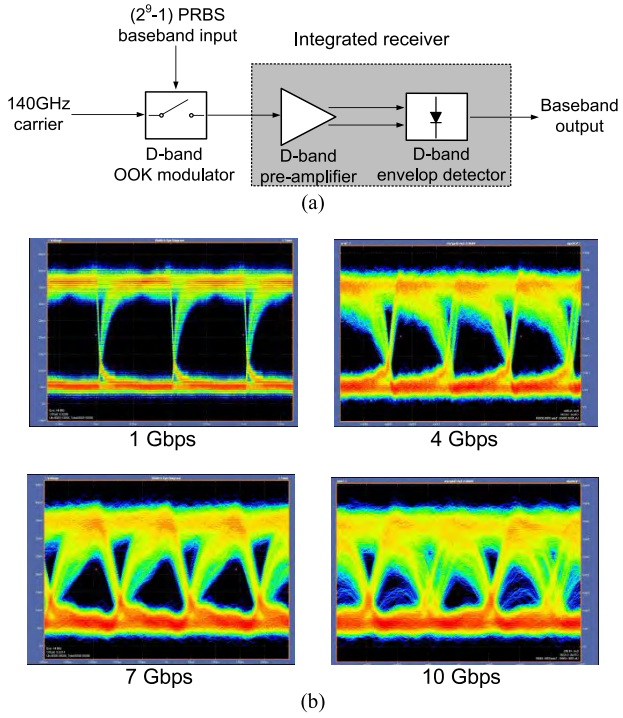


FIGURE 16. **(a) On-chip loopback transceiver system integrating the D-band receiver with an OOK modulator. (b) Measured eye diagrams of the demodulated signal at the D-band receiver output.**

to the pre-amplifier. The receiver consumes DC power of 32.5 mW.

The demodulation performance of the receiver is tested using an on-chip loopback transceiver system that integrates the receiver with an OOK modulator, as shown in Fig. 16(a). A 140-GHz carrier is externally injected, modulated, and then fed to the receiver for demodulation. Fig. 16(b) shows the measured eye diagrams of the demodulated output at 1, 4, 7, and 10 Gbps. It should be mentioned that measurement at higher data rates is limited by the oscilloscope bandwidth, not by the receiver demodulation capability.

C. WIRELESS DATA TRANSMISSION WITH TRANSCEIVER CHIPSET

A wireless data transmission is demonstrated using the proposed transceiver chipset, as shown in Fig. 17(a). A D-band horn antenna with 21-dBi gain is connected to each of the transmitter and receiver chips. The air-channel distance between the horn antennas is d. A $(2^9 - 1)$ PRBS data input modulates the D-band carrier that is internally generated in the transmitter chip. Fig. 17(b) shows the measured eye diagrams of the demodulated signal at the receiver output. The data rates are 1 and 2 Gbps at $d = 0.01$, 0.02, and 0.03 m. To confirm the communication quality, error vector magnitude (EVM) is calculated by post-processing the time-domain data of eye diagram for 1 Gbps at 0.02 m. The calculated EVM is 9.8 %. Note that the on-chip loopback transceiver in Fig. 17 exhibits a modulation/demodulation

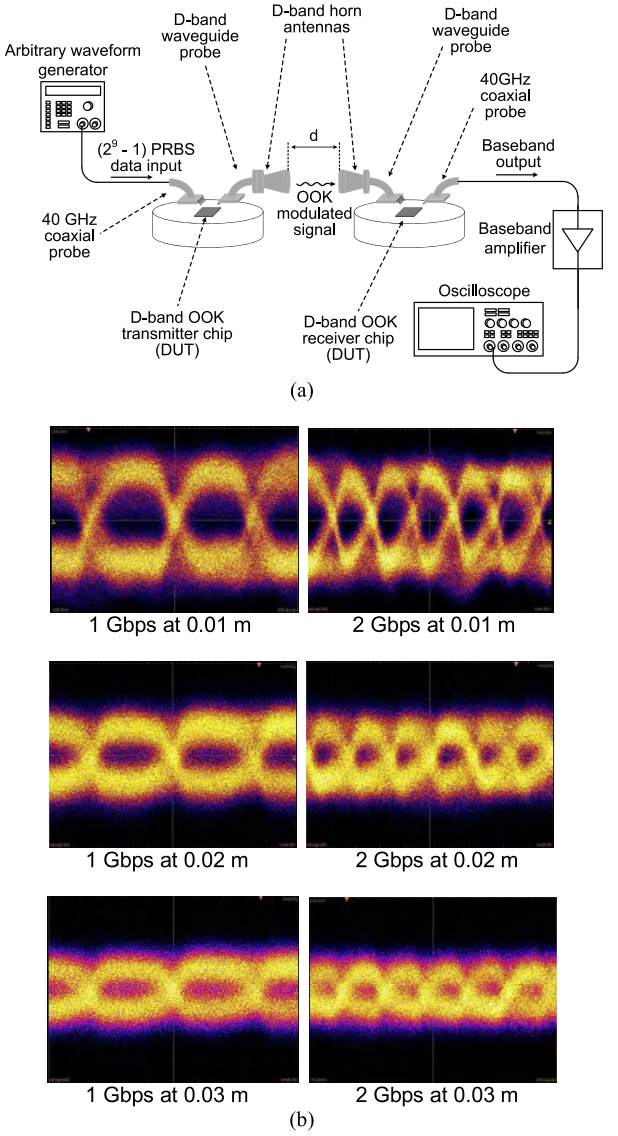


FIGURE 17. **(a) Measurement setup for demonstrating wireless data transmission using the proposed transceiver chipset. (b) Measured eye diagrams of the demodulated signal at the D-band receiver output.**

capability up to 10 Gbps. Therefore, the data rate and channel distance (d) can be further improved by increasing the output power of the transmitter.

In Table 2, the transceiver in this work is compared with other ASK/OOK transceivers operating above 100 GHz. The proposed transceiver achieves a high data rate of 10 Gbps with relatively low DC power and a small chip area owing to the simple architecture employing no PA, mixer, or LO. Relatively short channel distance is traded for the low DC power. More importantly, the proposed transceiver is fabricated in a low-cost low-speed technology compared with other transceivers [14]–[17]. The low transistor f_{max} and the inaccurate model are overcome by the multiplier-based architecture, supplementary modeling, and DC-coupled design technique.

TABLE 2. Performance comparison with other ASK/OOK transceivers operating above 100 GHz.

	Frequency (GHz)	Technology (CMOS)	Architecture		Data rate (Gbps)	Distance (m)	DC power (mW)	Chip area (mm^2)
			Transmitter	Receiver				
[11]	120	65 nm	OSC+MOD+PA	LNA+DET+LA+Buffer	9	-	80.9	0.94
[12]	113	65 nm	OSC+MOD	LNA+DET+LA+Buffer	2.5	0.2	176.4	1.26
[13]	260	65 nm	OSC+AMP+OD+PA	Mixer+OSC+AMP	10	0.04	1173	6
[14]	133.9	40 nm	OSC+MOD+PA	LNA+DET+LA+Buffer	11	3	209	1.57
[15]	135	40 nm	OSC+MOD	LNA+DET+LA+Buffer	10	0.1	98.4	2
[16]	210	32 nm	OSC+MOD+PA	LNA+DET	-	3.5	308	4.62
[17]	210	40 nm	OSC+MOD+PA	LNA+DET	10.7	0.01	421	2.71
This work	**140**	**65 nm**	**MOD**	**AMP+DET**	**10**	**-**	**32.5**	**1.10**
This work	**134.1**	**65 nm**	**OSC+MULT+MOD**	**AMP+DET**	**2**	**0.03**	**108.5**	**1.58**

OSC: oscillator, MOD: modulator, PA: power amplifier, MULT: multiplier, LNA: low-noise amplifier, AMP: amplifier, DET: detector, LA: limiting amplifier.

VI. CONCLUSION

A D-band OOK transmitter and receiver were demonstrated in a bulk 65-nm CMOS technology. To overcome the limitations of the low-cost low-speed technology for mm-wave circuit design, a new transceiver architecture and supplementary transistor modeling were proposed. The transceiver showed a decent data-communication performance comparable with those of other state-of-the-art transceivers fabricated in high-cost highly-scaled technologies. This work thus demonstrates a relatively low-cost, highly-integrative solution for short-distance wireless connectivity.

ACKNOWLEDGMENT

The authors would like to thank IC Design Education Center (IDEC) for MPW and CAD tool support.

REFERENCES

[1] A. Zolfaghari *et al.*, "A multi-mode WPAN (Bluetooth, BLE, IEEE 802.15.4) SoC for low-power and IoT applications," in *Proc. Symp. VLSI Circuits*, Kyoto, Japan, Jun. 2017, pp. C74–C75.

[2] W. Rhee, D. Liu, Y. Zhang, and Z. Wang, "Energy-efficient proprietary transceivers for IoT and smartphone-based WPAN," in *Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol. (RFIT)*, Seoul, South Korea, Aug. 2017, pp. 40–42.

[3] K. Kang *et al.*, "A 60-GHz OOK receiver with an on-chip antenna in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1720–1731, Sep. 2010.

[4] J. Lee, Y. Chen, and Y. Huang, "A low-power low-cost fully-integrated 60-GHz transceiver system with OOK modulation and on-board antenna assembly," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 264–275, Feb. 2010.

[5] Z. Lu, C. Feng, X. Yu, Y. Qin, and K. S. Yeo, "Design of a low power 60 GHz OOK receiver in 65 nm CMOS technology," in *Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol. (RFIT)*, Singapore, Nov. 2012, pp. 22–24.

[6] C. W. Byeon, C. H. Yoon, and C. S. Park, "A 67-mW 10.7-Gb/s 60-GHz OOK CMOS transceiver for short-range wireless communications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 9, pp. 3391–3401, Sep. 2013.

[7] H. J. Lee, J. G. Lee, C. J. Lee, T. H. Jang, H. J. Kim, and C. S. Park, "High-speed and low-power OOK CMOS transmitter and receiver for wireless chip-to-chip communication," in *Proc. IEEE MTT-S Int. Microw. Workshop Adv. Mater. Process. RF THz Appl. (IMWS-AMP)*, Suzhou, China, Jul. 2015, pp. 1–3.

[8] H. Takahashi, T. Kosugi, A. Hirata, J. Takeuchi, K. Murata, and N. Kukutsu, "120-GHz-band fully integrated wireless link using QSPK for realtime 10-Gbit/s transmission," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4745–4753, Dec. 2013.

[9] S. Carpenter *et al.*, "A *D*-band 48-Gbit/s 64-QAM/QPSK direct-conversion I/Q transceiver chipset," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1285–1296, Apr. 2016.

[10] A. Balteanu, S. Shopov, and S. P. Voinigescu, "A 2×44 Gb/s 110-GHz wireless transmitter with direct amplitude and phase modulation in 45-nm soi CMOS," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp. (CSICS)*, Monterey, CA, USA, Oct. 2013, pp. 1–4.

[11] R. Fujimoto, M. Motoyoshi, U. Yodprasit, K. Takano, and M. Fujishima, "A 120-GHz transmitter and receiver chipset with 9-Gbps data rate using 65-nm CMOS technology," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Beijing, China, Nov. 2010, pp. 1–4.

[12] N. Ono, M. Motoyoshi, K. Takano, K. Katayama, R. Fujimoto, and M. Fujishima, "A 113 GHz 176 mW transmitter and receiver chipset using 65 nm CMOS technology," in *Proc. Asia Pacific Microw. Conf.*, Kaohsiung, Taiwan, Dec. 2012, pp. 439–441.

[13] J. D. Park, S. Kang, S. V. Thyagarajan, E. Alon, and A. M. Niknejad, "A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication," in *Proc. Symp. VLSI Circuits (VLSIC)*, Honolulu, HI, USA, Jun. 2012, pp. 48–49.

[14] K. Katayama, M. Motoyoshi, K. Takano, L. C. Yang, and M. Fujishima, "209 mW 11 Gbps 130 GHz CMOS transceiver for indoor wireless communication," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Singapore, Nov. 2013, pp. 409–412.

[15] M. Fujishima, M. Motoyoshi, K. Katayama, K. Takano, N. Ono, and R. Fujimoto, "98 mW 10 Gbps wireless transceiver chipset with D-band CMOS circuits," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2273–2284, Oct. 2013.

[16] Z. Wang, P.-Y. Chiang, P. Nazari, C.-C. Wang, Z. Chen, and P. Heydari, "A CMOS 210-GHz fundamental transceiver with OOK modulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 564–580, Mar. 2014.

[17] S. Moghadami, F. Hajilou, P. Agrawal, and S. Ardalan, "A 210 GHz fully-integrated OOK transceiver for short-range wireless chip-to-chip communication in 40 nm CMOS technology," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 5, pp. 737–741, Sep. 2015.

[18] Y. Yang, S. Zihir, H. Lin, O. Inac, W. Shin, and G. M. Rebeiz, "A 155 GHz 20 Gbit/s QPSK transceiver in 45 nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Tampa, FL, USA, Jun. 2014, pp. 365–368.

[19] S.-K. Kim, R. Maurer, A. Simsek, M. Urteaga, and M. J. W. Rodwell, "Ultra-low-power components for a 94 GHz transceiver," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Austin, TX, USA, Oct. 2016, pp. 1–4.

[20] S. Park and S. Jeon, "A transformer-matched millimeter-wave CMOS power amplifier," *J. Semicond. Technol. Sci.*, vol. 16, no. 5, pp. 687–694, 2016.

[21] A. Nikpaik, A. H. M. Shirazi, A. Nabavi, S. Mirabbasi, and S. Shekhar, "A 219-to-231 GHz frequency-multiplier-based VCO with ∼3% peak DC-to-RF efficiency in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 389–403, Feb. 2018.

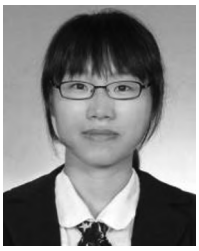
[22] S. Kim and S. Jeon, "140 GHz push-push oscillator using 65-nm CMOS process," in *Proc. Korean Inst. Electromagn. Eng. Sci. Summer Workshop*, Aug. 2014, p. 56.

[23] J. G. Proakis, *Digital Communications*, 5th ed. New York, NY, USA: McGraw-Hill, 2007.

[24] V. Mackowiak, J. Peupelmann, Y. Ma, and A. Gorges, "NEP—Noise equivalent power," Thorlabs, Newton, NJ, USA, Tech. Rep., 2016.
[25] Q. Tang, S. K. S. Gupta, and L. Schwiebert, "BER performance analysis of an on-off keying based minimum energy coding for energy constrained wireless sensor applications," in *Proc. IEEE Int. Conf. Commun.*, vol. 4, May 2005, pp. 2734–2738.
[26] D. M. Pozar, *Microwave Engineering*, 4th ed. New York, NY, USA: Wiley, 2011.
[27] (2016). *Nominal Horn Specifications*. Accessed: Oct. 23, 2017. [Online]. Available: http://vadiodes.com/images/AppNotes/VDI_Feedhorn_Summary_2016.02.pdf
[28] U. Yodprasit, R. Fujimoto, M. Motoyoshi, K. Takano, and M. Fujishima, "D-band 3.6-dB-insertion-loss ASK modulator with 19.5-dB isolation in 65-nm CMOS technology," in *Proc. Asia Pacific Microw. Conf.*, Yokohama, Japan, Dec. 2010, pp. 1853–1856.
[29] D.-H. Kim, D. Kim, and J.-S. Rieh, "A *D*-band CMOS amplifier with a new dual-frequency interstage matching technique," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 5, pp. 1580–1588, May 2017.

BOHEE SUH received the B.S., M.S., and Ph.D. degrees in electrical engineering from Korea University, Seoul, South Korea, in 2010, 2012, and 2018, respectively. He is currently with Samsung Electronics, South Korea. His research interests include D-band integrated circuits and transceiver systems.

HYUNKYU LEE received the B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2014, where he is currently pursuing the Ph.D. degree in electrical engineering. His research interests include microwave and millimeter-wave integrated circuits and transceiver systems.



SOOYEON KIM received the B.S. and M.S. degrees in electrical engineering from Korea University, Seoul, South Korea, in 2007 and 2009, respectively, where she is currently pursuing the Ph.D. degree in electrical engineering. Her research interests include microwave and millimeter-wave integrated circuits and systems.

From 2009 to 2012, she was a Member of Technical Staff with the Korea Astronomy and Space Science Institute.

SANGGEUN JEON received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1997 and 1999, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2004 and 2006, respectively.

From 1999 to 2002, he was a full-time Instructor in electronics engineering with the Korea Air Force Academy. From 2006 to 2008, he was a Research Engineer with the Caltech High-Speed Integrated Circuits Group, where he was involved in CMOS phased-array receiver design. Since 2008, he has been with the School of Electrical Engineering, Korea University, Seoul, where he is currently a Professor. His research interests include integrated circuits and systems at microwave, mm-wave, and terahertz bands for high-speed wireless communication and high-resolution imaging applications.