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Design of Broadband High-Efficiency Power Amplifier Through Interpolations on Continuous Operation-Modes

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ABSTRACT Besides various kinds of continuous-mode high-efficiency power amplifiers (HEPAs), there do exist many other undefined HEPA operations. In place of introducing variables into waveform equations, a numerical mode-interpolation method based on the nonlinear drain current calculations is used in this paper. The combinations of fundamental drain voltage's amplitude and phase boundaries from general continuous modes are used to form the interpolation grids. The interpolated high-efficiency operations determined by the practical transistor's characteristics are collected as perturbation seeds in a solution expansion procedure. Hence, the expanded optimized load impedances are defined as a candidate design space of a mixed-mode HEPA. A broadband HEPA design example from 0.5 to 4 GHz is given based on these interpolated impedances. Finally, this PA is fabricated and measured to offer 39.0- to 42.3-dBm power and 58.2% to 69.3% drain efficiency from 0.45 to 4 GHz.

INDEX TERMS Broadband power amplifiers, high-efficiency power amplifiers, operation-mode interpolations, optimized impedance calculations, and waveform engineering.

I. INTRODUCTION

Because broadband high-efficiency power amplifiers (HEPA) can be easily configured as a multi-band transmitter's front-ends [1], the researches on their design theories and methods were active in recent publications.

Besides class-E [2] and class-F [3] power amplifiers (PA), there are also many variant PA classes which can extend the HEPA load impedance solutions. New variables were introduced to the waveform expressions to extend the load impedance solution space [4]. For example, continuous class-F [5], class-J PAs [6]–[8], and even resistive harmonic impedances [9]. Furthermore, mode transferring design method was proposed in order to enrich the applicable impedance space in [10].

A load-pull system was usually used to determine practical optimal package-plane impedances, and it is a performance-oriented method, regardless of the exact operation modes [11], [12]. Thus, a broadband HEPA design can be realized through impedance solutions obtained from a load-pull searching [13], [14]. However, time-consuming load-pull measurements limit the possibility of traversing the multi-harmonic Smith chart to find all the HEPA impedances. In order to solve this problem, a sequential load-pull technique was proposed in [15] to reorganize a broadband impedance determination flow and to avoid harmonic impedances conflict.

Waveform engineering measurements can be used to identify PA's real operation modes if necessary [16], [17]. One should embed the package parasitics to convert the generator-plane waveforms to package-plane for a practical HEPA mode identification [18]. With considerations of thermal effects and dispersions of GaN devices, Jang *et al.* [19] proposed a nonlinear embedding process to support a HEPA design with a classical waveform projection. And it showed that ideal impedances from theories should be modified to implement a practical microwave power amplifier with considerations of a nonlinear transistor model.

To find more practical high-efficiency operation modes and to extend the load impedance solution space, a design process of a broadband HEPA is proposed based on numerical mode-interpolations and waveform perturbations. This paper is organized as follows; in Section II, the interpolated mixed HEPA operation mode is defined, and its performances are studied. Numerical examples are also given to show the

TABLE 1. Normalized drain voltage's Fourier series - summary of 4 continuous-mode PAs.

Operation Mode	V_1	ϕ_{V1}	V_2	ϕ_{V2}	V_3	ϕ_{V3}
Continuous class-F [20]	$[\frac{2}{\sqrt{3}}, \sqrt{\frac{7}{3}}]$	$[\frac{\pi}{2} - \arctan(\frac{\sqrt{3}}{2}), \frac{\pi}{2} + \arctan(\frac{\sqrt{3}}{2})]$	$[0, \frac{7\sqrt{3}}{18}]$	$-\pi \pm \frac{\pi}{2}$	$\frac{\sqrt{3}}{9}$	$\frac{\pi}{2}$
Continuous class-F^{-1} [9]	$\sqrt{2}$	$\pi/2$	0.5	π	0	N/A
Continuous class-B/J [6]	$[1, \sqrt{2}]$	$[\frac{\pi}{4}, \frac{3\pi}{4}]$	[0, 0.5]	$[-\pi, \frac{\pi}{2}]$	N/A	N/A
Continuous class-E [21]	[1.26, 1.70]	[1.57, 1.93]	[0.85, 1.00]	[-3.14, 1.21]	[0.22, 1.32]	[-1.563, 2.373]

process of impedance calculations based on a Wolfspeed's GaN device. To further extend the high-efficiency impedance space, a waveform perturbation and screening results are used. A broadband PA design example based on this mixed-mode impedance space is given in Section III, simulation results and discussions on design deviations are also given in this section. Experimental verification is shown in Section IV, and the conclusion is drawn in Section V.

II. NUMERICAL MODE-INTERPOLATION METHOD AND MIXED-MODE PA's DESIGN SPACE

Apparently, it is difficult to keep a single PA operation mode across a broad bandwidth, and it is helpful to allow a PA to switch among different modes [10]. With the developments in continuous mode PAs, more and more high-efficiency impedance space can be exploited. However, there are still many HEPA mode gaps to be found.

A. OPERATION-MODE INTERPOLATION SEEDS

Many kinds of continuous-mode PAs scatter in literature, and they can be grouped as interpolation seeds to form mixed-mode operations. Thus, the load impedance can be selected from a much bigger pool which can better adapt a broadband power amplifier design.

The voltage waveform position is mainly determined by the fundamental components which have the highest weight on HEPA's performances and waveform shapes. In Table 1, drain voltage's Fourier coefficients are summarized for 4 basic kinds of continuous-mode PAs. In this table, V_i and ϕ_{Vi} represent the i^{th} harmonic drain voltage magnitude and phase respectively. V_i is normalized to drain dc supply voltage, and the phase is aligned according to a sinusoidal input excitation with zero initial-phase.

Apparently, there is still some discontinuity in between fundamental voltage ranges as listed in Table 1. The continuous fundamental range is a feasible guess on high-efficiency operation waveforms, but they have not been united in current independent HEPA mode analysis. From this summary, the range of V_1 and ϕ_{V1} can be considered as a search starting point of the mode interpolations.

B. MODE INTERPOLATION SETTINGS AND PROCEDURES

The choices of the fundamental voltage's amplitude and phase combination range can be concluded from Table 1, i.e., the ranges of V_1 and ϕ_{V1} are [1, 1.70] and $[\pi/4, 3\pi/4]$ respectively from all listed PAs. A two-dimensional uniform interpolation grid is set to find continuous HEPA solutions in these ranges. Wolfspeed's GaN device CGH40010F is used in the following design, and the basic requirements of the waveforms and PA performances are listed as follows,

- Only up to the third harmonic is considered, and gate input is purely sinusoidal,
- Negative drain voltage is not allowed,
- Aim to obtain the highest drain efficiency (DE) for any combination of V_1 and ϕ_{V1} through waveform optimizations,
- Drain supply voltage is 28 V, and the output power P_{out} is kept as close to 10 W as possible.

From the above settings, the searching grid of V_1 is determined as [28 V, 46 V] with a 1-V step, and the grid of ϕ_{V1} is [0.8, 2.4] with a 0.1-rad step. For each combination of V_1 and ϕ_{V1}, PA performances and impedances are optimized and calculated according to the flowchart in Fig. 1 with a sinusoidal gate input of 4 V. After knowing the settings of gate input voltage and drain voltage's Fourier components, the time-domain drain current can be obtained as follows.

$$I_{ds}(t) = f\left[V_{gs}(t), V_{ds}(t)\right], \tag{1}$$

where $V_{gs}(t)$ and $V_{ds}(t)$ are the time-domain waveforms of gate-source and drain-source voltages respectively. Function $f[\cdot]$ represents a transistor's drain current equation. We will use interpolated dc I-V data to implement this function. In the following design example, internal dc I-V curves of CGH40010F are adopted, so the results are dedicated to this transistor. The information about the I-V curves and validity of this nonlinear current calculation method can be found in [22].

The grid scanning flowchart is shown in Fig. 1. In order to satisfy the above performance requirements, a gradient optimizer is used here to update harmonic component values of V_{ds} iteratively for each fundamental combination. Once an optimum efficiency is obtained, the PA performances, load impedances, and Fourier components are stored for this V_1 and ϕ_{V1} combination. The i^{th} load impedances Z_i can be obtained through harmonic components of drain voltage and current as follows,

$$Z_i = \frac{V_i \exp^{j\phi_{Vi}}}{I_i \exp^{j\phi_{Ii}}}, \tag{2}$$

where I_i and ϕ_{Ii} are the magnitude and phase of drain current's Fourier coefficients.

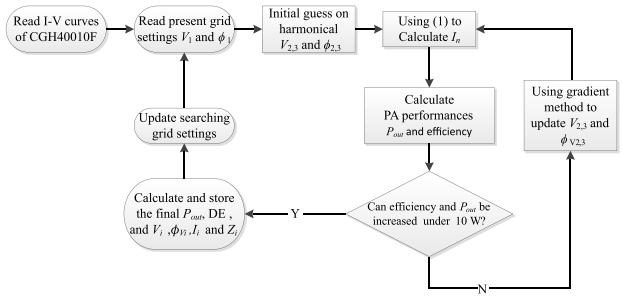


FIGURE 1. The flow-chart of a grid searching for mixed-mode HEPAs.

C. GRID SCANNING RESULTS OF OPERATION MODE-INTERPOLATIONS

The PA performances obtained from the grid scanning are shown in Fig. 2. There is no solution in black regions because negative drain voltage is recorded. The depicted solutions are of calculated highest efficiency for each combination. Along the no-solution boundary, the available drain efficiency becomes high at the cost of reduced output power and hazardous peak drain voltage.

After this scanning process, a part of the recorded waveforms is shown in Fig. 3. The drain voltage waveforms close to continuous class-F modes, and the current waveforms close to class-E and inverse class-F are colored in black. These waveform samples verify that this grid scanning can cover the standard PA operation modes and get interpolated high-efficiency Z_{opt} solutions for a practical device.

A mixed-mode PA can switch among the interpolated operations, only limited by output matching capability. Compared to design methods relied on load pull system and blind optimizations in a harmonic balance simulator, this alternative choice is available to build a complete Z_{opt} space for a specific transistor directly. The validity of this calculated impedance space will be studied in the following design example.

D. DESIGN SPACE EXPANSION AND IMPEDANCE SCREENING

In the last subsection, the optimum solutions were obtained from combinations of V_1 and ϕ_{V1} with a discrete step. The impedance space can be further enriched by introducing solutions with suboptimal performances and smaller grids. However, it is a time-consuming task to find out all the solutions in this way. Hence, fast voltage perturbations and impedance screening process are used here to quickly obtain suboptimal solutions, especially in between the discrete steps.

Up to $\pm 10\%$ relative random perturbations are introduced on every drain voltage's Fourier component of the grid searching results. Five hundred uniformly distributed perturbations are performed for every valid combination of Fig. 2. If there is any negative point in a perturbed voltage waveform, it is discarded.

Output fundamental power (P_o) and drain efficiency (DE) requirements are used to screen the perturbation results. The screened results are given in Fig. 4, and the adopted

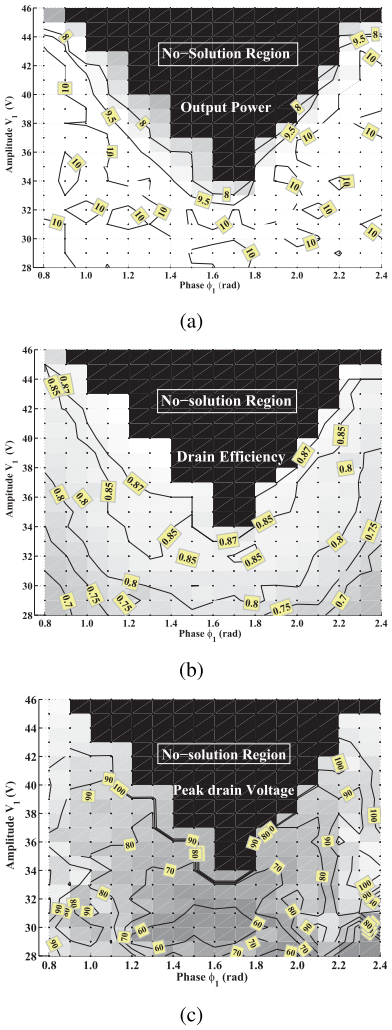


FIGURE 2. The PA performances of the grid search. (a) The fundamental output power (W) contours, (b) The drain efficiency contours, (c) The peak drain voltage (V) contours. There is no valid solution in the black region.

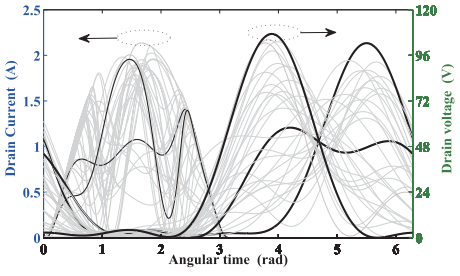


FIGURE 3. Sampled waveforms from the grid searches. Dark lines represents some typical operation modes.

screening performance requirements are DE≥74%, and $6 \leq P_o \leq 11$ W. Because only the fundamental load impedances (Z_1) are found closely clustered in a Smith chart, they are used to index the PA performances for the corresponding impedance vector $[Z_1, Z_2, Z_3]$. The harmonic impedance cannot be used separately, and they are affiliated to points of Z_1 of Fig. 4.

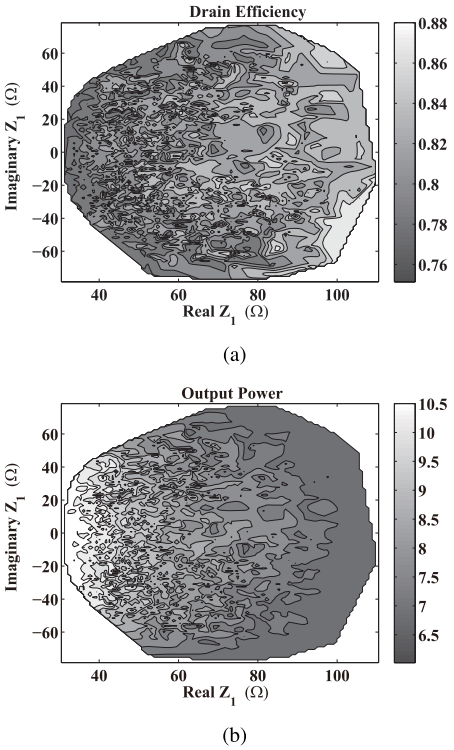


FIGURE 4. The PA performance contours of the screened results versus fundamental impedances. (a) The drain efficiency contours, (b) The fundamental output power (W) contours.

Obviously, the screened Z_{opt} solution space is further expanded compared to the grid searching results. The whole shaded area in Fig. 4 can be exploited as the candidate load impedances of a mixed-mode PA, and it will be used to design a broadband PA in the next section.

III. MIXED-MODE BROADBAND HEPA DESIGN EXAMPLE

Although the grid searching and voltage perturbations have provided a large number of Z_{opt}, the results are still discrete values which cannot form an analytical or continuous design space. However, this discrete impedance set can be regarded as a multi-dimensional cluster, and all the impedances inside this cluster can be regarded as a valid high-performance solution. In this example, a three-dimensional distance d_z defined as follows is used to quantify the efficiency and power performance.

$$d_Z = \sum_{i=1}^{3} W_i \left| \Gamma(\vec{Z}_{ai}) - \Gamma(\vec{Z}_{bi}) \right| \tag{3}$$

where W_i is the summation weight, and $\Gamma(\cdot)$ is the reflection coefficient function. If the distance d_Z, between an implemented load impedance and any vector in the mixed-mode cluster, is within an empirical value, this impedance can be regarded as a feasible solution, satisfying the PA performance requirements in the screening process. The empirical value can be determined according to the average distances of a cluster.

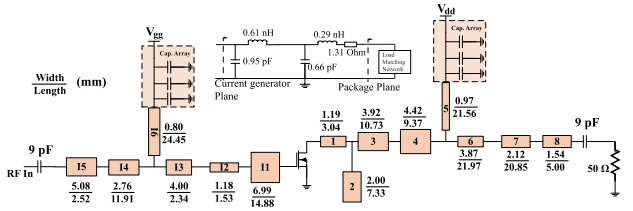


FIGURE 5. The final dimensions and topology of input and output matching network.

TABLE 2. The dimensions of the realized OMN.

	Ini.	Fin.	Dev.		Ini.	Fin.	Dev.
W1	1.15	1.19	3%	W5	0.96	0.97	1%
L1	3.17	3.04	4%	L5	21.49	21.56	0%
W2	1.97	2.00	2%	W6	3.70	3.87	5%
L2	7.10	7.33	3%	L6	22.45	21.97	2%
W3	4.09	3.92	4%	W7	2.16	2.12	2%
L3	10.50	10.73	2%	L7	21.48	20.85	3%
W4	4.62	4.42	4%	W8	1.54	1.54	0%
L4	9.26	9.37	1%	L8	5.00	5.00	0%

* 'Ini'. (Initial dimension, mm), 'Fin.' (Final dimension, mm), and 'Dev.' (Dimension deviation).

A. DESIGN PROCESS AND SIMULATIONS OF A MIXED-MODE HEPA EXAMPLE

Based on the above perturbation results, a mixed-mode broadband power amplifier from 0.5 - 4.0 GHz is designed to offer higher than 8 W (39 dBm) power and higher than 65% drain efficiency. Only a new impedance screen process should be run according to these new performance requirements.

1) PACKAGE EMBEDDING

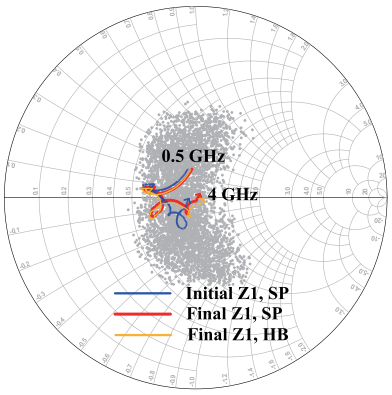
The screened Z_{opt} should be realized at the transistor's current generator plane, so the parasitics must be extracted and included in the load matching network. The linear parasitic model and the typical fitted values of each component at 1.8 GHz can be found in Fig. 5, which are obtained from Wolfspeed's dynamic-load-line model of CGH40010F.

2) INITIAL OUTPUT MATCHING NETWORK DESIGN

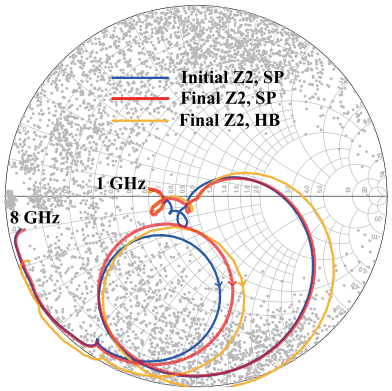
The used topology of the output matching network (OMN) is shown in Fig. 5. Other OMN topology can be used if applicable, and the design steps may involve necessary changes on OMN if one cannot satisfy the broad matching requirements. The dimensions of each microstrip line are optimized to realize the implemented load impedance, which is as close to the screened Z_{opt} cluster as possible at every frequency.

The dielectric constant and thickness of the Rogers 5880 substrate are 2.2 and 20 mil respectively. The OMN dimension optimizations, independent on transistor models, are guided by the impedance space and carried in a small-signal S-parameter simulator in ADS. The initially optimized dimensions of OMN are listed in Table 2.

The implemented fundamental and harmonic load impedances are shown in Fig. 6. Small dots represent the screened mixed-mode solution space, whose performance requirements are 8 W $\leq P_{out} \leq$ 14 W and DE $\geq$ 70%.



(a)



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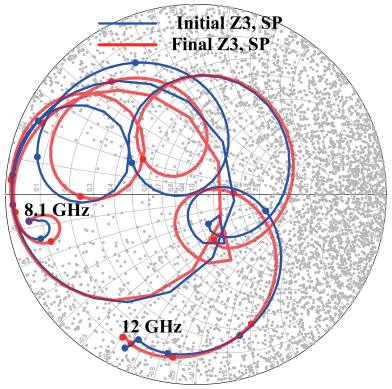
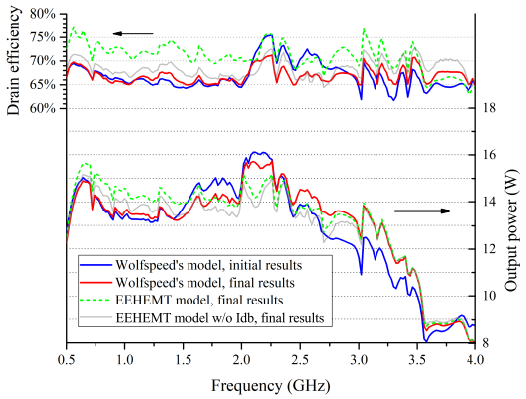


(c)

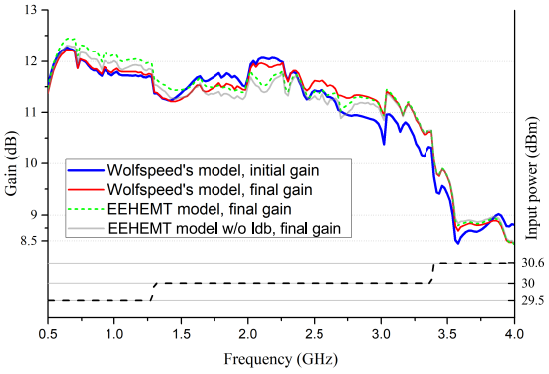
FIGURE 6. The implemented load impedances at current generator plane. SP represents small-signal S-parameter measurement results. HB means large-signal HB measurement results. (a) The fundamental impedances, Z_1. (b) The second-harmonic impedances, Z_2. (c) The third-harmonic impedances, Z_3. Small dots represents the impedances of the screened solution space.

The fundamental impedances Z_1 are clustered around 50 Ω. And the harmonic impedances are scattered almost across the whole Smith chart, except some null regions.

During the OMN realization process, the user-defined maximal distance d_Z is 0.17, and the summation weights W_i are [1, 0.3, 0.1]. In Fig. 6(c), it only shows the implemented Z_3 greater than 8.1 GHz to reduce the low-frequency duplication. The figures show that most of the implemented impedances are close to the solution space after the initial dimension



(a)



(b)

FIGURE 7. The HB simulation results of power amplifier performance. Both Wolfspeed's and EEHEMT model with or without I_{db} are given. (a) drain efficiency and output power, (b) gain and input power.

optimizations under the maximal constraints of d_Z. Following the assumption of this work, the initial OMN implementation can lead to a broadband HEPA close to the target performance.

3) INITIAL DESIGN PERFORMANCES

The harmonic balance (HB) simulated PA performance using the initial dimensions and a Wolfspeed's model is depicted in Fig. 7 (a). The input matching network's topology and dimensions, shown in Fig. 5 (b), are optimized for the desired PA performances. The input power level is from 29.5 to 30.6 dBm as frequency increases. The lowest initial drain efficiency (DE) is 61.7%, and the output power is in the range of 8.0 to 16.1 W (39.0-42.1 dBm). The obtained performance is close to the requirements and the screening criterion.

4) FINAL MATCHING OPTIMIZATIONS

In order to push the performance close to the targets, this PA's output matching network is slightly optimized in an HB simulator of ADS. The relative deviation of the final output-matching dimensions is constrained in case that the operation modes deviate far from the mixed-mode solution space.

The final dimensions are also listed in Table 2. It shows that the maximal deviation is just 5%. This final PA's simulated

TABLE 3. The HB simulated load-impedance deviation vs. input power back-off (BO) levels.

BO	Γ_1 (Z_1)		Γ_2 (Z_2)		Γ_3 (Z_3)	
	Range	Mean	Range	Mean	Range	Mean
0 dB	0.007, 0.029	0.015	0.023, 6.475	0.734	0.009, 0.668	0.173
5 dB	0.003, 0.017	0.011	0.024, 0.800	0.181	0.011, 0.676	0.198
10 dB	0.003, 0.021	0.010	0.005, 0.200	0.076	0.012, 0.794	0.226
15 dB	0.003, 0.023	0.009	0.005, 0.166	0.055	0.021, 0.757	0.202
20 dB	0.002, 0.022	0.009	0.009, 0.158	0.056	0.000, 0.686	0.177

performance is shown in Fig. 7(a). After the final HB optimization step, both the drain efficiency and output power are in the range of 65% to 71.2% and 8 W to 15.7 W respectively.

Because the gain of this PA is different across a broad bandwidth, the applied input power is a piecewise setting as shown in Fig. 7 (b). The final simulated gain is from 8.4 dB to 12.2 dB measured for 29.5 - 30.6 dBm input power.

B. DISCUSSIONS ON NON-IDEAL FACTORS AND DESIGN DEVIATIONS

1) THE EFFECTS OF NONLINEAR ACTIVE COMPONENTS ON LARGE-SIGNAL IMPEDANCE DEVIATIONS

The large-signal impedances measured in the internal current generator plane should also be obtained from an HB simulator to assess the deviations. The HB simulated final internal load-impedance results are also shown in Fig. 6. HB simulated Z_1 is measured at the same input level shown in Fig. 7 (a). Both final Z_1 in HB and SP are close to each other. However, obvious impedance deviations can be found for Z_2 and Z_3 especially at output saturation power level, and the real impedance part of them becomes negative in some frequency ranges. Actually, the load impedance calculated from the internal current and voltage probes, provided by the vendor's model, also contained some active parts. In Fig. 6(b), HB simulated Z_2 is measured at a 15-dB input power back-off to reduce the negative parts and impedance deviations, in case that the HB results get far outside this chart.

The impedance deviation statistics are summarized in Table 3. The deviation is measured by the error magnitude of reflection coefficient (Γ) in HB simulations in comparisons to the corresponding small-signal Γ. Z_1 is not significantly affected by input power, and the mean distance to the SP results keeps very low. However, the deviation of Z_2 is sensitive to power level, and it is sharply reduced after 5 dB input power back-off. However, the deviation of Z_3 is not obviously reduced with back-off.

These negative resistances and power-dependent impedance deviations, calculated from the internal current probe of Wolfspeed's model, can be mainly attributed to nonlinear feedback charges. If I_{ds}, I_{db} and Qgy paths in an EEHEMT model [23], [24] are added together to recalculate the load impedance, then no negative resistance or noticeable power-dependent deviations are found anymore. For example, only 2.2% relative $|\Gamma|$ deviation is measured for the worst case of Z_3 at different input power level, and it is mainly caused by the residual nonlinear Qgc. Hence, it verifies that the primary cause of negative resistance is the power-dependent feedback Q_{gy} path. The input network can affect the load impedances through feedback. However, the induced small performance deviations can be easily corrected from the final HB optimization.

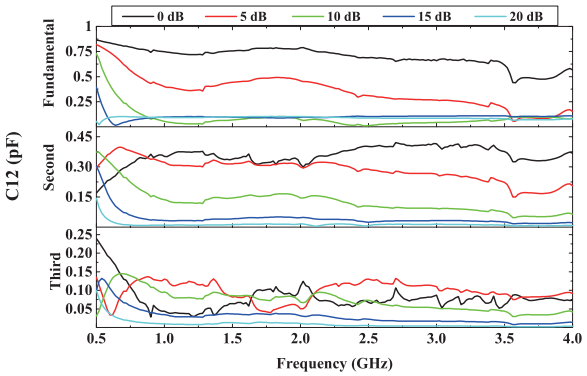


FIGURE 8. The simulated feedback capacitance C_{12} vs. frequency for different input power back-off level.

2) THE EFFECTS OF DISPERSION CURRENT ON I-V CURVES

Because our impedance calculation only involves dc I-V data, the performance errors induced by dispersion current I_{db} should be evaluated too. This evaluation is based on a self-coded EEHEMT model of CGH40010F [23], [24]. Its HB simulated PA performances are shown in Fig. 7 as a baseline. After removing the I_{db}, R_{db} and C_{db} branches, the simulated drain efficiency, marked with 'EEHEMT-w/o-I_{db}', drops by 3.5 points in average and 5.7 points at maximum from 0.5 to 3.5 GHz, and it increases by 3.0 points in average and 4.3 points at maximum from 3.5 to 4 GHz compared to the baseline. In conclusion, the performance deviations caused by dispersions can be acceptable in a broadband PA design.

3) NONLINEAR CAPACITANCES AND GATE TERMINATIONS

In an EEHEMT model, the nonlinear charges Qgy and Qgc can be characterized as a two-port capacitance network [23]. C_{12} is defined as the capacitor between input and output ports, and it can be regarded as the major part of feedback capacitance. In Fig. 8, it is simulated and extracted for this designed broadband PA. Due to its nonlinearity, it is shown in name of its equivalent capacitances from fundamental tone to the third harmonics.

C_{12}'s power dependency can be found, as it decreases with power back-off. In the case of 0 dB input power back-off, C_{12} at fundamental frequencies is the maximum. From this figure, the maximal C_{12} is less than 0.87 pF across the whole band. All of the capacitances from fundamental to harmonics decrease rapidly with back-off power level, and the feedback impedance increases accordingly. Thus, decreased C_{12} can mitigate the effects of gate terminations on the large-signal load impedance deviations. As shown in Fig. 6, significant deviations and negative impedances manifest in the Smith charts of Z_2 and Z_3 at high power level.

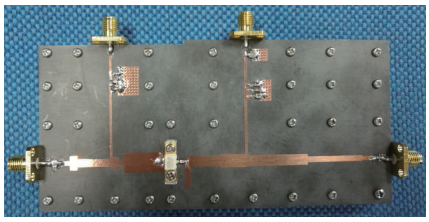


FIGURE 9. The photo of the designed broadband power amplifier.

Although the non-ideal effects were not considered in the impedance calculation results, the obtained design space can support a practical broadband power amplifier design through a rapid small-signal optimizer with minor errors.

IV. MEASUREMENTS

The designed broadband power amplifier is fabricated according to the final dimensions shown in Fig. 5. The board photo is shown in Fig. 9.

We calibrated the input driver and measured this PA at an excitation power range of 18-32 dBm. Input frequency is swept from 0.45 - 4 GHz at a 50 MHz frequency step. The gate bias is -2.8 V which is the measured turn-on threshold voltage for this onboard transistor. The drain bias is 28 V. The measured performances are shown in Fig. 10 in comparisons with simulated results of the fabricated topology. Among the measured input power range from 0.45 - 4 GHz, the measured maximal drain efficiency is 58.2%-69.3% (at 1.5 - 2 dB gain compression point). For most of the in-band frequency points, maximal DE can exceed 60%, and the average efficiency is 62.1%. Compared to the simulated maximal DE range of 64.1%-71.8%, the drain efficiency performance of this broadband PA follows the simulations at an average drop of 5.4%.

The maximal output power is 39.0 - 42.3 dBm, i.e., 8.0 - 16.8 W. In comparisons to the simulated results of 39.5 - 42.4 dBm, major power drop occurs at a frequency below 2 GHz. However, the measured power range still satisfies the initial performance requirements. The measured gain of this PA is recorded at the maximal PAE state. The measured gain varies from 8.0 to 17.2 dB across the whole band, and the corresponding simulated gain is from 8.5 to 19.5 dB. Because the intrinsic gain below 0.7 GHz is too high, the measured gain difference is about 9 dB between both ends. The detailed measured gain versus output power is shown in Fig. 11. High-efficiency performances are achieved in 2 - 3 dB gain-compression region. Thus, if modulated signals are used to excite this PA, digital predistortion technique should be adopted.

In order to compare the state-of-art performances, we list some recently reported results in Table 4. With enlarged design space, the relative bandwidth of 160% with up to 4 GHz operation is obtained in our measurements.

In order to evaluate this PA's performance when excited by modulated signals, baseband measurements across our designed bandwidth are also carried. The 20-MHz 64-QAM modulated signal's peak-to-average-power ratio (PAPR) is 6.5 dB. It is applied to 4 frequencies (0.6/2.2/2.8/3.6 GHz) separately with a fixed input power of 20 dBm for modeling convenience. The output spectrum is shown in Fig. 12, and degraded adjacent channel leakage ratio (ACLR) can be

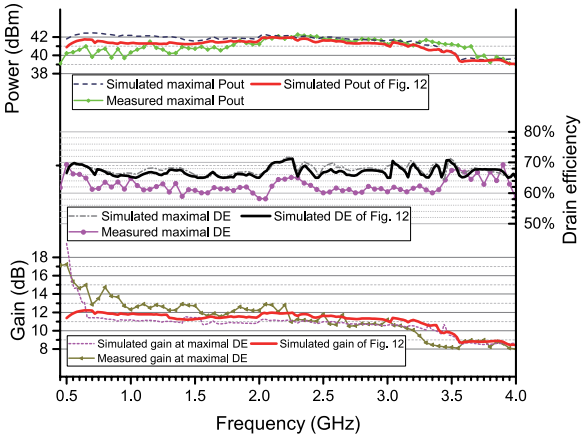


FIGURE 10. The measured PA performances in comparisons to simulations. Two kinds of simulation gains are given here. And the simulated gain at maximal DE.

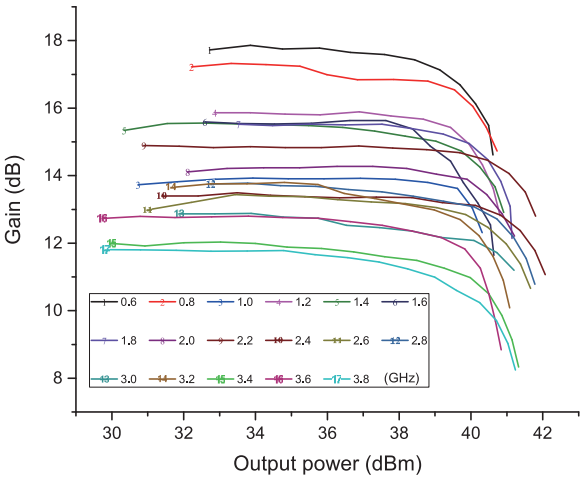


FIGURE 11. The measured gain vs. output power.

TABLE 4. Recent results of other high-efficiency broadband PAs.

Ref.	BW (GHz)	DE	Pout(dBm)	Gain (dB)	BW (%)
2015 [25]	0.4-3.0	58%-79%	40.0-42.0	10.0-12.0	153
2016 [26]	0.8-3.6	56%-74%	39.0-42.0	10.2-12.2	127
2016 [27]	0.6-3.8	51%-76%	40.0-41.9	9.0-14.0	127
2018 [28]	0.5-2.3	60%-81%	39.2-41.2	11.7-25.3	129
2018 [29]	0.2-1.8	60%-82%	42.0-45.1	12.0-15.0	160
2017 [30]	0.2-2.5	56%-70%	43.7-46.9	11.7-14.2	170
2016 [15]	0.7-4.0	53%-64%	37.5-39.1	6.0-13.0	140
2017 [31]	0.4-2.3	62%-81%	39.0-42.0	11-14	141
This work	0.45-4.0	58%-69%	39.0-42.3	8.0-17.2	160

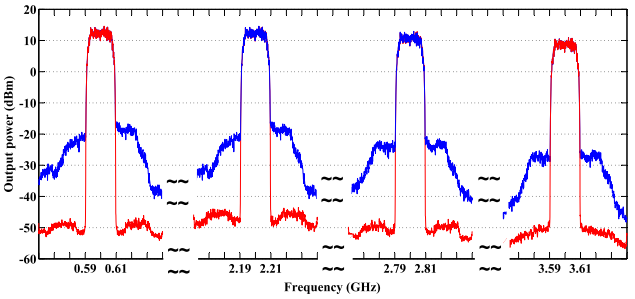


FIGURE 12. The measured output power spectrum at different frequencies. Red lines are with DPD, and blue lines are without DPD.

TABLE 5. The results of signal quality with/without DPD.

	Without DPD			With DPD		
Freq.	Power	ACLR (L/R)	EVM	Power	ACLR (L/R)	EVM
0.6 GHz	34.0	-35.2/-31.5	3.16%	34.0	-61.2/-61.0	0.07%
2.2 GHz	33.9	-35.4/-30.4	3.15%	33.8	-61.8/-60.6	0.11%
2.8 GHz	32.5	-35.2/-34.8	2.59%	32.4	-60.2/-60.4	0.10%
3.6 GHz	30.4	-36.9/-36.2	1.93%	30.4	-59.2/-59.3	0.14%

found if no digital pre-distortion (DPD) technique is used. We adopted a vector-switched model proposed in [32] to linearize this PA, and the final results are given in Table 5. Obviously, this PA can be linearized to satisfy ACLR and error-vector-magnitude (EVM) specifications.

V. CONCLUSION

By introducing the current equation (I-V curves) determined by a transistor's characteristic, practical waveforms and load impedances of a specific device are directly calculated in this work. Based on the impedance calculation method, mode-interpolations for high-efficiency operations are carried in the combinations of fundamental drain voltage's magnitude and phase. These uniform grid-searching results are adopted as the perturbation seeds to overcome the limitation of grid settings and to obtain much more sub-optimal waveforms and impedance solutions. The expanded waveform and solution space is adopted as a design tool to guide the implemented matching network, in order to guarantee the performance requirements. A broadband HEPA example is given to show the design procedures and to discuss some performance deviation factors. The designed PA performances only degrade within an acceptable range, though a lot of simplifications are made. This example PA is fabricated and measured to offer 39.0 - 42.3 dBm power, 8.0 -17.2 dB gain and 58.2% - 69.3% drain efficiency from 0.45 GHz to 4 GHz.

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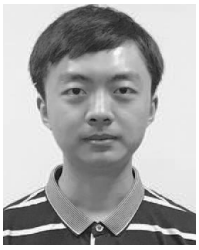

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