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A Compact Integration of a 77 GHz FMCW Radar System Using CMOS Transmitter and Receiver Adopting On-Chip Monopole Feeder

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ABSTRACT This paper presents 77-GHz CMOS radar transmitter and receiver chips equipped with monopole feeders for use in frequency-modulated continuous-wave radar systems. The on-chip monopole feeder can feed not only the aperture of waveguides but also the slots on planar circuits by simply attaching the chips to a printed circuit board using a low-cost non-conductive epoxy. With the aid of a high ratio multiplier and the proposed on-chip feeder, a radar system can easily be integrated without needing to use precise and expensive millimeter-wave packaging technologies. In order to experimentally confirm this, the chips integrated with waveguides are first measured and a full radar system integrated on the planar circuit is evaluated using the microstrip patch antennas. Finally, with the benefit of compact integration technology, the design of a five-channel 3-D environmental sensing radar for small-unmanned aerial vehicles is presented.

INDEX TERMS Radar, CMOS, frequency multiplier, millimeter-wave (mm-wave) packaging, on-chip feeder.

I. INTRODUCTION

Millimeter-wave (mm-wave) radar has gained an increasing amount of attention for use in various applications such as gesture recognition, noncontact vital signal detection, and 3-D imaging [1]–[3]. Especially, due to their sensing performance during day and night and under moist weather conditions, radars are mainly used for advanced driver-assistance systems in vehicles [4], [5]. In recent years, small-Unmanned Aerial Vehicles (UAVs) have attracted significant interest for use in commercial applications such as package delivery, aerial videography, surveillance, and agriculture. A required function for future commercial UAVs will be the ability to sense and avoid obstacles and other UAVs in close proximity. In recent years, X- and K-band radar based collision avoidance systems for small UAVs have been developed and demonstrated [6]–[8]. These applications require the compact integration of radar sensors with a small size, light weight, and low power.

Recent developments in CMOS technology have enabled the successful design of mm-wave transceivers for radar sensors [9]–[12]. Though there are still improvements to be made in mm-wave CMOS systems such as, in terms of noise figure (NF), voltage-controlled oscillator (VCO) phase noise, and achievable power and efficiency, as compared to the state-of-the-art III-V compound technology or Si-Ge technology, the mass production capability of CMOS technology with its good yield and low cost makes it an extremely attractive target for commercial applications. Excluding semiconductor technology, packaging technology for reliable low-loss interconnections between the integrated circuits (ICs) and the external components, including microstrip lines and antennas, is another major challenge in the implementation of these low-cost mm-wave systems. Conventional packaging technologies use wire bonding or flip-chip assembly for interconnections. In the case of wire bonding for mm-wave applications, wedge or ribbon bonding is widely used instead of ball bonding in order to reduce the inductance of wires. Although wire bonding is cheap and easily available, its bonding length cannot be shortened infinitely, leading to bandwidth (BW) limitation or unwanted resonance caused by

wire inductances [13]–[15]. The fine and repeatable control of wire bonding is also essential, since its inductance strongly depends on the geometry of the wire.

Flip chip bonding shows good radio frequency (RF) performance, because it is both more repeatable and shorter and thicker than wire bonding, resulting in lower inductances and a wider BW in the W-band and beyond [16], [17]. However, the flip chip bonding process is more complicated and expensive than traditional methods and is also not readily available for small volume production. Beyond their pros and cons, both interconnections require accurate models for mm-wave system design and often require additional matching networks as well. On-chip antennas or on-chip mounted antennas are low cost mm-wave system integration alternatives to costly and sensitive mm-wave packaging [18]–[20]. Because of their low achievable gain and efficiency, on-chip antennas on lossy silicon substrate are considered to be suitable for short range applications.

Meanwhile, waveguide transitions using electromagnetic wave coupling can serve as an alternative solution for mm-wave interconnections. Waveguide transitions in both compound and CMOS microwave ICs have been successfully developed using on-chip waveguide feeders with an E-plane split metal block [21], [22]. In a previous study in ours [23], the issues of through-silicon vias (TSV) from the chip ground to the waveguide wall along with additional back metallization that are not provided in the standard CMOS process have been resolved by using a segmented quarter-wave open stub in the chip ground plane in the silicon substrate. A high manufacturing cost of waveguides, however, still makes it difficult to integrate in a multi-channel radar system. Therefore, planar mm-wave systems using microstrip antennas are currently preferred for use in low-cost multi-channel applications due to their small size, light weight, and mass manufacturing capability. For the implementation of low-cost and compact mm-wave radar systems, this work presents a new chip to microstrip line interface, as well as an improved CMOS transceiver design as compared to that in our previous work [23] with the included features of good phase noise, low flicker corner frequency, and low reference frequency distribution.

The proposed 77 GHz radar module is composed of separate transmitter (Tx) and receiver (Rx) CMOS chipsets mounted on a Rogers RT/Duroid 5880 substrate as shown in Fig. 1. The 77 GHz signals are delivered from the chipset to the substrate through the proposed transition structure. The remaining low frequency signals including the modulated reference signal, IF signals, and dc biases are delivered using ball bonded wires. The Tx and Rx chipsets are designed using a 65 nm low-power RF CMOS process with 1-poly 9-metals. The RF nMOS field-effect transistors (FETs) used in the process show 126 GHz f_T and 225 GHz f_{MAX} at 250 μA/μm current density.

The rest of this paper is organized as follows. Section II will present details about the design of the proposed slot-coupled chip-to-microstrip transition using an on-chip monopole

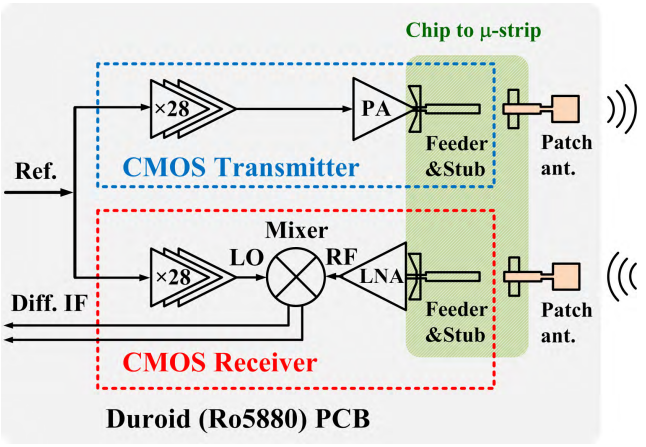

FIGURE 1. Block diagram of the proposed radar.

feeder and simulation results. Section III will explain the designs of the Tx and Rx chipsets along with their simulation and measurement results. Section IV will describe the mm-wave module implementation and their antenna pattern measurements. Section V will show system implementation and measurement results for small-UAV applications, followed by a conclusion in Section VI.

II. DESIGN OF SLOT COUPLED CHIP-TO-MICROSTRIP TRANSITION

The slot-coupled vertical microstrip transition is a well-known structure and has been investigated for use in various configurations [24]–[26]. The conventional transition consists of three simple layers, among which the middle layer forms the shared ground plane and the slot aperture for resonant coupling. In order to utilize the slot coupling structure between the mm-wave chip and the external substrate, a top microstrip line should be formed on the chip, with the other microstrip line placed on the backside of the substrate and the slot formed on the top layer of the substrate. A crucial difference between the proposed structure and the conventional multilayered printed circuit board (PCB) lies in the feeding structure of the top microstrip line. It appears that the feeding line on the chip is driven with its own reference ground in the chip which is isolated from the ground plane of the bottom microstrip line in the substrate. Therefore, the on-chip ground reference for the feeding microstrip in the chip should be tightly connected to the ground plane of the substrate. Unfortunately, since the standard CMOS process does not provide the TSV, the vertical microstrip transition cannot be readily used in the CMOS design. In this study, the slot-coupled microstrip transition structure is newly designed for the W-band chip-to-microstrip transition using an on-chip segmented quarter-wave open stub in order to achieve low impedance between the chip ground and the substrate ground. The on-chip ground open stub has already been evaluated and successfully used for the waveguide feeder in our previous work [23].

The geometries of the proposed transition are illustrated in Fig. 2. The design was carried out using the ANSYS

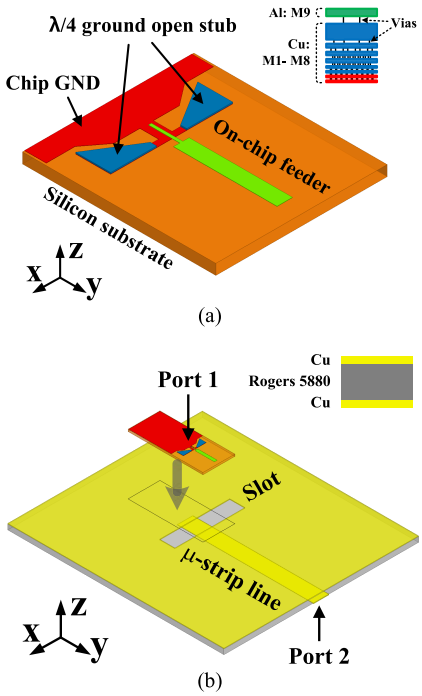

FIGURE 2. Geometries of the proposed (a) on-chip feeder and ground open stub, (b) slot-coupled chip-to-microstrip transition.

3-D electromagnetic (EM) simulator. The proposed transition structure is comprised of the feeder and ground open stub formed on the silicon substrate as well as a half-wavelength ($\lambda_g/2$) slot etched on the ground plane of the PCB substrate. A 50 Ω microstrip line is placed on the back side of the ground plane. The metal layers on the silicon used in the design of the feeder and stub are depicted in Fig. 2(a). The two lowest stacked metal layers (m1, m2) are used for the ground plane of the active circuit. The open stub uses entire copper (Cu) layers (m1-m8) in order to minimize metallic loss. The top aluminum (Al) metal layer (m9) is chosen for the feeder design since better return loss is acquired than the thick Cu layer. The chip is directly attached on the PCB board, and the feeder is placed perpendicularly at the center of the slot. Finally, the upper edge of the open stub is aligned with the lower edge of the slot, as shown in Fig. 4, along with the design parameters. As mentioned above, Rogers RT/Duroid 5880 substrates are used as PCB with a dielectric constant of 2.2, loss tangent of 0.0009, dielectric thickness of 5 mil, and Cu thickness of 18 μm. In order to minimize substrate loss, the thickness of the silicon substrate is polished to 50 μm as previously discussed in [23].

3-D EM simulation was performed to evaluate the performance of the proposed transition. As shown in Fig. 2(b), Port 1 is located at the feeder, and Port 2 is located at the end of the microstrip line on the PCB. The simulation model includes a microstrip line on the PCB 3 mm away from the middle of the slot. Fig. 3 shows the simulation results of the current and electric field (E-field) distributions in the xy- and xz-planes, which confirm that the slot and quasi-TEM transmission modes are both successfully excited.

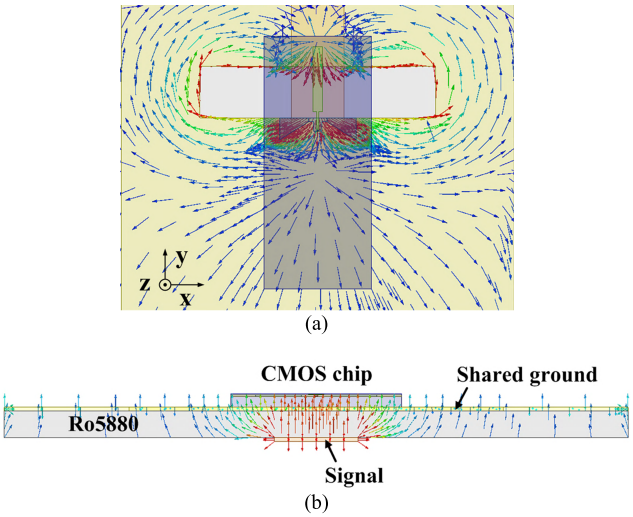

FIGURE 3. EM simulation results of (a) current distribution and (b) E-field distribution of the proposed transition structure at 77 GHz.

The simulated insertion loss between Port 1 and Port 2 is 2.05 dB, and the input return losses at Port 1 and Port 2 are over 20 dB at 77 GHz, as depicted in Fig. 5(a).

Additional simulation results showed that the insertion loss of the proposed transition was decreased to 1.07 dB when using a silicon substrate with a resistivity of 100 Ω·cm. Therefore, if a low loss Si-substrate like the RF-SOI CMOS process is utilized, the transition loss will be drastically reduced. From 62.2 GHz to 87.1 GHz with 32.2% BW, it is confirmed that the return loss is more than 10 dB, and the insertion loss is less than 2.05 dB. This indicates that the proposed transition can feed microstrip antennas without the need for sensitive bonding, vias, or additional matching networks.

Single patch and 4×4 patch array antennas were additionally designed on the PCB in order to build the Tx and Rx system according to the detection range. A microstrip feed network was realized using a λ/4 transformer and T-junction for input impedance matching. Fig. 5(b) shows the simulated S_{11}-parameters of the antennas. The simulated 10 dB BW of the single and array antennas were 3.3 GHz and 6.1 GHz, or 4.3% and 7.9%, respectively.

In consideration of the assembling tolerance of the die attachment, additional simulations were carried out with several chip positions within 100 um misalignment in all directions. As a result, it was revealed that the misalignments along both x and y-directions increased the insertion loss by less than 0.01 dB. However, the insertion loss increased to 0.7 dB when moving backward in the y-direction, because the offset length of the feeder with respect to the ground was changed. Thus, the chip is to be carefully attached so that the upper edge of the open stub in Fig. 4 is aligned with the lower edge of the slot.

The proposed on-chip monopole feeder and ground open stub can feed both types of external components: metallic waveguides and microstrip lines. The design of the chip-to-waveguide transition was additionally carried out. The design

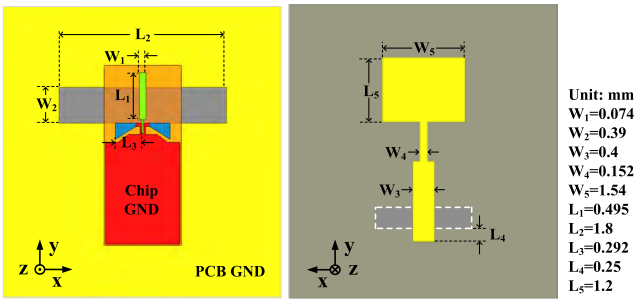

FIGURE 4. Top and bottom views of the transition and single patch antenna with dimensions.

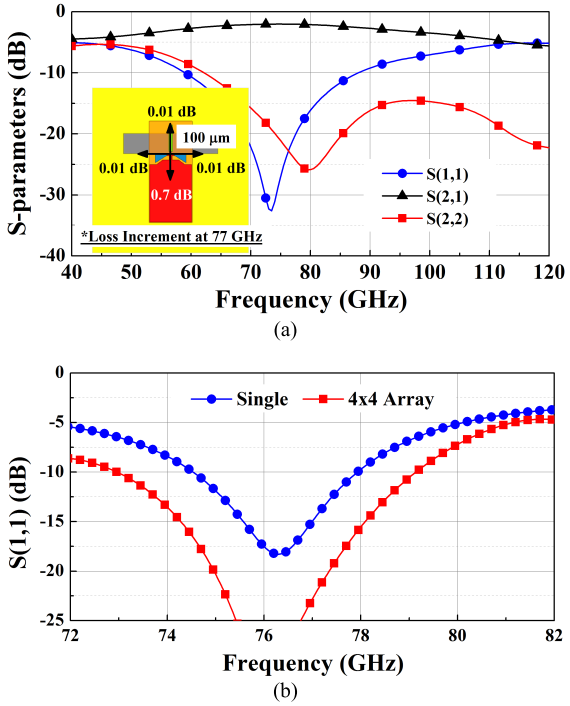

FIGURE 5. Simulated S-parameters of (a) the transition and (b) the transition with patch antennas.

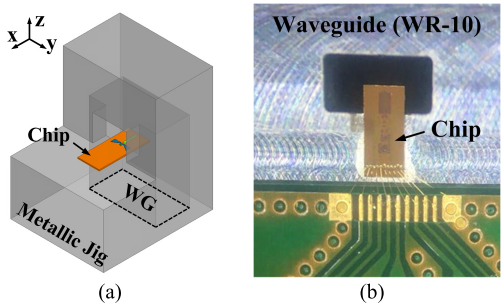

FIGURE 6. (a) Simulation model of the chip-to-waveguide (WG) transition and (b) photograph of the fabricated module.

process is similar to that used in our previous work [23]. As shown in Fig. 6(a), an aluminum metal block is used to realize the WR-10 waveguide. The chip is attached on the waveguide aperture so as to excite the 77 GHz signal. A standard UG-38/U waveguide flange was realized at the other side

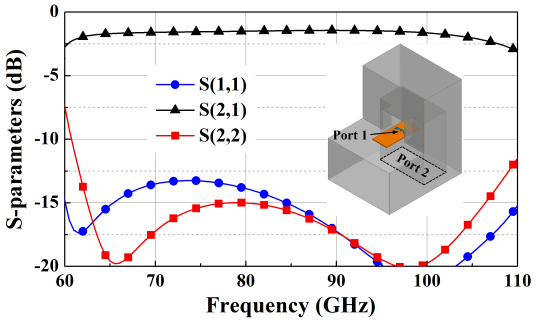

FIGURE 7. S-parameter simulation results of the waveguide transition.

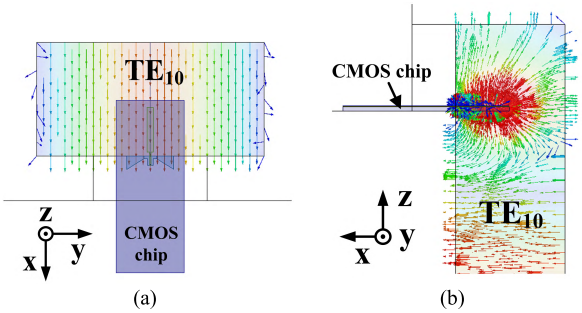

FIGURE 8. E-field distribution in: (a) xy-plane and (b) xz-plane.

TABLE 1. Performance summary.

Ref.	Transition	Frequency	Insertion Loss
[23]	Chip (CMOS) to WG	77 GHz	1.37 dB [a]
This work	Chip (CMOS) to μ-strip (PCB)	77 GHz	2.05 dB [a, c]
This work	Chip (CMOS) to WG	77 GHz	1.5 dB [a]
[27]	μ-strip (PCB) to WG	84 GHz	4–5 dB [a, c]
[28]	Chip (In HEMT) to WG	320 GHz	1.3 dB [b]

[a] Simulation result. [b] Measurement result. [c] Line loss included.

of the aperture in order to connect the input or output ports of the measurement instruments as well as waveguide-fed antennas. The reference signal for the multiplier chain and the dc bias are applied to the chip using the FR-4 PCB and bonding wires, as shown in Fig. 6(b). The Tx and Rx modules based on the waveguide transition are used to characterize the chip performance and build the long-range radar measurements in Section III-C.

In order to investigate the transition performance of the proposed structure at 77 GHz, 3-D EM simulation was performed. As shown in the inset of Fig. 7, Port 1 is located at the on-chip feeding point and Port 2 is located at the waveguide side 5 mm away from the chip. The simulated insertion loss between Port 1 and Port 2 is 1.5 dB, and the input return losses at Port 1 and Port 2 are greater than 13 dB. Fig. 8 shows the simulation results of the E-field distribution in the xy- and xz-planes, which confirm that the TE_{10} modes are successfully generated. The simulation results of the monopole feeder are summarized in Table 1 and compared with those of the previously developed mm-wave transitions.

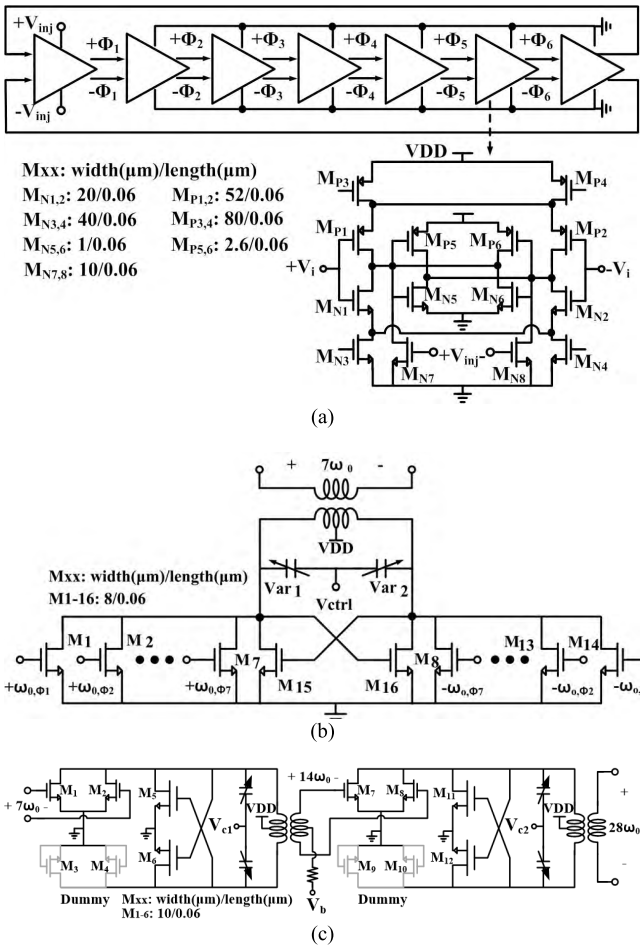

FIGURE 9. Schematic of ×28 frequency multiplier. (a) Ring oscillator. (b) Seven-push frequency multiplier. (c) Two stage push-push frequency doubler.

III. DESIGN OF FREQUENCY MULTIPLIER BASED TRANSCEIVER

A. FREQUENCY MULTIPLIER DESIGN

As discussed in Section I, for local oscillator (LO) signal generation, a frequency multiplier is used instead of phase locked loops (PLLs) for better phase noise; this is because it is easier to obtain good phase noise at mm-wave frequencies with a frequency multiplier than with PLLs [29], [30]. In this study, a ×28 frequency multiplier is adopted to lower the reference signal frequency to the sufficiently low frequency of 2.75 GHz, which can be easily distributed and ball-bonded on the low-cost FR-4 PCB. The multiplier chain is similar to the ×10 frequency multiplier used in our previous work [23], [31]. However, for the lower reference frequency, the higher order seven-push multiplier has been re-designed for this study. This seven-phase ring oscillator at 2.75 GHz also draws less power than the five-phase ring oscillator at 7.7 GHz. The schematic of the ×28 frequency multiplier is depicted in Fig. 9. A differential seven-push multiplier and a two-stage push-push doubler compose the multiplier chain in order to generate a 77 GHz signal. The basic operating principle of the proposed ×28 frequency multiplier is the same as that outlined in [31] and [32].

B. TX AND RX DESIGN

Fig. 10(a) shows the schematic diagram of the proposed frequency multiplier based Tx. The Tx consists of a ×28 frequency multiplier and a power amplifier (PA). Moreover, in order to transmit the mm-wave signal, the on-chip monopole feeder is attached to the PA output. The PA was designed with reference to [23] and [33], which employ a cross-coupled pair and neutralization techniques. Two Tx chips, one with the feeder and one with pads, were separately designed for comparison; the results of this comparison are given in the next section.

The Rx is composed of a low noise amplifier (LNA), a passive mixer, and a ×28 frequency multiplier, with a schematic shown in Fig. 10(b). The on-chip monopole feeder is coupled to the LNA through the transformer balun with a balancing capacitor C_1 [34]. The LNA consists of transformer-coupled four-stage CS amplifiers to provide sufficient gain to suppress the flicker noise of the mixer and baseband circuitry. The cross–coupled capacitors are used to neutralize the feedback capacitor C_{gd} in order to improve gain and stability [33]. The simulated LNA NF was 7.17 dB at 77 GHz. A standalone LNA with RF pads has been separately designed and fabricated for on-wafer measurement, and the results of this are shown in Fig. 11. The LNA shows a 28 dB gain at 77 GHz and a peak gain of 29.7 dB at 75.5 GHz. The 3 dB BW is 74.5-78.1 GHz and the LNA consumes 41 mA dc current.

When the beat frequency of the frequency modulated continuous wave (FMCW) radar falls below 1 MHz, the flicker corner frequency of the mixer critically affects the sensitivity of the Rx. In order to solve this issue, a passive mixer is adopted in the present design. The output current of the LNA is transformer-coupled to the mixer. The series capacitor C_{14} is used to improve the conversion from the differential output of the LNA to the single ended input to the mixer. It also ensures that the following passive mixer is biased at zero dc current. The gate-to-source voltage of the mixer switches is biased near the threshold voltage. A differential common-gate (CG) amplifier using pMOS FETs is followed so as to ensure low input impedance to the mixer switches and to convert the IF current to voltage.

Die microphotographs of the Tx and Rx are shown in Fig. 12. The chip sizes of the Tx and Rx are 0.9 mm × 1.7 mm and 0.9 mm × 1.8 mm, respectively. The measurement results of the entire Tx and Rx will be given in the next section.

C. TX AND RX MEASUREMENT RESULTS

As mentioned in Section II, the Tx and Rx modules based on the proposed waveguide transition are prepared with the ability to connect the input or output port of measurement instruments as well as waveguide-fed antennas. First, the Tx chip with pads has been measured using on-wafer probing as a reference. A 2.75 GHz reference signal of 0 dBm power is applied to the chips and modules using the synthesized sweeper (HP, 8340B). The waveguide Tx module achieved an output power of 8.3-9.1 dBm within a lock range

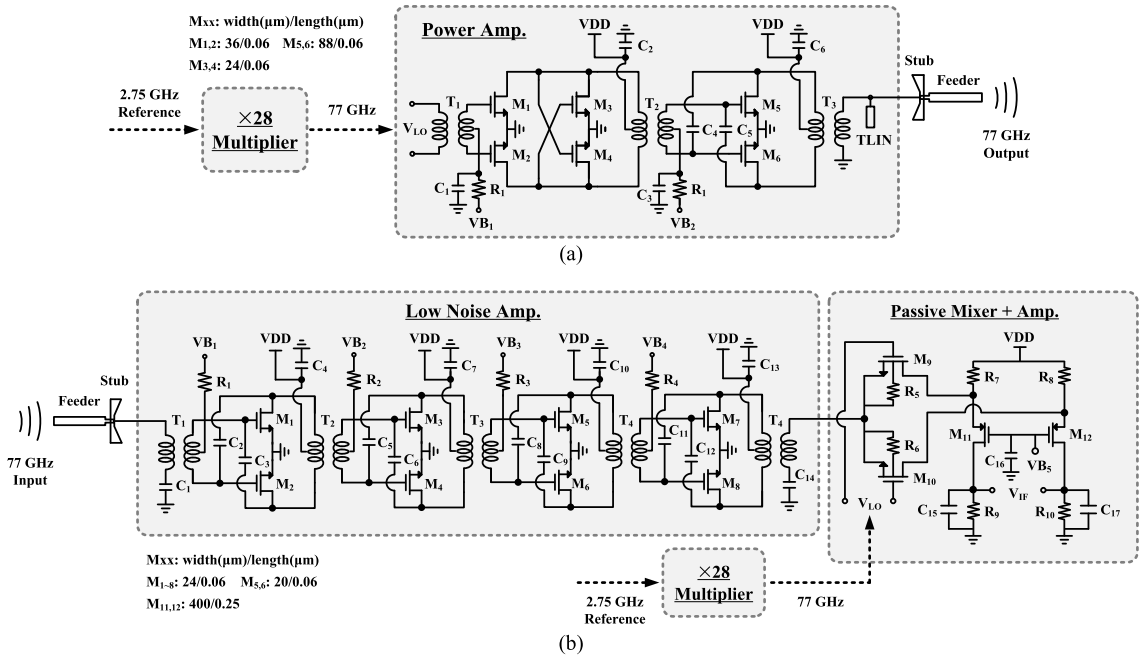

FIGURE 10. Frequency multiplier based Tx and Rx chipsets equipped with on-chip monopole feeders and open stubs. (a) Tx with an on-chip monopole feeder and an open stub. (b) Rx with an on-chip monopole feeder and an open stub.

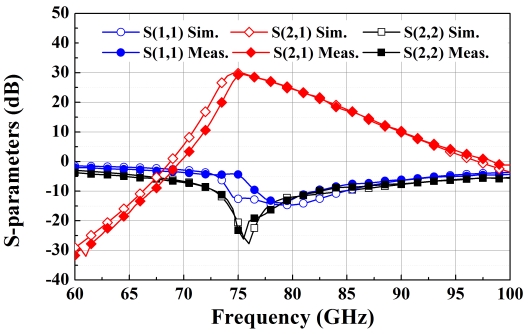

FIGURE 11. On-wafer measurement results of the standalone LNA.

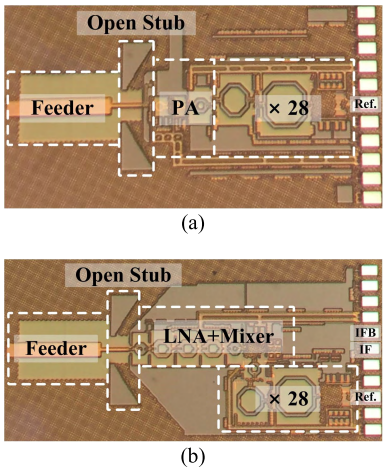

FIGURE 12. Die photographs. (a) Tx chip. (b) Rx chip.

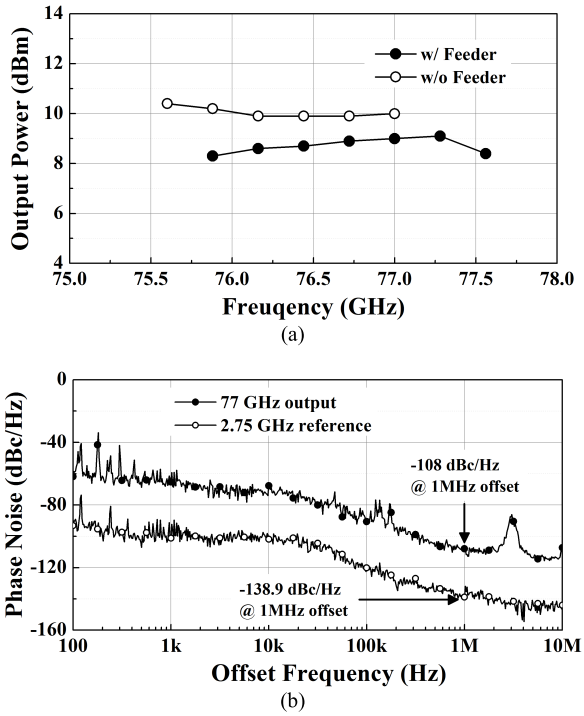

FIGURE 13. Tx measurement results. (a) Output power. (b) Phase noise.

of 75.88 to 77.56 GHz. The output power is 1-2 dB lower than that of the on-wafer measurement results, due to the loss of the transition as shown in Fig. 13(a). The 2.75 GHz reference signal shows −138.9 dBc/Hz phase noise at 1 MHz offset frequency and the 77 GHz output signal of the waveguide module achieves −108 dBc/Hz phase noise at the same offset frequency. The phase noise degradation is 30.9 dB, which is very close to the amount of the theoretical degradation of 28.9 dB. The multiplier chain and PA use 1.2 V supply voltage and the total dc power consumption is 217.2 mW.

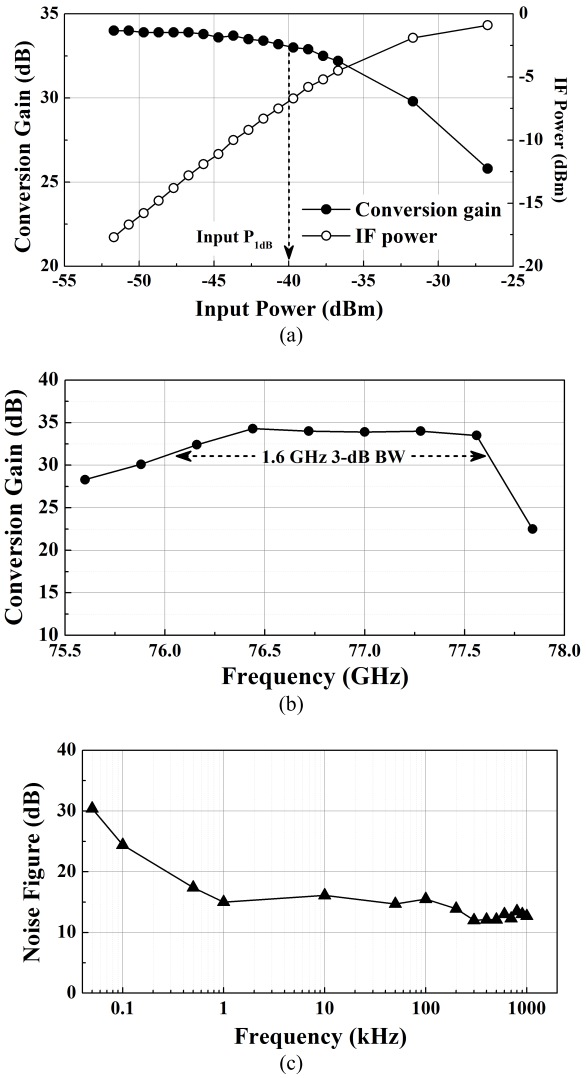

FIGURE 14. Rx measurement results. (a) Conversion gain and IF power at 500 kHz. (b) Conversion gain versus RF frequency. (c) Noise figure.

The sub-harmonics of the 77 GHz output signal were investigated with a spectrum analyzer (Agilent, N9030A) and a W-band harmonic mixer (Agilent, 11970W), and it was confirmed to have a spur suppression better than 51 dBc.

For gain measurement, the Rx waveguide module is driven by the W-band input signal from the vector network analyzer (Anritsu, ME7838A). The IF signal of the Rx module was measured using a spectrum analyzer and an external unity-gain preamplifier. The measurement results of the Rx module are shown in Fig. 14(a). The module achieves 34 dB gain for 77 GHz RF frequency and 500 kHz IF frequency. As shown in Fig. 14(b), the module has 3 dB BW of 1.6 GHz from 76-77.6 GHz RF input. The Rx NF is roughly determined by measuring the average noise power with a 50 Ω waveguide termination at the RF input using a spectrum analyzer and a low noise high gain IF preamplifier (AMETEK, Model 5113) in order to suppress the noise of the spectrum analyzer. The measured system NF is 12.7 dB at 1 MHz as shown in Fig 14(c). Although it is difficult to uniquely determine the flicker corner frequency of the receiver, it is confirmed that NF is below 15 dB down to 1 kHz, which is an improvement as compared with [23] due to the high gain LNA and passive mixer. The dc power consumption of the Rx module is 154.8 mW.

Long range detection of the radar using the proposed waveguide Tx and Rx modules was performed. The radar implementation, target, and measurement scenario are basically the same as those described in our previous work [23]. An external module composed of VCO (CRYSTECK, CVCO55CC) and PLL (Analog Device, ADF 4158) operating in a fractional mode is used to generate accurate ramp reference signals for FMCW implementation. The Tx signal has a 560 MHz BW at 77 GHz, and its measured phase noise was −103.6 dBc/Hz at 1 MHz. The commercial 24 dBi horn antenna is assembled at the waveguide flange of the Tx and Rx modules. The modules are placed about 50 cm above the ground surface.

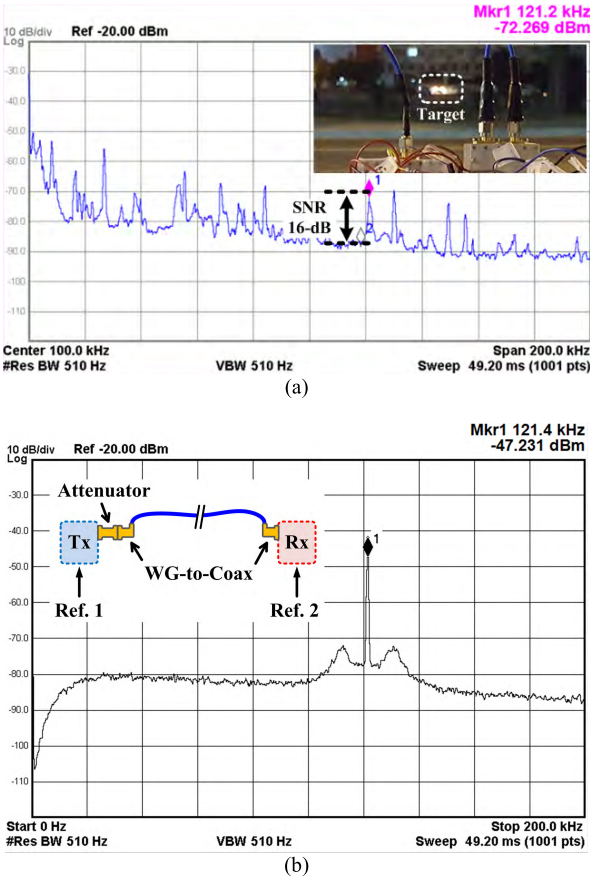

FIGURE 15. Measured IF spectrum. (a) Outdoor range detection measurement results. (b) Loop-back test results using the 90 dB attenuating chain.

Fig. 15(a) shows the IF spectrum measured in the campus parking lot. It was clearly observed that the changing IF frequency of the reflected signal from the slowly moving target (a sedan). As specified in [35], a 16 dB signal-to-noise ratio (SNR) was used to determine the maximum detectable range. For the specified SNR, the peak of the target echo

TABLE 2. Comparison of transceiver performance.

	2010 JSSC [10]	2010 JSSC [9]	2015 MTT [23]	2017 JSSC [12]	This Work
Application	Automotive	Automotive	Automotive	Automotive	Automotive/Small-UAV
Technology	90 nm CMOS	65 nm CMOS	65 nm CMOS	28 nm CMOS	65 nm CMOS
Transition	Wafer probing	Chip-to-WG	Chip-to-WG	Chip-to-μ line	Chip-to-μ line / Chip-to-WG
Mm-wave Packaging Technique	N/A	Bonding wire	On-chip feeder and λ/4 ground stub	Flip chip	On-chip feeder and λ/4 ground stub
Antenna Type	Horn	Patch array	Horn	Patch array	Patch array / Horn
Frequency (GHz)	78.1-78.8	75.6-76.3	76.8-77.4	79	75.88-77.56
Phase Noise (dBc/Hz @ 1MHz offset)	–85	–85.33	–97.6	–85	–103.6
Tx Output Power (dBm)	–2.8	5.1	8.9	8.5	9
PA Power Gain (dB)	14	13.7	8.5	N/A	N/A
Rx Conv. Gain (dB)	23.1	38.7	13	N/A	34
Rx NF (dB)	15.6	7.4*	7.95*	12	12.7
Max. Measured Distance (m)	8	106	85.2	N/A	162.3
Power Consumption (mW, Tx / Rx)	520	243	264.4 / 203	1000	217.2 / 154.8
Chip Area (mm^2, Tx / Rx)	3.5×1.95	0.95×1.1	0.91×1.36 / 0.91×1.46	7.9	0.9×1.7 / 0.9×1.8

* LNA noise figure.

was found at 121.2 kHz, which corresponded to a distance of 162.3 m from the radar. The other signals in Fig. 15(a) remained unchanged as the target was moving and therefore they were reflections from the stationary environment (trees and other cars). Assuming the radar cross section (RCS) of the vehicle as 10 m^2at 162 m away, the received power of the proposed radar system using the radar range equation [35] and the RX gain of 34 dB is about −68.5 dBm, which is reasonably similar to the measured power of −72 dBm in Fig. 15(a) considering additional losses and uncertainty of RCS.

In addition, a loop-back test for the proposed radar system was carried out in order to evaluate the radar operation. Fig. 15(b) shows the configuration and results of the test. The inset of Fig. 15(b) depicts the measurement setup composed of a 30 dB waveguide attenuator, waveguide-to-3.5 mm coaxial adaptor, and 3.5 mm flexible coaxial cable, which shows about a 90 dB loss at 77 GHz. The IF offset due to the round-trip delay was realized by applying two different reference frequencies. As shown in Fig. 15(b), a clear IF signal at 121 kHz was measured with a power level of −47 dBm. Considering the Tx output power of 9 dBm and the attenuation of 90 dB, the estimated Rx gain based on the loop-back test is about 34 dB, which is very close to the separately measured gain of the Rx. A performance comparison of published single-channel radar systems based on the CMOS process for 77 GHz FMCW automotive radar is presented in Table 2.

IV. PLANAR MODULE INTEGRATION AND ANTENNA PATTERN MEASUREMENTS

In this section, the integration of the planar Tx and Rx modules is discussed, and the simulation and measurement results of their radiation performances are given. As shown in Fig. 16, in order to build a planar radar system, the Tx and Rx modules were implemented using the chips and vertical transitions explained in the previous sections.

Based on the slot coupled chip-to-microstrip transition described in Section II, planar antennas with the advantages of small size and light weight can be used for the

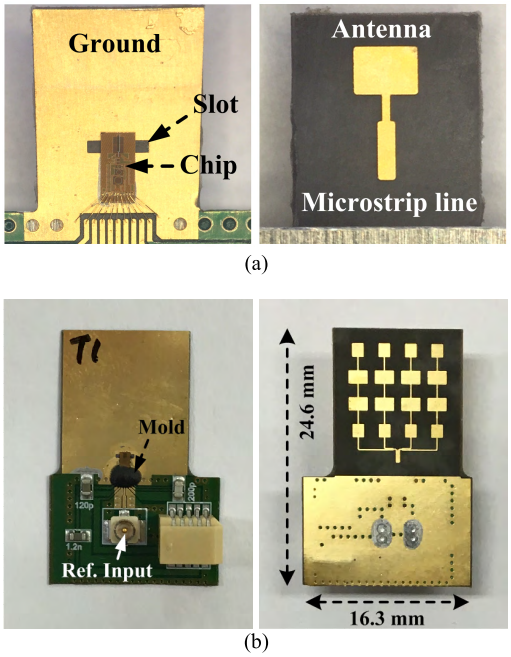

FIGURE 16. Fabricated Tx planar modules. (a) Single patch antenna module. (b) 4×4 Patch array module.

implementation of the Tx and Rx modules. Single and array antennas have been designed and fabricated. Similar to the waveguide module implementation described in Section III-C, the IF, reference signals, and dc bias are distributed using low-frequency wire bonding. Ball bonding was adopted and the bond-wires were molded so as to ensure higher mechanical reliability, as shown in Fig. 16(b). The reference signal is applied to the module through a U.FL connector, and the dc bias is supplied by board-to-board connectors, as shown in Fig. 16(b). The total size of the array antenna module is 16.3 mm × 24.6 mm. The chips are directly attached on the Rogers RT/Duroid 5880 PCB using low-cost non-conductive epoxy (STYCAST, A312-20) and conductive silver epoxy for comparison.

Fig. 17 shows a setup for far-field gain pattern measurement. A W-band standard horn antenna with a gain of 24 dBi

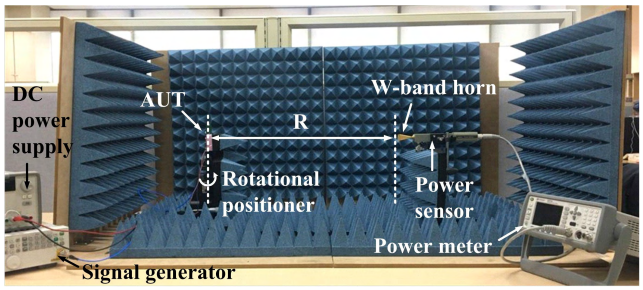

FIGURE 17. Gain pattern measurement setup.

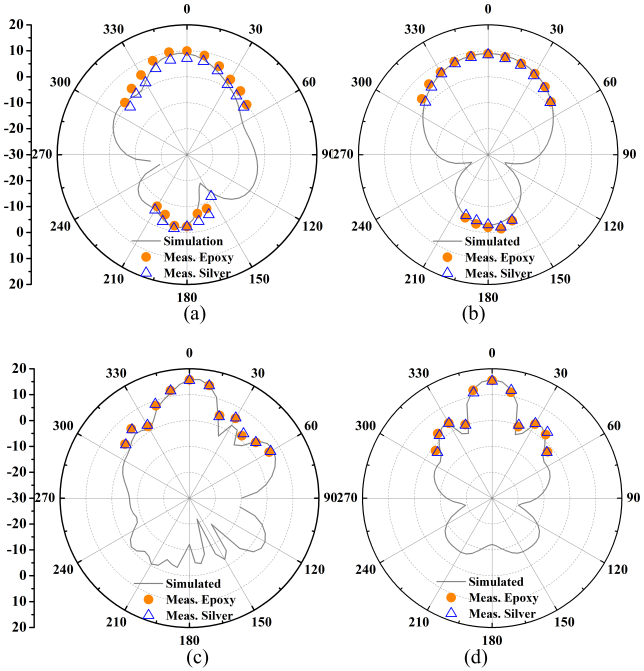

FIGURE 18. Simulated and measured gain patterns of the integrated Tx module at 77 GHz. (a) E-plane of single patch. (b) H-plane of single patch. (c) E-plane of 4×4 patch array. (d) H-plane of 4×4 patch array.

is placed at a distance of 25 cm from the antenna under test (AUT). The AUT are placed on a rotational positioner which scans between ±50°. RF absorbers are used around the setup so as to reduce unwanted reflections and standing waves. In order to measure peak gain, the system is calibrated with two identical horn antennas. The standard horn antenna is connected to the waveguide Tx module and pointed toward the already-known peak direction. Then, the received RF power is compared with that measured in the planar Tx module. The received power is detected using a Keysight W8486A power sensor combined with an N1914A power meter. The measured E- and H-plane patterns of a single antenna at 77 GHz are shown in Fig. 18 (a) and (b), respectively, which are highly consistent with simulation results. Backward radiation is further measured in order to confirm the change in front-to-back ratio (FBR) caused by the feeder and the slot. This confirms that the FBR is 11.5 dB, which is very similar to the simulated value of 11.8 dB. Fig. 18 (c) and (d) show the simulated and measured gain patterns of the array antenna, respectively.

Good agreement was observed between the simulation and measurement results for both the E- and H-planes. Due to the dynamic range of the power sensor, the FBR of the array antenna could not be measured. Based on the measurement results of the waveguide modules and planar modules, the proposed transition structure using the on-chip monopole feeder is considered to operate successfully at the W band. Additionally, a die attach using low cost insulating epoxy provides the same performance as one using costly silver epoxy, which enables simple and low-cost module integration.

V. RADAR SYSTEM IMPLEMENTATION AND MEASUREMENTS

In this section, highly compact W-band radar integration based on the proposed chip-to-microstrip transition was first performed for use in small-UAV applications.

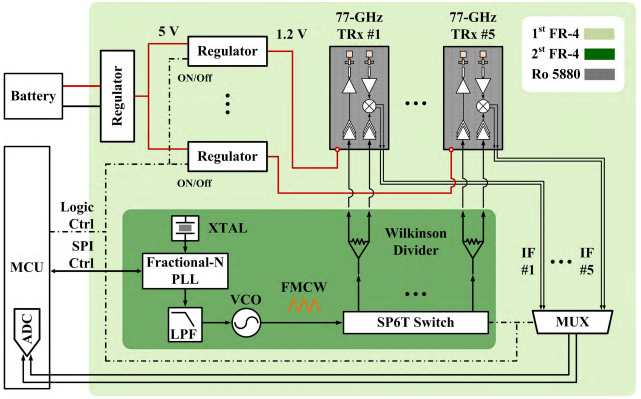

FIGURE 19. Proposed radar system architecture.

The proposed radar system architecture for small-UAVs is shown in Fig. 19. The system consists of 77 GHz Tx and Rx modules, fabricated and verified as discussed in the previous section, as well as a baseband board, which is composed of a reference generation part and bias circuits. As described previously, the 77 GHz Tx and Rx modules are comprised of the Tx and Rx chipsets together with the proposed chip-to-microstrip transition, along with patch array antennas on a Rogers RT/Duroid 5880 substrate. The 77 GHz Tx and Rx modules are connected to a modified multi-sector baseband board using board-to-board connectors. In order to reduce the size and fabrication cost of the proposed system, two independent PCBs for the baseband board are stacked together. The EM simulation was performed to evaluate the isolation characteristics between the Tx and Rx modules. The nearest Rx is 19.5 mm ($5 \times \lambda_0$ at 77 GHz) away from the Tx. The simulated isolation is about 64 dB at 77 GHz, which is sufficient to prevent Rx saturation.

The bias circuits and the multiplexer (MUX) for time-interleaved IF signals are mounted on the first layer PCB. The second layer PCB, as shown in Fig. 19, consists of a reference generation, synthesizer part, and power dividing part for LO signals. For FMCW implementation, the reference ramp signal with a 1 ms ramp time and 20 MHz BW at 2.75 GHz

is chosen. The final transmitting FMCW signal has 1 ms ramp time and 560 MHz BW at 77 GHz.

For efficient use of multi-sector radars with reduction of power consumption and complexity of data acquisition and concurrent signal processing, the time-interleaving operation of the radars was used in this work. The regulator connected to each radar was turned on and off sequentially. Further, the reference signal was distributed using a Wilkinson power divider, and a single-pole 6-throw (SP6T) switch was used to sequentially drive the reference signal. The IF signals collected in the MUX are transmitted in a multiplexed way in a time sequence to an analog-to-digital converter (ADC). The micro controller unit (MCU) board controls the PLL synthesizer, the regulators, the switch, and the MUX using their serial to peripheral interface (SPI) and logic interface. An Arduino DUE board was used as the MCU. Moreover, the IF signals were digitized by means of an internal ADC of the MCU board. The ADC provides a 12 bit output with sampling rates of 1 MSample/s. The fixed point FFT algorithm is implemented in the MCU in order to calculate the distance. The final results from the MCU are sent to the Wi-Fi module for data transmission to ground station. As shown in Fig. 20, the entire radar system is implemented into a small-UAV (DJI, Matrice 100) so that it can sense obstacles in the four sides and the downside.

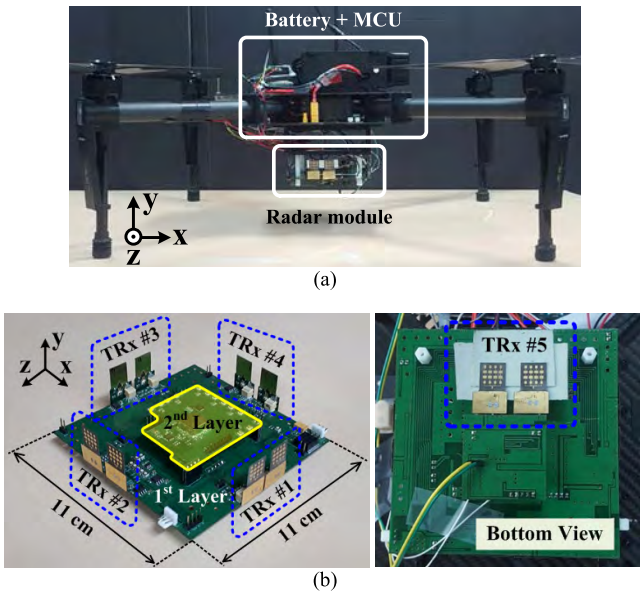

FIGURE 20. Radar system implementation for a small-UAV. (a) Side view of the UAV. (b) Proposed radar systems.

Fig. 21(a) shows the measurement scenario for the UAV to detect obstacles. The UAV was hovering at an altitude of 1 m and flying while detecting metal plates 2 m away from the UAV. The measurement results are shown in Fig. 21(b). The radar systems captured distance information between the UAV and any obstacle for all four sides, and detected its height from the ground. In Fig. 21(b), the x-axis depicts the measured range using TRx #1 and #3, while the y-axis represents the measured height using TRx #5.

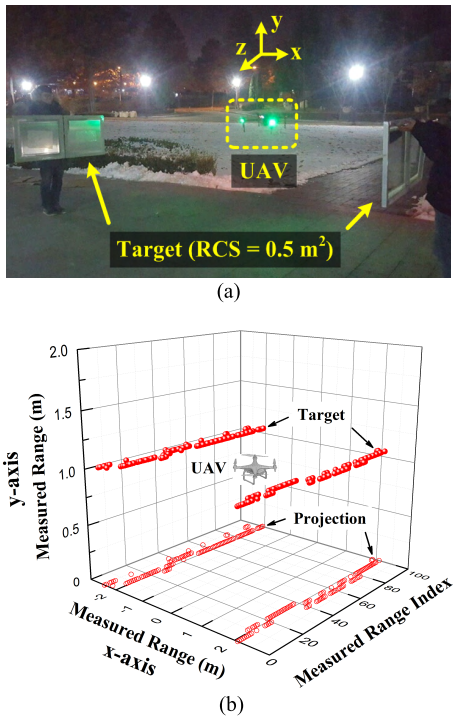

FIGURE 21. Range detection measurements for a small-UAV application. (a) Experiment environment. (b) Measured ranges.

VI. CONCLUSION

CMOS Tx and Rx chipsets adopting an on-chip monopole feeder for a 77 GHz radar system have been presented in this work. Using their high ratio multiplier and the proposed transition structure, the W-band radar system can be easily realized without the need for any complex mm-wave packaging techniques. Range detection measurements for applications in small UAVs as well as automobile were successfully demonstrated. Through the first demonstration for the UAV, it is particularly expected that the proposed compact 77 GHz radar system with a novel packaging technique can be employed to solve the problems of collision protection and indoor navigation for future UAV applications.

ACKNOWLEDGMENT

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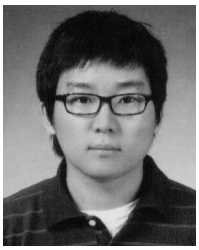

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