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Single Flip-Chip Packaged Dielectric Resonator Antenna for CMOS Terahertz Antenna Array Gain Enhancement

CHUN-HSING LI[1,2], (Member, IEEE), and TE-YEN CHIU[1]

[1]Department of Engineering and System Science, National Tsing Hua University, Hsinchu 30013, Taiwan
[2]Center for mmWave Smart Radar Systems and Technologies, National Chiao Tung University, Hsinchu 30013, Taiwan

Corresponding author: Chun-Hsing Li (chli@mx.nthu.edu.tw)

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ABSTRACT A single dielectric resonator antenna (DRA) capable of enhancing the antenna gain of each element of a 2×2 terahertz (THz) antenna array realized in a 0.18-μm CMOS technology is proposed in this paper. The DRA implemented in a low-cost integrated-passive-device technology is flip-chip packaged onto the CMOS antenna array chip through low-loss gold bumps. By designing the DRA to work at the higher order mode of $TE_{3,\delta,9}$, only a single DRA, instead of conventionally needing four DRAs, is required to simultaneously improve the antenna gain of each element of the 2×2 antenna array. This not only simplifies the assembly process, but it can also reduce the assembly cost. Moreover, the DRA can provide great antenna gain enhancement because of being made of high-resistivity silicon material and higher order mode operation. The simulated antenna gain of each on-chip patch antenna of the 2×2 CMOS antenna array can be increased from 0.1 to 8.6 dBi at 339 GHz as the DRA is added. To characterize the proposed DRA, four identical power detectors (PDs) are designed and integrated with each element of the 2×2 THz antenna array. By measuring the voltage responsivity of each PD output, the characteristics of each antenna of the antenna array with the proposed DRA, including the gain enhancement level and radiation pattern, can be acquired. The measurement results match well with the simulated ones, verifying the proposed DRA operation principle. The four PDs with the proposed DRA are also successfully employed to demonstrate a THz imaging system at 340 GHz. To the best of our knowledge, the proposed DRA is the one with the highest order operation mode at THz frequencies reported thus far.

INDEX TERMS Antenna, CMOS, dielectric resonator antenna, flip-chip packaging, higher-order mode, power detector, silicon, terahertz, terahertz imaging system.

I. INTRODUCTION

THz technology and science have attracted great attention recently because they can be employed for many useful applications, such as high-speed wireless data communication, non-invasive biomedical and medical imaging, stand-off detection of weapons and explosives in public places, etc [1]–[4]. Moreover, THz wave is nonionizing, very safe technology as compared with the X-ray. Using CMOS technology to realize the THz systems for the aforementioned applications is appealing since it can provide a low-cost, high-integration, and high-yield solution, having a great potential to enable the THz systems to step into the consumer market. Of the building blocks of these THz systems, antennas are critical components since their performances directly determine the equivalent isotropically radiated power (EIPR) of a transmitter and how much power a receiver can receive. However, a critical issue exists that CMOS on-chip antennas show low radiation efficiency due to the lossy silicon substrate and unfriendly back end of line (BEOL), dramatically degrading the THz system performance [5], [6]. For instance, the simulated antenna gain of an on-chip patch antenna realized in a 0.18-μm CMOS technology is only 0.1 dBi with the radiation efficiency of 20% at 340 GHz. Many techniques have been proposed to improve the on-chip antenna performance, such as antennas with artificial magnetic conductors [7], [8], substrate thinning [9], [10], silicon

lenses [9], [11], micromachined antennas [12], and superstrates [13], [14]. Yet these techniques either provide limited gain improvement or need complex fabrication process and also occupy a large volume.

A dielectric resonator antennas (DRA) is a good alternative to give large antenna gain enhancement for a single THz antenna [6], [15]–[22]. However, the DRA is not a good solution to improve the gain of a THz antenna array. Fig. 1(a) shows a 2×2 antenna array with inputs designated as P_{in1} to P_{in4}, respectively. For a 2×2 THz-phased array transceiver, four transceivers with independent phase and amplitude tuning capabilities are connected to P_{in1} to P_{in4} of the antenna array, respectively. DRAs can be employed to improve the antenna gain of these on-chip antennas. However, as illustrated in Fig. 1(a), conventionally four DRAs are required to improve each element of the 2×2 antenna array. This may face assembly difficulties because of the short distance between the DRAs, especially as the operation frequencies reach the THz band. For instance, the distance between two elements of an antenna array at 300 GHz is usually selected as a half wavelength, that is, 0.5 mm. Moreover, the assembly cost becomes higher if we would like to enhance the gain of a larger antenna array, for instance, 4×4 antenna array. If we can use a single DRA but with a larger size as shown in Fig. 1 (b) to simultaneously improve the antenna gain of each element of an antenna array, the aforementioned issues can be minimized. To reach this goal, the theoretical analysis and characterization of this large-sized DRA working at THz frequencies must be done first.

In this work, a single but large-sized DRA made of high-resistivity (high-Z) silicon (Si) material is proposed to enhance the antenna gain of each element a 2×2 THz antenna array realized in a 0.18-μm CMOS technology. The theoretical analysis shows that the proposed DRA works at a higher-order mode of $TE_{3,\delta,9}$. This higher-order mode operation not only boosts the antenna gain of an on-chip patch antenna from 0.1 to 8.6 dBi at 339 GHz, but it also allows to use a single DRA instead of 4 DRAs to simultaneously achieve the gain enhancement of each element of the antenna array, resulting in simpler assembly process and lower assembly cost. To characterize its performance, four identical power detectors (PDs) are designed and integrated with each element of the 2×2 CMOS THz antenna array. A flip-chip bonding technique is used to complete the assembly of the DRA and the CMOS chip, mitigating the issue of the assembly misalignment. By measuring the voltage responsivities of each PD output independently, the radiation pattern and the gain enhancement level of the proposed DRA can be acquired. The measurement results follow well with the simulated ones, verifying the operation principle of the proposed DRA. Subsequently this 2×2 CMOS THz PD array with the proposed DRA is successfully utilized to demonstrate a THz transmissive imaging system at 340 GHz. To the best of the authors' knowledge, the proposed DRA has the highest-order operation mode at THz frequencies reported thus far. Moreover, this paper is also the first work which uses the DRA to improve the antenna gain of each element of an antenna array at THz frequencies. This paper is organized as follows. Section II explains the design and theoretical analysis of the large-sized DRA. The characterization method for the proposed DRA is presented in Section III. Section IV illustrates the experimental results and the THz imaging system. Finally, Section V concludes this work.

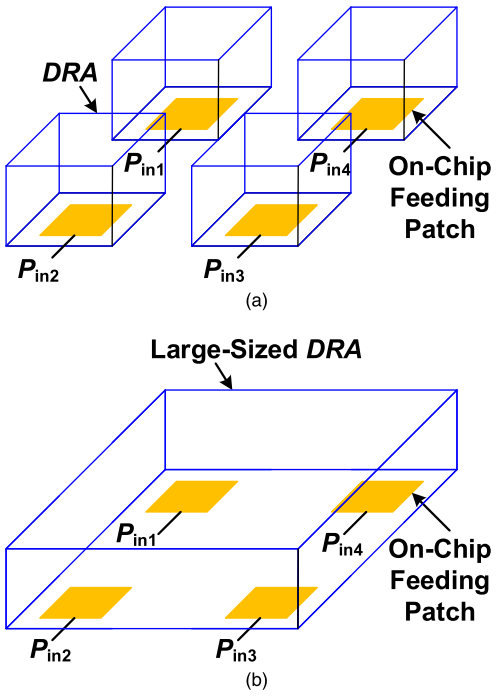


FIGURE 1. (a) Four DRAs required for 2 × 2 antenna array gain enhancement. (b) Single DRA for 2 × 2 antenna array gain enhancement.

II. LARGED-SIZED DRA DESIGN

Fig. 2(a) shows the proposed large-sized DRA used to enhance the antenna gain of each element Ant_{1-4} of a 2×2 THz antenna array realized in a 0.18-μm CMOS technology. In this scenario, the true radiating element is the DRA while the on-chip patch antennas work as feeding structures. The DRA is realized in an integrated-passive device (IPD) process with the cross-sectional view illustrated in Fig. 2(b). Note that the DRA height H_{DRA} is fixed at 625 μm due to the selected IPD technology. The remaining variables for the DRA design are the DRA width W_{DRA} and length L_{DRA}. The dielectric constant and resistivity of the Si material are 11.9 and higher than 3000 Ω-cm, respectively. Such a low-loss silicon material is very suitable to be utilized to improve the antenna gain of on-chip antennas. The top $M_{3,IPD}$ metal layer with the deposited Ni/Au thin films are used to implement the gold bumps which can be employed to thermo-compressively bond the DRA onto the CMOS chip by a flip-chip bonding machine under the conditions of 300 °C and 25 N applied bonding force for 3 minutes. Employing flip-chip packaging can provide a more reliable assembly as compared to the traditional method of using epoxy glue layers.

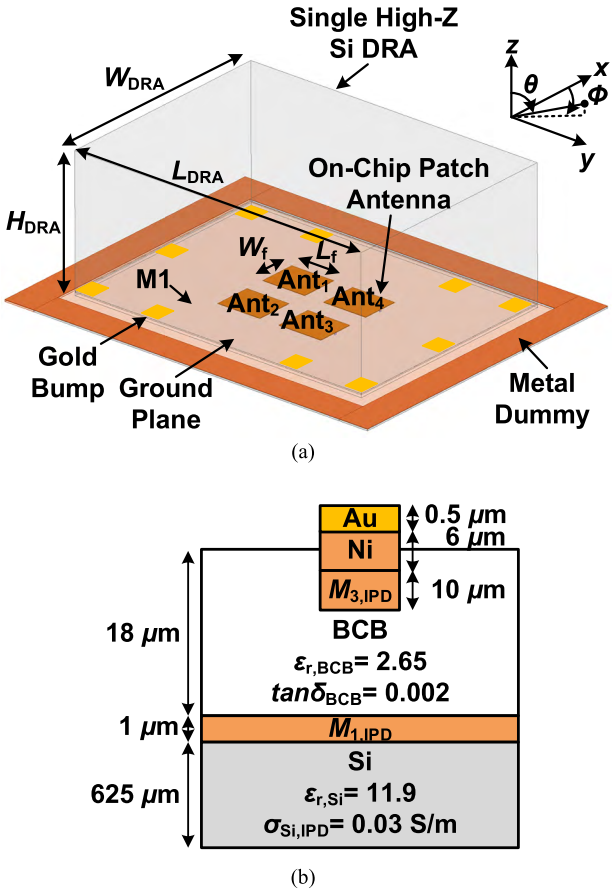


FIGURE 2. Proposed single DRA for 2 × 2 antenna array gain enhancement. (b) Cross-sectional view of the IPD technology for implementing the DRA.

For the proposed DRA mounted on a ground plane as shown in Fig. 2(a), its resonance frequency f_{mn} of $TE_{m,\delta,n}$ operation modes can be found by solving the following transcendental equation [21]:

$$k_y \tan(\frac{k_y W_{DRA}}{2}) = \sqrt{(\varepsilon_{r,Si} - 1)k_{mn}^2 - k_y^2} \quad (1)$$

where

$$k_{mn} = \frac{2\pi f_{mn}}{c}, \quad k_x = m\frac{\pi}{L_{DRA}},$$
$$k_z = n\frac{\pi}{2H_{DRA}}, \quad k_x^2 + k_y^2 + k_z^2 = \varepsilon_{r,Si}k_{mn}^2,$$

and c is the speed of the light. Traditionally, a single DRA is employed to enhance the antenna gain of a single on-chip antenna. In this case, m and n indexes are selected to be unity in order to have a compact DRA. To operate at a higher-order mode, the DRA can be designed to have index n higher than unity. By doing this, the DRA can be modeled as several magnetic dipoles separated by a distance s along the z-direction. By properly designing the aspect ratio of L_{DRA} and W_{DRA}, these magnetic dipoles can greatly enhance the antenna directivity, which implies higher antenna gain can be achieved. However, if a single DRA operating at a higher-order mode is intended to enhance the antenna gain of each element of an antenna array, not only n but also m must be designed to be higher than unity. The DRA operating at a mode $TE_{m,\delta,n}$ with m and n larger than unity simultaneously has not been investigated at THz frequencies reported thus far. To characterize its performance, we use ANSYS HFSS 3D electromagnetic (EM) simulation tool to design and simulate its radiation pattern and antenna gain.

TABLE 1. Calculated resonance frequencies of different operation modes.

Resonant Mode	$TE_{5,\delta,7}$	$TE_{1,\delta,9}$	$TE_{2,\delta,9}$	$TE_{3,\delta,9}$	$TE_{4,\delta,9}$	$TE_{5,\delta,9}$	$TE_{1,\delta,11}$	$TE_{2,\delta,11}$
f_{mn} (GHz)	314.8	316.8	324.1	335.9	351.8	371.3	393.5	399.4

The proposed DRA can be designed by noting that the on-chip feeding patch only affects the input impedance of the DRA but not the achievable antenna gain level. The initial size of the on-chip feeding patch can be selected to be equal to that of an on-chip patch antenna without the DRA. After the DRA size is designed, the on-chip feeding patch can then be adjusted to match the DRA input impedance to 50 Ω at 340 GHz. Fig. 3(a) shows the simulated peak antenna gain of the antenna Ant_1 at 340 GHz versus the DRA width as the length is fixed at 1.5 mm. Other antennas Ant_{2-4} show similar responses. Hence only simulation results of Ant_1 are shown here. Several gain peaks can be found for different width. It can be observed that the gain peak occurs at roughly the multiple of the wavelength λ, where λ is around 255 μm in the Si material at 340 GHz. The width of 1.1 mm, around 4λ wide, is designed due to its less sensitivity to the width variation while still providing high gain of 8.1 dBi and requiring small DRA size simultaneously. Note that the simulated antenna gain of an on-chip patch antenna realized in a 0.18-μm CMOS technology without the DRA integrated is only 0.1 dBi with the radiation efficiency of 20% at 340 GHz. Obviously, adding the DRA provides great antenna gain improvement. Fig. 3(b) illustrates the simulated peak antenna gain versus the DRA length as the width is fixed at 1.1 mm. The DRA length is designed as 1.5 mm to provide high gain. Though the antenna gain can be higher as L_S is 1.85 mm, it is not selected since its IPD fabrication cost is higher. In this first try of using the DRA for antenna gain enhancement, we need to make sure it works first. In a future design, if the budget is allowed, it is recommended to select L_S of 1.85 mm to have higher antenna gain.

With W_S and L_S designed as 1.1 and 1.5 mm, respectively, the resonance frequencies f_{mn} of the operation modes near the interested frequency range from 300 to 400 GHz can be found by solving (1). Note that only $TE_{m,\delta,n}$ mode with odd n index can be excited because of the boundary condition set by the ground plane. Moreover, the operation modes with even m index can be excited since the proposed antenna is not centrally fed, different from the centrally-fed case reported in [20]. Table 1 shows the calculated resonance frequencies

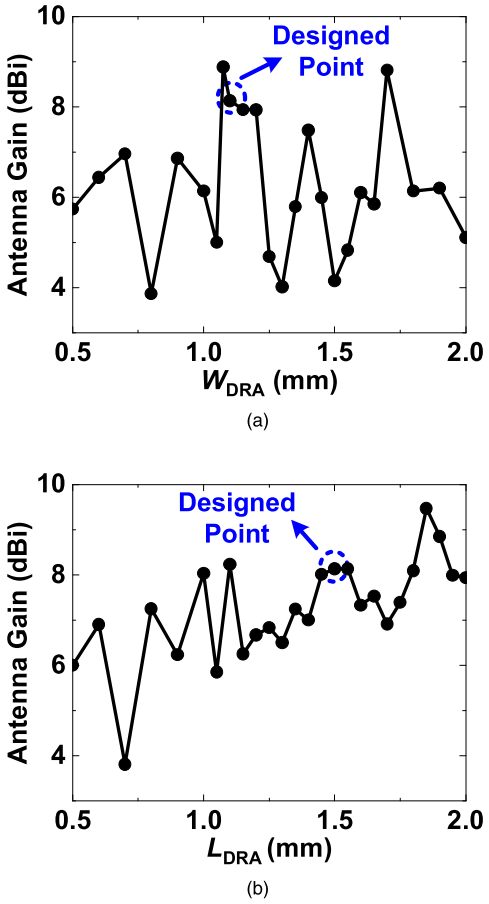


FIGURE 3. (a) Simulated antenna gain versus the width of the DRA. (b) Simulated antenna gain versus the length of the DRA.

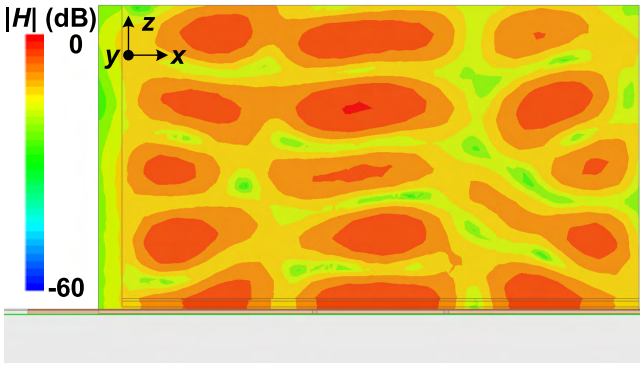


FIGURE 4. Simulated $|H_y|$ field distribution of the proposed DRA at 339 GHz.

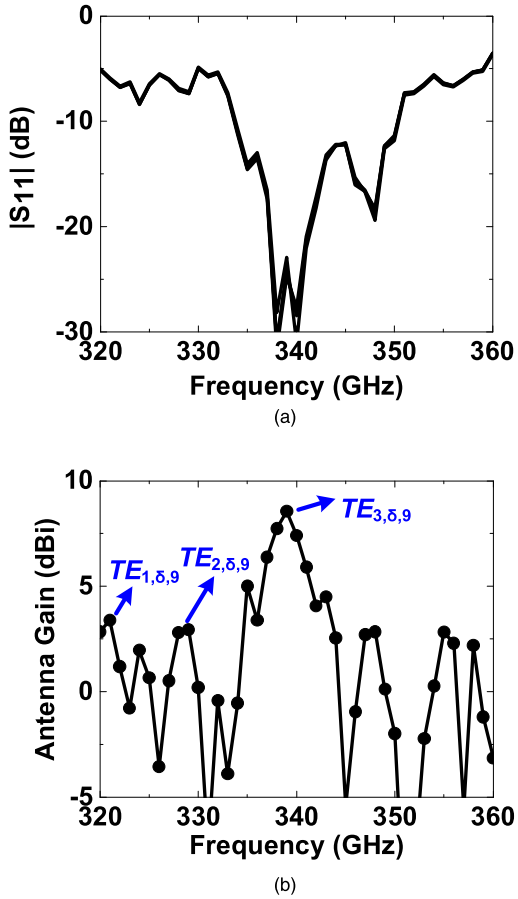


FIGURE 5. (a) Simulated input return loss of the proposed DRA. (b) Simulated antenna gain of the proposed DRA.

of different operation modes. The resonance frequency of the desired mode of $TE_{3,\delta,9}$ is 335.9 GHz, very close to the simulated one of 339 GHz. Moreover, single-mode operation can be achieved from 324.1 to 351.8, around 27.7-GHz bandwidth. Fig. 4 shows the simulated magnetic field along the y direction, i.e., $|H_y|$ of the proposed DRA at 339 GHz. Five and three extrema can be observed along the z and x directions, respectively, verifying that the proposed DRA is operated at the mode of $TE_{3,\delta,9}$. Similar magnetic field distribution can also be observed as one of other antennas Ant_{2-4} is excited. In other words, the proposed large-sized DRA operating at such a higher-order mode is able to simultaneously enhance the antenna gain of each element of the 2×2 THz antenna array instead of needing four separate DRAs using a conventional approach.

The proposed DRA can provide high antenna gain since it operates at the higher-order mode of $TE_{3,\delta,9}$ which can be modeled as several short magnetic dipoles arranged as an antenna array. Fig. 5(a) illustrates the simulated input return loss $|S_{11}|$ of the proposed DRA as Ant_1 is excited. $|S_{11}|$ can be kept below -10 dB from 334 to 350 GHz, roughly 16 GHz bandwidth. Fig. 5(b) shows the simulated realized antenna gain as θ and Φ are 20° and 210°, respectively, corresponding to the maximum gain direction. The maximum antenna gain of 8.6 dBi and the radiation efficiency of 54% can be obtained at 339 GHz. The antenna gain improvement of the proposed DRA over a traditional on-chip patch antenna can reach a value of 8.5 dB. There are other gain peaks occurred at 321, 329, and 375 GHz which are very close to the calculated resonance frequencies of the $TE_{1,\delta,9}$, $TE_{2,\delta,9}$, and $TE_{5,\delta,9}$ operation modes, respectively, as indicated in Table 1.

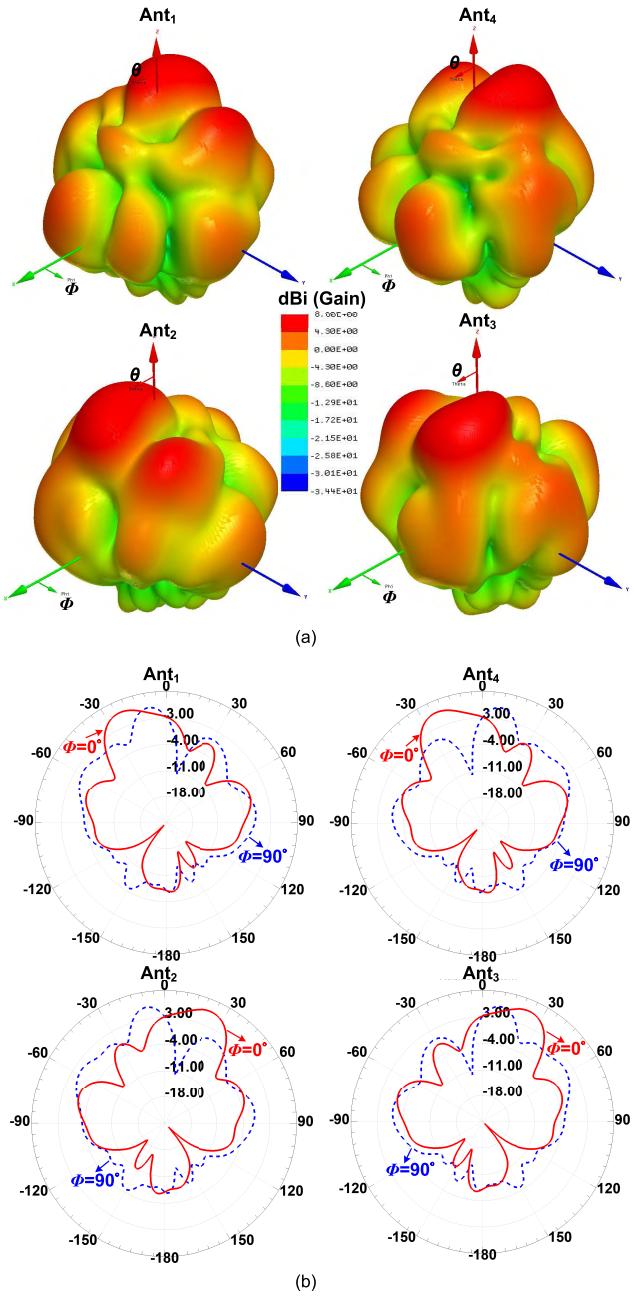
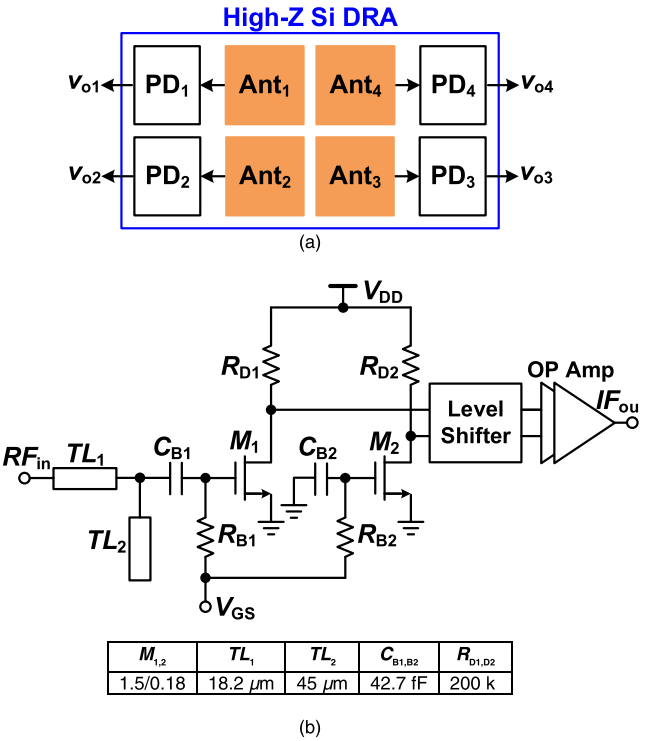


FIGURE 6. (a) Simulated 3D radiation patterns of the proposed DRA. (b) Simulated radiation patterns as Φ is 0° and 90°, respectively.

Fig. 6(a) shows the simulated three-dimensional (3-D) radiation pattern of each antenna of the 2×2 antenna array with the proposed DRA integrated. The radiation patterns as Φ is 0° and 90°, respectively, are illustrated in Fig. 6(b). Ant_1, Ant_2, Ant_3, and Ant_4 show peak gain at θ and Φ of 20° and 210°, 20° and 330°, 20° and 30°, and 20° and 150°, respectively, implying that the peak gain directions of the four antennas are all symmetric with respect to the broadside direction. Though the antenna gain does not have a peak at the broadside direction, i.e., $\theta = \Phi = 0°$, this will not be an issue. As mentioned before, four transceivers with



$M_{1,2}$	TL_1	TL_2	$C_{B1,B2}$	$R_{D1,D2}$
1.5/0.18	18.2 μm	45 μm	42.7 fF	200 k

(b)

FIGURE 7. (a) 2× 2 CMOS antenna array with four identical PDs integrated. (b) PD circuit schematic.

independent phase and amplitude tuning capabilities will be connected to these four antennas to form a 2×2 THz phased array transceiver. By controlling the phase shift and amplitude of each element, the phased array can steer the output beam in the desired direction. Therefore, the proposed DRA is able to simultaneously enhance the antenna gain of each element of a THz antenna array using a single DRA instead of needing multiple DRAs, reducing the assembly complexity and lower down the assembly cost. Moreover, such a large antenna gain improvement over traditional on-chip antennas can greatly enhance the THz system performance.

III. CHRACTERIZATION METHOD

Since on-wafer measurement instrument is not available, the characteristics of the proposed DRA cannot be measured directly. On the contrary, as illustrated in Fig. 7(a), the antenna performance is measured by an indirect method. Four identical power detectors are designed and integrated to Ant_{1-4}, respectively. By measuring the voltage responsivity of the four PDs in different receiving direction individually, the radiation pattern of each Ant_{1-4} with the proposed DRA can be acquired, respectively. The circuit architecture of the PD is shown in Fig. 7(b). Device parameters are also given. Transmission lines TL_1 and TL_2 are used to match the input impedance of the PD to 50 Ω for the maximum power transfer. By using the even-order nonlinearity property of the transistors, the transistor M_1 and M_2 can work as power detection devices to convert the incoming THz signal to a dc

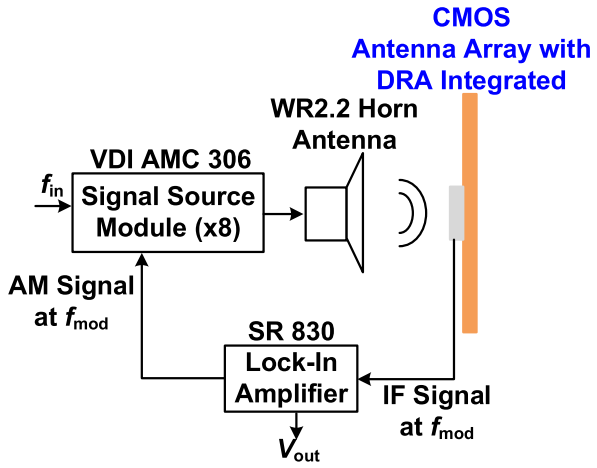


FIGURE 8. Experimental setup for characterizing each element of the 2 × 2 CMOS THz antenna array.

output current and then generates the output voltage by the load resistors R_{D1} and R_{D2}, respectively. The gate bias V_{GS} of the transistors is designed as 0.48 V to have the highest voltage responsivity. The output voltage magnitude is further enlarged by a baseband operational amplifier (OP Amp) with phase margin of 88°, voltage gain of 24.4 dB, and input referred noise of 7.7 μVHz$^{-0.5}$ at 1 kHz. Simulation results show that R_V of the PD can be 190.2 kV/W at 340 GHz while having the noise equivalent power (NEP) of 1.9 nWHz$^{-0.5}$ as the chopping frequency f_{mod} is 1 kHz. Note that the highest frequency of f_{mod} is only available up to 1 kHz due to the limitation of the used lock-in amplifier in the measurement. If a lock-in amplifier with a higher chopping frequency, for instance, 1-MHz f_{mod}, can be acquired, the NEP can be dramatically reduced from 1.9 nWHz$^{-0.5}$ to 24 pWHz$^{-0.5}$.

Fig. 8 shows the experimental setup for characterizing the proposed DRA with the four PDs integrated. A commercial signal source module from the Virginia Diode, Inc. (VDI) with the model number of AMC 306, is employed to generate the required THz signal. The output power of the THz signal source is calibrated by the Erickson power meter with the model number of PM4 from VDI. The AMC 306 module has a Transistor-Transistor-Logic (TTL) port which can be employed to conduct the required amplitude modulation to the THz signal for the lock-in amplifier operation. The THz signal generated by the AMC 306 module is radiated out by a WR2.2 horn antenna, propagates through the air, and is then received by the PDs with the proposed DRA. To detect a small output voltage from the PD output, a locking amplifier with the model number of SR830 from the Stanford Research Systems is utilized to filter out unwanted noise. A TTL signal provided by the lock-in amplifier is used to amplitude modulate the THz signal source. The output signal from the PD is hence located at the frequency of f_{mod} and then demodulated by the lock-in amplifier. The CMOS antenna array with the proposed DRA is attached on a step motor to control its position. The alignment between the THz

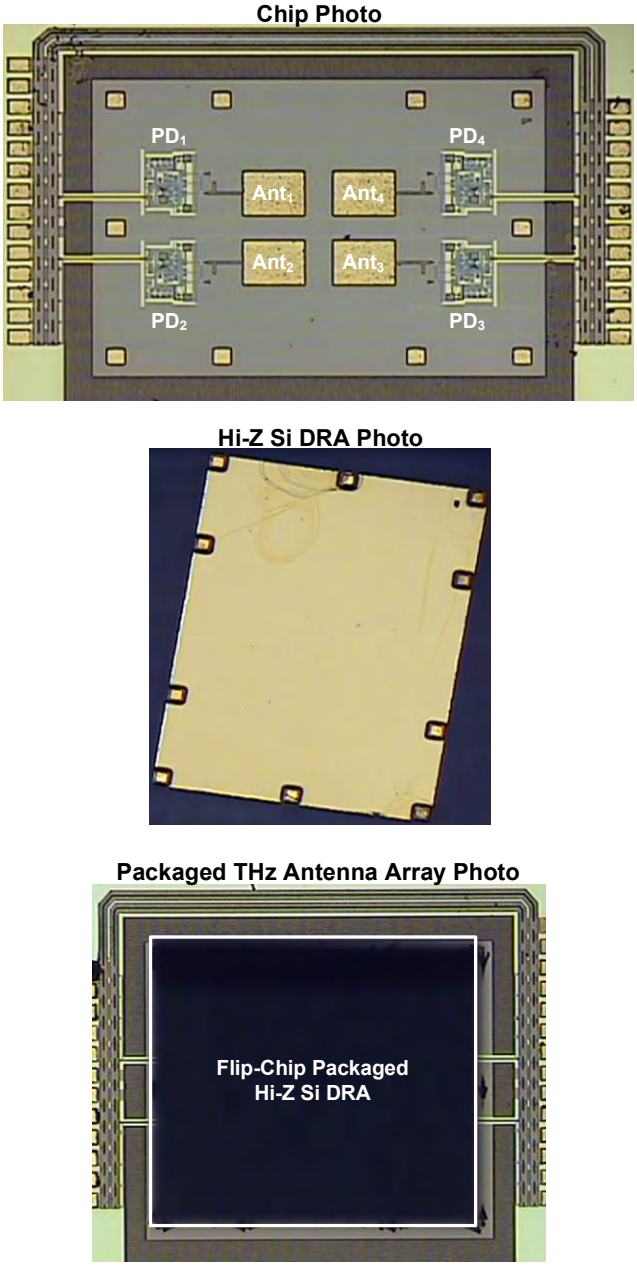


FIGURE 9. Chip photos of a CMOS chip, a high-Z Si DRA, and a 2 × 2 CMOS THz antenna array with the proposed flip-chip packaged high-Z Si DRA, respectively.

signal source and the antenna array is achieved by moving the antenna array to the position where the measured output voltage of the PD is maximal as it is scanned along a x-y plane. The received power can be calculated by using the Friis transmission equation, $P_R = G_T \times G_R \times (\lambda/4\pi R)^2 \times P_T$ where P_R, G_T, G_R, λ, R, and P_T are the received power, transmitter antenna gain, receiver antenna gain, wavelength, the distance between the transmitter and the CMOS antenna array chip, and the output power of the THz signal source, respectively. The output voltage of each PD can be written as $V_{out} = R_V \times P_R = R_V \times G_T \times G_R \times (\lambda/4\pi R)^2 \times P_T$, where R_V

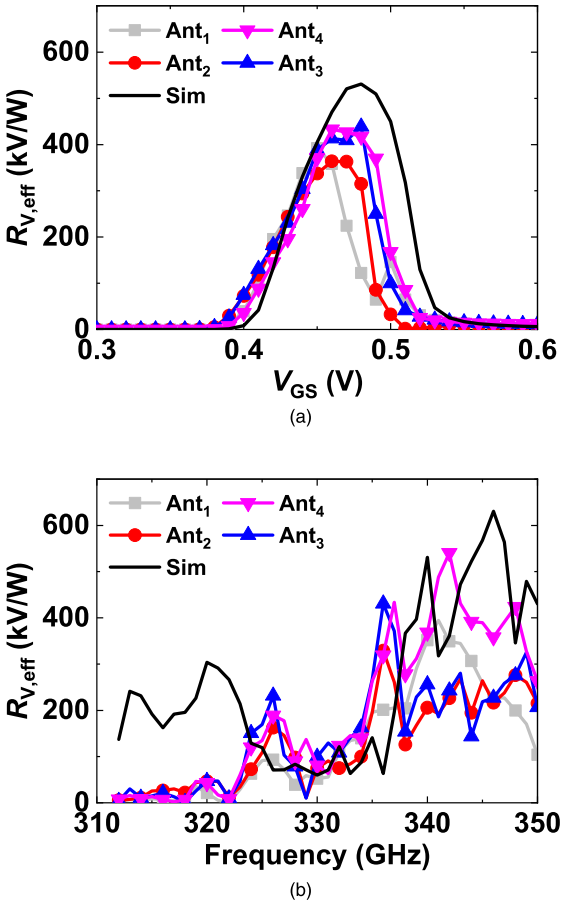


FIGURE 10. (a) Measured $R_{V,eff}$ versus V_{GS} and (b) measured $R_{V,eff}$ versus the input frequency of each PD of the 2 × 2 CMOS THz antenna array.

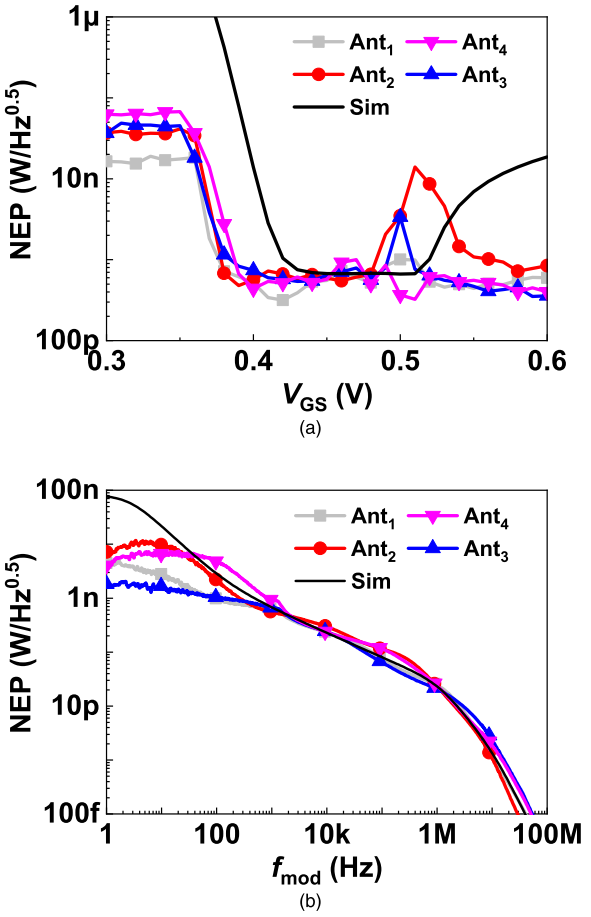


FIGURE 11. (a) Measured NEP versus V_{GS} and (b) measured NEP versus the chopping frequency f_{mod} of each PD of the 2 × 2 CMOS THz antenna array.

is the voltage responsivity of the PD. Since the antenna gain of Ant_{1-4} cannot be measured alone as mentioned before, we use the effective voltage responsivity $R_{V,eff}$ defined as the R_V of the PD times the antenna gain G_R of Ant_{1-4}, that is, $R_{V,eff} = R_V \times G_R$, to take the antenna gain into consideration. Now $R_{V,eff}$ can be accurately measured because G_T, λ, R, and P_T are known. Since R_V is the same for the four identical PDs, the antenna characteristics of Ant_{1-4} with the proposed DRA can be independently acquired by measuring $R_{V,eff}$. Moreover, we also design a PD with a conventional on-chip patch antenna without applying any gain enhancement technique. By doing this, with the aforementioned characterization method, the gain enhancement of the proposed DRA over the conventional on-chip patch antenna can also be measured. The effective voltage responsivities of the PD with the on-chip patch antenna and the PD with the proposed DRA can be written as $R_{V,eff,Patch} = R_V \times G_{R,Patch}$ and $R_{V,eff,DRA} = R_V \times G_{R,DRA}$, respectively. Obviously, the ratio between the measured effective voltage responsivities is equal to the ratio between the antenna gains, that is, $R_{V,eff,DRA}/R_{V,eff,Patch} = G_{R,DRA}/G_{R,Patch}$. Hence the antenna gain enhancement can be acquired by measuring $R_{V,eff}$.

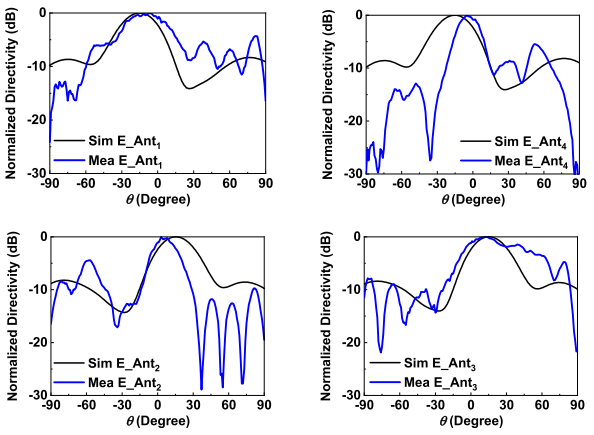


FIGURE 12. Measured radiation patterns of the four antennas as Φ is 0°.

IV. EXPERIMENTAL RESULTS

Fig. 9 shows the chip photos of a CMOS chip realized in a 0.18-μm CMOS technology, a high-Z Si DRA implemented in an IPD technology, and the CMOS antenna array with the flip-chip-packaged DRA, respectively. The chip size is 2.2 mm × 1.4 mm while the DRA size is 1.5 mm × 1.1 mm. The experimental setup and characterization method for charac-

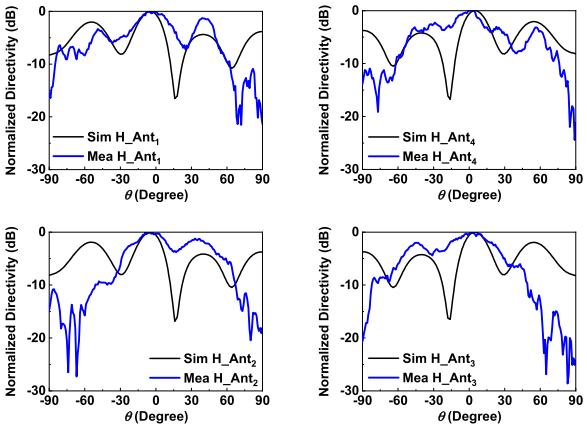


FIGURE 13. Measured radiation patterns of the four antennas as Φ is 90°.

terizing the performance of each element of the CMOS THz antenna array with the proposed DRA have been explained in the last Section. The CMOS antenna array is deployed 10 cm away from the THz signal source in order to ensure it is within the far-field region.

Fig. 10(a) shows the measured effective voltage responsivity of each PD versus the gate bias V_{GS} as the input frequency is 340 GHz. To ease the measurement, the PD is measured at $\theta = \Phi = 0°$. The simulation results also take the antenna gain at $\theta = \Phi = 0°$ to calculate $R_{V,eff}$. The optimal V_{GS} for the highest responsivity is around 0.45 V, close to the simulated value of 0.48 V. The measured $R_{V,eff}$ of the four PDs shows similar trends with the simulated ones. The highest $R_{V,eff}$ is 439 kV/W. The measured frequency response of $R_{V,eff}$ is illustrated in Fig. 10(b) as the transistors are biased at the optimal V_{GS}. Essentially, the measured result follows well with the simulated one. The antenna Ant_4 can obtain the maximum $R_{V,eff}$ of 540.6 kV/W at 342 GHz. However, the measured $R_{V,eff}$ of the four antennas Ant_{1-4} shows around 3-dB variation with respect to the operation frequency. The reason for this might be due to fact that the measurement setup is not easy to adjust each Ant_{1-4} to the specific direction of $\theta = \Phi = 0°$, especially as the operation frequency is high and the antennas Ant_{1-4} do not have the same radiation patterns, resulting in variations seen in the measured data. This can be observed in the measured radiation patterns shown in Fig. 12 and 13, respectively, which will be explained later.

The measured NEP versus the gate bias is depicted in Fig. 11(a). The minimum NEP occurs at the gate bias corresponding to the highest voltage responsivity. The NEP versus the chopping frequency is also measured as shown in Fig. 11(b), assuming that $R_{V,eff}$ is constant with f_{mod}.

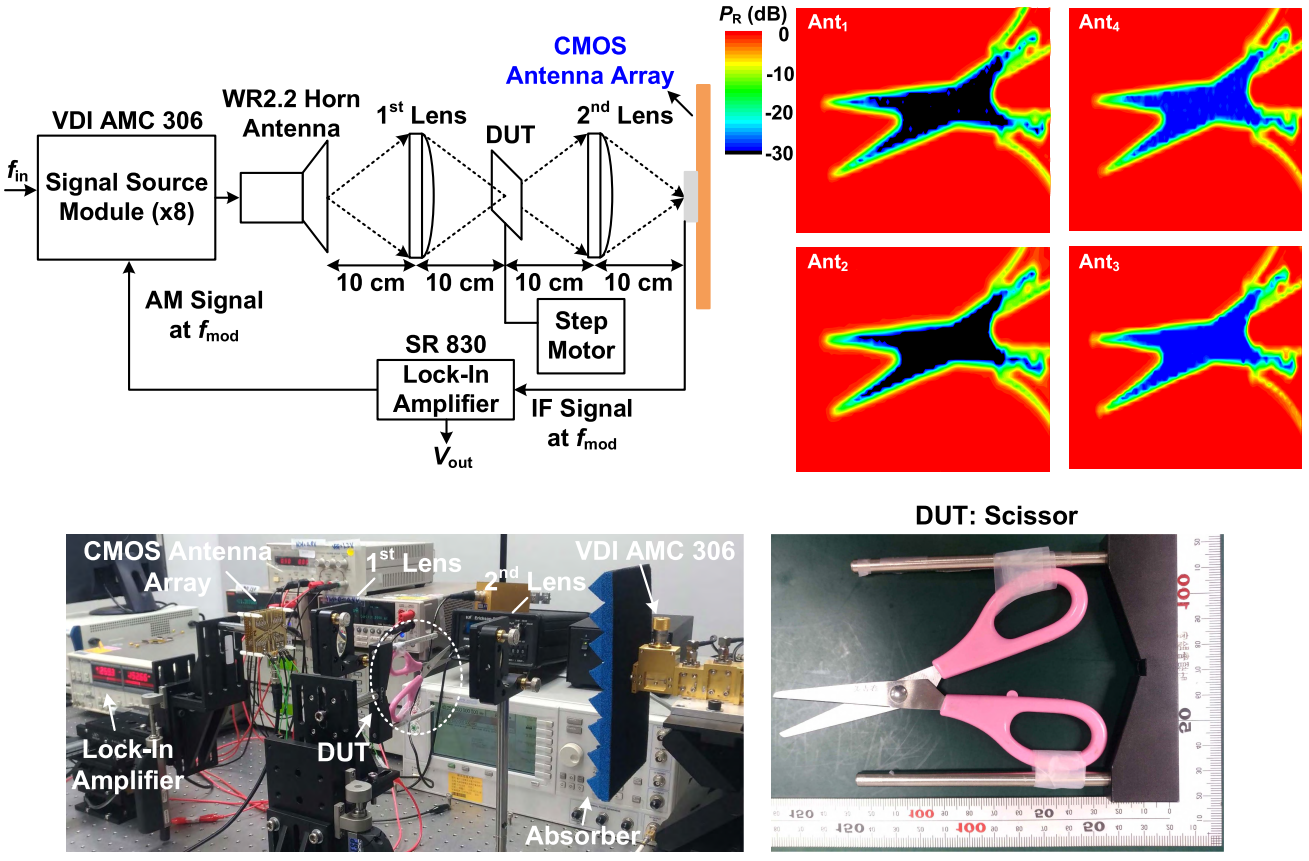


FIGURE 14. Experimental setup of the THz transmissive imaging system using the PD with the proposed DRA.

Due to the used lock-in amplifier, the highest available f_{mod} frequency is only limited to 1 kHz. The minimum NEP of the four PDs can be 0.55 nWHz$^{-0.5}$ at f_{mod} of 1 kHz. If f_{mod} can be increased to, for instance, 100 MHz, the NEP actually can be smaller than 100 fWHz$^{-0.5}$.

The radiation patterns of the four antennas Ant_{1-4} at Φ of 0° and 90°, respectively, are measured by recording the output voltage as θ is varied from −90° to 90°. The recorded voltage at each angle is then normalized to the peak measured voltage to acquire the normalized directivity of the antenna. The radiation pattern at other Φ angle can be obtained by using the same approach. The measured radiation pattern as Φ is 0° is shown in Fig. 12. The measured results show similar trends with the simulated ones. For the case with Φ of 90°, the measured results also follow well with the simulated ones as illustrated in Fig. 13. As mentioned before, we also design a PD with a conventional on-chip patch antenna. The measured $R_{\mathrm{V,eff,Patch}}$ shows a peak value of 135 kV/W at 330 GHz. The antenna gain enhancement of the proposed DRA over the conventional on-chip patch antenna can be obtained by $R_{\mathrm{V,eff,DRA}}/R_{\mathrm{V,eff,Patch}} = G_{\mathrm{R,DRA}}/G_{\mathrm{R,Patch}}$. Take the antenna Ant_4 as an example. The antenna gain enhancement ratio can be calculated as 4, i.e., 6 dB. Moreover, according to the measured radiation patterns shown in Fig. 12 and 13, respectively, additional 1 dB gain improvement should be added since $R_{\mathrm{V,eff,DRA}}$ is measured in the direction at $\theta = \Phi = 0°$, not corresponding to the maximum gain direction. In a word, the total antenna gain enhancement can reach a value of 7 dB, very close to the simulated one of 8.5 dB. The consistency between the simulation and measurement results verifies the design and the performance of the higher-order mode DRA proposed in this work.

It is worth to see that the PD with the proposed DRA can be employed to realize a THz imaging function. A THz transmissive imaging system is hence established by using each PD with the proposed DRA as the THz receiver unit while the VDI signal source module working as the transmitter unit as illustrate in Fig. 14 on the next page. Two lenses (1st lens and 2nd lens) are used to focus the beam on the device under test (DUT) and the imaging array, respectively. A two-axis step motor with the moving resolution of 1 mm is employed to move the DUT along a x-y plane with an area of 5 cm × 10 cm. By recording the measured output voltage at each position, a THz image with size of 5 cm × 10 cm can be taken. The whole imaging process is automatically completed by using the LabVIEW program. The DUT is selected to be a scissor in this work. Fig. 14 shows the taken THz images of the scissor by the four PDs with Ant_{1-4}, respectively. The shape of the DUT can all be clearly seen.

V. CONCLUSION

A single large-sized DRA able to enhance the antenna gain of each element of a CMOS antenna array is proposed and successfully verified by experiment results. By designing the DRA to work at a higher-order mode of $\mathrm{TE}_{3,\delta,9}$, only single DRA implemented in an IPD process is required to simultaneously improve the antenna gain of each element of a 2×2 CMOS THz antenna array realized in a 0.18-μm CMOS technology. This not only reduces the assembly process but it can also lower down the assembly cost. Moreover, the proposed higher-order mode DRA can provide measured antenna gain enhancement of 7 dB over a traditional on-chip patch antenna. Such a large gain enhancement can be employed to greatly improve the THz system performance.

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CHUN-HSING LI (S'10–M'13) received the B.S. degree in electrophysics and the M.S. and Ph.D. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2005, 2007, and 2013, respectively.

In 2014, he joined MediaTek, Hsinchu, as a Senior Engineer, and the Department of Electrical Engineering, National Central University, Jhongli, Taiwan, as an Assistant Professor. Since 2018, he has been with the Department of Engineering and System Science, National Tsing Hua University, Hsinchu, where he is currently an Assistant Professor. His research interests include RF, millimeter-wave, and terahertz circuits and system design.

Dr. Li was a recipient of the FineTek Technology Gold Award, in 2013, and the Excellent Young Engineer Award from the Chinese Institute of Engineers, in 2013. He was a co-recipient of the Best Paper Award of the 13th IEEE International Conference on Electronics, Circuits, and Systems, Nice, France, in 2006.

TE-YEN CHIU received the B.S. degree in communication engineering from Chung Hua University, Hsinchu, Taiwan, in 2015, and the M.S. degree in electrical engineering from National Central University, Jhongli, Taiwan, in 2017. He is currently pursuing the Ph.D. degree with the Department of Engineering and System Science, National Tsing Hua University, Hsinchu.