IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received December 5, 2018, accepted December 17, 2018, date of publication December 24, 2018,
date of current version January 29, 2019.

Digital Object Identifier 10.1109/ACCESS.2018.2889154

Improved Performance of CMOS Terahertz Detectors by Reducing MOSFET Parasitic Capacitance

QIXUAN YANG[1], XIAOLI JI[1], YUE XU[2], (Member, IEEE), AND FENG YAN[1]
[1]School of Electronic Science and Engineering, Nanjing University, Nanjing 210023, China
[2]College of Electronic and Optical Engineering and College of Microelectronics, Nanjing University of Posts and Telecommunications, Nanjing 210023, China

Corresponding authors: Xiaoli Ji (xji@nju.edu.cn) and Feng Yan (fyan@nju.edu.cn)

This work was supported in part by the National Key Research and Development Program of China under Grant 2016YFA0202102 and Grant 2016YFB-0402403, in part by the China Academy of Space Technology Foundation under Grant CAST 08201601, and in part by the NSFC Project under Grant 61627804.

ABSTRACT The parasitic circuit elements significantly affect rectification performance of metal–oxide–semiconductor field-effect transistor devices. In this paper, we develop a gate–source parasitic capacitance reduction technique by shifting the source lightly doped drain region and analyze the effectiveness on the improved performance of complementary metal–oxide–semiconductor (CMOS) terahertz (THz) detectors. It is experimentally found that for a 0.65-THz integrated CMOS detector, the maximum improvement of voltage responsivity and noise-equivalent power can be 155% and 70%, respectively, by suppressing the gate–source parasitic capacitance. The device simulation further quantitatively evaluates the gate–source parasitic capacitance under different gate–source overlap areas in the novel fabricated transistor structure. It reveals that a smaller gate–source overlap area can result in a lower gate–source parasitic capacitance, which is more favorable for reducing input THz signal leakage and therefore for increasing the THz responsivity. The works open a wide range of possibilities for the ease of design and fabrication of the high-performance THz detectors in standard CMOS technology.

INDEX TERMS Terahertz (THz) detector, gate-source overlap capacitance, responsivity, noise-equivalent power.

I. INTRODUCTION

Complementary Metal Oxide Semiconductor (CMOS) Terahertz (THz) detectors have attracted great interest in room temperature THz imaging [1]–[3] due to their excellent advantages such as low cost, low power consumption and large-scale integration of circuits by using readout electronics and on-chip signal processors. To enhance the detectors' performance, several CMOS techniques with high-frequency capabilities have been applied. These techniques include fully-integrated SiGe-based BiCMOS technology [4], the thinned substrate technology with the reduction of the signal losses in the substrate [5] and the more advanced 65 nm Silicon-On-Insulator (SOI) technology [6] or by modified circuit concepts with a careful design of the gate length of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), a thinned substrate and a proper connection of the integrated antenna [7]. Although these detectors achieve high performance, the fabrication of THz detectors needs to change standard CMOS production process or require dedicated manufacturing facilities as well as much more advanced technologies, which inevitably imposes a burden on fabrication cost and makes the THz imaging more expensive for commercial applications. Compared with these advanced technologies, device structure engineering has been adopted to improve the performance of CMOS THz detectors. MOSFETs with asymmetric-structure have shown better THz performance. These asymmetries include the asymmetry by using an external capacitance [8], the asymmetry in the source and drain boundary conditions [9] and by applying an additional dc current between source and drain terminals [10]–[14]. Additionally, careful MOSFET structural parameters design can also enhance the detector performance well [15]. On the other hand, it is worth to stress that the parasitic elements introduced by the fabrication flow of MOSFETs often have a negative impact on the performance of CMOS THz detectors. However, little research has been

done to reduce the influence of parasitic capacitance in the asymmetric-structure. To reduce this parasitic effect, the relevant research works are very necessary.

In this paper, we demonstrate performance improvement of the MOSFET-based THz detector by reducing the device's gate-source parasitic capacitance based on a standard CMOS process. A novel method by implanting asymmetric lightly doped drain (LDD) regions at the source-drain terminals without modifying standard CMOS process flow is proposed and the integrated CMOS THz detectors working at 0.65THz with different gate-source overlap regions were constructed. The voltage responsivity R_V and NEP characteristics of the THz detectors were then experimentally analyzed in combination with device simulation.

II. EXPERIMENTS AND RESULTS

Fig. 1 illustrates the principle diagram of the THz detector. The self-mixing CMOS THz detector includes two parts: a Si-based MOSFET and an integrated metal patch antenna. Incident THz signal, received by the antenna structure, can be efficiently converted into the input signal of MOSFET at the source terminal. A DC bias V_{GS} is applied between the gate and source terminals. The MOSFET structure operating at a non-resonant mode can detect the THz wave power by measuring the dc voltage at the drain terminal. The parasitic capacitance at the source terminal may significantly affect the THz response. As shown in Fig.1, a part of THz signals will leak through the parasitic capacitance C_{GS}, which seriously attenuates the THz signal input to the channel. To study the influence of the gate-source capacitance on the characteristics of THz detectors, the novel MOSFET structures with the asymmetric source-drain LDD regions were fabricated in 0.18 μm standard CMOS technology. Fig. 2 (a) and (b) show the fabrication process flow and the cross-sectional view for MOSFET structure with asymmetric source-drain implantation, respectively. In the standard CMOS technology, after the formation of shallow trench isolation (STI), the implantation of P-well and N-well and thermal annealing are performed in turn. Then, the gate oxide is grown and the

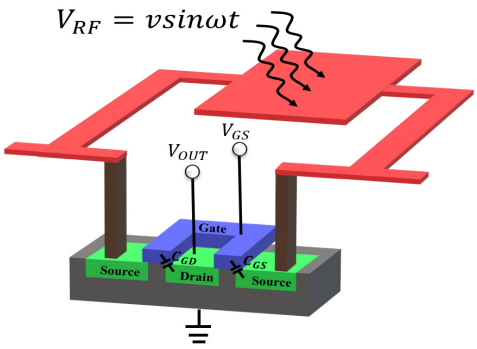


FIGURE 1. Principle diagram of THz detector circuit including a MOSFET detector.

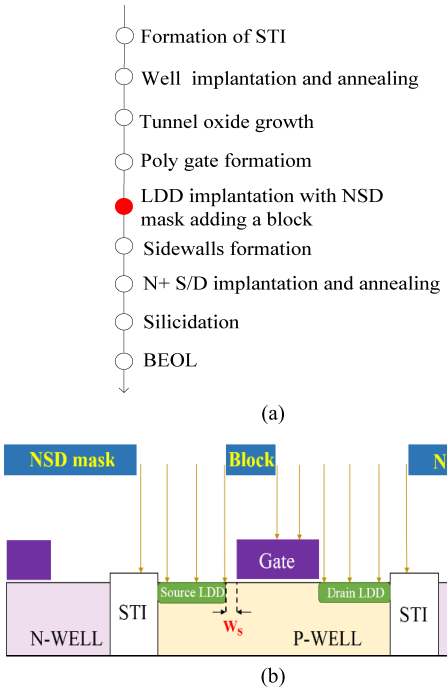


FIGURE 2. (a) Process flow and (b) Cross-sectional view of novel NMOS structure. A source block is added on NSD mask for constructing different gate-source overlap regions. The W_S presents the displacement of source LDD relative to standard structure.

poly-Si gate is deposited and etched. After that, the source and drain structures including LDD implantation are fabricated by gate-self-aligned technique, where the poly-Si gate together with N^+ Source/Drain (NSD) structure are used as the pattern mask. Although the self-alignment gate technique can reduce the gate-source/drain overlap, there still exists a relatively large overlap area between the gate and the LDD region after subsequent thermal treatment, which may lead to the degradation of THz detector performance. Different from the conventional one, in the novel fabrication method, a source block is added on NSD mask for reducing the gate-source overlap region. As shown in Fig.2 (b), by shifting the block left with a displacement of W_S relative to the standard structure, the source LDD implantation region can be forced to move away from the channel, resulting in the reduction of the overlap area between the source and gate terminals. After LDD implantation, gate sidewalls are grown. Finally, N^+ implantation with the sidewalls is performed to form source and drain of MOSFETs. Because the thickness of the sidewalls is much larger than the displacement of W_S, the shift of source LDD region normally does not affect the formation of the source and drain terminals. By the way, the MOSFET structures with various source-gate overlap regions surrounded by STI are fabricated without modifying the poly-Si standard process.

It is obvious that the larger W_S is, the smaller overlap area between gate and source terminals is. However, too large displacement easily results in excess gate parasitic

capacitance due to no channel connection with the source terminal. To avoid this case, four appropriate displacements with W_S = 10 nm, 20 nm, 30 nm, and 40 nm are selected for NMOSFETs. The channel length and width for all asymmetric devices are 0.5μm and 1μm, respectively. The thickness of the polysilicon gate and gate oxides are 200 nm and 3.9 nm, respectively.

These asymmetric MOSFETs are then integrated with on-chip metal patch antenna working at 0.65 THz, which can be implemented by using the top metal layer in standard CMOS process. In order to obtain high-performance, the patch antenna is carefully considered to match the input impedance of MOSFETs. The input impedances of the asymmetric MOSFETs with different displacements are calculated by Technology Computer Aided Design (TCAD) device simulation. Subsequently, the sizes of metal patch antennas matched with these input impedances are designed and optimized by High Frequency Structure Simulator (HFSS). In the HFSS simulation, the top metal layers in 0.18 μm CMOS technology are used for the patch antenna. The separation of the patch and the ground plane, as well as the thickness of the patch metallization and the dielectric condition, is determined by the given process conditions. The simulation results, including input impedance of NMOSFETs and the gain and S_{11} parameters (input reflection coefficient) of the patch antennas, are shown in Table 1. It is seen that the patch antennas with modified sizes are well matched with these impedances of each modified MOSFET with a different W_S. It can ensure that the improvements in detector performance in our work come from the reduction of C_{GS}, not from the changes of input matching.

TABLE 1. The calculated input impedance of asymmetric NMOSFETs and the gain and S_{11} parameters of the patch antennas.

MOSFETs			Antenna at 0.65 THz		
W_S (nm)	Input impedance Re (Ω)	Im(Ω)	Patch size ($m^{2)}$	S_{11} (dB)	Gain (dB)
0	182	-592	90× 80	-19	3.0
10	257	-644	80×120	-34	3.0
20	265	-752	80 × 90	-21	2.9
30	364	-914	80×135	-20	3.3
40	314	-1022	77×100	-18	2.9

The THz detectors were manufactured using SMIC 0.18 μm standard CMOS technology. Fig. 3(a) displays the micrograph of a 0.65 THz detector die with a patch antenna taken by laser microscope, occupying 80 × 80 μm^2 area. The MOSFET transistor is placed in the center of the patch antenna. The R_V and *NEP* characteristics of the novel fabricated detectors were then experimentally characterized. Fig. 3(b) shows the schematic of the experimental set-up of R_v and NEP measurements. The test 0.65 THz light source is generated by VDITx187 signal generator and chopped by a 3 KHz square-wave. By means of two parabolic mirrors, the modulated THz light source is converged into a spot and

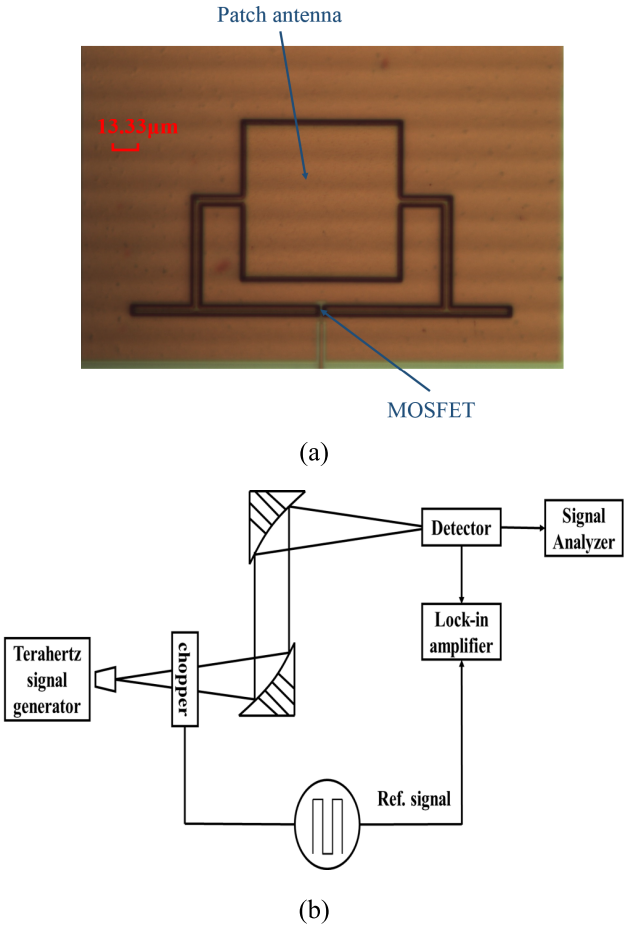


FIGURE 3. (a) Micrograph of a 0.65 THz detector die with 80 × 80 μm^2 area, showing a metal patch antenna taken by laser microscope. (b) Schematic of the experimental set-up of R_V and *NEP* measurements.

projected onto the detector. The radiation is received by the integrated patch antenna and the detected THz signal is then imported to the source terminal of MOSFET. Due to the rectifying effect of the MOSFET transistor, the induced voltage response of the detector at the drain terminal is measured by using a lock-in amplifier SR830. Besides, the noise voltage fluctuation spectral density was measured by Agilent 35670A signal analyzer. Note that additional components such as integrated amplifiers are not included in the measurement to avoid excess noise.

Firstly, we tested the basic transfer characteristics of the MOSFET detectors with different displacements. Fig. 4 shows the measured I_D–V_{GS} transfer characteristics as well as simulation results at V_{DS} = 0.1 V. The derivatives of the transfer characteristics for both experimental and simulation results are also illustrated in the inset of Fig. 4. The consistent I_D–V_{GS} transfer characteristics between test data and device simulation indicate almost the same sub-threshold swing (*SS*) and threshold voltage (V_{TH} = 0.53 V) for these structures, informing that the device process with the additional source block does not degrade the basic switch properties of standard MOSFETs.

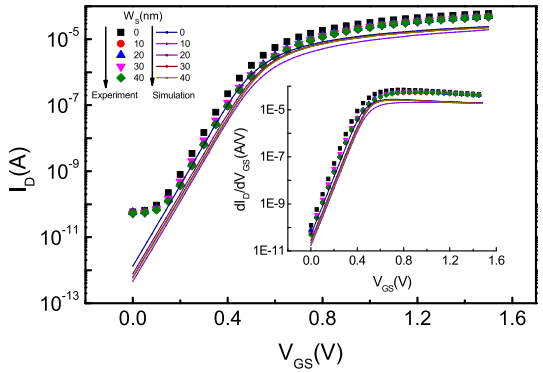


FIGURE 4. The measured and simulated I_D-V_{GS} transfer characteristics at V_{DS} = 0.1 V for the fabricated devices with different displacements W_S. The inset picture shows the gate bias dependence of the derivatives dI_D/dV_{GS}.

Then, the voltage responsivity R_V was measured and calculated by the following formula [16]:

$$R_V = \frac{\Delta u \times S_t}{P_{total} \times S_{antenna}} \tag{1}$$

where Δu is the response voltage amplitude, P_{total} is the total power of the source, S_t is the radiation beam spot area and $S_{antenna}$ is the area of the antenna.

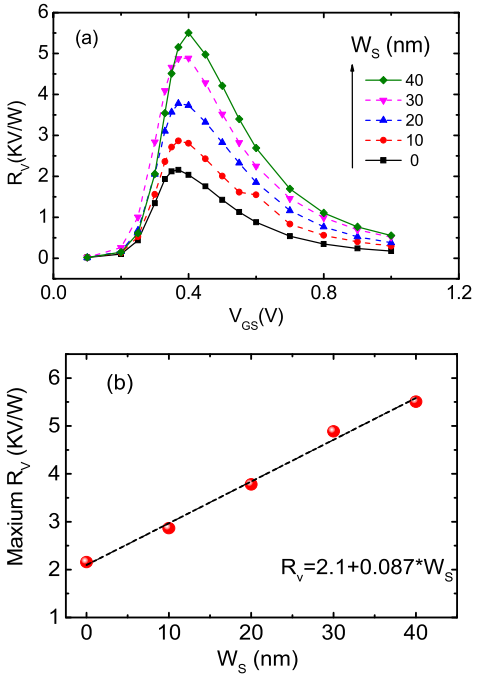


FIGURE 5. (a) Measured R_V under different gate voltages V_{GS} at 0.65THz and (b) Extracted maximum R_V as a function of displacement W_S. The black dashed line represents the linear fitting result. All data appears to fall on the fitting curve.

Fig. 5(a) illustrates voltage responsivity R_V at 0.65THz for asymmetric detectors under various gate voltage V_{GS}. It is seen that when V_{GS} is changed from 0.1 V to 1 V, the R_V increases first and then decreases, showing a maximum value below the threshold voltage. This characteristic is in good agreement with the plasma wave detection theory for FETs THz detectors [17], [18]. We also found that the larger displacement is, the higher THz responsivity R_V of the devices is. Fig. 5(b) further demonstrates the extracted maximum R_V as a function of displacement for asymmetric detectors. The black dashed line represents the linear fitting result as follows:

$$R_V = 2.1(KV/W) + 0.087(KV/(W * \text{nm})) \times W_S(nm) \tag{2}$$

It is obviously observed that all experimental data appears to fall on one fitting curve, informing the maximum R_V linearly increases with W_S ranging from 0 to 40 nm. Comparing to standard one with $W_S = 0$, the asymmetric detector with $W_S = 40$ nm achieves 155% improvement on responsivity.

Further, the *NEP* is evaluated from the experimental data of R_V and the noise spectral density S_V [17], which is given by

$$NEP = \frac{\sqrt{S_V}}{R_V} \tag{3}$$

where S_V is the measured noise spectral density by using an Agilent 35670a signal analyzer. In order to avoid the low frequency 1 / f noise, the noise spectral density was measured at the modulating frequency of 3 KHz.

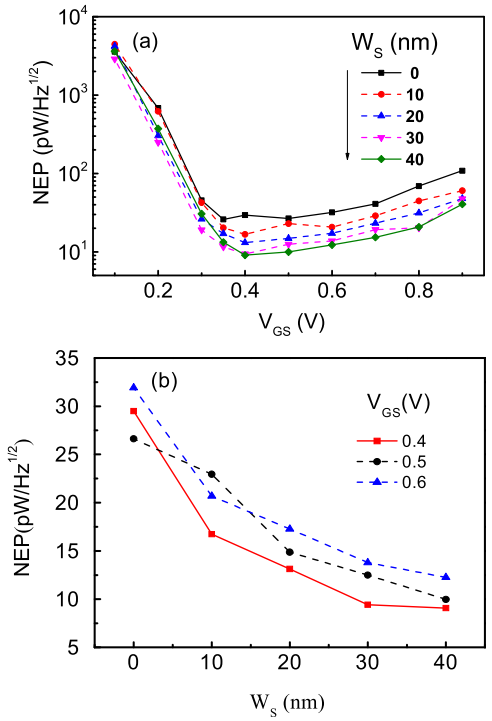


FIGURE 6. Evaluated *NEP* value under various gate bias (V_{GS}) at 0.65THz for asymmetric MOSFET detectors and (b) Extracted *NEP* as a function displacement (W_S) at different gate voltages.

Fig. 6(a) shows the gate bias voltage dependence of the *NEP*. It is seen that the magnitude of *NEP* is dramatically reduced when the gate bias increases from the sub-threshold

to the inversion region. The lowest *NEP* value is achieved at the gate bias near the threshold voltage. Fig. 6(b) illustrates the extracted *NEP* value as a function of W_S at three different gate biases. It is distinctly found that the *NEP* decreases rapidly with the increase of W_S, while the noise of the transistors under the condition is usually attributed to the thermal noise from the channel resistance. For the standard detector with $W_S = 0$, the *NEP* is about 30pW/$\sqrt{}$Hz at $V_{GS} = 0.4$V, which is comparable to those in reported CMOS detectors operating at room temperature [19], while for the detector with $W_S = 40$ nm, the *NEP* value is reduced to 9 pW/$\sqrt{}$Hz, that is a 70% reduction on *NEP* comparing to the standard MOSFET structure. These experimental results indicate that the reduction of gate-source overlap area is effective in reducing noise-related characteristic of the detectors.

III. DEVICE SIMULATION AND DISCUSSION

To better understand the experimental results, TCAD simulation was performed to study the parasitic capacitance effect on the performance of the novel detectors by use of Cogenda VisualTCAD software. The Drift-Diffusion, Shockley-Read-Hall recombination, Fermi-Dirac, Low-Field mobility, Incomplete Ionization, and Doping Dependent mobility models are used in this simulation. The simulation structure of MOSFET is exactly the same as that of fabricated one. The channel length/width is 0.5μm/1μm and the gate oxide thickness is 3.9 nm. Fig. 7(a) shows the sub-circuit model structure of MOSFETs, which includes the main input parasitic capacitances in CMOS THz detector. When the THz signal is connected to the source terminal, the input equivalent capacitance C_{TS} mainly consists of three components:

$$C_{TS} = C_{GS} + C_{BS} + C_{DS} \tag{4}$$

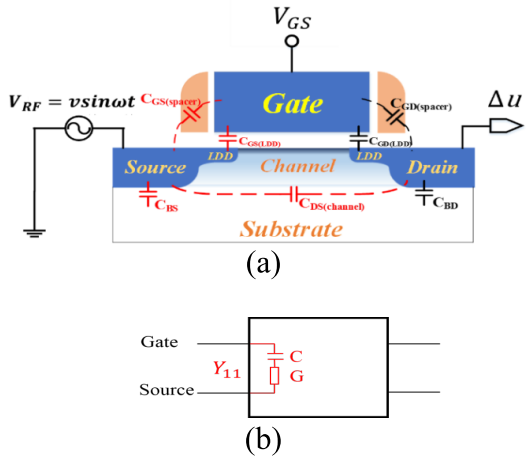


FIGURE 7. (a) Sub-circuit model structure of CMOS THz detector and (b) Schematic of Y_{11}-parameter extracted from AC small-signal simulation result, here C and G present the capacitance and conductance, respectively.

Here, C_{GS}, C_{BS} and C_{DS} are the gate-to-source, source-to-bulk, drain-to-source capacitance respectively. C_{GS} is mainly constituted by the parallel connection of spacer capacitor ($C_{GS(spacer)}$) and LDD capacitor ($C_{GS(LDD)}$). The AC small-signal simulation was carried out to calculate C_{GS}, C_{BS} and C_{DS}, respectively. In the simulation, a small-signal sinusoidal source with the frequency of 0.65 THz is applied on the related electrodes and Y-parameter values are extracted from simulation results. For example, as shown in Fig. 7(b), when the AC small-signal is applied between the source and the gate terminals, the imaginary component of the Y_{11} parameter between gate and source electrodes is obtained, then the capacitance C_{GS} is evaluated by

$$I_m(Y_{11}) = \omega C_{GS} \tag{5}$$

where, ω is the angular frequency of the AC small-signal. It is noted that the THz signal is imported from the source terminal and the gate of the device is AC grounded, thus the capacitance C_{GD} has no effect on the capacitance C_{GS} in Equation (5).

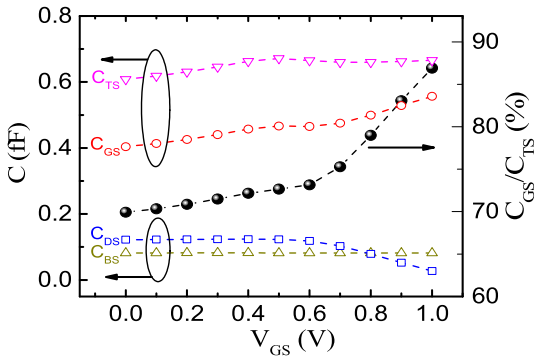


FIGURE 8. Extracted parasitic capacitances at the source terminal under various bias.

Fig.8 displays the extracted parasitic capacitances at the source terminal. It is seen that the input total equivalent capacitance C_{TS} is few fF for MOSFETs, weakly dependent on the gate voltage. Under the threshold voltage ($V_{TH} \approx 0.53$ V), C_{TS} is about 0.67 fF. C_{DS} and C_{BS} only contribute a small part to C_{TS} while C_{GS} accounts for 70% of C_{TS}, informing the poly gate overlapping source terminal is the dominant component of C_{TS}.

Fig. 9 shows the simulated gate-source overlap capacitance C_{GS} and gate-drain overlap capacitance C_{GD} as a function of W_S at 0.65 THz. As expected, C_{GS} is linearly reduced from 0.4 fF to 0.25 fF as the W_S increases from 0 to 20 nm, while C_{GD} almost keeps unchanged because the shifting source LDD has no impact on the gate-drain overlap area. Accordingly, the measured maximum responsivity is also enhanced linearly with the reduction of C_{GS}, seen in the blue dot line in Figure 9. This is due to the fact that the reduction of gate-source overlap capacitance by shifting LDD from the channel can effectively lower the source parasitic capacitance. As a result, input leakage through source parasitic capacitance is suppressed and the THz signal coupling to the channel is enhanced, leading to the significant improvement

TABLE 2. Performance comparison of the proposed CMOS THz detectors with the previously reported THz detectors fabricated in different technologies.

Ref.	Technology	Responsivity	*NEP*	Antenna	Area chosen
[20]	Schottky barrier diode(SBD)	2KV/W@0.11-0.17THz	13.2 pW/Hz$^{0.5}$ (1MHz mod.)	Nonuse	NA
[21]	GaN/AlGaN	3.6KV/W@0.897THz	40pW/Hz$^{0.5}$ (317Hz mod.)	Use	Antenna area
[22]	Si_xGe_y:H microbolometer	170V/W@0.934THz	200 pW/Hz$^{0.5}$ (100Hz mod.)	Nonuse	diffraction-limited area
[23][24]	90nm CMOS	351V/W@0.595THz	20 pW/ Hz$^{0.5}$ (1KHz mod.)	Use	Antenna area
[25]	65nm CMOS	1.5KV/W@0.2THz	15pW/ Hz$^{0.5}$ (1MHz mod.)	Use	Antenna area
This work	0.18 m CMOS, Ws=20nm	3.8KV/W@0.65THz	13.1pW/Hz$^{0.5}$ (3KHz mod.)	Use	Antenna area
	0.18 m CMOS, Ws=40nm	5.5KV/W@0.65THz	9.1pW/Hz$^{0.5}$ (3KHz mod.)	Use	Antenna area

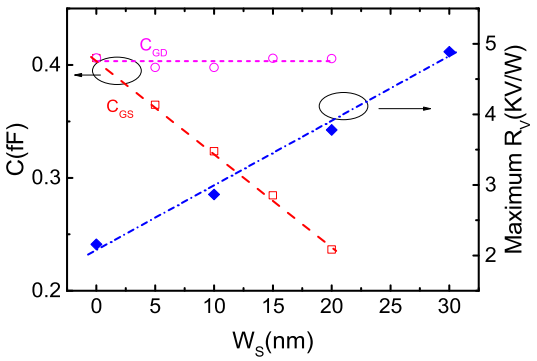


FIGURE 9. Gate-source overlap capacitance C_{GS} under V_{GS} of 0V and maximum responsivity at 0.65 THz under different displacements of W_S.

of responsivity. In addition, the thermal noise induced by channel resistance does not obviously increase with W_S, therefore the significant increase in responsivity and little change in thermal noise enable the remarkable reduction in *NEP* characteristic, as shown in Fig. 6(b).

Table 2 compares the responsivity and *NEP* characteristics of the proposed CMOS THz detectors with the reported THz detectors using different technologies, including BiCMOS and advanced CMOS technologies. Thanks to the reduction of gate-source parasitic capacitance by shifting LDD region, the proposed THz detector acquires a higher responsivity with a lower *NEP* in standard cost-efficient CMOS technology, showing the significant advantages over the reported ones.

It should also be noticed that the excessive W_S would cause no connection between the source and the channel, which could destroy the basic switch characteristic of MOSFET devices. Moreover, the increasing channel length due to excessive W_S will degrade the responsivity and *NEP* properties. To avoid these problems, the maximum W_S is limited to 40 nm in our work.

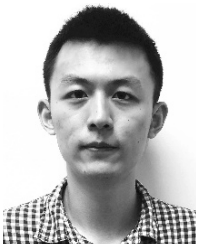
IV. CONCLUSION

We comprehensively studied the influence of gate-source capacitance on performance of CMOS THz detectors with various gate-source overlap areas. Based on standard 0.18 μm CMOS technology, a new asymmetric MOSFET process flow is proposed to reduce the gate-source overlapping area by adding a block in the NSD implantation mask. It is experimentally found that the responsivity and noise equivalent power are significantly improved by reducing the gate-source overlap area. For the integrated CMOS THz detectors working at 0.65 THz, the maximum R_V and the minimum *NEP* at 0.65 THz radiation are 5.5 KV/W and 9 pW/$\sqrt{}$Hz, respectively. The improvement of voltage responsivity and noise-equivalent power can attain 155% and 70%, respectively by suppressing gate-source parasitic capacitance. The device simulation further reveals that the gate-source overlap capacitance is the dominated factor on the performance of the MOSFET THz detector. Reducing the gate-source overlap area can effectively mitigate the gate-source capacitance effect, thus significantly improves the voltage responsivity and noise equivalent power. These results inform that the asymmetric MOSFET structure by reducing gate-source overlap capacitance is a promising solution to achieve high-performance and low-cost on-chip THz detectors in standard CMOS technology.

REFERENCES

[1] T. Morf *et al.*, "Room-temperature THz imaging based on antenna-coupled MOSFET bolometer," in *Proc. IEEE 26th Int. Conf. Micro Electro Mech. Syst.*, vol. 215, Jan. 2013, pp. 745–748.
[2] E. Ojefors, U. R. Pfeiffer, A. Lisauskas, and H. G. Roskos, "A 0.65 THz focal-plane array in a quarter-micron CMOS process technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1968–1976, Jul. 2009.
[3] T. Morf *et al.*, "Wide bandwidth room-temperature THz imaging array based on antenna-coupled MOSFET bolometer," *Sens. Actuators A, Phys.*, vol. 215, pp. 96–104, Aug. 2014.
[4] K. Sengupta, D. Seo, and A. Hajimiri, "A terahertz imaging receiver in 0.13μm SiGe BiCMOS technology," in *Proc. Int. Conf. Infr. Millim., Terahertz Waves*, Oct. 2011, pp. 1–2.
[5] D. Coquillat, J. Marczewski, P. Kopyt, N. Dyakonova, B. Giffard, and W. Knap, "Improvement of terahertz field effect transistor detectors by substrate thinning and radiation losses reduction," *Opt. Express*, vol. 24, no. 1, pp. 272–281, Jan. 2016.
[6] H. Sherry *et al.*, "Lens-integrated THz imaging arrays in 65nm CMOS technologies," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2011, pp. 1–4.
[7] F. Schuster *et al.*, "Broadband terahertz imaging with highly sensitive silicon CMOS detectors," *Opt. Express*, vol. 19, no. 8, pp. 7827–7832, Apr. 2011.

[8] A. Lisauskas, U. Pfeiffer, E. Öjefors, P. H. Bolìvar, D. Glaab, and H. G. Roskos, "Rational design of high-responsivity detectors of terahertz radiation based on distributed self-mixing in silicon field-effect transistors," *J. Appl. Phys.*, vol. 105, no. 11, Jun. 2009, Art. no. 196601.
[9] M. W. Ryu, J. S. Lee, K. Park, W.-K. Park, S.-T. Han, and K. R. Kim, "Photoresponse enhancement of plasmonic terahertz wave detector based on asymmetric silicon MOSFETs with antenna integration," *Jpn. J. Appl. Phys*, vol. 53, no.4S, Apr. 2014, Art. no. 04EJ05.
[10] M. Dyakonov and M. Shur, "Shallow water analogy for a ballistic field effect transistor: New mechanism of plasma wave generation by DC current," *Phys. Rev. Lett.*, vol. 71, no. 15, p. 2465, Oct. 1993.
[11] S. Boubanga-Tombet *et al.*, "Current-driven detection of terahertz radiation using a dual-grating-gate plasmonic detector," *Appl. Phys. Lett.*, vol. 104, no. 26, p. 262104, Jun. 2014.
[12] A. Lisauskas *et al.*, "Terahertz responsivity and low-frequency noise in biased silicon field-effect transistors," *Appl. Phys. Lett.*, vol. 102, no. 15, pp. 368–380, Apr. 2013.
[13] D. Veksler *et al.*, "Detection of terahertz radiation in gated two-dimensional structures governed by DC current," *Phys. Rev. B, Condens. Matter*, vol. 73, no. 12, Mar. 2006, Art. no. 125328.
[14] J.-Q. Lü and M. S. Shur, "Terahertz detection by high-electron-mobility transistor: Enhancement by drain bias," *Appl. Phys. Lett.*, vol. 78, no. 17, pp. 2587–2588, Apr. 2001.
[15] M. W. Ryu, J. S. Lee, K. Park, K. R. Kim, W.-K. Park, and S.-T. Han, "TCAD modeling and simulation of non-resonant plasmonic THz detector based on asymmetric silicon MOSFETs," in *Proc. Int. Conf. Simulation Semiconductor Processes Devices*, Sep. 2013, pp. 200–203.
[16] S. Boppel *et al.*, "Monolithically-integrated antenna-coupled field-effect transistors for detection above 2 THz," in *Proc. 9th Eur. Conf. Antennas Propag.*, Apr. 2015, pp. 1–3.
[17] M. Dyakonov and M. Shur, "Detection, mixing, and frequency multiplication of terahertz radiation by two-dimensional electronic fluid," *IEEE Trans. Electron Devices*, vol. 43, no. 3, pp. 380–387, Mar. 1996.
[18] R. Tauk *et al.*, "Plasma wave detection of terahertz radiation by silicon field effects transistors: Responsivity and noise equivalent power," *Appl. Phys. Lett.*, vol. 89, no. 25, pp. 253511-1–253511-3, 2006.
[19] S. Boppel *et al.*, "CMOS integrated antenna-coupled field-effect transistors for the detection of radiation from 0.2 to 4.3 THz," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 3834–3843, Dec. 2012.
[20] S. S. Dhillon *et al.*, "The 2017 terahertz science and technology roadmap," *J. Phys. D, Appl. Phys.*, vol. 50, no. 4, Jan. 2017, Art. no. 043001.
[21] J. D. Sun, Y. F. Sun, D. M. Wu, Y. Cai, H. Qin, and B. S. Zhang, "High-responsivity, low-noise, room-temperature, self-mixing terahertz detector realized using floating antennas on a GaN-based field-effect transistor," *Appl. Phys. Lett.*, vol. 100, no. 1, Jan. 2012, Art. no. 013506.
[22] A. Kosarev, S. Rumyantsev, M. Moreno, A. Torres, S. Boubanga, and W. Knap, "Si_xGe_y: H-based micro-bolometers studied in the terahertz frequency range," *Solid State Electron.*, vol. 54, no. 4, pp. 417–419, Apr. 2010.
[23] A. Lisauskas *et al.*, "Exploration of terahertz imaging with silicon MOSFETs," *J. Infr., Millim., Terahertz Waves*, vol. 35, no. 1, pp. 63–80, Jan. 2014.
[24] M. Bauer *et al.*, "Antenna-coupled field-effect transistors for multi-spectral terahertz imaging up to 4.25 THz," *Opt. Express*, vol. 22, no. 16, pp. 19235–19241, Aug. 2014.
[25] M. W. Ryu *et al.*, "High-performance plasmonic THz detector based on asymmetric FET with vertically integrated antenna in CMOS technology," *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1742–1748, Apr. 2016.



QIXUAN YANG received the bachelor's degree in electronics science and technology from Nanjing University, Nanjing, China, in 2012.

He is currently pursuing the master's degree with Nanjing University.

XIAOLI JI received the B.S. degree from the Physics Department, Jilin University, and the Ph.D. degree from the University of Tsukuba, Japan. She is currently a Professor with Nanjing University, China. Her research interests include the area of microelectronics.

YUE XU received the Ph.D. degree in microelectronics and solid-state electronics from Nanjing University, China, in 2012.

He is currently a Professor with the Nanjing University of Posts and Telecommunications, Nanjing, China. His main research interests include complementary metal–oxide–semiconductor detector, analog integrated circuit design, and device reliability.

FENG YAN photograph and biography not available at the time of publication.