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Performance Improvement of Microwave Vector Modulator Through Coupler Characteristic Impedance Optimization and Bond-Wire Inductance Utilization

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ABSTRACT An improved technique for the design of an unbalanced analog reflection-type on-chip vector modulator is presented. At microwave frequencies, voltage-controlled high-electron-mobility transistor (HEMT) like pseudomorphic HEMT (pHEMT) is often chosen as the variable termination in vector modulator. However, the parasitic elements of the transistor introduce amplitude and phase errors, which will degrade the overall performance of the vector modulator. Based on the establishment of pHEMT scalable parasitic model and characterization of bond-wire interconnection, we propose a method and a corresponding design procedure that mitigate the parasitic effects of pHEMT and achieve optimum performance of the vector modulator. The influences of Lange coupler characteristic impedance and compensation inductance on the vector modulator are analyzed first. Then, a method to determine the optimal values of characteristic impedance and compensation inductance is given, which relieves parasitic effects and obtains symmetric constellation. In our proposed design, the compensation inductance is realized through bond-wire inductance, eliminating the requirement of the on-chip inductor. To validate the design concept, a vector modulator module, composed of power divider, Lange coupler, and variable termination, is designed with each part fabricated separately using 0.15-μm GaAs pHEMT process and assembled on Rogers 5880 substrate with 10-mil-thick printed circuit board. The assembled vector modulator is characterized using an automatic test setup. The measured symmetric constellation is in good agreement with the simulation result, which indicates the effectiveness of the proposed design method and assembly process.

INDEX TERMS Cold pHEMT, bond-wire, microwave integrated circuit (MMIC), parasitic elements, vector modulator.

I. INTRODUCTION

Microwave vector modulator is a kind of component that can be electronically controlled for simultaneous adjustment of amplitude and phase of the signal in electronic systems. With the rapid development of large scale array technology, amplitude and phase modulation are put into use in more systems with radar and wireless communication applications. The ability of 360° phase control and wide amplitude control range makes it an appropriate candidate for quadrature amplitude modulation [1], [2] and phased-array systems [3]–[5].

For reflection-type vector modulator, the function is generally achieved by in-phase addition of two orthogonal signals that are modulated by voltage controlled bi-phase variable attenuators (BVA) [6]. 3-dB hybrid coupler (normally Lange coupler) is employed inside the vector modulator to obtain two signals with quadrature phase and same amplitude. Then, two BVAs controlled relatively by two independent voltages function to adjust the phase and amplitude of signals, after which the two signals are combined by power divider to form the output signal. The performance of the vector modulator is mostly affected by BVA, which normally uses variable termination for amplitude and phase control. Another 3-dB hybrid coupler splits the input signal of the BVA into two paths, with each reflected by voltage-controlled variable termination.

Reflected signals combine at the isolation port of the coupler while cancel each other at the input port. Cold transistors are often used as variable termination.

However, at microwave and millimeter-wave frequencies, the parasitic elements inside the devices impact the balance between 'on' and 'off' states of BVA, along with degrading its insertion loss. Consequently, the symmetry of constellation for vector modulator deteriorates and insertion loss is increased as well. To offset the amplitude imbalance of BVA, shunt resistor has been introduced in [7]. This method improves the mismatch but the minimum insertion loss is increased. Another proposed method is to use balanced structure to remove the mismatch error [8], [9], but circuit area of balanced vector modulator is at least twice larger and another penalty is the elevated insertion loss due to the usage of passive components in large number. Lately, a novel balanced structure with circuit area comparable to the unbalanced structure is proposed [10], but the requirement for four control voltages increases the complexity and cost of multi-channel system when vector modulator is employed in large quantity. Thus, there is need for a design method which should improve the constellation symmetry with minimal omni-directional insertion loss of the vector modulator. Also, the method should be area efficient with less complexity.

This paper presents a design method for unbalanced reflection-type vector modulator to obtain improved transmission performance. We have utilized bond-wire parasitic inductance for compensation of BVA imbalance. Through optimization of inductance and Lange coupler characteristic impedance simultaneously, the BVA exhibits improved balance performance and high isolation. Consequently, the vector modulator can produce symmetric constellation and insertion loss is also minimized. The three building blocks of vector modulator, including power divider, Lange coupler and variable termination, are fabricated separately on GaAs substrate and connected together by bond-wire to verify the proposed method. The accuracy of bond-wire simulation model is experimentally verified and two-bond-wire interconnection model from microstrip to chip pad is optimized.

In the rest of the paper, Section II first analyzes the parasitic model of cold pHEMT and then the proposed design method is discussed. The design and measurements of three building blocks as well as the bond-wire interconnection are presented in Section III. In Section IV, the realization of vector modulator on PCB, the assembly process and measurement results are given. The work is finally concluded in Section V.

II. PROPOSED METHOD FOR OPTIMUM PERFORMANCE OF VECTOR MODULATOR

The basic working topology of analog reflection-type vector modulator is shown in Fig. 1, where V_I and V_Q represent control voltages. By assuming perfect condition for power divider and Lange coupler, the transmission function of vector modulator in frequency domain can be written as [11]:

$$T_{vm} = \frac{1}{2}(S_{21}^{I} + jS_{21}^{Q})\exp(j\theta) \tag{1}$$

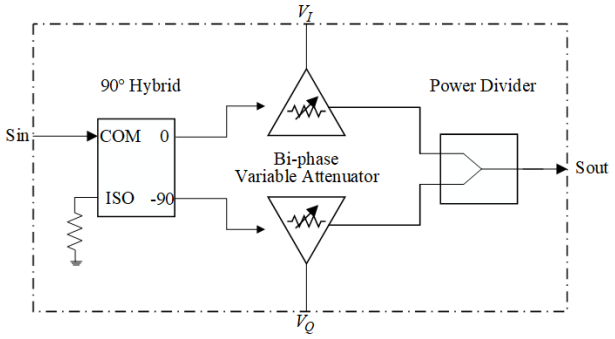

FIGURE 1. Schematic diagram of the unbalanced reflection-type vector modulator.

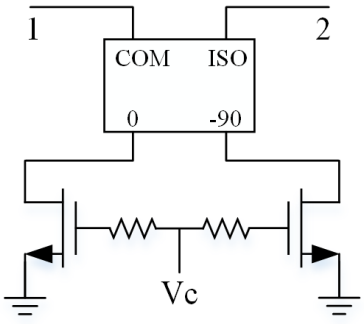

FIGURE 2. Topology of bi-phase variable attenuator.

where S_{21}^{I} and S_{21}^{Q} represent transmission coefficients of attenuator in I and Q path, θ and $1/2$ are relatively denoted as phase addition and amplitude attenuation factor resulting from the structure itself. From (1), the omni-directional insertion loss of vector modulator can be calculated to be 6 dB under the assumption that the minimum and maximum loss of attenuator are relatively to be 0 dB and infinity.

The topology of BVA is depicted in Fig. 2. Supposing the characteristic impedance of Lange coupler is Z_{L0} and input impedance of termination is Z_{in}, then S_{21}^{I} or S_{21}^{Q} can be described as:

$$S_{21} = j\frac{Z_{L0} - Z_{in}}{Z_{L0} + Z_{in}}. \tag{2}$$

From (2), to obtain variable attenuator with ideal feature, the target curve for Z_{in} with the change of control voltage should range from 0 to ∞ and intersect with Z_{L0}. However, the parasitic elements in cold pHEMT introduce deviation to target curve and deteriorate the attenuator performance. In order to mitigate this unwanted effect, detailed analysis of equivalent circuit model of cold pHEMT and corresponding design method are required.

A. COLD-pHEMT MODEL EXTRACTION

In this work, the equivalent circuit model of cold pHEMT proposed in [7] is utilized and shown in Fig. 3(a). In this model, R is the summation of drain and source resistance that come from extrinsic parasitic effects and ohmic contacts. L represents the summation of extrinsic parasitic inductance from drain and source. The parameters R_{ds} and C_v,

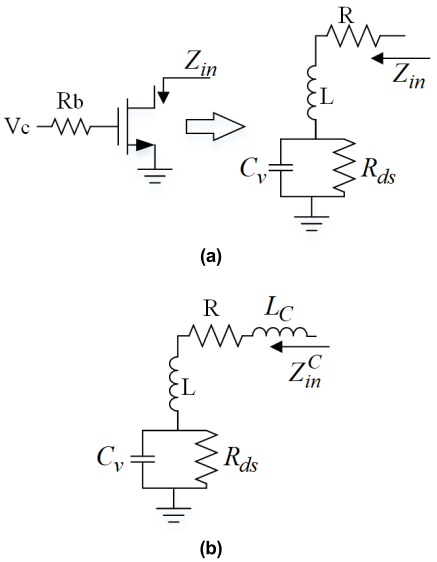

FIGURE 3. Circuit diagrams of (a) equivalent circuit of cold pHEMT and (b) equivalent circuit of cold pHEMT with compensation inductance.

which are bias controlled elements, are used to represent drain to source resistance and capacitance. C_v is the total capacitance between three electrodes of the transistor:

$$C_v = C_{ds} + \frac{C_{gd} \times C_{gs}}{C_{gd} + C_{gs}}. \tag{3}$$

The parasitic elements of the gate are absorbed by the resistor R_b with large value. The parameters of the model are extracted below. Input impedance Z_{in} of the model is given by:

$$Z_{in} = R + j\omega L + \frac{R_{ds}}{1 + j\omega C_v R_{ds}}. \tag{4}$$

At the pinch-off condition, R_{ds} increases to kilo-ohms, so it can be neglected and Z_{in} is simplified to:

$$Z_{in} = R + j\omega L + \frac{1}{j\omega C_v}. \tag{5}$$

From (5), R can be obtained from $real(Z_{in})$, and L can be calculated via differentiating ωZ_{in} by ω^2, owing that only L contributes to the second-order term of ωZ_{in}. After the calculation of R and L , C_v and R_{ds} at different bias points can be further extracted given Z_{in} at these states.

The simulated reflection coefficients of $0.15-\mu m$ pHEMT models that are fabricated on $100 - \mu m$ thick GaAs substrate are shown in Fig. 4. The control voltage is swept from -1V to 0V. It can be noted from Fig. 4 that the termination resistance is large at 'off' state, but the impedance is decreased due to the existence of parasitic capacitance. The extracted values of C_v and R_{ds}, as shown in Fig. 5, agree well with this condition. Moreover, at 'on' state, the existence of parasitic resistance R_{ds} and R, as shown by extracted curve of R_{ds}, result in non-zero termination impedance.

Gate width plays an important role in the value of parasitic elements. Though the larger gate width leads to decreased

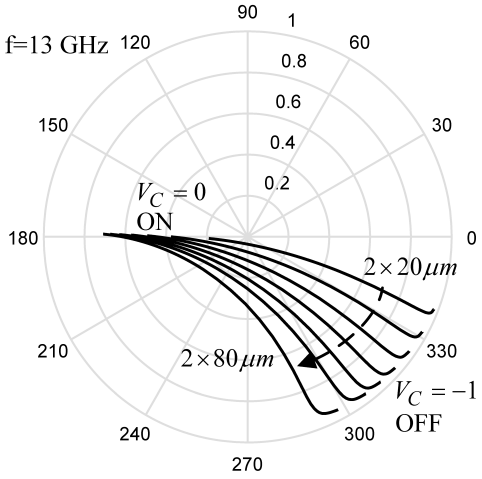

FIGURE 4. Reflection coefficients of cold pHEMTs with different sizes.

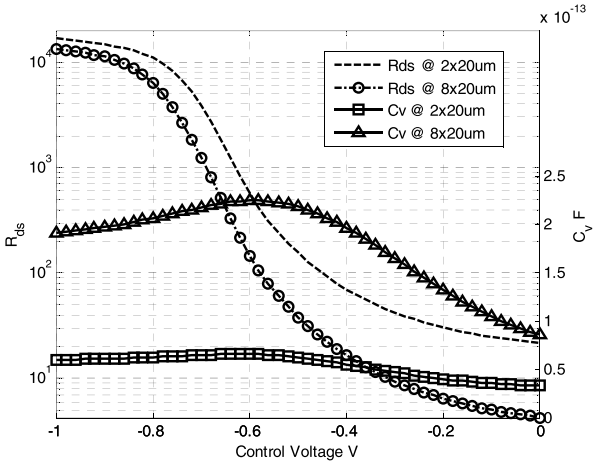

FIGURE 5. Extracted R_{ds} and C_V with the change of control voltage.

parasitic resistance, parasitic capacitance is increased and the infinity resistance at pinch-off state is consequently diminished further. For the convenience of gate width choice and analysis, as suggested by Hou *et al.* [11], the scaling factor F is defined, and the scalable model is established to characterize the cold pHEMTs with arbitrary gate width during the design process.

B. OPTIMUM DESIGN OF VARIABLE ATTENUATOR

As expressed in (2), the attenuation range of variable attenuator is determined by both Z_{L0} and Z_{in}. The proposed method aims to control Z_{L0} and Z_{in} simultaneously to achieve improved performance of BVA. With an inductance L_C introduced to the drain-source path [7], the amplitude and phase of Z_{in} can be improved for better reflection coefficient. However, 50 Ω may not be the best choice for Z_{L0} any longer when large and equal reflection coefficients at 'on' and 'off' states are needed. Additionally, the optimum Z_{L0} and L_C are supposed to be changing with gate width. Thus, it is necessary to analyze the influence of these three variables on BVA and deduce the optimum combination.

According to Fig. 3(b), the termination impedance Z_{in}^{C} after inductance compensation can be written as:

$$Z_{in}^{C} = R + j\omega(L + L_C) + \frac{R_{ds}}{1 + j\omega C_v R_{ds}}. \quad (6)$$

Assuming the reflection coefficients of compensated termination impedance at 'on' and 'off' states to be Γ_{on} and Γ_{off}, respectively and we can calculate them relatively using (2) with specified gate width and Z_{L0}. For symmetric variable attenuator design, the following equations should be satisfied:

$$\begin{aligned} |\Gamma_{on}| &= \left|\Gamma_{off}\right| \\ \left|\angle\Gamma_{on} - \angle\Gamma_{off}\right| &= 180°. \end{aligned} \quad (7)$$

Since there are two variables in (7) with fixed gate width, analytical solution to (7) should exist. Instead of getting the analytical solution, a value function is proposed here to obtain Z_{L0} and L_C that can meet (7) with minimal error. The error function of amplitude and phase are firstly defined by

$$\begin{aligned} Err_{amp} &= \left||\Gamma_{on}| - \left|\Gamma_{off}\right|\right| \\ Err_{phase} &= \left|\left|\angle\Gamma_{on} - \angle\Gamma_{off}\right| - 180°\right| \end{aligned} \quad (8)$$

where the absolute error is used so that score equation of amplitude and phase can be defined as the followings:

$$\begin{aligned} Scor_{amp} &= (1 - \frac{Err_{amp}}{max(Err_{amp})}) \times 100 \\ Scor_{phase} &= (1 - \frac{Err_{phase}}{max(Err_{phase})}) \times 100. \end{aligned} \quad (9)$$

Thus, the value function of variable attenuator can be further defined by

$$Scor = \frac{Scor_{amp} + Scor_{phase}}{2}. \quad (10)$$

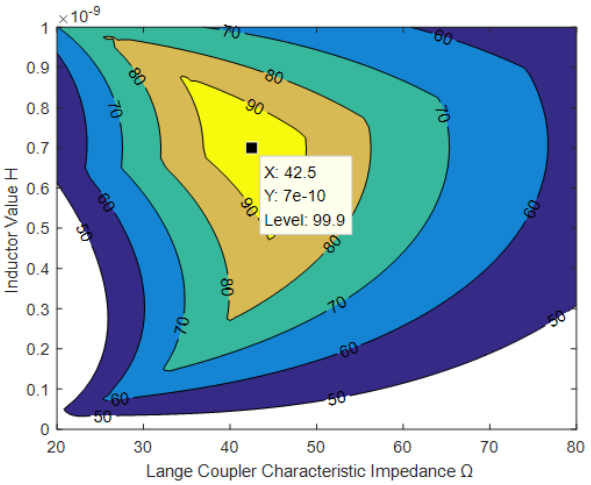

FIGURE 6. Simulation result of value function for bi-phase variable attenuator using pHEMT with 120 μm gate width.

With the definition of value function, the performance of variable attenuator can be estimated for different combination of Z_{L0} and L_C at each gate width. As an example, the simulation result of transistor with 120 μm gate width is shown in Fig. 6, where Z_{L0} is swept from 20 to 80 Ω and L_C is chosen from 0 to 1 nH. It is evident from Fig. 6 that there is a point whose score can get as high as 100, which implies that the condition in expression (7) can be satisfied using Z_{L0} and L_C of this point. Thus, with proper compensation inductance and Lange coupler characteristic impedance, the balanced amplitude and phase for BVA can be satisfied. Simulation results with gate width from 40 μm to 160 μm have similar pattern and perfect compensation point. In addition, the results also verify the existence of single analytical solution to (7).

The reflection coefficients with the change of control voltage after using the optimum values obtained at each gate width are simulated and shown in Fig. 7. The total gate width is swept from 40 μm to 160 μm with a step of 20 μm. It is shown in Fig. 7 that after compensation, the BVA based on arbitrary gate width can be designed to have balanced insertion loss and 180° phase difference between 'on' and 'off' states, meaning that the parasitic elements which lead to imbalance of attenuator and the resulting asymmetry in constellation of vector modulator has been canceled.

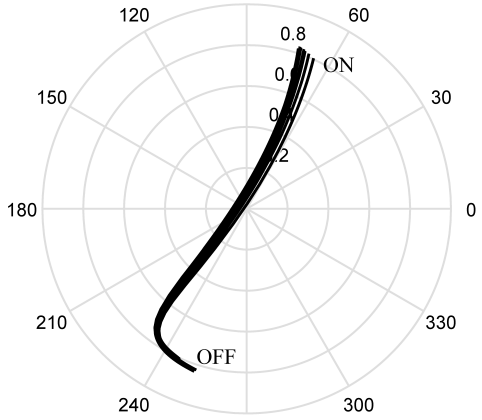

FIGURE 7. Reflection coefficients of cold pHEMTs with different sizes after optimization.

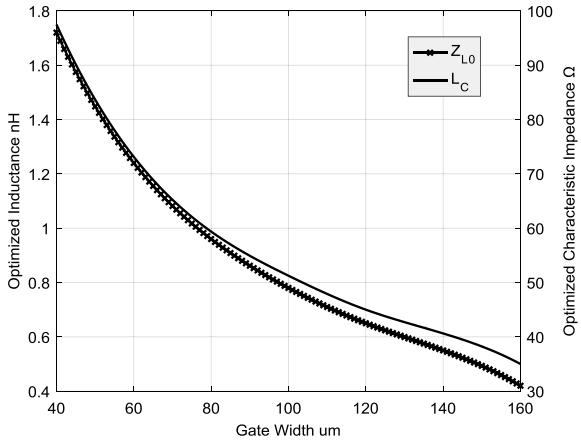

FIGURE 8. Optimization results of Z_{L0} and L_C.

Fig. 8 shows the obtained optimum values for different gate widths. Optimum compensation inductance and the Lange coupler characteristic impedance both drop with the increase of gate width. This result can be explained as follows. When the gate width becomes larger, the termination impedance

deviates away from infinite impedance, as shown in Fig. 3. So, less inductance is needed to move the impedance at 'on' state upward so that the phase difference between 'on' and 'off' states can be 180°. Under such condition, the average real part of termination impedance tends to be smaller. In order for equivalent insertion loss at 'on' and 'off' conditions, the normalization impedance Z_{L0} should be chosen with reduced value.

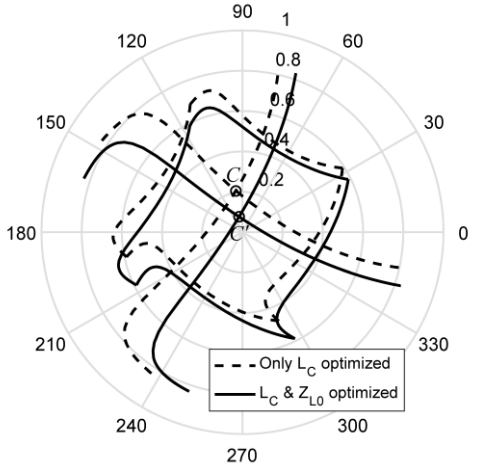

FIGURE 9. Vector addition diagram in vector modulator with optimized L_C only and with optimized L_C and Z_{L0}.

The effect of Z_{L0} optimization is further explained. Fig. 9 shows two constellations that are obtained using pHEMTs with 120 μm gate width. It can be observed that the constellation obtained with optimized Z_{L0} and L_C is more symmetric, and exhibits smaller omni-directional insertion loss when compared with the other, which is obtained with optimized L_C only. The parasitic elements in pHEMT shift the middle position of BVA transmission coefficient, where the maximum insertion loss is acquired, away from the origin. This deviation is one of the reason to asymmetric constellation. Process of optimization for Z_{L0} moves the middle point closer to the origin so that asymmetric vector combination can be avoided and the minimum insertion loss is improved. It is seen in Fig. 9 that when middle position C is moved to C', the insertion loss at the direction around 330 degree is decreased and the constellation turns to be more symmetric.

III. BLOCK LEVEL DESIGN AND INTEGRATION SIMULATION

Although it can be inferred from Fig. 7 that pHEMTs with gate width from 40 μm to 160 μm can be used for vector modulator design, other factors, related to the optimized Z_{L0} and L_C, limit the choice of gate width. Considering the input matching of the vector modulator, 50 Ω, rather than the optimized value, is the typical choice for Z_{L0}. And since the physical realization of L_C is achieved by parasitic inductance from bond-wire in this paper, a smaller value for L_C is preferred for better bond-wire model accuracy and to save circuit area. Though the repeatability and accuracy of bond-wire is worse than on-chip inductor, it can be flexibly adjusted to different values for convenience of method verification. After compromise, gate width is chosen to be 120 μm (6×20 μm), and the values for Z_{L0} and L_C are 45 Ω and 0.6 nH, respectively. Each part of vector modulator is designed separately using $0.15 - \mu m$ pHEMT technology with $100 - \mu m$ GaAs substrate, after which the behavior of vector modulator is simulated through combination of every part using bond-wire.

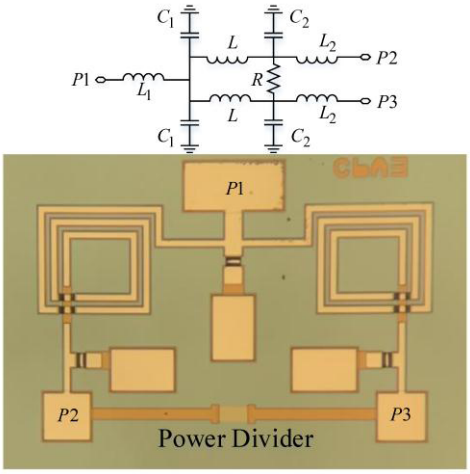

FIGURE 10. Schematic and microphotograph of power divider.

A. POWER DIVIDER DESIGN

The Wilkinson power divider is used for addition of two orthogonal signals and generation of the output. Since parasitic inductance will be introduced from bond-wire during assembly, we replace the traditional $\lambda/4$ transmission lines with lumped components of π type [12] for convenience of matching, as shown in Fig. 10. The power divider is designed to work at the chosen frequency 13 GHz, Ku band. After calculation of the values for lumped components in π model, the parasitic inductance value of bond-wire is preset in the simulation circuit, which results in deteriorated port matching and S21. The acquirement of the inductance value will be introduced later. Even-mode circuit of the power divider with bond-wire inductance added is designed independently, and two capacitances in the π model are optimized for better port matching, after which their values are further adjusted for the isolation and matching of P2/P3 in the whole power divider circuit. The final values of lumped components are: $L = 0.938$ nH, $C_1 = 0.13$ pF and $C_2 = 0.17$ pF, with parasitic inductance $L_1 = 0.3$ nH and $L_2 = 0.54$ nH. The simulated return loss and isolation at 13 GHz are below −14 dB, and insertion loss of 0.45 dB is achieved. The fabricated chip occupies an area of 0.9 mm× 0.45 mm and is shown in Fig. 10.

B. LANGE COUPLER DESIGN

The Lange coupler is designed employing the normal method [13]. The width of the line is calculated to be 8 μm and for 3 dB coupling coefficient, the spacing between two

lines is 7 μm. In order to efficiently utilize the chip area, the Lange coupler is designed in meandered shape. The layout dimension is 0.9 mm$\times$ 1.0 mm, as shown in Fig. 11. Also, the introduction of bond-wire parasitic inductance (0.2 nH) decreases the coupling level and harms the port matching. This is improved by adding parallel capacitance at each port. In order to reduce the error of small value capacitance from process variation, two capacitors with twice larger value in series structure are used to achieve the parallel capacitance. The simulation shows the return loss and isolation at 13 GHz are below -15 dB, and that the phase and amplitude imbalance are 4.5 degree and 0.75 dB, respectively.

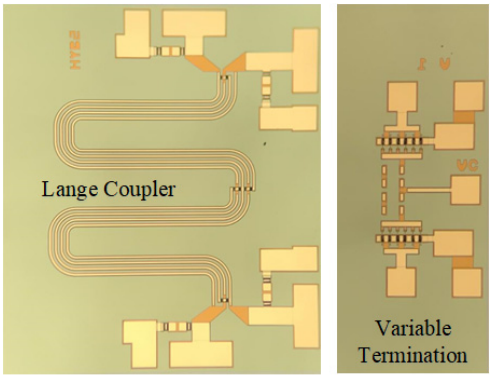

FIGURE 11. Microphotograph of lange coupler and variable termination.

C. VARIABLE TERMINATION DESIGN

Fig. 11 also shows the fabricated variable termination chip, which includes two 120 μm ($6\times 20\mu m$) pHEMTs. The source of the transistors are directly connected to ground by through vias. Gate resistor R_b is chosen to be 1 $k\Omega$ and a common pad is employed to provide control voltage to both transistors.

D. BOND-WIRE SIMULATION AND EXPERIMENT VERIFICATION

In our design, we have intentionally utilized the parasitic inductance of bond-wire as compensation inductance. Thus, its value should be accurately predicted in the design phase. We carried out full wave simulation and measurement experiment of bond-wire to verify accuracy of the simulation model and subsequently utilized simulation results for design.

For measurement, bond-wires are fabricated on a test fixture that is made of 10 mil Rogers 5880 substrate with 50Ω microstrip. As depicted in Fig. 12, the fabricated bond-wire can be approximated by three line segments. For the bond-wire simulation, JEDEC 5-Point model in HFSS, a full wave EM solver, is chosen. Though there are four sections in the JEDEC 5-Point model, it can be adjusted to match the three-segment shape of practical bond-wire well. Four parameters are used to describe the bond-wire model: the distance between two bonding points D, the height of the bond-wire H and the attack angles of the first and second bonding point α and β. The height difference between two bonding points is normally fixed by real condition, so it is not treated as a variable here.

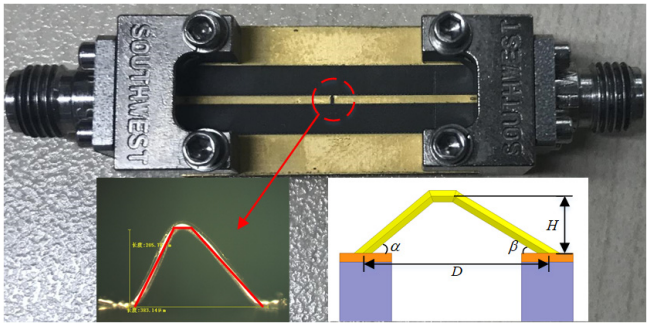

FIGURE 12. Test fixture of bond-wire with fabricated bond-wire and bond-wire model displayed in detail.

TABLE 1. Various bond-wire interconnect configurations and extracted parasitic inductance values.

Configuration	S1	S2	S3	S4	D1	D2
$D(um)$	240	240	380	380	380	380
$H(um)$	150	270	200	350	200	350
$\alpha(\circ)$	60	85	65	86	65	86
$\beta(\circ)$	46	50	42	50	42	50
L_π -SIM(nH)	0.27	0.35	0.40	0.54	0.28	0.35
L_π -MEAS(nH)	0.28	0.41	0.40	0.54	0.29	0.36
Error(%)	3.6	15	0	0	3.4	2.8

Models S1-S4 have one bond-wire while models D1-D2 have two bond-wires with a distance of 170 μm . The error is calculated by the absolute difference between simulated and measured inductance divided by measured value.

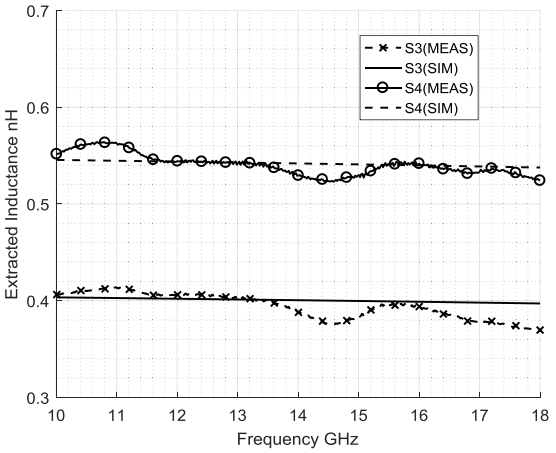

FIGURE 13. Extracted inductance values for two kinds of bond-wires.

Bond-wires with six different sets of parameters are fabricated and their S-parameters from 10 GHz to 18 GHz are measured by Agilent N5225A vector network analyzer. The parameter setups for bond-wire are listed out in Table 1. After measurement, the effects induced by connector and transmission lines are de-embedded using TRL calibration method and the conventional π equivalent circuit model [14] is employed to characterize the bond-wire. The series inductance of the model is extracted for comparison between simulation and measurement results, with two examples shown in Fig. 13. It is seen that the simulation results match well with

the average value of measured results. However, fluctuation occurs in the measurement data across the frequency band, which attributes to the inconsistency from both TRL kits and test fixture during fabrication and measurement. The extracted values at 13 GHz are listed out in Table 1. The large error in configuration S2 results from discrepancy between simulation model and fabricated prototype under the settings of D and H. However, the small error in most models proves the consistency between the simulation and measurement.

After verification of bond-wire simulation accuracy, the bond-wire simulation model is used in the design phase. Considering the value of L_C and dimension relation between Lange coupler and variable termination, the bond-wire physical parameters can be obtained. When the distance between the pads on Lange coupler and variable termination is 400 μm, in order to get parasitic inductance of 0.6 nH, the simulated values of the bond-wire model parameters are $D = 400\ \mu m$, $H = 420\ \mu m$, $\alpha = 74°$ and $\beta = 64.5°$. In addition, the parasitic elements induced from bond-wire for interconnection between different blocks can be estimated and used in block circuit design as well as vector modulator performance simulation.

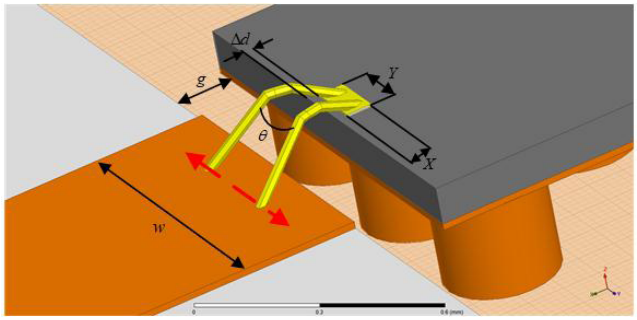

FIGURE 14. Bond-wire interconnection transition model between microstrip line and integrated chip.

The bond-wire interconnection from assembled vector modulator to 50 Ω microstrip line is optimized for better matching and insertion loss by simulation. Two-bond-wire structure with splitting angle is often chosen as board to chip transition in practical utilization. But the relation between splitting angle and matching is not clarified yet. The complete transition model is established and shown in Fig. 14. In the model, the GaAs chip is mounted on the copper pad which is grounded by multiple vias. The substrate Rogers 5880 below the grounding copper is hidden for better display of vias. The defined parameters in the transition model are the width of transmission line $w = 0.75$ mm, the distance between transmission line and grounding copper $g = 0.15$ mm, the pad dimension $X = 70\ \mu m$ and $Y = 140\ \mu m$, and the distance between pad to chip edge $\Delta d = 32\ \mu m$. The splitting angle θ is treated as optimization variable. It should be pointed out that during optimization of θ, the bonding point on microstrip line is fixed on a line that is parallel to the ending edge of it, as denoted by red arrows in Fig. 14. So, the length of bond-wire is actually increased with larger θ.

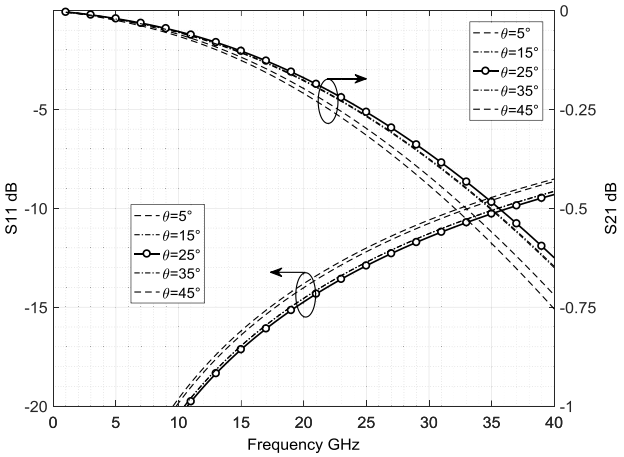

FIGURE 15. Simulation results of S11/S21 with different splitting angles of the two-bond-wire transition model.

The simulation results with the change of θ are shown in Fig. 15. As can be seen from the result, the insertion loss and return loss firstly improve with the increase of θ, and then begin to deteriorate after passing optimum value of θ. This is the combined consequence of mutual inductance, current return path and bond-wire length. When θ is small, the reduction in mutual inductance between two bond-wires by increasing θ influences the transition mostly. In addition, with the increase of θ, cross section area of the current return path below the bond-wire is enlarged so that the parasitic effects from return path are decreased. As a result, the total inductance and resistance in the transition become smaller, thus improving the transition performance. But after θ gets its optimum value and is further increased, the effect of bond-wire length will weigh more than that from mutual coupling and return path, which degenerates the transition behavior due to larger parasitic values. The optimized value for θ under current settings is 25°, and it is found by simulation that this value does not change when g and D become larger. Though the insertion loss and return loss improvement through θ optimization in 13 GHz are relatively small, the transition performance will improve more for higher frequency and longer bond-wire, making it useful in bond-wire interconnection design.

E. VECTOR MODULATOR SIMULATION

The behavioral simulation of the complete vector modulator is performed. The following steps elaborate the simulation methodology:

- Utilize the layout of the three building blocks to finish the total layout drawing of the vector modulator and measure the distance and relative position of each pair of pads that should be connected by bond-wire.
- Establish physical model of bond-wire for each connection place according to the measured dimensions and simulate the model in HFSS: for transition from microstrip line to chip pad, the optimized model in last subsection is used; for connection providing

compensation inductance, the model is adjusted to supply 0.6 nH parasitic inductance; for the rest connections between chips, low profile and short length is taken as principle for modeling.

- Extract parasitic inductance and resistance of each bond-wire model from the simulated S-parameters in HFSS.
- Combine simulated S-parameters of power divider and Lange coupler, extracted bond-wire parasitic elements and momentum model of variable termination in Agilent Advanced Design System (ADS), and then simulate the behavior of vector modulator.

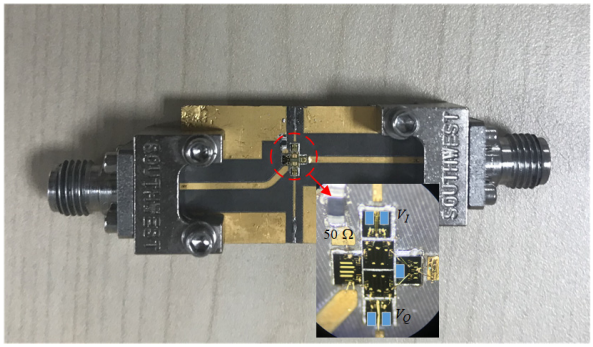

FIGURE 16. Assembled vector modulator module and enlarged chips.

IV. ASSEMBLY AND MEASUREMENT

A. ASSEMBLY

The assembled vector modulator module is shown in Fig. 16, with microphotograph of the chips displayed in detail. 10 mil Rogers 5880 substrate is used and 50 Ω microstrip line is designed for input and output connection. The input transmission line is bent in order to become closer to the input pad of Lange coupler, shortening the length of bond-wire. All chips are epoxied to the first layer, which is grounded using multiple vias. 50 Ω resistance in the isolation port of input Lange coupler is implemented using 0402 package surface mounted device (SMD) component.

I/Q control voltages are supplied by vertical microstrip lines. The three blocks of vector modulator and input/output transmission lines are interconnected through bond-wires. The bond-wires for inductance compensation are bonded carefully to satisfy the simulated dimension values. High frequency K connectors are used for the measurements.

B. MEASUREMENT

The transmission characteristic of vector modulator is measured using Agilent N5225A network analyzer. The reference power is set to −20 dBm and the effect of cables is calibrated before measurement. For providing two paths control voltage from −1 V to 0 V, HMP 4040 four-channel power supply from Rohde & Schwarz is used. The established automatic testing platform for constellation measurement is shown in Fig. 17, where the computer is used to control the power supply and network analyzer.

With a step of 20 mV for the control voltage, the measured constellation is shown in Fig. 18, along with the

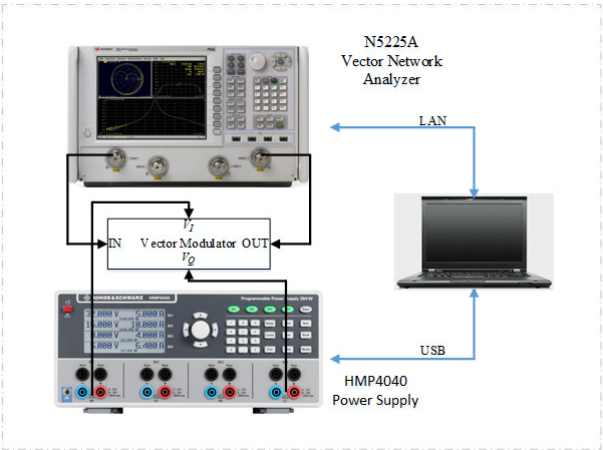

FIGURE 17. Automatic test platform for vector modulator constellation.

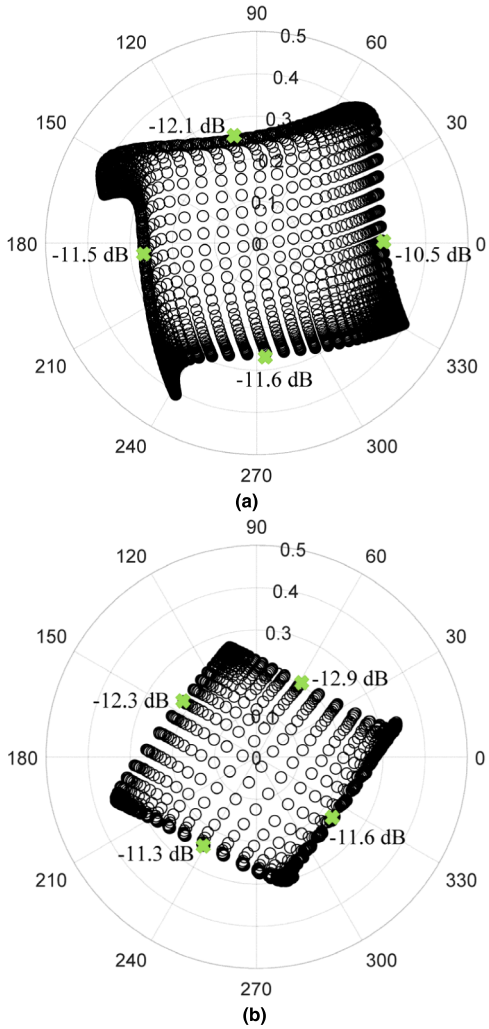

FIGURE 18. Constellations of the (a) simulated and (b) measured vector modulator.

simulated result. From the result, it can be noted that though rotation happens due to the phase delay of passive components and test fixture, the center of the pattern is nearly located at the origin and the result exhibits good

symmetric shape. The minor degradation in symmetry when compared with the simulation result may be due to the deviation in demension of compensation bond-wire. In addition, the two axes are not orthogonal to each other any longer due to the parasitics introduced from the isolation port of input Lange coupler and imbalance in two orthogonal paths during assembly process, including bond-wire length and relative position of the chips.

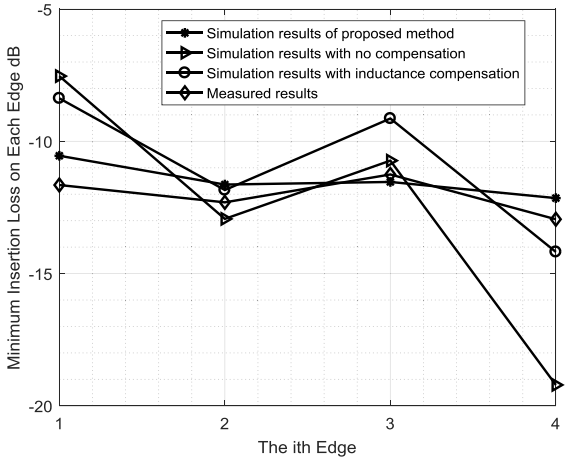

FIGURE 19. The minimum insertion loss on four edges of constellation.

TABLE 2. Comparison of microwave vector modulator designs.

Ref.	Type	Frequency	Omni-directional Insertion Loss	Constellation Shape
[1]	Balanced	110 GHz	12 dB	One Quadrant (90° relative phase shift)
[2]	Balanced	45-75 GHz	10 dB	-
[10]	Balanced	20.35 GHz	16 dB	Symmetric
[11]	Unbalanced	40 GHz	10.6 dB	Asymmetric
THIS WORK	Unbalanced	13 GHz	12.9 dB	Symmetric

In order to obtain insertion loss of vector modulator, the test fixture loss which includes loss of transmission lines and connectors is removed from the measurement results through TRL de-embedding method. The measured maximum insertion loss on each edge of constellation is shown in Fig. 19. The measured constellation shows a minimum omni-directional insertion loss of 12.9 dB, which is 0.8 dB larger than the simulated result, proving the accuracy of our simulation method and robustness of assembly process. Moreover, we have compared the simulated results of vector modulator without compensation and only with inductance compensation, as depicted in Fig. 19. It is indicated that the proposed design shows less amplitude imbalance (0.7 dB and 1.6 dB on two directions) and reduced omni-directional insertion loss. The comparison between the proposed and the published microwave vector modulators is summarized in Table 2, which further validates the improvements obtained using the proposed technique.

V. CONCLUSION

The experiment and measurement results in this paper indicate that the proposed technique for the design of unbalanced analog reflection-type on-chip vector modulator can offer improved symmetric constellation. It is found that when pHEMT is used as variable termination, though different values of parasitic resistance and capacitance will be introduced under different gate widths, symmetric features of BVA can be obtained with proper design of compensation inductance and Lange coupler characteristic impedance. In practical condition, the matching of vector modulator should be also considered, meaning the choice of impedance for Lange coupler is limited. The parasitic inductance in bond-wire is utilized to provide compensation inductance in this paper. And for the two-bond-wire transition from chip to microstrip line on substrate, optimum splitting angle exists for best matching. The measured result of the assembled vector modulator exhibits symmetric constellation with minimum omni-directional insertion loss of 12.9 dB, proving the effectiveness of the method in adjusting constellation pattern.

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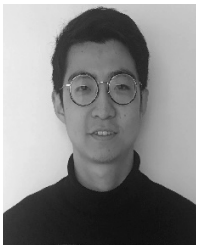

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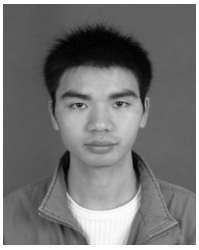

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