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A Highly Efficient Multifunctional Power Electronic Interface for PEV Hybrid Energy Management Systems

XIAOYING LU[1,2,3], (Student Member, IEEE), AND HAOYU WANG[1], (Senior Member, IEEE)

[1]School of Information Science and Technology, ShanghaiTech University, Shanghai 201210, China
[2]Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China
[3]University of Chinese Academy of Sciences, Beijing 100049, China

Corresponding author: Haoyu Wang (wanghy.shanghaitech@gmail.com)

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ABSTRACT In the hybrid energy management systems of plug-in electric vehicles (PEVs), a power electronic interface (PEI) is required to connect the grid side dc link, the ultracapacitor bank, and the battery pack. To realize this PEI, the conventional method is deploying multiple independent dc/dc converters and it suffers from bulky size and high hardware cost. In this paper, an integrated multifunctional PEI is proposed to effectively mitigate those issues. The proposed PEI enables three functions—grid to vehicle (G2V), vehicle to grid (V2G), and PEV driving. It integrates the CLLC resonant topology with the bidirectional interleaved buck/boost topology, in which the former is utilized in the G2V and V2G modes, while the latter is in charge of the driving mode. Due to circuit reuse of the secondary side full-bridge structure, the system components count is reduced effectively. A synchronous rectification (SR) technique is developed to actively control the MOSFETs in CLLC rectification stage. Soft switching and SR techniques work in synergy to ensure a high conversion efficiency. An experimental prototype is designed, optimized, and tested for all three working modes. A peak efficiency of 98.27% for the G2V mode, 98.04% for The V2G mode, 98.56% for the PEV driving mode and good overall efficiency performances are reported.

INDEX TERMS CLLC, interleaved bidirectional buck/boost converter, plug-in electric vehicles, power electronic interface, synchronous rectification.

I. INTRODUCTION

Ultracapacitor (UC)/battery hybrid energy storage systems (HESS) have been comprehensively investigated in plug-in electric vehicles (PEVs). This is because this kind of hybridization brings many benefits including high energy/power density, extended battery lifetime and enhanced electric mileage [1]–[4]. A typical structure for the PEV power management system with onboard charger and semi-active UC/battery HESS is shown in Fig. 1. It is shown that an onboard charger is configured to charge the battery pack, and the HESS is in charge of PEV driving mode. In PEV driving mode, the battery and UC work together to provide/absorb power for the loads, and a dc/dc converter is utilized to link UC bank into the motor-drive side dc link [5]. Conventionally, the two parts are well separated.

The onboard lithium-ion battery pack is featured with a wide voltage range (typically 250 - 420 V) over a wide state-of-charge (SOC) range [6], [7]. Thus, the output

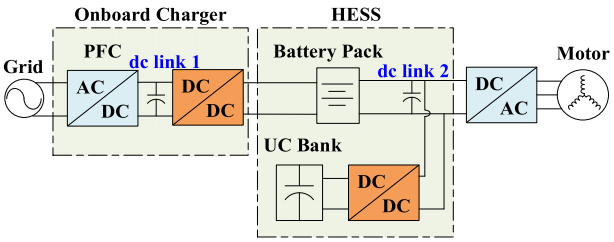

FIGURE 1. Conventional structure of the PEV power management system with onboard charger and semi-active UC/battery HESS.

characteristics of the dc/dc converter in the onboard charger need to be matched with the charging profile of the battery pack. Moreover, soft switching techniques such as zero-voltage-switching (ZVS) and zero-current-switching (ZCS) are expected when designing the dc/dc converter: they are utilized to achieve high conversion efficiency. LLC resonant

converter gains high popularity in battery charging applications due to its benefits of soft switching and wide output voltage range [8]–[10]. CLLC converter inherits the merits of LLC topology and is able to achieve bidirectional power flow [11]–[13].

A critical issue with CLLC converter is how to achieve power flow on the rectification stage. Generally, there are three feasible solutions: MOSFET body diode conduction (body diode solution), extra anti-parallel diode conduction (anti-parallel diode solution), and synchronous rectification (SR solution). The disadvantages of body diode solution lie in high conduction loss and MOSFET channel mis-conduction issue when the gate is floating. The anti-parallel diode solution causes extra cost, and cannot resolve the MOSFET channel mis-conduction issue using regular MOSFET drivers. SR solution is a cost-effective way to solve the above problems and to enhance the conversion efficiency.

One feasible SR technique is to detect the cross-zero-point by utilizing dedicated current sensors. In [14], two current transformers are embedded into the resonant tank to detect the zero crossing instant of the current. Then a DSP-based digital control method is utilized to generate the SR signals for the rectification side MOSFETs. This technique results in extra hardware cost and suffers from limited sensor bandwidth and controller sampling rate. Thus, this method is unsuitable for high-frequency applications and it is preferable to predict the SR signal without current sensors. Reference [15] introduces a technique to calculate the phase-shift angle between the primary MOSFET gate pulse and the resonant current on the secondary side to achieve SR. However, this phase-shift calculation method only maintains good accuracy with sinusoidal currents and voltages. Therefore, a more accurate SR solution without current sensors is desired.

In summary, reduced hardware cost, soft switching, wide output range, as well as enhanced conversion efficiency are the main desired features of the power electronic interface (PEI) for PEV hybrid energy management systems. In this paper, we propose a three-port bidirectional CLLC resonant converter based PEI for this specific application. The schematic of the proposed PEI is shown in Fig. 2. The idea is partially presented in [16]. This work is the extension of the conference paper. The proposed PEI is capable of effectively managing the power flows a) from the grid to the battery pack in grid to vehicle (G2V) mode; b) from the battery pack to the grid in vehicle to grid (V2G) mode; and c) among battery, UC, and load in PEV driving mode. Moreover, a sensor-less SR technique based on an accurate prediction of the rectifying current is proposed to generate the secondary side SR signals.

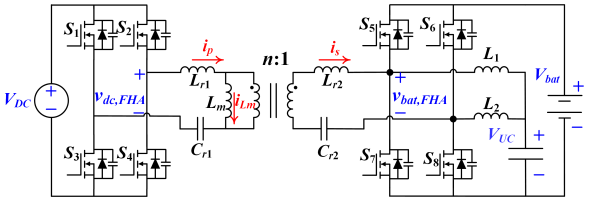

FIGURE 2. Schematic of the proposed multifunctional PEI.

This paper is organized as follows: Section II provides a comprehensive introduction to the PEI. Detailed analysis of the proposed PEI is presented in Section III. Optimal design considerations and procedure are listed in Section IV. Section V introduces the proposed SR technique and Section VI shows the experimental results. Finally, Section VII concludes this paper.

II. PROPOSED MULTIFUNCTIONAL PEI AND THREE WORKING MODES

A. TOPOLOGY DESCRIPTION

As shown in Fig. 2, the proposed PEI integrates the full-bridge bidirectional CLLC resonant topology and the interleaved buck/boost topology.

The full-bridge CLLC resonant converter consists of three main parts: a) the grid side power MOSFETs $S_1 \sim S_4$ are utilized to constitute a square-wave generator; b) the resonant network consists of the resonant capacitors C_{r1} and C_{r2}, resonant inductors L_{r1} and L_{r2}, and magnetizing inductor L_m; c) on the battery side, four MOSFETs $S_5 \sim S_8$ are configured to form a full-bridge rectification stage to charge the battery pack. The CLLC converter is bidirectional due to its symmetric structure. This means the battery is also able to feed power to the grid by actively controlling $S_5 \sim S_8$.

MOSFETs $S_5 \sim S_8$ not only act as the inverter/rectifier switches of the CLLC converter, but also function as switches of the buck/boost converter. It is shown that the two-phase interleaved buck/boost converter consists of four power MOSFETs ($S_5 \sim S_8$) and two inductors (L_1 and L_2). Interleaved structure is introduced to increase the power rating, to reduce the inductor size, and to accommodate the CLLC battery side full bridge.

B. THREE WORKING MODES

The proposed PEI is able to provide three working modes as shown in Fig. 3: a) G2V mode when $S_1 \sim S_4$ function as active switches and grid feeds power to the battery pack; b) V2G mode when $S_5 \sim S_8$ work as active switches and the battery pack regenerates the grid; and c) PEV driving mode when the grid side full bridge and the resonant network are idle. In this mode, interactive power flows are realized among battery, UC and the load of the PEV through the buck/boost converter. At the steady state of G2V and V2G modes, the buck/boost inductor currents (i_{L1} and i_{L2}) are trivial and circulating. Their dc biases are zero while the peak values depend on the inductance. The circulating currents facilitate an easier ZVS of the active switches.

III. ANALYSIS OF THE PROPOSED MULTIFUNCTIONAL PEI

A. G2V AND V2G MODES

In PEV G2V mode, $S_1 \sim S_4$ operate complementarily to generate a square-wave voltage (amplitude $\pm V_{DC}$, switching

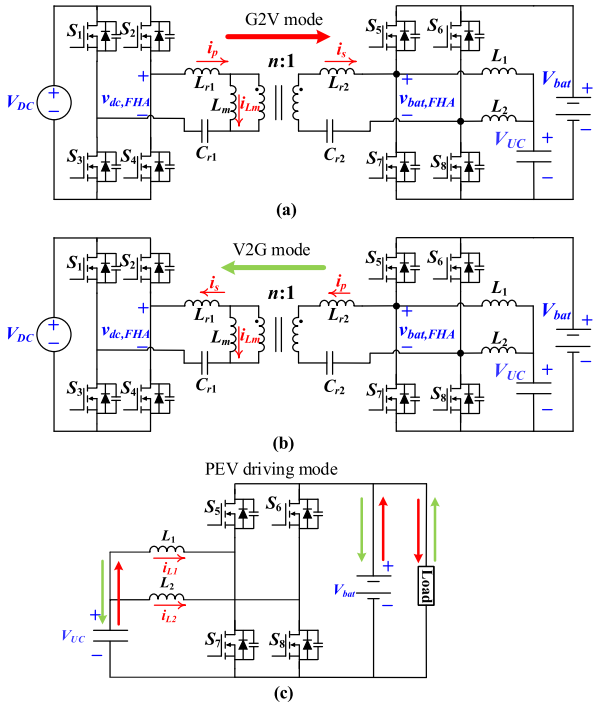

FIGURE 3. Equivalent circuits in three operation modes.

frequency f_s). A small dead time is needed between the consecutive transitions, both to prevent the feedthrough and to facilitate ZVS. This square wave is fed into the resonant network. For the secondary side, $S_5 \sim S_8$ constitute the rectifier bridge.

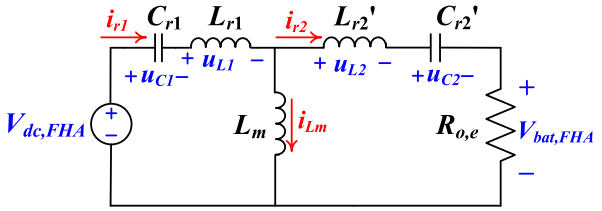

FIGURE 4. The equivalent circuit for G2V mode under FHA.

Fig. 4 illustrates the equivalent circuit model of the CLLC converter in G2V mode by utilizing first-harmonic-approximation (FHA) method. $V_{dc,FHA}$ represents the root-mean-square (rms) value of $v_{dc,FHA}$, the fundamental component of v_{dc}. Whereas, $V_{bat,FHA}$ is the rms value of $v_{bat,FHA}$. They are calculated as,

$$V_{dc,FHA} = \frac{2\sqrt{2}}{\pi} V_{DC}$$
$$V_{bat,FHA} = \frac{2\sqrt{2}}{\pi} V_{bat} \tag{1}$$

In G2V mode, the battery can be modeled as a resistor, whose resistance is,

$$R_{o,e} = \frac{8n^2}{\pi^2} \cdot R_{bat} \tag{2}$$

where, n is the turns ratio of the transformer, and R_{bat} is the equivalent resistance of the battery load. Then the transfer function of the resonant network in G2V mode can be expressed as,

$$\begin{aligned} H_r &= \frac{V_{UC,FHA}}{nV_{dc,FHA}} = \frac{1}{n} \cdot \frac{Z_o}{Z_{in}} \\ &= \frac{1}{n} \cdot \frac{(R_{o,e} + Z_{C'_{r2}} + Z_{L'_{r2}}) // Z_{Lm}}{Z_{C_{r1}} + Z_{L_{r1}} + (R_{o,e} + Z_{C'_{r2}} + Z_{L'_{r2}}) // Z_{Lm}} \\ &\quad \cdot \frac{R_{o,e}}{R_{o,e} + Z_{C'_{r2}} + Z_{L'_{r2}}} \end{aligned} \tag{3}$$

where, $L'_{r2} = n^2 L_{r2}$ and $C'_{r2} = C_{r2}/n^2$. They are the equivalent inductance/capacitance of the secondary side inductor/capacitor, respectively.

The gain of the resonant network in G2V mode is calculated as,

$$G_{G2V}(f_n) = \|H_r(f_n)\| = \frac{1}{n} \cdot \frac{1}{\sqrt{a^2 + b^2}} \tag{4}$$

where,

$$\begin{aligned} a &= k(1 - \frac{1}{f_n^2}) + 1 \\ b &= -Q[(kp + p + 1) \cdot f_n \\ &\quad - \left(kp + \frac{1+k}{q} + 1\right) \cdot f_n^{-1} + \frac{k}{q} \cdot f_n^{-3}] \end{aligned} \tag{5}$$

The normalized switching frequency (f_n) can be represented by the ratio between f_s and the resonant frequency (f_r), Q represents the quality factor, and k represents the ratio between L_{r1} and L_m, respectively,

$$\begin{aligned} &f_n = \frac{f_s}{f_r}, \quad f_r = \frac{1}{2\pi\sqrt{L_{r1}C_{r1}}}, \quad Z_r = \sqrt{\frac{L_{r1}}{C_{r1}}}, \quad Q = \frac{Z_r}{R_{o,e}}, \\ &k = \frac{L_{r1}}{L_m}, \quad p = \frac{L'_{r2}}{L_{r1}}, \quad q = \frac{C'_{r2}}{C_{r1}} \end{aligned} \tag{6}$$

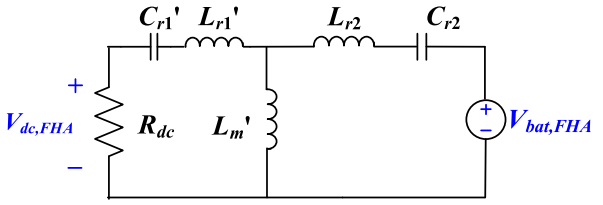

FIGURE 5. The equivalent circuit for V2G mode under FHA.

The equivalent circuit in V2G mode is modeled as Fig. 5. Where, $L'_{r1} = L_{r1}/n^2$ and $C'_{r1} = n^2 C_{r1}$ while $L'_m = L_m/n^2$, $R_{dc} = 8R_o/n^2\pi^2$. Therefore, the transfer function of the resonant network in V2G mode is expressed as,

$$G_{V2G}(f_n) = n \cdot \frac{1}{\sqrt{c^2 + d^2}} \tag{7}$$

where,

$$
\begin{aligned}
c &= k'(1-\frac{1}{f_n'^2})+1 \\
d &= -Q'[(k'p'+p'+1)\cdot f_n' \\
&\quad -\left(k'p'+\frac{1+k'}{q'}+1\right)\cdot f_n'^{-1}+\frac{k'}{q'}\cdot f_n'^{-3}] \\
f_n' &= \frac{f_s}{f_r'},\quad f_r' = \frac{1}{2\pi\sqrt{L_{r2}C_{r2}}},\quad Z_r' = \sqrt{\frac{L_{r2}}{C_{r2}}}, \\
Q' &= \frac{Z_r'}{R_{dc}},\quad k' = \frac{L_{r2}}{L_m'},\quad p' = \frac{L_{r2}}{L_{r1}'},\quad q' = \frac{C_{r2}}{C_{r1}'}.
\end{aligned} \tag{8}
$$

Based on (4-8), the gain curves versus the normalized switching frequency for G2V and V2G modes in different load conditions are depicted in Figs. 6 and 7, respectively. As shown, by modulating the normalized switching frequency, the voltage gain can be adjusted in a wide range. The normalized voltage gain is unity at the resonant frequency regardless of the load conditions. Whereas, the gain of the converter increases with a lower quality factor at other frequency.

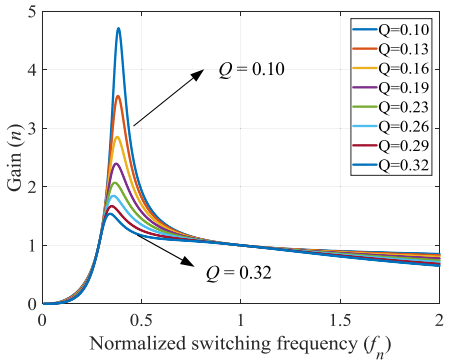

FIGURE 6. Gain curves in G2V mode versus normalized switching frequency with different values of Q.

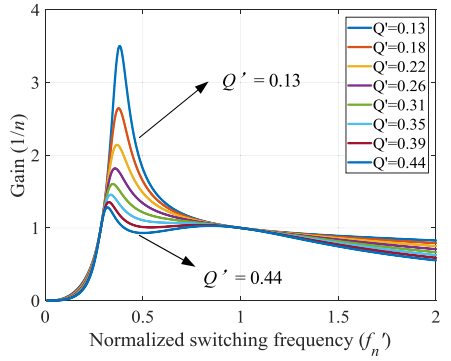

FIGURE 7. Gain curves in V2G mode versus normalized switching frequency with different values of Q'.

One benefit for the CLLC resonant converter is its ZVS features for all the active switches. For achieving ZVS, the dead time t_{dead} between the upper and lower MOSFETs should be sufficient to ensure that the output capacitances of the four switches are fully charged and discharged. Therefore, t_{dead} can be determined by,

$$t_{dead} \geq 8C_{oss}f_sL_m \tag{9}$$

where C_{oss} is the equivalent output capacitance of the MOSFETs.

B. PEV DRIVING MODE

During PEV driving mode, by operating at buck mode or boost mode, the synchronous interleaved buck/boost converter is capable of realizing the power interaction among UC, battery, and load. A 180° phase difference exists between the gate signals of S_5 and S_6 as well as S_7 and S_8. Assume the duty ratio of S_5 and S_6 is D, the duty ratio of S_7 and S_8 is $1-D$. Then the voltage gains for the interleaved converter in buck mode and boost mode are expressed as,

$$G_{buck} = D \tag{10}$$

$$G_{boost} = \frac{1}{D} \tag{11}$$

This buck/boost converter either works in continuous conduction mode (CCM) or critical conduction mode (CRM) based on the following relationship,

$$\text{Buck: } \frac{2Lf_{s,buck/boost}}{R_{UC}} > 1-D \text{ for CCM} \tag{12}$$

$$\text{Boost: } \frac{2Lf_{s,buck/boost}}{R_{bat}} > (1-D)\cdot D^2 \text{ for CCM} \tag{13}$$

where, $f_{s,buck/boost}$ is the switching frequency of the buck/boost converter, and R_{UC} is the equivalent resistance of the UC bank load. The rectifier MOSFETs of the synchronous converter (S_7 and S_8 in buck mode, S_5 and S_6 in boost mode) achieve ZVS naturally since the body diode conducts before the gate-source pulse. For the active switches (S_5 and S_6 in buck mode, S_7 and S_8 in boost mode), if the converter works in CCM, they are switched with hard-switching. However, in CRM, i_{L1} and i_{L2} are bidirectional (positive and negative). Therefore, both active MOSFETs and rectifier MOSFETs are switched with ZVS [17].

IV. OPTIMAL DESIGN CONSIDERATIONS

As discussed in Section III, the voltage gains in (4) and (7) are functions of multiple parameters. Nevertheless, it is hard to find a solution to determine all the parameters simultaneously. Fig. 8 illustrates the diagram of the optimal design considerations. These considerations are proposed to realize squeezed frequency modulation range, extended ZVS capabilities, and enhanced power density. The parameters need to be tuned to achieve the optimal performance tradeoff. The optimal design process is shown in the following steps.

1) Determine the suitable f_r. For design simplicity and circuit symmetry considerations, L_{r2} and C_{r2} are selected as L_{r1}/n^2 and n^2C_{r1}, respectively. Then f_r for G2V mode and f_r' for V2G mode are identical. f_r is selected to be 95 kHz considering tradeoffs between power density, EMI, conversion efficiency as well as control complexity [18].

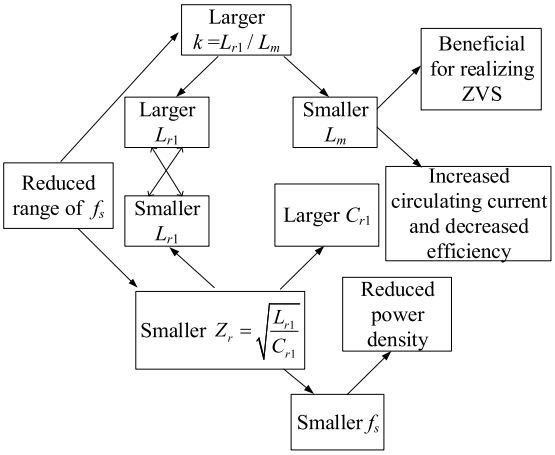

FIGURE 8. Diagram of the optimal design considerations.

2) n is designed as 1.2:1 considering 390V input and 250V∼420V output under G2V mode. G_{G2V} can be designed following the equation,

$$\frac{V_{bat}}{V_{DC}} = G_{G2V} \tag{14}$$

Similarly, G_{V2G} can be designed by,

$$\frac{V_{DC}}{V_{bat}} = G_{V2G} \tag{15}$$

3) Determine L_m according to (9).

4) Sweep parameter $k = L_{r1}/L_m$ at full load condition. The voltage gain curves under different k are depicted in Fig. 9. It is illustrated that to obtain a wide adjustable output voltage within a relatively narrow frequency range, a larger k is desired.

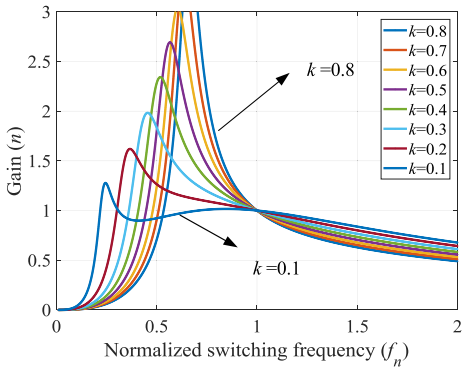

FIGURE 9. Curves of gain versus normalized switching frequency with different values of k.

5) Sweep parameter $Z_r = \sqrt{L_{r1}/C_{r1}}$ at full load condition. The corresponding gain diagram is depicted in Fig. 10. We can find that there are two local maximum points when Z_r is sufficiently large, which is unfavorable for frequency modulation. Whereas, a smaller Z_r is also able to ensure a wide adjustable voltage range and a narrow frequency modulation range. Hence, Z_r needs to be minimized.

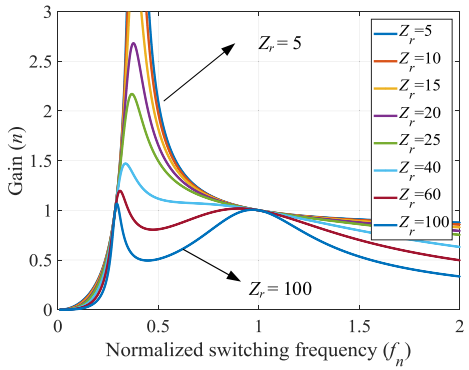

FIGURE 10. Curves of gain versus normalized switching frequency with different values of Z_r.

6) Select L_{r1} and C_{r1} based on the results in steps 4) and 5) as well as Eq. (6).

7) Calculate the accessible maximum and minimum voltage gains based on (4) to (8). If the voltage gain meets the design requirements, we move on to the next step. If not, we go back to step 4) to select a new k.

8) Select suitable L_1 and L_2 for the buck/boost converter. The inductance can be chosen as following,

$$L = (V_{bat,\max} - V_{UC}) \cdot \frac{V_{UC}}{V_{bat,\max}} \cdot f_{s,buck/boost} \cdot \frac{1}{LIR \cdot I_{UC,\max}} \tag{16}$$

where, V_{UC} is the terminal voltage of the UC bank, I_{UC} is the current of the UC bank, and LIR represents inductor-current ratio derived as a percentage of I_{UC}. An LIR value of 0.3 is a good tradeoff between load-transient response and conversion efficiency [19]. As discussed, all switches are able to achieve ZVS in CRM for PEV driving mode. However, considering half of the switches are in hard-switching conditions in CCM, $f_{s,buck/boost}$ is selected as the minimum f_s (switching frequency range of the CLLC converter) to ensure an overall high efficiency.

V. PROPOSED SR TECHNIQUE

A novel SR technique is proposed in this paper to reduce hardware cost, and to enhance the conversion efficiency. This technique calculates the ON time of the rectifier MOSFETs in advance and generates the corresponding gate signals. Taking the G2V mode as a case study, there are two different situations: a) operations at and below f_r; b) operations above f_r.

A. $f_s \le f_r$

Fig. 11 illustrates the theoretical waveforms when the CLLC converter operates at and below f_r. After a short dead time, MOSFETs S_1 and S_4 are turned on at t_0 and grid transfers the power through the transformer to the secondary rectification stage. During $[t_0 \sim t_1)$, i_{Lm} rises linearly while i_{r1} increases sinusoidally. On the secondary side, i_{S6} and i_{S7} are proportional to the difference between i_{r1} and i_{Lm}. When i_{r1} equals i_{Lm}, i_{S6} and i_{S7} become zero, and it indicates the end of resonance. $\Delta t_1 = t_2 - t_1$ is the duration between the

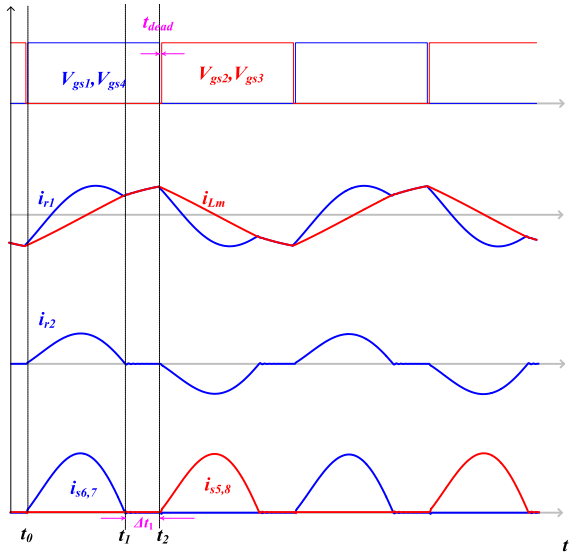

FIGURE 11. Theoretical waveforms of the bidirectional CLLC resonant converter when $f_s \leq f_r$.

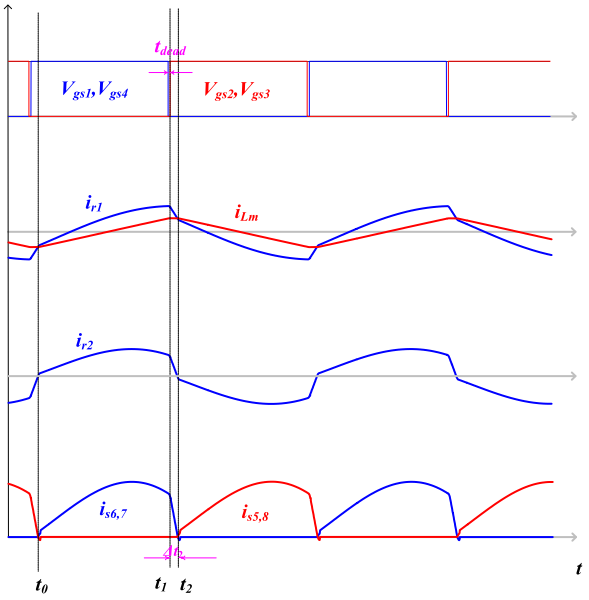

FIGURE 12. Theoretical waveforms of the bidirectional CLLC resonant converter when $f_s > f_r$.

endings of the secondary-side freewheeling and the primary control signals. When the converter operates at $f_s = f_r$, Δt_1 becomes zero. When the converter operates at $f_s < f_r$, $\Delta t_1 = (T_s - T_r)/2$, where T_s is the switching period and T_r is the resonance period.

Based on the above analysis, SR can be easily implemented when $f_s \leq f_r$. The secondary side MOSFETs should be turned on simultaneously with the primary side MOSFETs. For the turning-off instant, when $f_s = f_r$, the gate signal for the secondary side MOSFETs coincides with the primary side MOSFETs. However, when $f_s < f_r$, the conduction time of $S_5 \sim S_8$ during one switching period is still half of T_r. This means the secondary side MOSFETs should be turned off earlier than the primary side MOSFETs by $\Delta t_1 = (T_s - T_r)/2$.

B. $f_s > f_r$

Fig. 12 illustrates the theoretical voltage and current waveforms of the CLLC converter operating above f_r. The resonant current is continuous. Thus, the ON time for each rectifier switch is just half of the switching period. However, the secondary side rectifier switches should be turned on shortly after the turning-on of the primary-side MOSFETs. Hence, the calculation of the delay $\Delta t_2 = t_2 - t_1$ becomes crucial.

As shown, S_1 and S_4 start conducting before t_0. Then S_6 and S_7 start freewheeling at t_0. During $[t_0 \sim t_1)$, i_{Lm} increases linearly. i_{r1} and i_{r2} are sinusoidal, and i_{r1} is greater than i_{Lm}. According to the FHA model of the resonant tank (Fig. 4), the differential equations of the voltages and currents can be derived as,

$$\begin{cases} C_r \dfrac{du_c}{dt} = i_r \\ L_r \dfrac{di_r}{dt} + u_c = \dfrac{V_{dc,FHA} - V_{bat,FHA}}{2} \\ L_m \dfrac{di_{Lm}}{dt} = \dfrac{V_{dc,FHA} + V_{bat,FHA}}{2} \end{cases} \tag{17}$$

with the initial conditions of

$$\begin{cases} i_r(0) = i_r(t_0) \\ u_r(0) = u_r(t_0) \\ i_{Lm}(0) = i_{Lm}(t_0) \end{cases} \tag{18}$$

Hence, i_{r1}, i_{r2}, i_{Lm}, and voltages of the resonant capacitors (u_{c1} and u_{c2}) can are derived from (17) and (18) as,

$$\begin{cases} i_{r1}(t) = i_{r1}(t_0)\cos[2\pi f_r(t - t_0)] \\ + \dfrac{V_{dc,FHA} - V_{bat,FHA} - 2u_{c1}(t_2)}{2Z_r}\sin[2\pi f_r(t - t_0)] \\ i_{Lm}(t) = i_{Lm}(t_0) + \frac{V_{dc,FHA}+V_{bat,FHA}}{2L_m}(t - t_0) \\ i_{r2}(t) = i_{r1}(t) - i_{Lm}(t) \\ u_{c1}(t) = \dfrac{V_{dc,FHA} - V_{bat,FHA}}{2} + Z_r i_{r1}(t_0)\sin[2\pi f_r(t - t_0)] \\ + (u_{c1}(t_0) - \dfrac{V_{dc,FHA} - V_{bat,FHA}}{2})\cos[2\pi f_r(t - t_0)] \\ u_{c2}(t) = u_{c1}(t - \pi) \end{cases} \tag{19}$$

During $[t_1 \sim t_2)$, i_{r2} falls from a positive value to zero. The voltage across the secondary-side resonant inductor (u_{L2}) can be seen as constant. Hence, Δt_2 can be calculated by $i_{r2}(t_1)$, $i_{r2}(t_2)$, L_{r2}, and u_{L2}. At $t_1 = T_s/2 - \Delta t_2$, i_{r2}, and u_{L2} can be expressed as,

$$\begin{cases} i_{r2}(t_1) = i_{r1}(t_1) - i_{Lm}(t_1) \\ u_{L2} = \dfrac{V_{dc,FHA} + V_{bat,FHA}}{2} - V_{bat,FHA} - u_{C2}(t_1) \end{cases} \tag{20}$$

According to the voltage and current relationship of L_{r2}, Δt_2 can be calculated,

$$\frac{u_{L2}}{L_{r2}} \cdot \Delta t_2 = i_{r2}(t_1) - 0 \tag{21}$$

Therefore, when the CLLC resonant converter operates above f_r, there should be a delay of Δt_2 between the secondary and primary sides MOSFETs, while the ON time is identical.

The SR analysis of V2G mode is similar to that of G2V mode and is omitted here.

C. SR IMPLEMENTATION

Ideally, the turning-on and turning-off of the secondary-side MOSFETs should be strictly synchronized with the secondary-side rectifier current (i_s). However, circuit non-idealities might incur feedthrough issues. Therefore, redundancy control is necessary to secure a robust SR. As shown in Fig. 13, the MOSFET is turned on slightly after the calculated on-time, and is turned off slightly before the calculated off-time. The MOSFET body diode conducts during the redundancy time. It should be noted that this also facilitates a better ZVS on the secondary side MOSFETs.

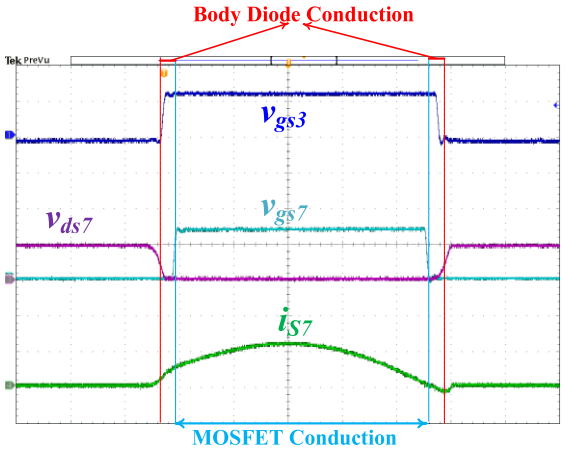

FIGURE 13. SR operation of the CLLC resonant converter.

To make a fair comparison, the proposed SR solution is compared with body diode solution and anti-parallel diode solution experimentally. For anti-parallel diode solution, there is a SiC Schottky diode in parallel with each MOSFET to act as a rectifier diode when the bridge is in rectification state. The specific results are shown in the following section.

VI. EXPERIMENTAL VALIDATION

A 1 kW experimental prototype is implemented and tested to verify the operating principle and the performances of the proposed PEI. Table 1 lists the design parameters of the prototype. The picture of the experimental test bench is shown in Fig. 14. The input voltage is generated by a dc power supply. The battery pack in G2V mode and grid side dc link in V2G mode are emulated by a programmable dc electronic load (Chroma Model 63212). Parallel arrays of large electrolytic capacitors are utilized to emulate the UC bank. The control algorithm is implemented in TMS320F28379D from Texas Instruments. All the three working modes are tested.

TABLE 1. Design parameters.

Parameter	Symbol	Quantity
DC voltage	V_{DC}	390V
Battery voltage	V_{bat}	250 ~ 420V
Rated power	P_{max}	1 kW
Resonant inductor	L_{r1}, L_{r2}	62μH, 44μH
Resonant capacitor	C_{r1}, C_{r2}	44nF, 62nF
Magnetizing inductor	L_m	350μH
Resonant frequency for CLLC	f_r	95kHz
Switching frequency for CLLC	f_s	60 ~ 140kHz
Transformer turns ratio	n	1.2
Dead time	t_{dead}	50ns
Switching frequency for interleaved buck/boost converter	$f_{s,buck/boost}$	60kHz
Inductance for interleaved converter	L_1, L_2	620μH
MOSFET	S_1~S_8	C3M0120090D
Schottky diode in parallel (test for comparison)	D_1~D_8	C3D10060A

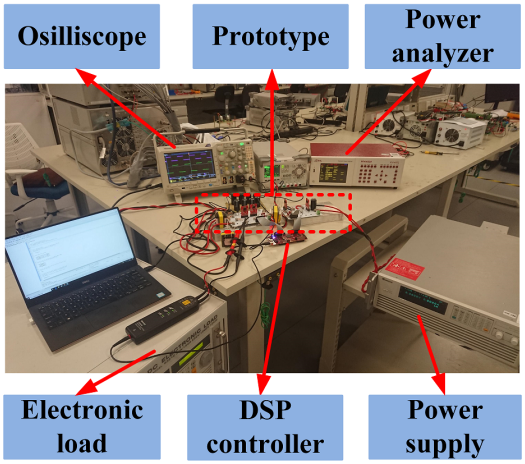

FIGURE 14. Experimental test bench.

A. G2V MODE

Critical steady-state waveforms in G2V mode are illustrated in Figs. 15-17. Fig. 15 shows v_{gs3}, v_{ds3}, i_s and the output voltage (v_{bat}) at f_r. As shown, the output voltage is 315V. It is obvious that the MOSFET realizes ZVS during its turning-on process. Furthermore, reverse recovery is mitigated in the turning-off process of $S_5 \sim S_8$. This is because there is no

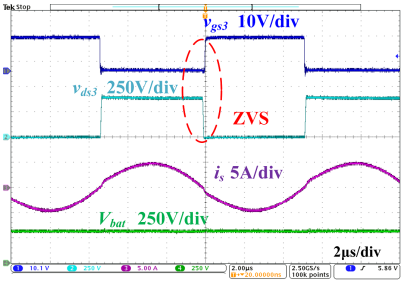

FIGURE 15. Experimental waveforms of v_{gs3}, v_{ds3}, the transformer secondary side current i_s and the output voltage v_{bat} in G2V mode when f_s = 95kHz.

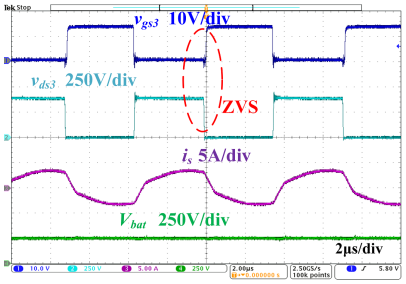

FIGURE 16. Experimental waveforms of v_{gs3}, v_{ds3}, the transformer secondary side current i_s and the output voltage v_{bat} in G2V mode when $f_s = 140$kHz.

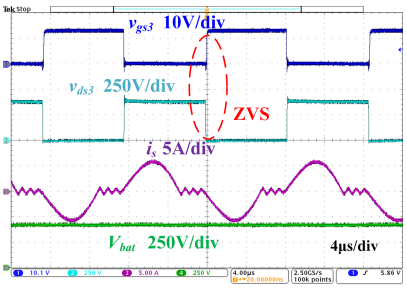

FIGURE 17. Experimental waveforms of v_{gs3}, v_{ds3}, the transformer secondary side current i_s and the output voltage v_{bat} in G2V mode when $f_s = 60$kHz.

steep change of i_s, which ensures ZCS turning-off of the body diode. Hence, soft commutation is achieved for all the switches, and the switching loss is minimized significantly. Similar experimental waveforms of the converter operating at 140kHz and 60kHz are depicted in Figs. 16 and 17, respectively. It is shown that v_{bat} at 140kHz is 250V while the voltage at 60kHz is 420V. Thus, the designed prototype is able to charge a 250V∼420V battery pack by modulating f_s within [60 kHz, 140 kHz].

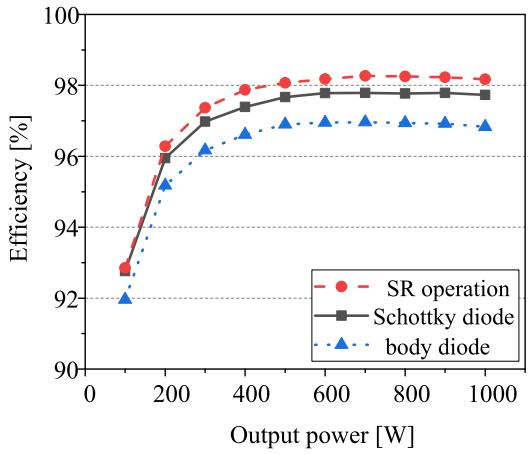

FIGURE 18. Efficiency comparison of the CLLC converter in G2V mode.

A high-precision power analyzer (N4L PPA4530) is utilized to measure the efficiency data. Fig. 18 depicts the curves of the efficiency versus output power with 390V input voltage and 315V output voltage. Using the proposed SR technique, a 98.27% peak efficiency is captured at 700W. Compared with body diode solution, a maximum 1.34% efficiency improvement is observed. Compared with the anti-parallel Schottky diode solution, a maximum 0.48% efficiency improvement is observed.

B. V2G MODE

In V2G mode, the input voltage varies from 250V to 420V while the output voltage is fixed at 390V. The experimental steady-state waveforms are shown in Figs. 19-21. Fig. 19 shows v_{gs7}, v_{ds7}, the secondary-side MOSFET current (i_{S3}) and the output voltage (V_{DC}) at f_r with 336V input voltage and 390V output voltage. As illustrated, ZVS is realized during the turning-on process of the MOSFETs and

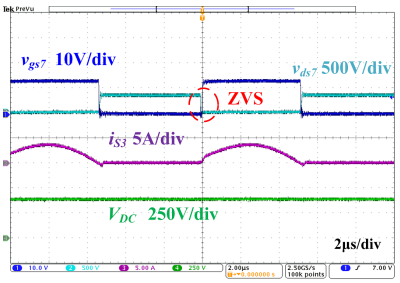

FIGURE 19. Experimental waveforms of v_{gs7}, v_{ds7}, the transformer secondary side MOSFET current i_{S3} and the output voltage v_{DC} in V2G mode when $f_s = 95$kHz.

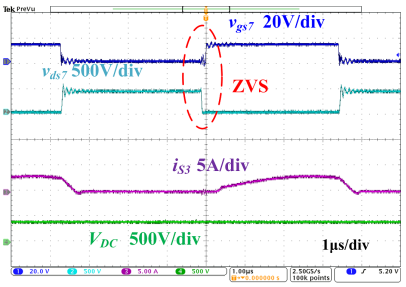

FIGURE 20. Experimental waveforms of v_{gs7}, v_{ds7}, the transformer secondary side MOSFET current i_{S3} and the output voltage v_{DC} in V2G mode when $f_s = 140$kHz.

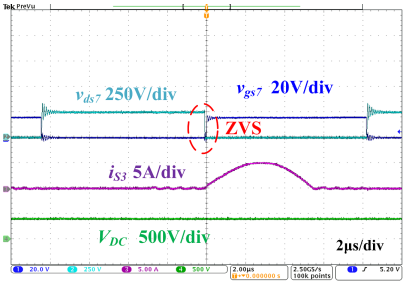

FIGURE 21. Experimental waveforms of v_{gs7}, v_{ds7}, the transformer secondary side MOSFET current i_{S3} and the output voltage v_{DC} in V2G mode when $f_s = 60$kHz.

ZCS is achieved during the turning-off of the body diodes. Figs. 20 and 21 illustrate the voltage and current waveforms of the prototype operating at 140kHz and 60kHz, respectively. In Fig. 20, the input voltage is 420V. While in Fig. 21, the input voltage is 250V. As shown, the designed prototype is able to maintain a 390V output voltage by modulating f_s within [60 kHz, 140 kHz].

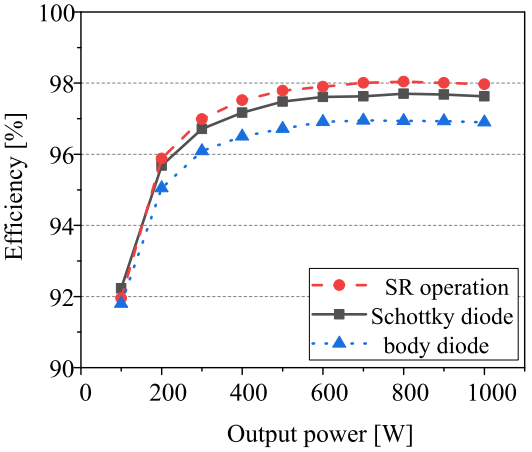

FIGURE 22. Efficiency comparison of the CLLC converter in V2G mode.

Fig. 22 plots curves of the measured efficiency versus the output power under 336V input voltage and 390V output voltage. Using the proposed SR technique, the prototype demonstrates 98.04% peak efficiency at 800W. Compared with body diode solution, a maximum 1.07% efficiency improvement is observed. Compared with the anti-parallel Schottky diode solution, a maximum 0.38% efficiency improvement is observed.

C. PEV DRIVING MODE

In PEV driving mode, the interleaved buck/boost converter works either in buck mode or boost mode. In each mode, based on the design parameters, the converter works in CRM in low power condition while in CCM in high power condition. Figs. 23-25 illustrate the critical waveforms of the interleaved converter working in buck mode. As shown, all the switches can realize ZVS in CRM while the rectifier switches can realize ZVS in CCM. Similar results are observed for the interleaved converter operating in boost mode, as illustrated in Figs. 26-28.

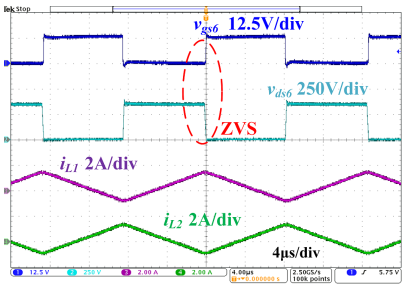

FIGURE 23. Interleaved buck converter: v_{gs6}, v_{ds6}, i_{L1} and i_{L2} in CRM.

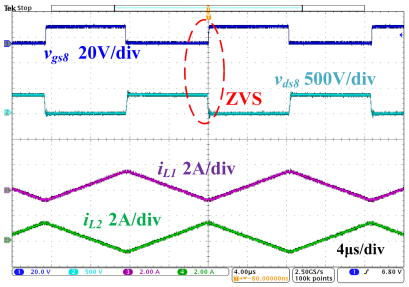

FIGURE 24. Interleaved buck converter: v_{gs8}, v_{ds8}, i_{L1} and i_{L2} in CRM.

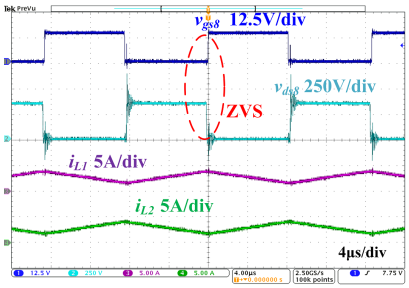

FIGURE 25. Interleaved buck converter: v_{gs8}, v_{ds8}, i_{L1} and i_{L2} in CCM.

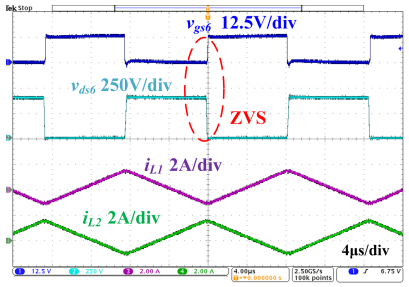

FIGURE 26. Interleaved boost converter: v_{gs6}, v_{ds6}, i_{L1} and i_{L2} in CRM.

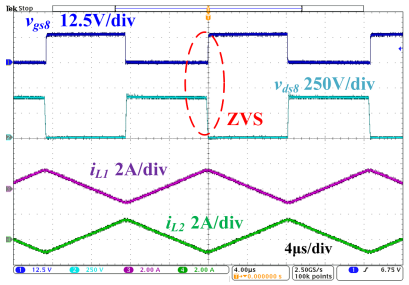

FIGURE 27. Interleaved boost converter: v_{gs8}, v_{ds8}, i_{L1} and i_{L2} in CRM.

The measured efficiency of the buck/boost converter is captured in Fig. 29. It is seen that a 98.56% peak efficiency in buck mode and a 98.43% peak efficiency in boost mode are reported.

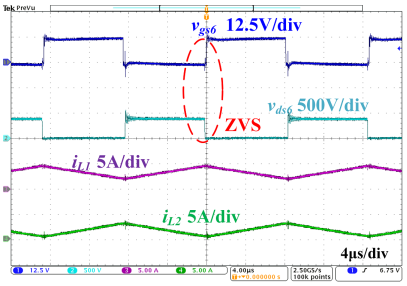

FIGURE 28. Interleaved boost converter: v_{gs6}, v_{ds6}, i_{L1} and i_{L2} in CCM.

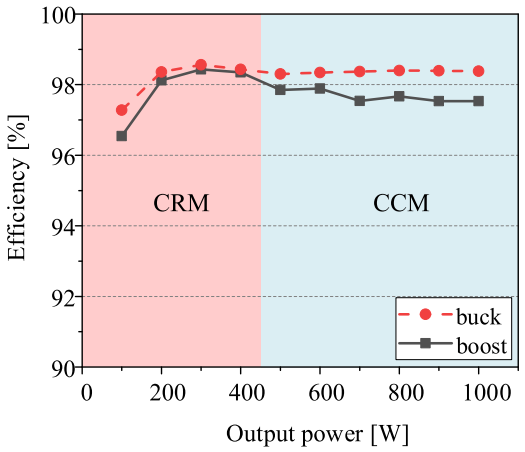

FIGURE 29. Measured efficiency versus output power in PEV driving mode.

VII. CONCLUSION

In this paper, a novel multifunctional PEI is proposed for hybrid energy management systems of PEVs. This PEI integrates the full-bridge CLLC resonant topology and the interleaved synchronous buck/boost topology. The proposed PEI achieves all the three operation modes of PEVs: G2V, V2G, and PEV driving. It brings advantages including a) ZVS for the primary switches and ZCS for the rectifier switches under G2V and V2G modes; b) a wide adjustable output voltage range with frequency modulation for battery charging and discharging; c) improved efficiency and reduced hardware cost due to merged structure and the innovative SR technique; and d) multiple operation functions.

Optimal parameter design procedures are presented to facilitate the design process. A 1 kW experimental prototype is tested for all the three operation modes. The prototype demonstrates peak efficiency of 98.27% in G2V mode, 98.04% in V2G mode, 98.56% in PEV driving mode and good overall efficiency performances. Finally, two other sets of experiment are also conducted for comparison. The comparison verifies the effectiveness of the SR technique. It is reported that the efficiency is improved effectively by incorporating the proposed SR technique.

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XIAOYING LU (S'17) was born in China, in 1994. She received the B.S. degree (Hons.) in microelectronics from the Chongqing University of Posts and Telecommunications, Chongqing, China, in 2016. She is currently pursuing the M.S. degree in power electronics with ShanghaiTech University, Shanghai, China.

She was an IC Validation Engineer Intern with Freescale Semiconductor Limited, Shanghai, China, in 2015. Since 2016, she has been a Graduate Research Assistant with the Power Electronics and Renewable Energies Laboratory, ShanghaiTech University. Her current research interests include power electronics, plug-in electric vehicles, resonant dc/dc converters, and power management of hybrid energy storage systems.

HAOYU WANG (S'12–M'14–SM'18) received the bachelor's degree (Hons.) from Zhejiang University, Hangzhou, China, and the master's and Ph.D. degrees in electrical engineering from the University of Maryland at College Park, College Park, MD, USA.

He is currently a Tenure-Track Assistant Professor with the School of Information Science and Technology, ShanghaiTech University, Shanghai, China. His research interests include power electronics, plug-in electric and hybrid electric vehicles, the applications of wide bandgap semiconductors, renewable energy harvesting, and power management integrated circuits.

Dr. Wang is an Associate Editor of the IEEE TRANSACTIONS ON TRANSPORTATION ELECTRIFICATION, and a Guest Associate Editor of *CPSS Transactions on Power Electronics and Applications*.