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A Novel VLSI Architecture for Multi-Constellation and Multi-Frequency GNSS Acquisition Engine

YUHENG YANG[1,2], XIAOHUI BA[1,2], AND JIE CHEN[1]
[1]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing 100029, China
[2]University of Chinese Academy of Sciences, Beijing 100049, China

Corresponding author: Jie Chen (jchen@ime.ac.cn)

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ABSTRACT This paper proposes a novel VLSI architecture of GNSS acquisition engine based on short-time correlation combined with an FFT scheme. The architecture supports multi-constellation systems and multi-frequency satellite signals flexibly by the manner of time-division multiplexing. The supported signals include GPS, BDS, GLONASS, GALILEO, QZSS, IRNSS, and SBAS. Compared with other direct acquisition structures, the search efficiency of the acquisition engine is improved by using the IF playback structure. Based on the characteristics of L1C and B1C signal spread spectrum codes, an efficient generation method and the circuit structure of Legendre sequence which is compatible with L1C and B1C spread spectrum codes are proposed. It can effectively reduce the die area of the spread spectrum code generator and the generation time of the L1C/B1C spread spectrum code. Combining with the acquisition scheme adopted in this paper, the structure of the short-time correlators' array is optimized, and the maximum clock frequency of the acquisition engine is significantly improved. The acquisition engine proposed in this paper is implemented in a 55-nm CMOS technology. The system occupied a silicon area of 2.1 mm^2 and consumes only 72.02-mW power while realizing the maximum clock frequency at about 333.33 MHz.

INDEX TERMS GNSS, acquisition, multi-constellation, multi-frequency, VLSI.

I. INTRODUCTION

Global Satellite Navigation System (GNSS) has been widely used in various fields. Multi-constellation GNSS receivers can provide more observation information especially in more complex urban road conditions. It can provide a better positioning accuracy, availability and reliability compared with single-constellation GNSS receivers [1]–[4]. Making full use of the redundant information of multi-constellation multi-frequency satellite signals can enhance the robustness and anti-jamming ability of GNSS [5]. Therefore, multi-constellation multi-frequency GNSS receivers have become an active research area in recent years.

The acquisition engine is the key part in a GNSS receiver design. Reference [6] analyzes the influence of the search efficiency and compatibility of the acquisition engine on the performance of high-precision multi-constellation multi-frequency GNSS receiver. However, it would directly deteriorate the positioning accuracy, the real-time performance and the compatibility of the GNSS receivers. Therefore, we mainly focus on optimizing the real-time performance and the compatibility of the GNSS acquisition engine.

Reference [7] presents a real-time GNSS software receiver architecture. The architecture can support GPS, GLONASS, GALILIEO and SBAS constellation signals, and realize the data acquisition function by using the FPGA. It is necessary to rely on high-performance CPU to ensure the real-time performance of the system.

Reference [8] illustrates a software receiver that is compatible with GPS, GLONASS and GALILIEO systems. It has implemented up to 100 physical correlators using FPGA to improve the acquisition efficiency of the software receiver. Compared with [7], the searching speed is improved. However, the acquisition process of satellite signals requires software support, the GNSS receiver

topology still needs 35.09ms to search a GPS L1C/A satellite. In the case of searching for multiple satellite signals, the search efficiency is very low and is not comparable with the acquisition engine of the hardware architecture.

TABLE 1. The signal types supported by the acquisition engine architecture proposed.

Constellations	Frequency point	Signal	Carrier frequency (MHz)	Modulation mode	Code rate (Mbps)
GPS	L1	L1 C/A	1575.42	BPSK	1.023
		L1C		BOC	
	L2	L2C	1227.6	TDM	1.023
	L5	L5 I	1176.45	QPSK	10.23
		L5 Q			
GLONASS	L1	L1OF	1602	BPSK	0.511
		L1OC	1600.995	TDM	0.511
	L2	L2OF	1246	BPSK	1.023
		L2OC	1248.060	TDM	1.023
	L3	L3OC	1202.025	QPSK	10.23
IRNSS	L5	SPS	1176.45	BPSK	1.023
	S	SPS	2492.028	BPSK	
SBAS	L1	L1C/A	1575.42	BPSK	1.023
QZSS	L1	L1 C/A	1575.42	BPSK	1.023
		L1C		BOC	
		L1-SAIF		BPSK	
	L2	L2C	1227.6	BPSK	
	L5	L5-I	1176.45	QPSK	10.23
		L5-Q			
BDS	B1	B1I	1561.098	BPSK	2.046
	L1	B1C	1575.42	BOC	1.023
	B2	B2I	1207.14	BPSK	2.046
	L5	B2a	1176.45	QPSK	10.23
	B3	B3I	1268.52	BPSK	
GALILEO	E1	E1-B	1575.42	CBOC	1.023
		E1-C			
	E5	E5a	1176.45	QPSK	10.23
		E5b	1207.14	QPSK	10.23

In order to ensure the real-time performance of GNSS receiver. A reconfigurable ASIC architecture acquisition engine is designed in [9], which is compatible with GPS/GLONASS dual system and L1/L2 dual-frequency point. However, the proposed solution is focused on RF front-end, so that the acquisition engine in the receiver cannot extend its support for other signals.

Different from the ASIC architecture, FPGA has better flexibility. Reference [10] takes full advantage of the reconfigurable structure of FPGA. They proposed a BDS/GPS dual-mode GNSS receiver based on FPGA. The overall acquisition engine is implemented by hardware and real-time performance of the system is improved. Nevertheless, the contents of the on-chip spread spectrum code RAM of FPGA still need to be modified in order to extend the satellite signal of other constellation systems. Moreover, compared with ASIC architecture, the maximum operating frequency of the similar circuit structure is lower due to the redundant structure of reconfigurable FPGA.

Considering the similarity of satellite signals in different constellation systems, this paper proposes a VLSI architecture of compatible multi-constellation multi-frequency GNSS acquisition engine based on short-time correlation and FFT scheme. This novel architecture is implemented by time-division multiplexing with flexible parameter configuration without additional hardware overhead. To support a variety of satellite signals, the satellite signal supported by the proposed acquisition engine in this paper are listed in TABLE 1. In order to improve the search efficiency of the acquisition engine, an IF playback structure is adopted to ensure that the acquisition engine can work at the frequency of higher than the sampling rate. Furthermore, the circuit structure of the acquisition engine is optimized. Compared with other structures, the capture engine used in this paper has less hardware resource requirements and higher search efficiency. The rest of the article is organized as follows:

The second section describes the short-time correlation plus FFT acquisition algorithm, analyzes the characteristics of the multi-constellation systems and the

multi-frequency signals. The hardware architecture is given. In the third section, we present a hardware architecture of the spread spectrum code generator in the acquisition engine by analyzing the generation mode of the spread spectrum code of each frequency point signal and constellation system. Then, a fast generation method and hardware structure of the Legendre sequence according to the generation characteristics of the spread spectrum code of L1C and B1C signals is raised in this section as well. In the fourth section, the structure of the coherent integration circuit in acquisition engine and the data flow between the coherent integration and non-coherent integration phase is analyzed. In order to improve the search efficiency of acquisition engine, an optimization method and the specific hardware structure of short-time correlation array are proposed. Finally, the VLSI implementation results of the acquisition engine designed in this paper and the comparison with other state-of-arts are given in the fourth section.

II. ARCHITECTURE DESIGN OF MULTI-CONSTELLATION AND MULTI-FREQUENCY POINT ACQUISITION ENGINE

All the satellite signals listed in Table 1 can be divided into four types in regards to modulation scheme: BPSK modulation signal, BOC modulation signal, TDM modulation signal, and QPSK modulation signal. BSPK modulation signal can be expressed by formula (1), A indicating signal amplitude, $D(t)$ indicating navigation message, $c(t)$ indicating spread spectrum code, f_c indicating carrier frequency, $n(t)$ indicating Gaussian white noise.

$$r(t) = AD(t)\,c(t)\cos(2\pi f_c t) + n(t) \tag{1}$$

In this paper, the acquisition method of short-time correlation combine with FFT is adopted. The short-time correlation results of section k can be expressed by formula (2). L is the total number of segments, assuming the total coherent integration time is T_A, then the short-time coherent integration time is $T_{coh} = T_A/L$, M is the number of sampling points of each segment, then the short-time coherent period is $T_s = T_{coh}/M$, I_k, Q_k are the in-phase component and the orthogonal component of the signal. Δf is the difference between the local carrier frequency and signal carrier frequency.

$$\begin{aligned} I_k + jQ_k &= \sum_{i=kM}^{i=kM+M-1} r(iT_s)\,c(iT_s)\exp(j2\pi f_L iT_s) \\ &= \frac{A\sin(\pi\Delta fMT_s)}{2\sin(\pi\Delta fT_s)}\exp(j\pi\Delta f\,(2kM+M-1)\,T_s) \end{aligned} \tag{2}$$

After the short-time correlation operation, the result of L segment is computed by FFT. The number of points for FFT analysis is N ($N \geq L$), which is used to calculate the absolute value of FFT. The absolute value of the spectral line m in the FFT result can be expressed in formula (3):

$$\begin{aligned} M(m) &= \left|\sum_{k=0}^{L-1}(I_k + jQ_k)\exp\left(j\frac{2\pi nk}{N}\right)\right| \\ &= \frac{A}{2}\left|\frac{\sin(\pi\Delta fMT_s)}{\sin(\pi\Delta fT_s)}\frac{\sin\left(\pi\Delta fLMT_s - \frac{\pi mL}{N}\right)}{\sin\left(\pi\Delta fMT_s - \frac{\pi m}{N}\right)}\right| \end{aligned} \tag{3}$$

Non-coherent accumulation of FFT results can further improve the acquisition performance. The maximum value of the spectral line m corresponds to the deviation of the true frequency. The Doppler frequency can be expressed by formula (4). The frequency acquisition range is $[-1/2T_{coh}, 1/2T_{coh}]$ and the resolution is about $1/(NT_{coh})$ Hz.

$$\Delta f = \frac{1}{MT_s}\frac{m}{N} = \frac{m}{T_{coh}N} \tag{4}$$

The BOC modulation signal can be expressed as formula (5) with data channel and pilot channel included in the signal. To be specific, the subscript D represents data channel, subscript P represents pilot channel and $O(t)$ represents quadratic code.

$$\begin{aligned} r(t) = {} & A_D D(t)\,c_D(t)\,sign(\sin(2\pi f_{sc}t))\cos(2\pi f_c t) \\ & + A_P O(t)\,c_P(t)\,sign(\sin(2\pi f_{sc}t))\cos(2\pi f_c t) + n(t) \end{aligned} \tag{5}$$

The expression of the data channel and the pilot channel in Formula (5) is like Formula (1). BPSK-like acquisition scheme can be used to search the upper and lower side-bands in the manner of time division multiplexing. After the acquisition of the pilot channel, the data channel can be captured and the results of the two acquisitions can be non-coherent product to achieve full utilization of signal energy. In the acquisition process, BOC (6,1) component is not considered, but BOC (1,1) component is captured. The pilot channel can be approximated by formula (6):

$$\begin{aligned} r_P(t) \approx {} & A_P O(t)\,c_P(\sin(2\pi\,(f_{sc}+f_c)\,t) \\ & - \sin(2\pi\,(f_c - f_{sc})\,t))\,n(t) \end{aligned} \tag{6}$$

Data channels can also be calculated in a form like Formula (1), so that the BPSK acquisition schemes can be used for the BOC modulation signals to improve the compatibility of the acquisition engine.

Although TDM modulation signal belongs to BSPK signal, it uses CM code and CL code multiplexing method. It can be expressed by formula (7) and (8), n is a non-negative integer.

$$r(t) = Ac'(t)\cos(2\pi f_c t) + n(t) \tag{7}$$

$$c' = \begin{cases} c_L(t) & (2n+1)\,T_c \leq t \leq (2n+2)\,T_c \\ D(t)\,c_M(t) & (2n)\,T_c \leq t \leq (2n+1)\,T_c \end{cases} \tag{8}$$

In equation (7), RZ-CM (Return-to-Zero Civil-Moderat) code acquisition strategy is considered as TDM modulated signals. Since the acquisition engine designed in this paper

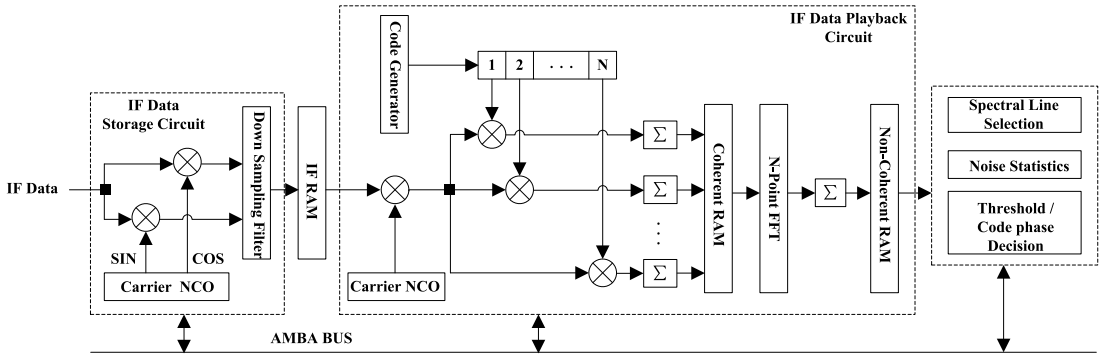

FIGURE 1. Proposed hardware architecture of multi-constellation and multi-frequency GNSS acquisition engine.

captures CM code, it can also capture TDM modulated signals by BPSK acquisition scheme.

QPSK modulation signal can be expressed as formula (9), similar to BOC modulation and TDM modulation signal, and can also be divided into data channel and pilot channel similar to formula (1), so QPSK modulation signal can also use BPSK modulation signal acquisition scheme.

$$r(t) = A_D D_D(t) c_D(t) \cos(2\pi f_c t) + A_P D_P(t) c_P(t) \sin(2\pi f_c t) + n(t) \quad (9)$$

In summary, the acquisition engine architecture proposed in this paper can support BPSK, BOC, TDM and QPSK modulated signals by time division multiplexing (TDM) without increasing hardware resources through the acquisition scheme of BSPK modulated signals. And the IF data playback method is used to acquisition the signal. The hardware architecture of the acquisition engine proposed in this paper is shown in Figure 1, and its work flow is summarized as follows:

(1) IF data are filtered out of band noise by anti-aliasing filter, and the filtered data are stored in IF RAM array according to the sampling frequency of the signal.

(2) After the IF data storage is completed, the data in the IF RAM is replayed by the playback module at a high speed to the short-time correlator array for coherent integration operation, and the results of short-time correlation are stored in coherent RAM array.

(3) When the coherent integration stage is completed, the short-time correlation results are sent to the N point FFT unit, and the non-coherent integration results are stored in the non-coherent RAM array.

(4) After the non-coherent accumulation, the maximum of the first K lines are located and the noise background is counted. The decision module makes decisions according to the maximum of the first K lines and offset of the frequency in corresponding chip, noise background and playback start time.

The acquisition engine proposed in this paper can receive the flexible configuration of the processor through AMBA bus to adapt to the different carrier frequency and code rate of each satellite signal in Table 1. The circuit structure of IF data playback allows the acquisition engine to work at a frequency much higher than the signal sampling rate during the acquisition phase. If the data sampling rate is f_s and the data playback rate is f_{re}, the working frequency of the playback acquisition engine is f_{re}/f_s times of the sampling rate. When the satellite signals of multiple constellation systems at the same frequency are searched, the search efficiency of acquisition will be improved.

III. ARCHITECTURE DESIGN OF THE SPREAD SPECTRUM CODE GENERATOR

In order to support all the satellite signals in Table 1, the spread spectrum codes of each satellite signal in Table 1 can be grouped into three categories according to the mode of generation:

The first type of satellite signal code generator is polynomial structure, such as GPS L1C/A, L2C, L5 signals, GLONASS L1OF, L1OC, L2OF, L2OC, L3OC signals, IRNSS SPS signals, QZSS L1C/A, L1-SAIF, L2C, L5 signals, SBAS L1 signals, GALIO E5a, E5b signals and BDS B1I, B2I, B2a, B3I signals. Taking the GPS L1C/A signal as an example, the generating polynomial of its spreading code is:

$$G(x) = G_1(x) + G_2(x) \quad (10)$$

$$G_1(x) = 1 + x^3 + x^{10} \quad (11)$$

$$G_2(x) = 1 + x^2 + x^3 + x^6 + x^8 + x^9 + x^{10} \quad (12)$$

The difference of this kind of signal spread spectrum code generation mode is only that the code length and tap are different. The circuit structure of code generator can be realized by shift register. The spread spectrum code of the second kind of satellite signal is given in the form of Memory Code. The spread spectrum code can only be pre-stored in the local ROM CODE. This kind of signal also includes Galileo E1 signal.

The generation of spread spectrum codes for the third kind of satellite signals is more complex, and it needs to rely on Legendre sequence to generate corresponding spread spectrum codes. Such signals include GPS L1C signal and BDS B1C signal. Taking GPS L1C signal as an example,

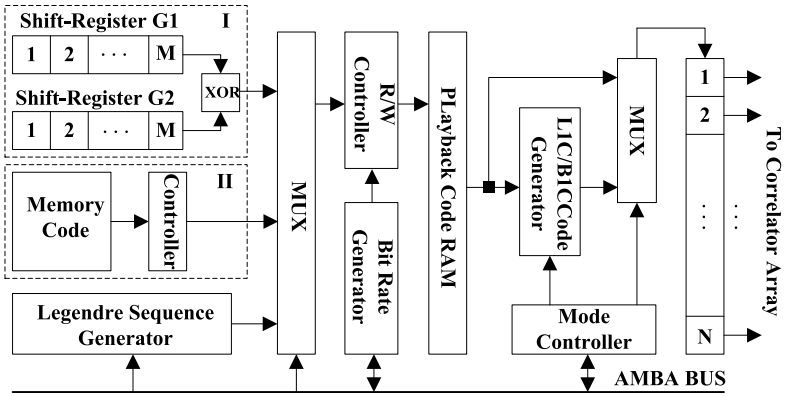

FIGURE 2. Proposed hardware architecture of the spread spectrum code generator.

the generation method of spread spectrum code [11]: 7-bit fixed sequence '0110100' is inserted into Weil code generated by Legendre sequence, and the insertion position is p, $p \in [1, 10223]$. The Legendre sequence can be expressed by formula (13):

$$L(n) = \begin{cases} 0, & n = 0 \\ 1, & \text{existence of integer } x, \quad k = x^2 \bmod N \\ 0, & \text{otherwise} \end{cases} \tag{13}$$

For GPS L1C signal and BDS B1C signal, the calculation first needs to determine the value range of x, assuming that $x = A * N + B$, A is an integer, $B \in [0, N-1]$, the result of $B^2 \bmod N$ can be expressed as:

$$\begin{aligned} x^2 \bmod N &= (A * N + B)^2 \bmod N \\ &= \left((A * N)^2 + 2(A * N * B) + B^2\right) \bmod N \\ &= B^2 \bmod N \end{aligned} \tag{14}$$

If $b \in [0, (N-1)/2]$, then B^2 modular division operation on N can be expressed in formula (15) when $B = b$.

$$B^2 \bmod N = b^2 \bmod N \tag{15}$$

If $B = N - b$, the result of $B^2 \bmod N$ can be expressed as:

$$B^2 \bmod N = (N-b)^2 \bmod N = b^2 \bmod N \tag{16}$$

The formula (15) and formula (16) is concede with the results, the range of x is $[0, (N-1)/2]$, This means that the value of each $L(n)$ is computed, according to formula (13), the square operation of $(N-1)/2$ times and the remainder operation of $(N-1)/2$ times are required.

In order to support the above three types of satellite signals, we designed a architecture of spread spectrum code generator, which is compatible with multi-frequency signals and multi-constellation system, and the playback method is adopted in the architecture of the code generator to ensure the synchronization of spread spectrum code and high speed playback IF data in the searching phase of acquisition engine. The hardware architecture is shown in Figure 2. The shift register G1/G2 supports the first type of satellite signal by time division multiplexing and the Memory Code supports the second type of satellite signal. The Legendre sequence generator supports the third type of satellite signal, and the L1C/B1C code generator in Figure 2 only performs XOR operation and inserts a fixed sequence into Weil code. Its work flow can be summarized as follows:

1) According to the working mode of the processor configuration, the code generator generates the spread spectrum code needed in the acquisition process and writes it into the playback local code RAM.
2) Read the code data in the playback code RAM and move the spread spectrum code data sequentially into the N bits code register to complete the initialization phase, N is same as the number of physical short-time correlation branches.
3) In the playback stage of the acquisition engine, the spread spectrum code is read from the local code RAM and shift into the N bits code register according to the corresponding code rate sequence, and the short-time correlation operation is performed with the playback IF data.

From the above analysis, it can be seen that the generator of the spread spectrum code for the first and second kind of signals is relatively simple, but the length of the Legendre sequence code required for the generation of the spread spectrum code for the third type of signals is very long. Therefore, it is difficult to calculate the Legendre sequence directly according to the formula (13) (15) (16) to meet the real-time requirements of the acquisition engine, additional square operation and modular division operation are required. Reference [12] by introducing the quadratic reciprocity law, the calculation of Legendre sequence can be split, which can reduce the computation time by half. Taking GPS L1C signal as an example: Computing all $L(n)$ requires $[(N-1)/2]^2/2 = 13061160$ times square operation and remainder operation, $N = 10223$. The amount of computation is still very large, which cannot meet the real-time requirements of the acquisition engine. Moreover, the method proposed in [12] still needs modular division operation, which will greatly increase the hardware area

of the system for the hardware architecture of acquisition engine.

In order to ensure the real-time performance of the acquisition engine, [7] and [13] use a code RAM to support GPS L1C and BDS B1C signals. In the searching phase, the Legendre sequence is read directly from code RAM to generate spread spectrum code. This method does not need to compute Legendre sequence, and can effectively solve the real-time problem of acquisition engine, but the method requires additional RAM resources. For the acquisition engine compatible with L1C and B1C signals, two block code RAM of Legendre sequences of L1C and B1C signals need to be stored separately.

In order to reduce the hardware cost of acquisition engine and the computational complexity of Legendre sequence, we present an efficiently method for generating Legendre sequences and the corresponding hardware architecture. This method can support GPS L1C signals and BDS B1C signals by time division multiplexing through parameter configuration. It does not require additional memory resources and avoids square and modular division operation by combining the characteristics of playback code generator, and the computational complexity can be greatly reduced for Legendre sequences. The method proposed no longer solves every $L(n)$, but finds all $L(n) = 1$ positions according to the value range of x. It transforms the problem of Legendre sequence calculation into the problem of calculating the modular division result of $k(n) = x^2 \bmod N$.

For $x \in [0, (N-1)/2]$, according to $k(n) = x^2 \bmod N$, the $k(n)$ is the location of $L(n) = 1$.

Set $X(n) = a*N+b$, $X(n+1) = X(n)+1$ and $X(n) \in [0, (N-1)/2]$ Formula(17) can be obtained:

$$\begin{aligned} &X(n) \bmod N \\ &= (a*N+b) \bmod N = b \bmod N \end{aligned} \tag{17}$$

$$\begin{aligned} &X(n+1) \bmod N \\ &= (X(n)+1) \bmod N \\ &= (a*N+b+1) \bmod N = (b \bmod N)+1 \end{aligned} \tag{18}$$

$$\begin{aligned} &X^2(n) \bmod N \\ &= (a*N+b)^2 \bmod N \\ &= \left[(a*N)^2 + 2ab*N + b^2\right] \bmod N = b^2 \bmod N \end{aligned} \tag{19}$$

$$\begin{aligned} &X(n+1)^2 \bmod N \\ &= (a*N+b+1)^2 \bmod N \\ &= \left[(a*N)^2 + 2a(b+1)*N + (b+1)^2\right] \bmod N \\ &= (b+1)^2 \bmod N = \left[\left(b^2+2b\right) \bmod N\right] + 1 \end{aligned} \tag{20}$$

According to formula (17) (18) can be obtained by formula (21):

$$X(n+1) \bmod N = (X(n) \bmod N) + 1 \tag{21}$$

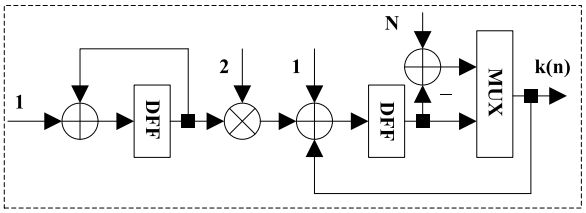

FIGURE 3. Proposed hardware structure of the Legendre sequence generator.

According to formula (17) (18) can be obtained by formula (22):

$$\begin{aligned} X^2(n+1) \bmod N = &\left(X^2(n) \bmod N\right) \\ &+ 2*(X(n) \bmod N) + 1 \end{aligned} \tag{22}$$

According to formula (21) (22), all the results of $X^2(n) \bmod N$ can be obtained by recurrence formula, and all the computational cycles required by formula (22) can be calculated as $(N-1)/2$. Considering the overflow problem in the recursive process, when the modular division result of $X^2(n) \bmod N$ is greater than $N-1$, the value of $k(n)$ needs to be updated to $N-k(n)$. All computational procedures only require addition, subtraction, shift operations, without any square and modular division operation. The corresponding hardware structure is shown in Figure 3.

The hardware structure in Figure 3 only contains registers, adders, and gates, which not require additional memory resources, reduce the hardware cost, and do not need square and modular division circuit units, and also reduce the computational complexity compare with [12], which result in improving of the real-time performance for the acquisition engine. And by configuring different N values, it can support GPS L1C signals and BDS B1C signals flexible.

IV. OPTIMIZATION OF CORRELATOR ARRAY CIRCUIT STRUCTURE

The correlator array is an important part in the acquisition engine architecture. Especially for the hardware architecture, the speed and structure of the correlator array circuit determines the number of equivalent correlators and the search efficiency for searching satellite signals. In the design of VLSI architecture, we need to consider the performance, area and other aspects of the circuit. Reference [14] compared a variety of acquisition engine architecture based on FPGA. The hardware architecture of acquisition engine proposed by Shivaramaiah et al.is, compared with other schemes, RAM is used to replace registers to save coherent integration results. When the number of correlator branches is large, the circuit area of the acquisition engine can be significantly reduced. The hardware architecture is shown in figure 4.

In Figure 4, multiplexers are used as the data path between the correlator array and the coherent RAM. As the number of the physical correlator branches increases, the number and logic depth of the gates increase, the circuit performance of the acquisition engine will be lost. Taking the two-input

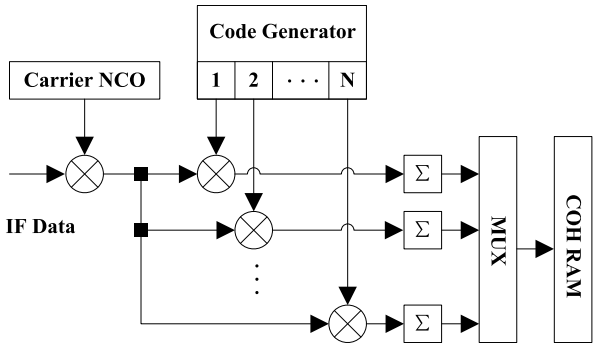

FIGURE 4. Correlator structure proposed in [14].

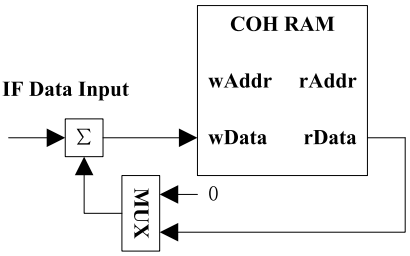

FIGURE 5. Correlator structure proposed in [15].

multiplexer as an example, each correlator of the structure proposed in [14], The required number of multiplexer is $N_{mux2} = K_{COH}{}^{*}W_{COH}/W_{RAM}$, and the logical depth of the multiplexer is $L_{mux2} = \log_2(N_{mux2})$, where K_{COH} is the number of short-time correlator physical branches, W_{COH} is the output bit width of each short-time correlator branch, and W_{RAM} is the bit width of each coherent RAM.

Reference [15] presented an implementation method of correlator array based on FPGA, which optimizes the circuit structure of the correlator branch in order to increase the clock frequency of the correlator array. The hardware structure is shown in Figure 5. The dual-port RAM resources in the FPGA are used to replace the registers in the correlator circuit, Thus reducing the timing path between the correlator array and coherent RAM, This method makes full use of the RAM resources of the FPGA devices and the reconfigurable structure characteristics, but because each correlator branch require an independent RAM, the number of blocks of the coherent RAM increases with the number of the correlator breach increase.

According to the work flow of the acquisition engine, after the coherent integration, the acquisition engine starts the FFT unit, reads the coherent RAM data for non-coherent integration, The inputs of each FFT operation is the M segment short-time correlation result of the i branch short-time physical correlator branch. K times FFT calculation is required. M is the maximum number of short-time coherent segments, which is consistent with the number of FFT operation points, and K is the number of physical short-time correlator branches.

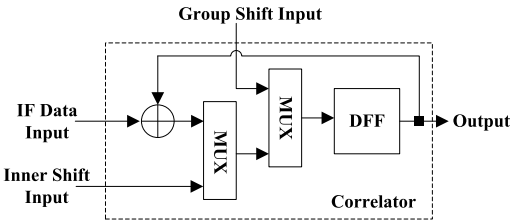

FIGURE 6. Proposed correlator optimization structure.

Assuming that the coherent RAM bit width is the same as the output bit width of the correlator, the structure of short-time correlator array proposed in [14], since the data path between the correlator and coherent RAM is fixed, write all the coherent integration results into coherent RAM require $T_{wr1} = K/N$ writing cycles. N is the number of coherent RAM blocks. In the process of non-coherent integration, each FFT operation at least requires M operation cycles to read coherent RAM and $T_{rd1} = K * M$ reading cycles to complete all non-coherent integrals.

Using the RAM-based correlator structure proposed in [15], since the results are synchronously written into coherent RAM during the coherent integration process, no additional coherent RAM storage operation is required compared with [14]. However, the reading period of incoherent integral operation is the same as that of [14] because the different piecewise integral results of each correlator are written to the same RAM. Moreover, when the number of correlators increases, the number of coherent RAM blocks proposed in [15] is much higher than that in [14]. Unlike FPGA architecture, in the implementation of VLSI architecture, the reliability and area optimization of VLSI design will be undesirable.

In this paper, an optimized correlator circuit structure is proposed, which can improve the clock frequency of the correlator array circuit and significantly reduce the reading period of the acquisition engine for coherent RAM in the non-coherent integration stage. The hardware structure is shown in figure 6. In our design, a two-stage gate is added between the accumulator register and the adder. The correlator branches are grouped according to the number of coherent RAM blocks, which is the same as the analysis condition of the correlator structure proposed in [14]. Assuming that the output bit width of the correlator is the same as the coherent RAM bit width, each group contains N correlator branches and is divided into K/N groups. When the acquisition engine is in the coherent integration stage, the correlator in Figure 6 selects the IF data input and performs the coherent integration operation. After the coherent integration, the correlator branch selects the inner-group shift input and the other group shift input data respectively to complete the coherent RAM storage operation. The hardware connection between the coherent array and coherent RAM designed in this paper is shown in figure 7.

The correlator array optimization method proposed in this paper can be summarized as the following two stages for the write operation of coherent RAM:

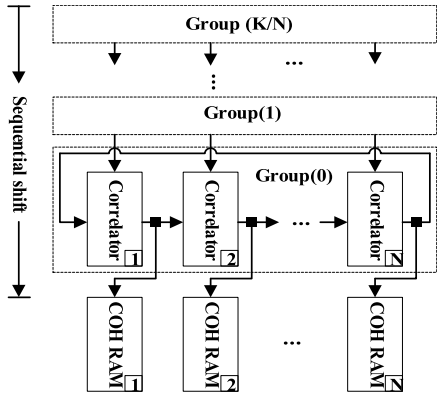

FIGURE 7. Proposed connection structure between correlator array and coherent RAM.

Firstly, according to the short-time correlation segment numbers in the current acquisition process, cyclic shifts are performed in all group of correlator arrays. The number of cyclic shifts within the group is i mod N. After cyclic shifts within the group, the initialization process of the output of each correlator is completed.

After the inner-group cyclic shift, the sequential shift between groups of correlator arrays is performed. During the shift operation, all zeros are used as the shift input data, and the shifted data is written into the coherent RAM. The sequential shift times between groups is K/N. After sequential shifts, the coherent RAM storage operation is completed.

According to the above description of the coherent RAM writing process, the acquisition engine completed all the short-time correlation process. Note that the zero segment has the shortest storage time and the number of operation cycles is the same as the block number of the coherent RAM. The $N-1$ segment of the short-time correlation of the storage time is the longest, the operation cycle is $N-1+K/N$. Due to the difference of short-time correlation segments in different constellation systems and different frequency signals, the average operation period of the optimized short-time correlation array to write coherent RAM is $T_{wr2} = (N-1+2K/N)/2$.

Since all zero input is used in the sequential shift process of coherent RAM storage phase, all short-time correlator arrays complete the zero-clearing operation at the same time when each segment of coherent RAM writing operation is completed. Compared with the structure proposed in [14], the high fan-out zero-clearing logic circuit is avoided when the size of correlator is large. Furthermore, a large number of gates between the correlator array and the coherent RAM are allocated equally to each correlator branch. Compared with the structure proposed in [14], the logic level between the correlator array and the coherent RAM is zero, and the timing of the coherent RAM array circuit is optimized. Compared with the structure proposed in [15], each correlator circuit only adds one two-input multiplexers, but the requirement for the number of coherent RAM blocks is reduced.

According to the above process, after all the short-time correlation results are written to coherent RAM array.

TABLE 2. The VLSI implementation results of the capture architecture proposed in this paper (iWorst Corner).

Area(mm2)	Maximum clock frequency (MHz)	Average power consumption (mW)
2.1	333.33	72.02

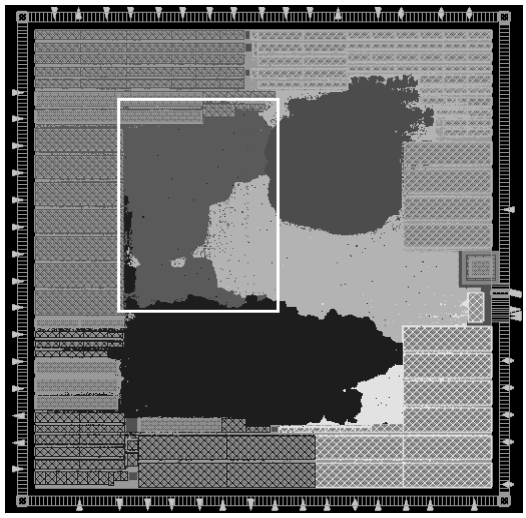

FIGURE 8. The results of the VLSI layout design of the acquisition engine architecture.

The results of all M segment integrals of the correlator branch j are written in the coherent RAM of different block numbers respectively. In the non-coherent integration stage, the FFT unit can read the coherent integration results of Ncoherent branches at the same time in each reading cycle, which improves the parallelism of FFT reading coherent RAM. Assuming that the number of FFT units is N_{FFT}, the reading period of each round of FFT operation is $T_{rd2} = N_{FFT}/N$, N is the number of coherent RAM blocks. Compared with [14] and [15], the reading efficiency of FFT is improved by using the same number of coherent RAM blocks.

V. IMPLEMENTATION RESULTS AND COMPARATIVE ANALYSIS

As part of the baseband SoC chip of GNSS receiver compatible with multi-constellation system and multi-frequency point, the acquisition engine circuit proposed in this paper realizes the VLSI design using 55nm digital technology, through the RTL function design, logic synthesis and layout design of the digital circuit implementation process, finally the chip design of the acquisition engine is realized. TABLE 2 shows the VLSI implementation results under the conditions of 1.08V voltage and 125 °(Worst Corner).

Figure 8 shows the VLSI layout of the baseband SoC chip of the GNSS receiver which supporting multi-constellation systems and multi-frequency points. The white box is the acquisition engine circuit proposed in this paper.

TABLE 3 shows the acquisition engine architecture proposed in this paper, and compares with other architectures

TABLE 3. Comparison of working frequency and compatibility.

Content		Reference [7]	Reference [8]	Reference [10]	Proposed
Working frequency (MHz)		80	40	62	333
Constellation system	GPS	Y	Y	Y	Y
	BDS	N	N	Y	Y
	GLONASS	Y	Y	N	Y
	GALILEO	Y	Y	N	Y
	IRNSS	N	N	N	Y
	QZSS	N	N	N	Y
	SBAS	N	N	N	Y
Signal frequency	L1	Y	Y	Y	Y
	L2	Y	Y	Y	Y
	L5	Y	Y	N	Y
	E1	Y	Y	N	Y
	E5	Y	Y	N	Y
	B1	N	N	Y	Y
	B2	N	N	Y	Y
	B3	N	N	N	Y

TABLE 4. Comparison of working frequency and compatibility.

Content	Reference[12]	Reference[13]	Proposed
Requirement RAM (bit)	20453	0	0
Modular division resources	No requirement	Requirement	No requirement
Maximum initialization cycle number	0	13061160	5115

TABLE 5. Comparison of circuit structure of correlator ARRAY.

Content	Reference [14]	Reference [15]	Proposed
Gate level of Coherent RAM data path	$\log_2 K$	0	0
Requirement of Coherent RAM block	M	K	M
Storage cycle of Coherent RAM	K/N	0	$(N-1+2K/N)/2$
Read cycle of Coherent RAM	$K*M$	$K*M$	K

in terms of working frequency and compatibility. In TABLE 3, ''Y'' indicates support, and ''N'' means no support. As can be seen from the frequency comparison data listed in In TABLE 3, other acquisition engines with direct search structure can only work at the sampling frequency of the RF signal, while the playback structure used in this paper allows the acquisition engine to work at frequencies far higher than the signal sampling rate, which can greatly improve the search efficiency. And in terms of compatibility, the hardware architecture designed in this paper is also better than other flexible software acquisition engine architecture based on FPGA acceleration.

Taking GPS L1C signal as an example, it illustrates the advantages of the acquisition engine architecture proposed in this paper compared with the direct acquisition architecture. The improvement of working frequency leads to the improvement of search efficiency. The GPS L1C signal has 10230 code phases. In this design, the acquisition engine contains 1024 physical correlator branches. Due to the half code search accuracy is used, therefore, it require $N = 20$ times to cover all the half-chip phases of GPS L1C signals. Assuming that 100ms IF data needs to be used, and $C = 5$ frequency points are searched, and the down-sampling frequency of the filter at the front-end of the acquisition engine is $F_{down} = 4.092$ MHz, the playback correlator array works at 333.33MHz, when the acquisition engine searches all the code phases and all the frequency points of the GPS L1C signal, the actual time required is $100*N*C*F_{down}/F_{replay} \approx$ 123 ms, and the direct search architecture require $100 * N * C * F_{down} \approx 41$ s.

TABLE 4 shows the comparison between the hardware resource requirements and the calculation efficiency of the Legendre sequence generator designed in this paper when it is compatible with L1C and B1C signals.

If the number of segments of short-time correlation is M, and the number of correlator is K, N is the number of coherent RAM blocks, the points of FFT units is the same as the short-time correlation segment, and the coherent RAM data width is the same as the output width of the correlator, TABLE 5 lists The correlator optimization method proposed in this paper is superior to other design in circuit structure.

As can be seen from TABLE 5, the optimized correlator array circuit in this paper reduces the combinational logic gate level of the data path connection between the correlator and coherent RAM reduce to 0 compared with the scheme in [14], same as the scheme in [15]. The storage cycle of coherent RAM is slightly higher than [14], but the reading cycle of FFT in non-coherent integration phase for coherent RAM is obviously reduced. The computational efficiency of the correlator array is improved, and compared with [15], the requirement for the number of blocks of the coherent RAM is significantly reduced when the number of correlator arrays remains unchanged.

The test environment of the acquisition engine is shown in Figure 9 which includes GNSS signal generator, RF ADC and the GNSS baseband SoC chip. The GNSS baseband SoC chip contains the acquisition engine circuit designed in this paper. The GNSS signal is generated by the signal generator as the input signal of the test board, after converted by RF ADC, the GNSS signal is input to the GNSS baseband SoC chip. The baseband SoC chip enable the acquisition engine circuit and outputs the result of the acquisition engine to the PC through the UART interface.

To fully verify the function of the acquisition engine proposed in this paper, the signal generator generates all the GNSS signals listed in Table 1. For each test group of GNSS signals, the satellite number and the center frequency of the GNSS signal generated by the signal generator are set randomly, and the result of the acquisition engine is observed

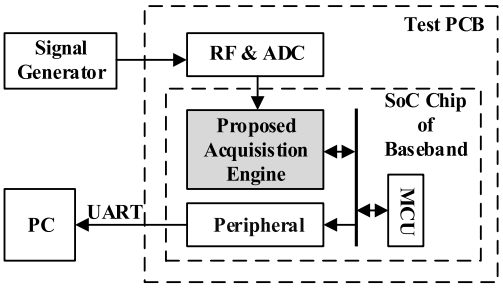

FIGURE 9. The test environment of proposed acquisition engine.

FIGURE 10. The RF signals generator.

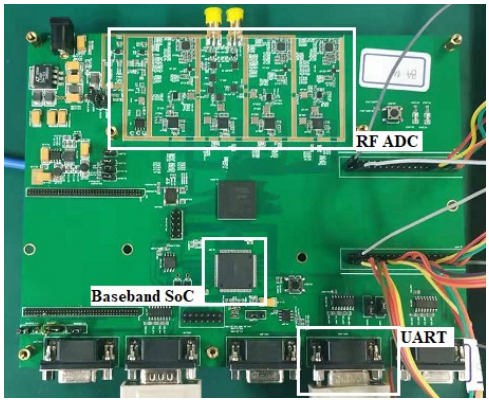

FIGURE 11. The PCB of acquisition engine.

on the PC side. If the satellite number result is the same as the setting of the signal generator, and the deviation between the center frequency result and the setting value of the signal generator is within the frequency resolution range of the acquisition engine, which indicates that the acquisition engine has the correct function and is in accordance with the design expectation.

The signal generator used to verify the function of the acquisition engine circuit is shown in Figure 10, The model is GSS6700, which can generate multiple GNSS signals, and the test PCB of the acquisition engine is shown in Figure 11.

The test results of the acquisition engine circuit are listed in TABLE 6. As can be seen from TABLE 6, the satellite number result collected from the acquisition engine circuit is consistent with the set value of the signal generator, and the center frequency is also close to the preset value.

Taking the GPS L1C signal as an example, the correctness of the test results of the center frequency in TABLE 6 is

TABLE 6. Test results of acquisition engine circuit.

Constellations System	Signals	Setting of RF generator		Result of testing	
		No. Of Satellite	Center Frequency(Hz)	No. of Satellite	Center Frequency(Hz)
GPS	L1C/A	4	653	4	687.5
	L1C	2	1039	2	1031.3
	L2C	10	1135	10	1203.1
	L5	8	-739	8	-687.5
BDS	B1I	8	-867	8	-859.4
	B1C	11	471	11	515.6
	B2I	13	-975	13	-1031.3
	B2a	6	561	6	565.6
	B3I	13	773	13	687.5
GALILEO	E1-B	6	867	6	859.4
	E1-C	11	-636	11	-687.5
	E5a	7	-256	7	-171.875
	E5b	14	412	14	343.8
GLONASS	L1OF	14	579	14	546.9
	L1OC	5	848	5	875.0
	L2OF	8	-366	8	-328.1
	L2OC	11	-840	11	-875.0
	L3OC	9	207	9	218.8
SBAS	L1C/A	11	-571	11	-515.6
IRNSS	L5	12	-1094	12	-1031.3
	S	9	612	9	687.5
QZSS	L1 C/A	16	-618	16	-687.5
	L1C	4	-138	4	-171.9
	L1-SAIF	2	451	2	515.6
	L2C	2	-338	2	-343.8
	L5	7	567	7	515.6

explained: the GPS L1C signal in the process of acquisition of coherent integral segment number $N_{COH} = 11$, the signal sampling time is $T = 1$ ms, the points of FFT operation units is 64, The frequency resolution of the acquisition engine proposed in this paper is $T/N_{COH}/64 = 171.875$ Hz. The deviation between the center frequency result of the GPS L1C signal and the presetting value of the signal generator is 7.7 Hz in the TABLE 6. It is less frequency resolution of the acquisition engine, which shows that the acquisition engine is correct in function and in accordance with the design expectation and achieves the goal of supporting multi-satellite system and multi-frequency GNSS signals with the circuit architecture of the time division multiplexing.

VI. CONCLUSION

In this paper, a short-time correlation combining with FFT scheme based GNSS acquisition engine architecture is proposed. Meanwhile, a playback structure is adopted to improve the working frequency. The acquisition engine architecture can support multi-constellation and multi-frequency satellite signals by flexible configuration without increasing hardware resources. It meets the compatibility of high-precision positioning applications. The structure of spread spectrum code generator and short-time correlator array in acquisition engine is also optimized in this paper. The maximize clock frequency and searching efficiency of the optimized acquisition engine is improved. The acquisition engine proposed in this design only takes 123ms to search all code phases and frequency points of GPS L1C signals, which satisfies the real-time performance of high-precision GNSS receivers.

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YUHENG YANG was born in 1987. He received the B.S. degree in microelectronics from the North University of China, in 2010, and the M.S. degree in integrated circuit engineering from the Harbin Institute of Technology, in 2012. He is currently pursuing the Ph.D. degree in communication engineering with the School of Microelectronics, University of Chinese Academy of Science, Beijing, China. He is involved in research on SoC design for satellite navigation.

XIAOHUI BA received the B.S. degree in electronic engineering and the M.S. degree in electronic engineering, signal and information processing from the Dalian University of Technology, in 2001 and 2004, respectively, and the Ph.D. degree from the School of Microelectronics, University of Chinese Academy of Science. He is involved in research on satellite navigation and positioning algorithm and receiver design.

Since 2007, he has been an Associate Researcher and a Tutor of master's degree with the SoC Laboratory of Communication and Multimedia, Institute of Microelectronics, Chinese Academy of Sciences.

JIE CHEN received the Ph.D. degree. From 1994 to 2001, he served as an Associate Researcher with the University of Electro-Communications (UEC), Japan, as a Senior Project Leader with Japan YOZAN Co.Ltd., and as an Associate Professor with UEC. Since 2001, he has been a Director Professor of the Department of ASIC Design, Communications and Multimedia SoC Research, R&D Center for Green Energy Vehicles, and a Deputy CTO of the Institute of Microelectronics, Chinese Academy of Sciences. His research interests include signal processing, data compression, mixed-signal circuits design, and multi-core processor design. He received the National Science Fund for Distinguished Young Scholars, China, in 2015.