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Fully Coupled Electrothermal Simulation of Large RRAM Arrays in the "Thermal-House"

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ABSTRACT Thermal crosstalk in a highly integrated RRAM array due to the self-heating effect is one of the most critical issues affecting device reliability. In this paper, two types of ''thermal-house'' structures are proposed to optimize the thermal management of the RRAM array. An in-house developed parallel simulator is employed to study the performance of the proposed thermal house structures in terms of resistance ratio and crosstalk temperature. It is demonstrated that the proposed thermal house structures can help to reduce thermal crosstalk in high-density RRAM arrays. Some suggestions are also provided for further improving the thermal management capability of the thermal houses as well.

INDEX TERMS Electrothermal simulation, low power consumption, parallel simulator, resistive-switching random access memory (RRAM), thermal-house, thermal management, thermal crosstalk.

I. INTRODUCTION

Management of big data in the information age has spurred many research activities in academia and industry with the goal of facilitating every-day life. In order to satisfy the exponential growth of demand for big data storage, new devices with versatile characteristics are required.

As a result, the development of next-generation memory techniques has triggered renewed interest. In the past decades, several emerging techniques, including ferroelectric random access memory (FRAM) [1], [2], phase-change RAM (PRAM) [3], [4], magneto-resistive RAM (MRAM) [5], [6], and resistive-switching RAM (RRAM) [7]–[11], have been verified with better scalability and logic compatibility. Among them, RRAM is a promising candidate, due to its fast write/erase speed, large storage density, high efficiency, and low power operation [10]. However, with growing storage density which leads to higher power density, thermal issue becomes one of the most critical problems and must be treated appropriately in the development of 3D RRAM array as the temperature highly affects its switching behavior and reliability.

Recently, physical modeling of the electrothermal process in RRAM cells and the thermal crosstalk effects induced by self-heating effect (SHE) have been investigated [12]–[14], with some practical guides given for the thermal management optimization [13]–[17]. In this work, we propose two types of structures coined as 'thermal-house' (TH) that facilitate thermal management and their performance in thermal management of both RRAM cell and array will be studied in detail. To study thermal effects in large scale RRAM arrays, an in-house simulator based on a hybrid numerical discretization scheme is developed and used to perform fully coupled electrothermal analysis. In this numerical approach, finite-element method (FEM) is used to solve the current continuity and thermal conduction equations, while a mixed finite volume-finite element method is used to solve

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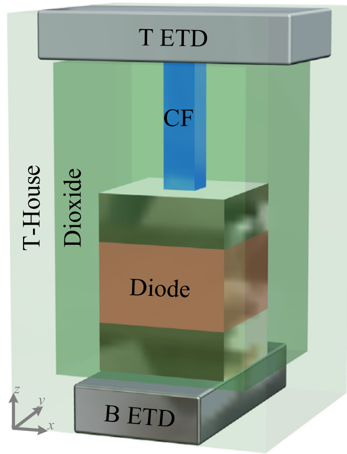

FIGURE 1. Schematic of a 1D1R RRAM cell.

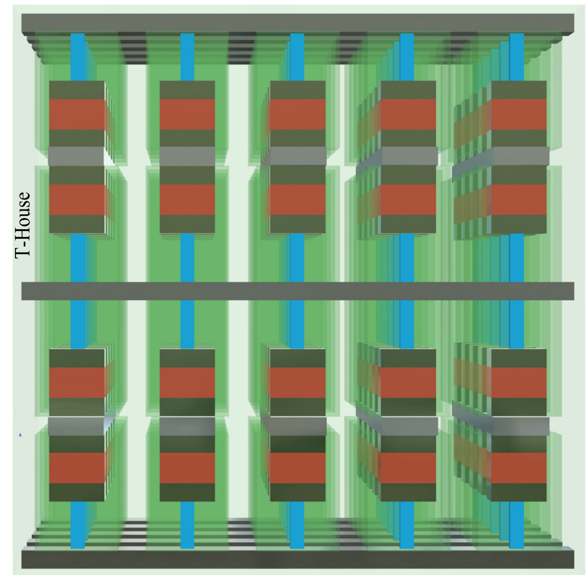

FIGURE 2. Schematic of a 100-bit SBL RRAM array (5×5×4) in the TH. The gray strips, blue quadrangular prisms, and red quadrangular prisms denote the electrodes, resistors, and diodes, respectively.

the highly nonlinear particle transport equation [18], [19]. Moreover, in order to enhance the capability of the simulator in simulating large scale structures, J parallel Adaptive Unstructured Mesh applications INfrastructure (JAUMIN) and domain decomposition method (DDM) based double-level parallel scheme is utilized in the in-house simulator development [20]–[24].

The rest of this paper is organized as follows. In Section II, the geometrical and physical models of RRAM in the TH are introduced and a possible manufacturing process is described. The implementation of the numerical approach is outlined in Section III. In Section IV, electrothermal characteristics of the RRAMs in the proposed TH structures are studied in detail. Finally, some conclusions are drawn in Section V.

II. MODEL DESCRIPTION

A. ARCHITECTURE

In recent years, various types of RRAM array architectures have been proposed [25], wherein the crossbar array is one of the most popular architectures for high density integration. Fig. 1 shows the schematic diagram of a one-diode-one-resistor (1D1R) RRAM cell in the TH. The RRAM, consisting of a Ti/TiO_2/Pt diode element and a Pt/HfO_2/Pt resistive switching (RS) memory element [16], [26], is sandwiched between the top electrode (T-ETD) and bottom electrode (B-ETD). After an initial forming process, a conductive filament (CF) is built in the reduced oxide region, which contains many oxygen vacancies. The CF resistance is toggled from high resistivity state (HRS) to low resistivity state (LRS), and vice versa, in the set and reset operations, respectively.

As illustrated in Fig. 1, the TH structure is a box designed to alleviate the thermal crosstalk effect in large scale RRAM arrays. The TH, depending on its component material, acts as a heat passageway or high thermal insulation layer. Here, the TH material is chosen to be diamond and Si_3N_4 for low thermal resistance TH (LRTH) and high thermal resistance TH (HRTH), respectively.

B. MANUFACTURING PROCEDURE

According to the procedure given in [11] and [28], the platinum B-ETDs with thin Ti adhesion layer can be deposited onto the substrate by using the electron beam evaporation and patterned by a lithograph and lift-off process. The diamond or Si_3N_4 layer can be deposited as the TH for heat dissipation or insulation, respectively. A lithography and etching process is performed to form cell via holes [27], and the TiO_2 oxide diode and RS memory cell can then be fabricated sequentially in each cell via hole [28] and the T-ETDs are finally patterned. Following the procedure described above, the multilayer RRAM array can be fabricated layer by layer. A schematic of a 100-bit shared-bit-line (SBL) cross-bar RRAM array in the TH is illustrated in Fig. 2.

C. PHYSICAL MODEL

As proposed in [13] and [14], the electrical property of RRAM can be described by the drift-diffusion equation. The transport of particles and current should satisfy the continuity equations, i.e.,

$$\frac{1}{q}\nabla\cdot\vec{J} = \nabla\cdot\Big(\mu(T)n_D\vec{E} - D(T)\nabla n\Big) = \frac{\partial n_D}{\partial t} + RG \quad (1)$$

$$\nabla\cdot(\sigma(n_D, T)\nabla V) = 0 \quad (2)$$

where V is the voltage, $\sigma(n_D, T)$ is the temperature- and particle concentration-dependent electrical conductivity, $\vec{E} = -\nabla V$ is the electric field, $\mu(T)$ is the temperature-dependent mobility, and RG is the generation/recombination rate [14]. The ion diffusion coefficient $D(T)$ is temperature

activated through the Arrhenius law

$$D(T) = D_0 \exp\left(-\frac{E_A}{k_B T}\right) \quad (3)$$

where D_0 is the coefficient of diffusivity, k_B is Boltzmann's constant, and T is the local temperature. According to the Einstein relationship, μ can be expressed as

$$\mu(T) = \frac{kT}{q} D(T) \quad (4)$$

As stated in the previous works [29], [30], D_0 and E_A are set to be 2×10^{-3} cm^2/s and 1 eV, respectively.

To capture the temperature distribution due to self-heating, the thermal conduction equation needs to be solved, i.e., [15], [17]

$$c_p(T)\,\rho(T)\frac{\partial T}{\partial t} = \nabla \cdot (\kappa(T)\,\nabla T) + Q \quad (5)$$

where $c_p(T)$ and $\kappa(T)$ are the temperature-dependent heat capacity and thermal conductivity of the materials involved, respectively. Q is the heat generation rate, and it is calculated as

$$Q = \vec{J}\cdot\vec{E} \quad (6)$$

The electrical conductivity of CF can be expressed as [14]

$$\sigma(T) = \sigma_0 \exp\left(-\frac{E_{AC}}{k_B T}\right) \quad (7)$$

where σ_0 is the pre-exponential factor, and E_{AC} is the activation energy for conduction. Since the heat capacity and thermal conductivity are usually temperature-dependent, the thermal conduction equation should be treated as a nonlinear system. A constant temperature boundary condition (T_0 = 300 K) is added at both top and bottom surfaces of the RRAM cell or array.

It is worth noting that all material parameters in (1)-(7) depend on temperature, which provide links between the electric and thermal fields during electrothermal co-simulation. As shown in Fig. 3, based on the Joule heat calculated from the electric field, the thermal conduction equation is solved to capture the 3D temperature distribution, which is then feedback to the electrical equations to start a new process.

III. NUMERICAL IMPLEMENTATION

Fig. 3 outlines the hierarchical structure of the in-house parallel simulator developed. As described in the flowchart of 'Physical Level', the nonlinear electric model is first solved, and the heat generation rate is then calculated as the thermal source in the thermal conduction equation. Next, a new temperature distribution is captured and coupled back to initialize a new iteration until the convergence criteria is satisfied. The FEM is utilized for discretizing the current continuity equation and thermal conduction equation while a hybrid FVFEM-SG method is used to solve the particle transport equation [31]. Specially, both space and time discretization of the particle transport equation are discussed below.

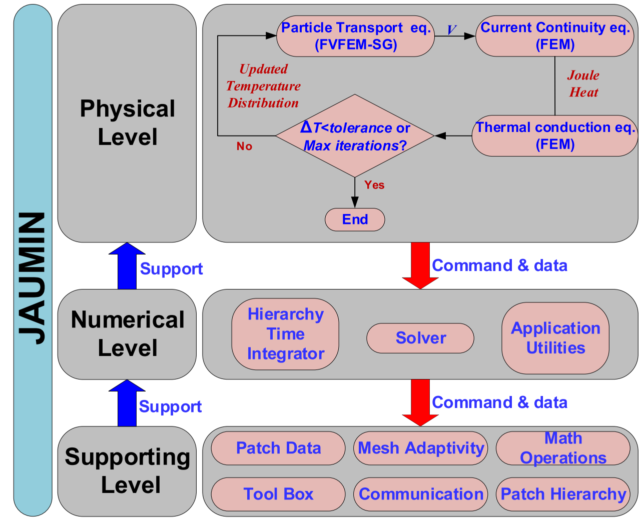

FIGURE 3. Hierarchical structure of the in-house developed parallel simulator.

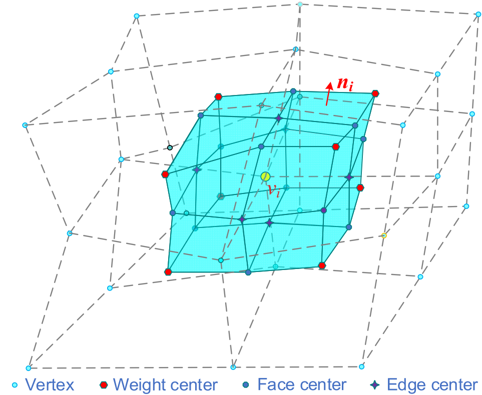

FIGURE 4. The control volume cell Ω_i at vertex v_i for grid composed of hexahedron. n_i indicates the outward normal vector of the surface.

Because of its diffusion-advection features and strong nonlinearities, the particle transport equation cannot be spatially discretized directly [18]. Here, a hybrid finite volume-finite element method is used to overcome this difficulty [31]. Unlike the traditional SG strategy, the element weight center and edge centers are introduced to construct the control volume cell of FVM. A schematic of the cell in the 3D hexahedral mesh is depicted in Fig. 4. The implementation of hybrid FVFEM is described as follows.

At first, (1) is integrated over each control volume cell Ω_i as

$$\frac{1}{q}\int_{\Omega_i} \nabla\cdot\vec{J}\,d\Omega = \int_{\Omega_i}\left(\frac{\partial n_D}{\partial t} + R\right)d\Omega \quad (8)$$

The divergence theorem is applied to the left-hand side of (8) to get its 'weak' form as

$$\frac{1}{q}\int_{\partial\Omega_i} \vec{J}\cdot\vec{n}dS = \int_{\Omega_i}\left(\frac{\partial n_D}{\partial t} + RG\right)d\Omega + \int_{\partial\Omega_i^N} h_n dS \quad (9)$$

The upwind current density $\vec{J}$ in (9) is computed by

$$\vec{J} = \sum_{e_{ij}\in E(\Omega)} \frac{\mu}{2}\left(n_{Dj}\left(\coth\left(a_{ij}\right)-1\right) - n_{Di}\left(\coth\left(a_{ij}\right)+1\right)\right) W_{ij} \tag{10}$$

where a_{ij} is the Peclet number along the edge e_{ij}, and it can be computed by

$$a_{ij} = \frac{\mu_n I_{ij}}{2D_n} \tag{11}$$

W_{ij} is the FE vector base function [32]. By substituting (10) into (9) and extending it to the whole computational domain, the system equation can be formulated as

$$\sum_{j\in\Omega\cup\Gamma_N} \frac{\partial n_{Dj}(t)}{\partial t}\int_{\Omega_i} N_j d\Omega - \sum_{j\in\Omega\cup\Gamma_N} n_{Dj} \sum_{e_{kj}\in E(v_j)} \frac{\sigma_{kj}\mu}{2} \times \left(\coth\left(a_{ij}\right)-\sigma_{kj}\right)\int_{\partial\Omega_i} W_{kj}\cdot n dS = -\int_{\Omega_i} RG d\Omega - \int_{\partial\Omega^N} h_n dS \tag{12}$$

Finally, the matrix description for (12) is constructed as

$$[M_e]\frac{\partial}{\partial t}\{n\} - [K_e]\{n\} = \{f_e\} \tag{13}$$

By conducting the backward difference with respect to time, the matrix form of (13) is written as

$$([M_e]-[K_e])\{n\}_{t+\Delta t} = [M_e]\{n\}_t + \{f_e\} \tag{14}$$

Here, $[M_e]$ is the coefficient matrix of the time-dependent term, $[K_e]$ is the 'upwinding' stiffness matrix, and Δt is the time step for time evolution. For the steady-state situation, the time-dependent term is removed and the matrix equation is turned into

$$-[K_e]\{n\} = \{f_e\} \tag{15}$$

To enhance the simulator capability for simulation of large scale structures, a double-level parallel scheme based on JAUMIN [33] and DDM is employed and extended to parallelize the numerical simulation.

IV. SIMULATION RESULTS AND DISCUSSION

Due to the high power density in RRAM arrays, the thermal problem has become a major issue which affects device reliability and retention time directly. In particular, the generated heat of active cells may lead to performance and reliability degradation of victim cells. Therefore, two types of TH structures are proposed in this study to alleviate the thermal crosstalk effects in high density RRAM arrays. In this section, the internal parallel simulator is firstly validated and then used to study the electrothermal characteristics of 3D crossbar RRAM (CRRAM) arrays in the TH. The reset process is simulated in the following analysis.

TABLE 1. Geometrical and physical parameters of the involved materials.

Comp.	Materials	Geometrical parameters	Physical parameters
B/W Line	Pt	$W_{\mathrm{BWL}} = 50$ nm $H_{\mathrm{BWL}} = 50$ nm	$k_{\mathrm{Pt}} = 71.6$ W/(m · K) $\sigma_{\mathrm{Pt}} = 8.9 \times 10^6$ S/m $c_{\mathrm{Pt}} = 710$ J/kg · °C
	PGEC [34], [35]	$W_{\mathrm{BWL}} = 50$ nm $H_{\mathrm{BWL}} = 50$ nm	$k_{\mathrm{PE}} = 0.5$ W/(m · K) $\sigma_{\mathrm{PE}} = 6.8 \times 10^6$ S/m $c_{\mathrm{PE}} = 710$ J/kg°C
Diode	Pt	$W_{\mathrm{diode}} = 50$ nm $H_{\mathrm{DT}} = 30$ nm	–
	TiO_2	$H_{\mathrm{TiO}} = 50$ nm	$k_{\mathrm{TiO}} = 11.7$ W/(m · K) $c_{\mathrm{TiO}} = 133$ J/kg°C $\sigma_{\mathrm{TiO}} = 3.07 \times 10^3$ S/m (on-state) $\sigma_{\mathrm{TiO}} = 5 \times 10^{-2}$ S/m (off-state)
	Ti	$H_{\mathrm{DB}} = 30$ nm	$k_{\mathrm{Ti}} = 21.9$ W/(m · K) $c_{\mathrm{Ti}} = 523$ J/kg°C $\sigma_{\mathrm{Ti}} = 2.56 \times 10^6$ S/m
CF	HfO_2	$W_{\mathrm{CF}} = 10$ nm $H_{\mathrm{CF}} = 80$ nm	k_{CF}: Eq. (16) $c_{\mathrm{CF}} = 445$ J/kg°C σ_{CF}: Eq. (7)
Cell Via Hole	HfO_2	$W_{\mathrm{CVH}} = 60$ nm $H_{\mathrm{CVH}} = 190$ nm	$k_{\mathrm{CVH}} = 0.5$ W/(m · K) $c_{\mathrm{CVH}} = 445$ J/kg°C σ_{CVH}: Eq. (7)
TH	Diamond [36], [37]	$W_{\mathrm{TH}} = 80$ nm $T_{\mathrm{TH}} = 10$ nm	$k_{\mathrm{dia}} = T_{TH} \cdot K_D/\Lambda_D$ $c_{\mathrm{dia}} = 790$ J/kg°C $\sigma_{\mathrm{dia}} = 1 \times 10^{-6}$ S/m
	Si_3N_4 [38]		$k_{\mathrm{SiN}} = 0.02$ W/(m · K) $\sigma_{\mathrm{SiN}} = 6.8 \times 10^6$ S/m $c_{\mathrm{SiN}} = 710$ J/kg°C

A. VALIDATION

To validate the accuracy of internal simulator, the electrothermal characteristics of a 1D1R RRAM cell shown in Fig. 1 are simulated. The geometrical and physical parameters of the RRAM cell are summarized in Table 1, in which Λ_D and K_D represent the phonon mean free path and thermal conductivity of the cube diamond. The dioxide is HfO_x, while a uniform doping concentration of $n_D = 1.2 \times 10^{21}$ cm^{-3} is defined within the CF [13]. A nonlinear thermal conductivity model for HfO_x is specified as [14]

$$k_{\mathrm{HfO}} = k_{\mathrm{HfO}\ 0}\left(1 + \lambda\left(T - T_0\right)\right) \tag{16}$$

where $\lambda = 0.01$ is the linear thermal coefficient. $k_{\mathrm{HfO}\ 0}$ is the thermal conductivity at $T_0 = 300$ K, and it is a function of the doping concentration as specified in [13]. As shown in Fig. 5, the results obtained by the in-house developed simulator and COMSOL Multiphysics agree well with each other.

B. 1D1R RRAM CELL

As mentioned above, two types of THs are proposed: 1) LRTH composed of diamond films; and 2) HRTH composed of Si_3N_4 films. The LRTH provides a low thermal resistance path for heat flow to the substrate, while the HRTH alleviates the thermal crosstalk between RRAM cells by increasing the thermal resistance. To further suppress the thermal crosstalk between adjacent cells, the material of bit line (T-ETD) of the RRAM in the HRTH is substituted by the phonon glass and electron crystal (PGEC), which possesses both low thermal conductivity and high electrical conductivity [34], [35]. Here, the electrothermal characteristics

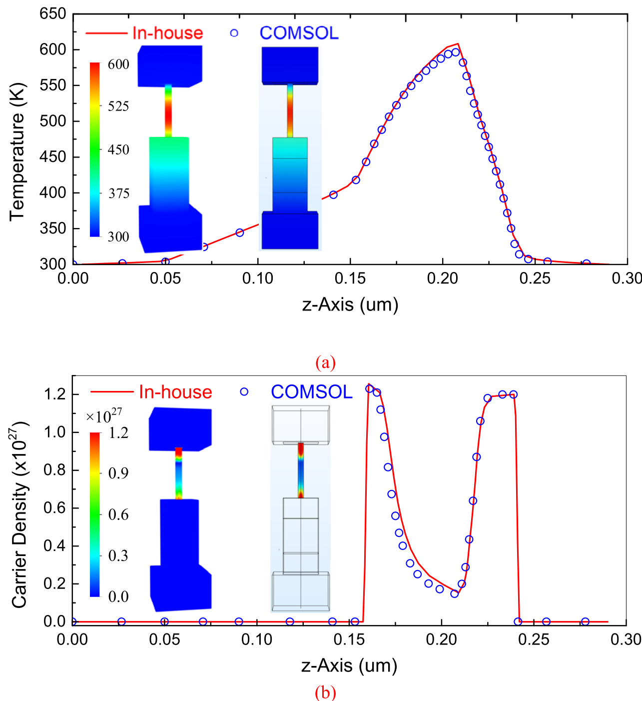

FIGURE 5. Comparison of the simulated results at 0.52 s along the cylindrical axis of 1D1R RRAM cell biased by a voltage source with ramp rate 1 V/s between the in-house simulator and COMSOL. (a) Temperature and (b) particle concentration distributions. The insets show the corresponding quantities on the CF.

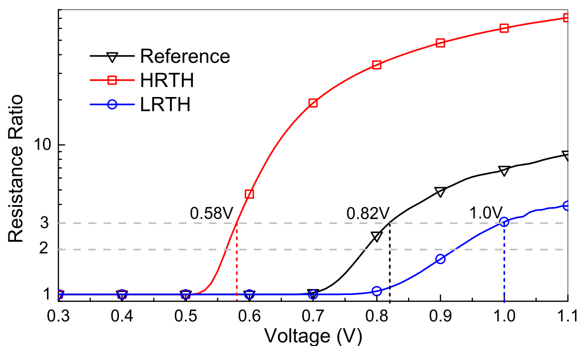

FIGURE 6. Resistance ratio as a function of bias voltage.

of 1D1R RRAM cells with LRTH and HRTH are investigated in detail. In the following analysis, the 1D1R RRAM cell without the TH is also studied as a reference.

Fig. 6 shows the resistance ratio (to the initial value of CF resistance) of the 1D1R RRAM cell as a function of the bias voltage, which increases from 0.3 to 1.1 V with a biasing time of 0.01 s for reset process [13]. The threshold resistance ratio is set to 2:1. It can be seen that the cell resistance in the HRTH is more sensitive to the bias voltage than the others, while the cell in the LRTH has the highest reset voltage. In the following analysis, the operating voltage is defined as the one at which the cell resistance reaches triple the initial value. As indicated in Fig. 6, the operating voltages of the reference RRAM, and the RRAMs in the HRTH and LRTH are 0.82, 0.58, and 1.0 V, respectively.

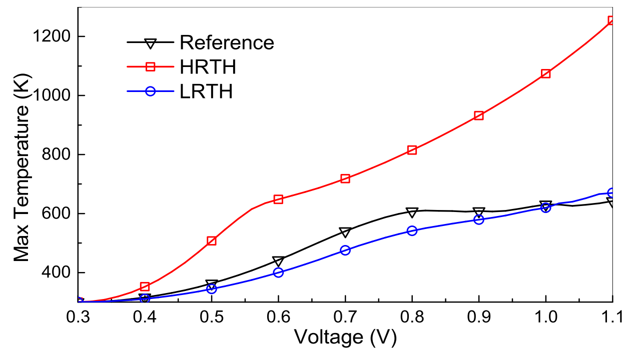

FIGURE 7. The maximum temperature as a function of bias voltage.

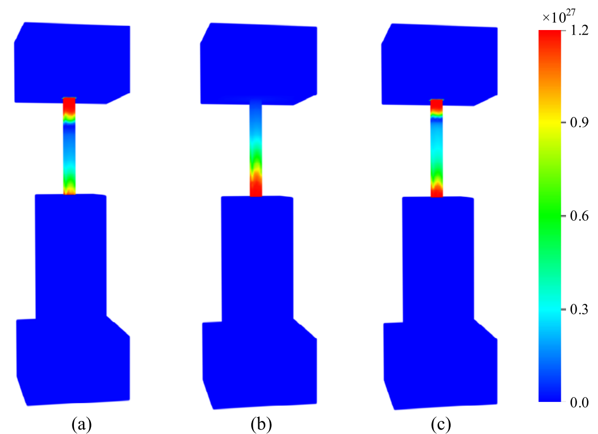

FIGURE 8. Particle concentration distributions of the CFs in (a) reference RRAM cell, (b) RRAM cell in the HRTH, and (c) RRAM cell in the LRTH.

Fig. 7 shows the maximum temperature of the RRAM cells as a function of the bias voltage. The temperature of the cell in the LRTH is much lower than that of the cell in the HRTH. This is because the LRTH provides an effective heat dissipation path to the heat flow, while almost no heat is dissipated through the HRTH. According to the physical model in Section II, the RRAM state is susceptible to the bias voltage and temperature. It is evident that high temperature rise of the cell in the HRTH causes high resistance ratio and low operation voltage (see Fig. 6). Therefore, it can be expected that the cell in the HRTH possesses lower power consumption, which is critical for real-world applications of the high density RRAM array.

The particle concentration and temperature distributions of the single RRAM cells at their operating voltages are plotted in Figs. 8 and 9, respectively. It is found that the gap depletion occurs exactly at the highest temperature. The particle concentration and temperature distributions along the z-axis at the centers of RRAM cells are depicted in Fig. 10. It is seen that the position of the lowest particle concentration corresponds well with that of the highest temperature, indicating that the resistance ratio is sensitive to the temperature.

C. 5×5×4 RRAM ARRAY

In this subsection, the electrothermal characteristics of a 5×5×4 RRAM array shown in Fig. 2 are investigated

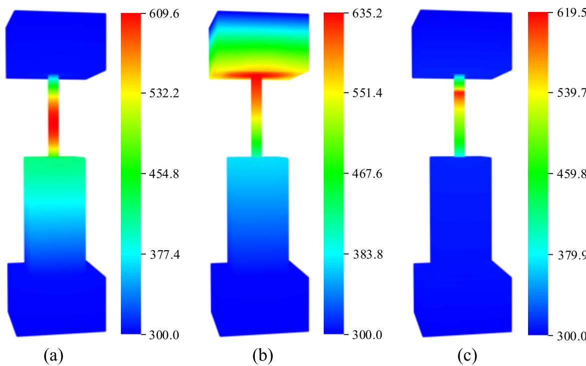

FIGURE 9. Temperature distributions of (a) reference RRAM cell, (b) RRAM cell in the HRTH, and (c) RRAM cell in the LRTH.

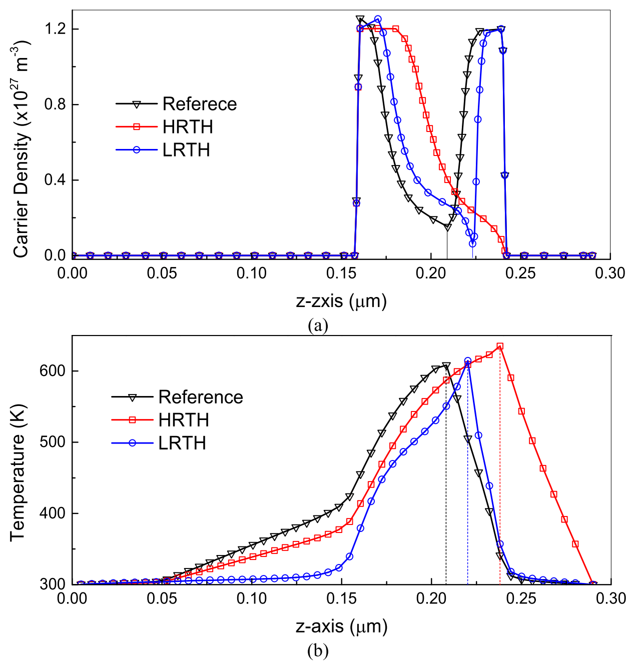

FIGURE 10. (a) Particle concentration and (b) temperature distributions along the z-axis at the center of the RRAM cell.

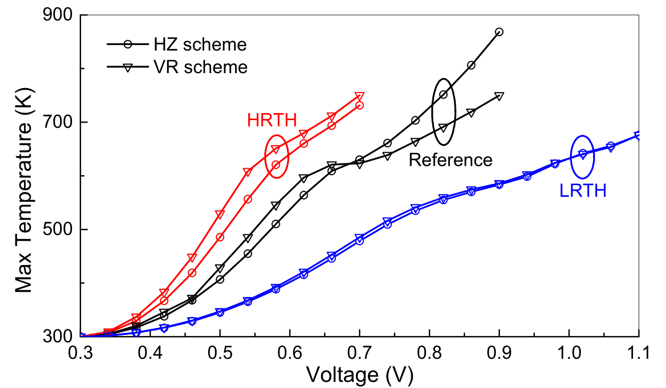

FIGURE 11. Maximum temperature in the 5×5×4 RRAM arrays as a function of bias voltage.

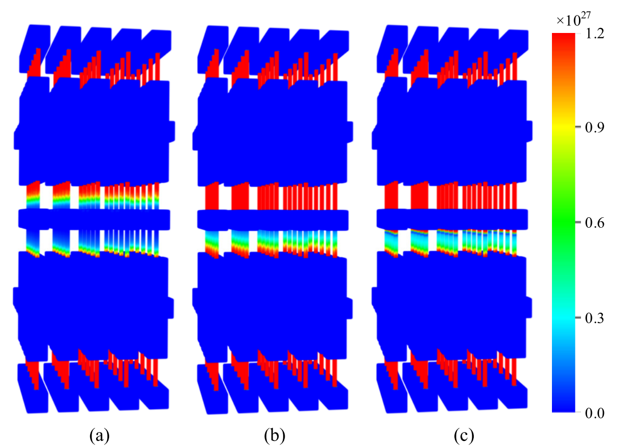

FIGURE 12. Particle concentration distributions of the CFs in (a) reference RRAM array, (b) RRAM array in the HRTH, and (c) RRAM array in the LRTH in the HZ programming scheme.

in detail. For convenience, the cells in the 3D RRAM array are marked in the form of $xyz\,(ijk)$, where $i, j = 1, \ldots, 5$ and $k = 1, \ldots,$ and 4. In order to study the intra- and inter-layer crosstalk, two types of programming schemes are conducted, namely the HZ and VR ones. In the HZ scheme, the cells $xyz\,(1:5; 1:5; 2)$ are programmed, i.e., all the cells in the second layer (counted from the bottom) are programmed. In this scenario, thermal crosstalk effects between the layers sharing the bit lines (first- and second-layers) and between the layers sharing the write lines (second- and third-layers) are studied. In the VR scheme, the cells $xyz\,(2, 4; 2, 4; 2, 3)$ of the 5×5 array in one layer are programmed, i.e., the cells (2; 2), (2; 4), (4; 2), and (4; 4) in the second- and third-layer are programmed. In this scenario, thermal crosstalk effects between the cells in the same layer are captured.

Fig. 11 shows the maximum temperatures in the 5×5×4 RRAM arrays with and without TH in the HZ and VR programming schemes. Similar trends in temperature can be observed in the RRAM array as in the 1D1R RRAM cell. Moreover, the difference in temperature rise between the two programming schemes is much more significant in the reference RRAM array than in the others. Therefore, it can be concluded that both array size and programming scheme have influence on the performance of reference RRAM array, while RRAM array in the LRTH slightly depends on these factors. This indicates that the LRTH can enhance the memory stability.

As stated earlier, the operating voltages are set to be 0.82, 0.58, and 1.0 V for the reference RRAM array and RRAM arrays in the HRTH and LRTH, respectively. The particle concentration distributions in the RRAM arrays in the HZ programming scheme are shown in Fig. 12. Note that the initial value of the particle concentration of the CFs is 1.2×10^{27} m^{-3}. It can be seen in Fig. 12(a) that the particle concentration distributions in the victim cells $xyz\,(1:5; 1:5; 3)$ which share the bit lines with the active cells (*i.e.*, the cells in the third layer counted from the bottom) of the reference RRAM array are seriously influenced, while there is almost no inter-layer crosstalk in the others

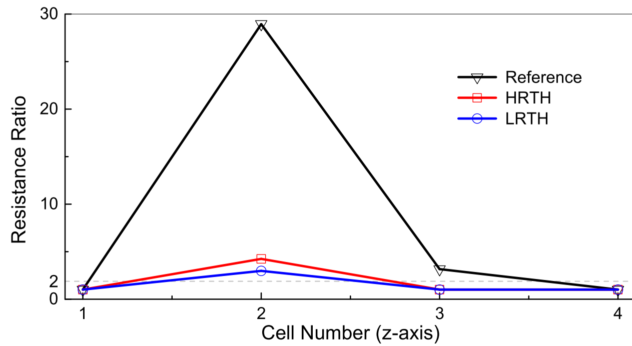

FIGURE 13. Resistance ratios of CFs in cells *xyz*(3; 3; 1 : 4) for RRAM arrays in the HZ programming scheme.

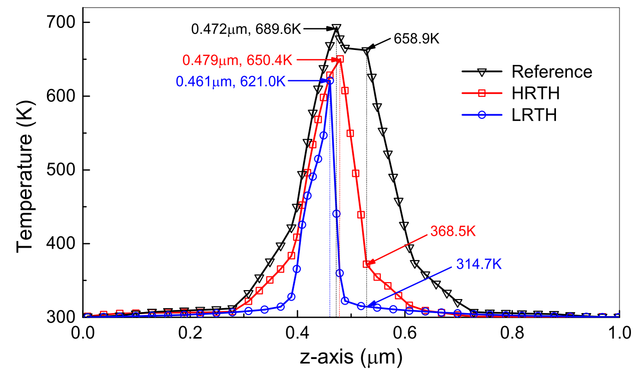

FIGURE 15. Temperature distributions along the *z*-axis at the center of cells *xyz*(3; 3; 1 : 4) in the 5×5×4 RRAM arrays.

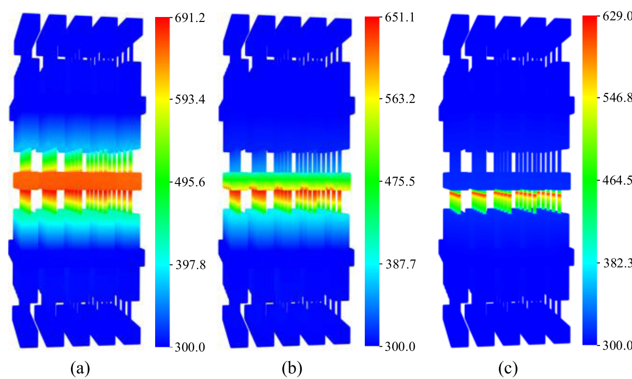

FIGURE 14. Temperature distributions of (a) reference RRAM array, (b) RRAM array in the HRTH, and (c) RRAM array in the LRTH in the HZ programming scheme.

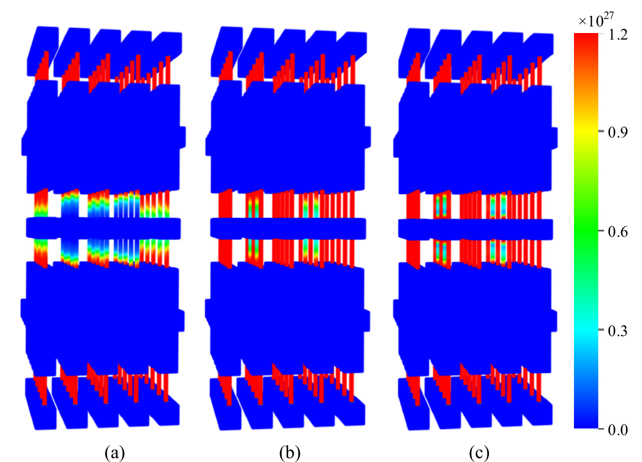

FIGURE 16. Particle concentration distributions of the CFs in (a) reference RRAM array, (b) RRAM array in the HRTH, and (c) RRAM array in the LRTH in the VR programming scheme.

(see Figs. 12(b) and (c)). It can also be seen that, in all three cases the particle concentration distributions in the cells *xyz* (1 : 5; 1 : 5; 1) which share bit lines with the active cells are rarely affected. For greater certainty, the resistance ratio of the cells *xyz* (3; 3; 1 : 4) are plotted in Fig. 13 where the second cell is programmed, while the others are victims. It is evident that the resistance of the cell *xyz* (3, 3, 3) in the reference RRAM array exceeds the threshold level while they are kept almost unchanged in the others, which is consistent with the phenomenon observed in Fig. 12. Consequently, only the thermal crosstalk effect between the layers sharing the bit lines will be discussed below.

Fig. 14 shows the temperature distributions of the RRAM arrays in the HZ programming scheme. A significant inter-layer thermal crosstalk can be observed in the reference RRAM array, whereas it shows no significant crosstalk in the RRAM array in the LRTH. The temperature distributions along the *z*-axis at the center of cells *xyz* (3; 3; 1 : 4) are illustrated in Fig. 15. It can be seen that the temperature in the victim cells reaches 658.9 K in the reference RRAM array, while it drops rapidly to 368.5 K and 314.7 K by utilizing the HRTH and LRTH, respectively. This demonstrates that both HRTH and LRTH can suppress the inter-layer thermal crosstalk in a high density RRAM array.

Next, the intra-layer thermal crosstalk effects in high density RRAM array are investigated by performing the VR programming scheme. Fig. 16 shows the particle concentration distributions of the RRAM arrays in the VR programming scheme. It is shown that the particle concentration distributions of the cells in the vicinity of the programmed cells are almost unaffected for the RRAM arrays in the HRTH and LRTH, as shown in Figs. 16(b) and (c). On the contrary, there is apparently intra-layer crosstalk in the reference RRAM array (see Fig. 16(a)). To describe it clearly, the resistance ratios of the cells *xyz* (2 : 3; 2 : 3; 2) are shown in Fig. 17 in which the cell *xyz* (2; 2; 2) is programmed, while the others are victims. It can be seen that the resistance ratios of the victims in the reference RRAM array exceed the programming level significantly, while it is stable for the others.

Fig. 18 shows the temperature distributions of the RRAM arrays in the VR programming scheme. In order to make them easier to observe, the temperature distributions along the *z*-axis at the centers of the cells *xyz* (2 : 3; 2 : 3; 1 : 4) are illustrated in Fig. 19. A significant intra-layer thermal crosstalk can be observed in the reference RRAM array, whereas there is almost no crosstalk in the RRAM arrays in the TH. Therefore, it can be concluded that both LRTH and HRTH can suppress the intra-layer crosstalk significantly.

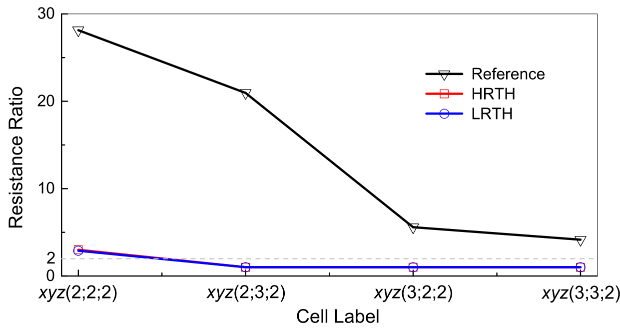

FIGURE 17. Resistance ratio of CFs in the cells *xyz*(2 : 3; 2 : 3; 2) for the RRAM arrays in the VR programming scheme.

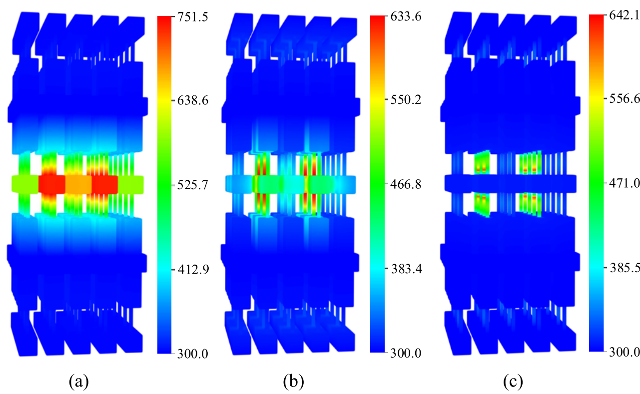

FIGURE 18. Temperature distributions of (a) reference RRAM array, (b) RRAM array in the HRTH, and (c) RRAM array in the LRTH at operating voltage in the VR programming scheme.

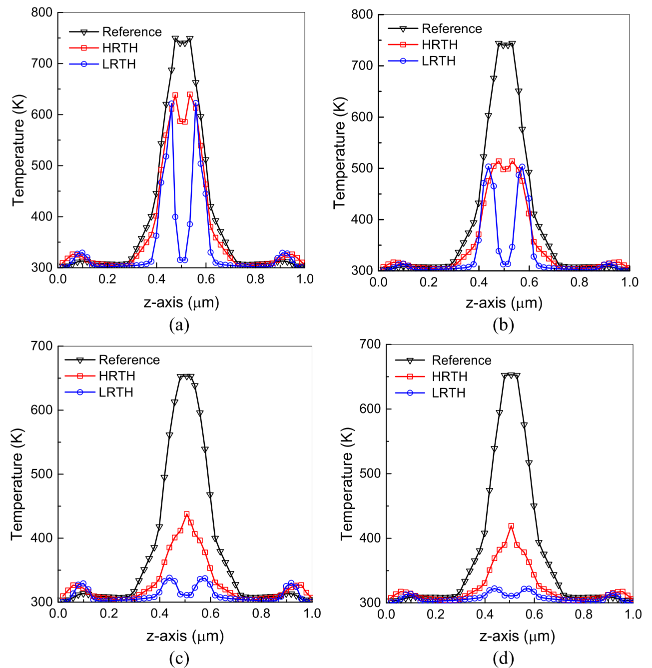

FIGURE 19. Temperature distributions along the z-axis at the centers of cells (a) *xyz* (2; 2; 1 : 4), (b) *xyz* (2; 3; 1 : 4), (c) *xyz* (3; 2; 1 : 4), and (d) *xyz* (3; 3; 1 : 4).

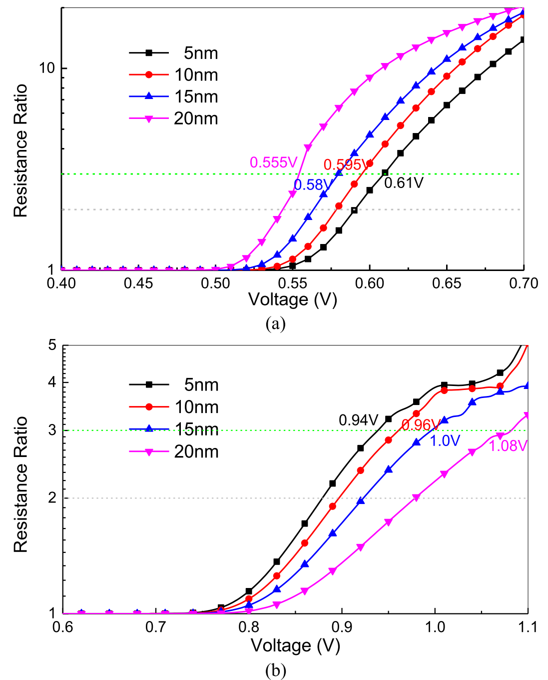

FIGURE 20. Resistance ratio as a function of bias voltage for the RRAM cells with different TH wall thicknesses in the (a) HRTH and (b) LRTH.

As shown in Figs. 19(b) and (c), the crosstalk temperatures of the cells *xyz* (2; 3; 2, 3) are much larger than those of the cells *xyz* (3; 2; 2, 3), due to the influence of the shared electrodes between the programmed and victim cells. Moreover, the cells *xyz* (3; 3; 2, 3) are affected by four programmed cells simultaneously, and therefore, they have comparable crosstalk temperatures to the cells *xyz* (3; 2; 2, 3), as shown in Fig. 19(d).

D. WALL THICKNESS OF THE THERMAL HOUSE

To clarify the influence of the TH wall thickness on the performance of RRAM, electrothermal simulations of the RRAMs with different TH wall thicknesses are conducted. The resistance ratios of the RRAM cells in the HRTH and LRTH are plotted as a function of the bias voltage in Fig. 20. As the TH wall thickness increases from 5 to 20 nm, the operating voltage of the RRAM cells in the HRTH drops from 0.61 to 0.555 V, while it increases from 0.94 to 1.08 V for the RRAM cells in the LRTH. This is because the increase in TH wall thickness enhances the thermal shielding effect of the HRTH and the thermal sinking effect of the LRTH, respectively. The enhancement of the thermal shielding effect of the HRTH can impede the heat spreading and therefore, cause a higher heating rate. Consequently, lower operating voltage, better performance, and lower power consumption can be achieved. On the contrary, the enhanced thermal sinking effect of the LRTH reduces the heating rate, thereby leading to a higher operating voltage. So, thick TH wall thickness is preferred for the HRTH but the reverse is the case for the LRTH.

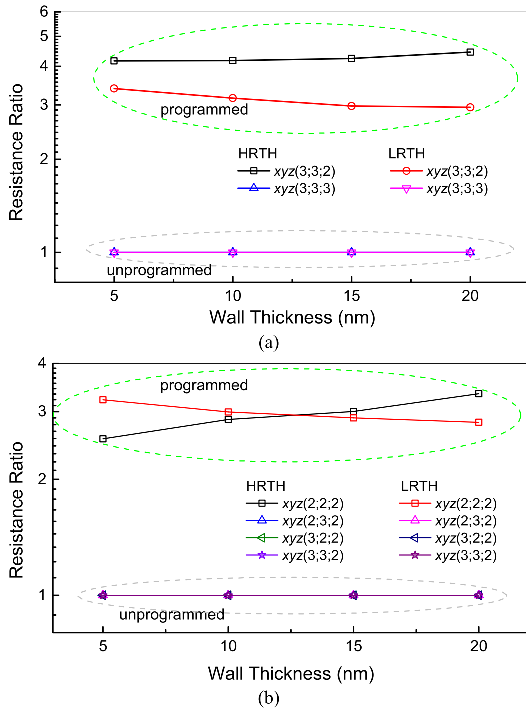

FIGURE 21. Resistance ratio as a function of TH wall thickness for programmed and victim cells in the RRAM arrays operating in the (a) HZ and (b) VR programming schemes.

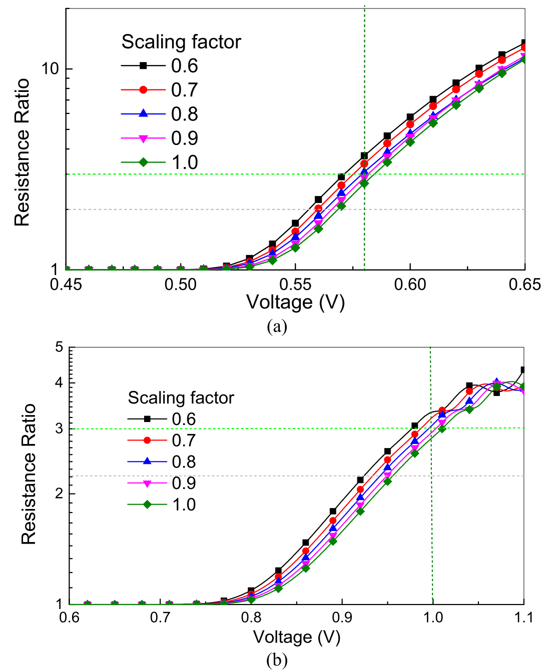

FIGURE 22. Resistance ratio as a function of bias voltage for the RRAM cells with different scaling factors in the (a) HRTH and (b) LRTH.

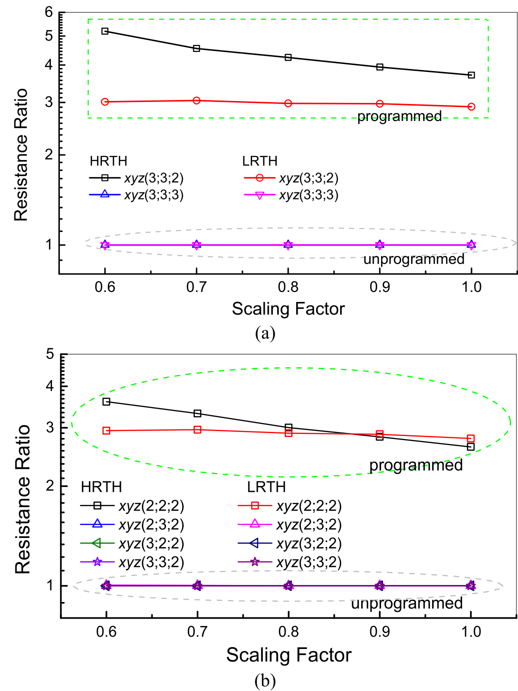

FIGURE 23. Resistance ratio as a function of scaling factor for programmed and victim cells in the (a) HZ and (b) VR programming schemes.

Further, the resistance ratios of the programmed cells and victim cells in the RRAM arrays operating in the HZ and VR programming schemes are plotted in Fig. 21. It is seen that the victims are well protected in these cases.

In summary, the wall thickness has a remarkable influence on the operating voltage, as well as the power consumption, of the programmed RRAM cells, but its effect on the thermal crosstalk is fairly small. That is, the THs can keep high efficiency for thermal crosstalk management.

E. SCALING EFFECT

As technology scaling is always desirable due to lower cost for unit storage space, it is necessary to investigate the scaling of the RRAMs in the TH. To alleviate the thermal effect brought by the electrodes during scaling down as stated in [39], all parts in RRAM cell are scaled down simultaneously [25], thereby keeping the resistance ratio between the electrode and CF stable. The scaling factor is from 1.0 to 0.6 with 0.1 intervals. The resistance ratios of the RRAM cells in the HRTH and LRTH are plotted in Figs. 22(a) and (b), respectively. As the cell scales down, the resistance ratio increases. For instance, as shown in Fig. 22(a), in the case of bias voltage of 0.58 V, the resistance ratio increases from 2.695 to 3.699 with the scaling factor decreasing from 1.0 to 0.6, which is mainly attributed to the increase in power density. A similar phenomenon can be observed in the RRAM cells in the LRTH, as shown in Fig. 22(b). In short, the scaling of RRAMs in the TH can lead to reduced area and power consumption.

Finally, the influence of scaling factor on the RRAM array performance is investigated in Fig. 23. The operating voltage is set as 0.58 and 1.0 V for the RRAM arrays in the HRTH and LRTH, respectively. It is shown that, the resistant ratio of the programmed cell increases as the cell scales down, while the victim cells are well protected from the thermal crosstalk.

V. CONCLUSION

In this paper, two types of 'thermal house' (TH) structures, namely, high thermal resistance TH (HRTH) and low thermal resistance TH (LRTH), have been proposed to facilitate the thermal management in high density RRAM arrays. Their electrothermal characteristics were investigated using a fully coupled electrothermal simulator. The simulated results indicate that both the HRTH and LRTH can suppress the inter- and intra-layer thermal crosstalk effects in the RRAM arrays. Particularly, the power consumption of the RRAMs can be reduced significantly by utilizing the HRTH, which can be further enhanced by increasing the TH wall thickness. In comparison with the LRTH, the HRTH can protect the RRAMs against the environmental interference, which makes it more potential for practical applications. Finally, it was demonstrated that the scaling of the RRAMs in the TH could improve the performances of the programmed cells without distorting the functionality of the TH in suppressing thermal crosstalk.

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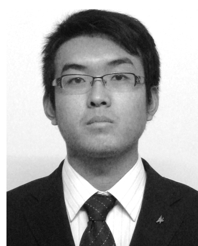

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