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State-of-Charge Balancing Control for ON/OFF-Line Internal Cells Using Hybrid Modular Multi-Level Converter and Parallel Modular Dual L-Bridge in a Grid-Scale Battery Energy Storage System

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ABSTRACT Cell state-of-charge (SoC) balancing within a battery energy-storage system (BESS) is the key to optimizing capacity utilization of a BESS. Many cell SoC balancing strategies have been proposed; however, control complexity and slow SoC convergence remain as key issues. This paper presents two strategies to achieve SoC balancing among cells: main balancing strategy (MBS) using a cascaded hybrid modular multi-level converter (CHMMC) and a supplementary balancing strategy (SBS) using a cascaded parallel modular dual L-bridge (CPMDLB). The control and monitoring of individual cells with a reduction in the component count and the losses of BESS are achieved by integrating each individual cell into an L-bridge instead of an H-bridge. The simulation results demonstrate a satisfactory performance of the proposed SoC balancing strategy. In this result, SoC balancing convergence point for the cells/modules is achieved at 1000 min when cell-prioritized MBS-CHMMC works without SBS-CPMDLB and at 216.7 min when CPMBS-CHMMC works together with SBS-CPMDLB and when the duration required reduces by 78.33 %. Similarly, a substantial improvement in SoC balancing convergence point for the cells/modules is achieved when module-prioritized MBS-CHMMC works together with SBS-CPMDLB; the duration needed to reach the SoC balancing convergence point for the cells/modules is achieved after 333.3 and 183.3 min.

INDEX TERMS Cell balancing, half-bridge multi-level converter, hybrid multi-level converter, lithium-ion battery (Li-ion), state-of-charge (SoC).

I. INTRODUCTION

Large-scale battery energy storage systems (BESSs) are constructed by connecting numerous cells in series or parallel to obtain the desired voltage and capacity ratings [1], [2]. BESS is a promising technology for power grid applications because it has several attractive features, such as improving power grid quality via voltage and frequency disturbance regulation, immediate response to grid demands, enhancing the power supply reliability by providing backup electricity, and accelerating the interaction between electric vehicle and smart grid [3]–[5]. *Lithium-ion* (Li-ion) cells have received considerable interest from researchers due to their several advantages, such as long lifecycle, high specific energy, cell safety, fast charge capability and low self-discharge rate [6]–[8]. However, cell parameter differences as a result of manufacturing tolerances or during BESS operation lead to inequality in *state-of-charge* (SoC) among the cells within a BESS [9]. All cells in a BESS should not be overcharged or deeply discharged [4]; otherwise, the BESS will be forced to stop operating when any cell reaches its voltage limit where the cells are connected in series [10], [11]. Accordingly, the available capacity of BESS is not fully utilized even if

one cell has a different SoC than the others [10]. Therefore, an SoC balancing circuit is required to utilize fully the available capacity of BESS [12], [13].

Different cell-balancing circuits have been stated in the literature [14]–[41]. The circuits are categorized as passive or active depending on their energy trading approaches. Passive cell-balancing circuits [14], [15], also known as dissipative cell-balancing circuits, operate by eliminating excess energy of the cells in the form of heat by connecting a shunt resistor to each cell. The passive approach has advantages, such as simple implementation, small size and low cost. However, it has some drawbacks, such as energy loss, heat problems and its need for a relatively long time to achieve the SoC balancing of cells. Active cell-balancing circuits [16]–[41] are designed to transfer energy among the cells without shunt resistors, where the energy is moved from cells with high energy to cells with low energy. Accordingly, the drawbacks of the passive approach have been overcome. The active approach can be categorized into three distinct methods based on inductors [16]–[18]/transformers [19]–[23], capacitors [24]–[28] and energy converters [29]–[41].

In recent years, modular cascaded H-bridge (MCHB) multi-level converter topologies have received a considerable interest for their use in BESS because of their features of using *MOSFET* switches, possessing inherent modularity and reducing output voltage harmonics [30]. In [31], each individual cell is integrated with a non-isolated DC/DC converter and an additional capacitor to achieve SoC balancing among the cells. However, this topology is unsuitable for grid-scale BESS applications due to the complexity and cost with a lot of cells required. While the researchers in [32]–[36] have proposed to integrate each pack of cells with DC/DC converter and additional capacitors to achieve SoC balancing, the main drawback is the inability to control and monitor each individual cell. In addition, SoC balancing for the internal cells of BESS is not achieved. SoC balancing among the phases and sub-modules has been achieved by using MCHB without adding external balancing circuits [13], [37]–[40]. However, the main drawback of these topologies is that the SoC among the internal cells of BESS is not addressed. SoC balancing among the modules was achieved in [13] by controlling their duty cycle, where each H-bridge of the cascaded topology was connected to a pack of cells and these cells were connected to one another in series. Pack terminal voltage measurements are used to achieve the balancing among the modules which is another drawback for the approach used in [13] due to the inability to provide an accurate estimation of SoC. SoC balancing among the modules was also achieved in [39] by releasing the output power of each module depending on their SoC, and SoC balancing among the three phases was achieved by controlling the zero-voltage component of the output voltage. Each pack of cells is connected to a single converter. Thus, an additional battery management system is required to achieve a balancing among the cells as well as for SoC estimation.

A multi-level battery management system is developed in [40] to address SoC balancing among the cells within a battery pack. Additional DC–AC inverters and a multi-winding transformer are used to achieve SoC balancing at pack level and cell level, respectively. Module balancing and phase balancing are achieved using the same approach employed in [39]. SoC is estimated for each pack instead of each individual cell by using *Extended Kalman* filter to estimate SoC, which is considered an extremely complicated method. SoC balancing among the internal cells of BESS was achieved by integrating each cell into an H-bridge without additional components [11], [41]. Topology [41] has attractive features, such as controlling and monitoring of each individual cell of BESS, SoC balancing for each internal level of BESS cells and increasing the reliability of the system by the possibility of insulation of the failure cells. Moreover, control complexity was addressed in [41] by using a hierarchical control strategy. However, despite the aforementioned attractive features, using a high number of *MOSFET* switches and taking a long duration to achieve SoC balancing among the cells are the drawbacks of this topology. In [42] and [43], a parallel hybrid modular multi-level converter without SoC balancing strategy is proposed. Compared with traditional MCHB, the hybrid MCHB can potentially minimize the number of converter components and power losses [43].

This work aims to address the challenges arising from using hundred thousand cells as required in a grid-scale BESS. The main challenges are control complexity and slow balancing. In this study, two original contributions are included. First, main balancing strategy (MBS) using a cascaded hybrid modular multi-level converter (CHMMC) is proposed to maintain the attractive features of the proposed topology in [11] and [41] while overcoming its drawbacks. In comparison with the topology used in [11] and [41], CHMMC is proposed to reduce the control complexity by reducing the number of *MOSFET* switches to almost half while achieving the same attractive features. Second, supplementary balancing strategy (SBS) using a cascaded parallel modular dual L-bridge (CPMDLB) is proposed to reduce the duration needed to achieve SoC balancing among the cells in a grid-scale BESS. The methodology of this novelty topology is described in *Section II*. The balancing of BESS for the proposed topology using control strategy is presented in *Section III*. Simulation results of the proposed SoC balancing strategy with comparative analysis are discussed in *Section IV*. The experimental set-up is presented in*Section V*, and *Section VI* concludes this paper.

II. METHODOLOGY

A. DESCRIPTION AND CIRCUIT DIAGRAM

Fig. 1 depicts the proposed topology for a three-phase grid-scale BESS. Each phase consists of *Z banks* and *modules* (*M*) and *ZN sub-modules* (*SM*) and *cells*, where *Z* is the number of banks and modules, and *N* is the number of cells and *SM* into each *M*. The value of *N* is unified for all the modules. A *bank*

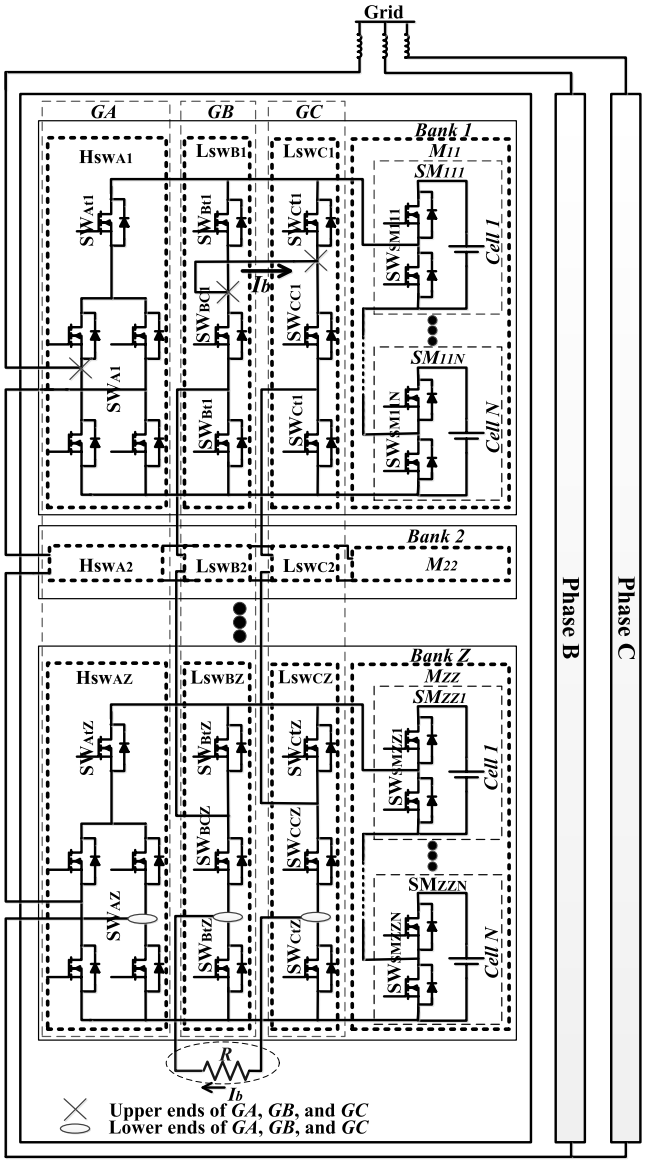

FIGURE 1. Schematic of the proposed topology for a three-phase BESS using CHMMC and CPMDLB.

consists of M, H-bridge group A (H_{SWA}), L-bridge group B (L_{SWB}) and L-bridge group C (L_{SWC}), which are connected in parallel. M is divided into N sub-module connected together in series, where each *SM* consists of an integration of a cell and L-bridge. The H_{SWA} consists of an integration of H-bridge (SW_A) and one additional *MOSFET* switch (SW_{At}). Each L_{SWB} and L_{SWC} contains two L-bridges with a shared *MOSFET* switch (three switches in series), where the terminal switches are SW_{Bt} and SWCt and the center switches are SW_{BC} and SW_{CC} for L_{SWB} and L_{SWC}, respectively. Banks are connected together in a series through three ports via H_{SWA}, L_{SWB} and L_{SWC}. However, in each *bank*, only one of them (H_{SWA}, L_{SWB} or L_{SWC}) can be connected with the related module by controlling their internal switches. Accordingly, the proposed system can divide the modules into three groups, namely, *Group A* (GA), *Group B* (GB) and *Group C* (GC) using H_{SWA}, L_{SWB} and L_{SWC}, respectively; thus, it can distribute the modules over two balancing strategies (i.e., MBS and SBS).

In Fig. 1, *GA* with its corresponding modules is connected to the grid, and the ends of *GB* and *GC* modules are connected together in parallel. Each internal part of *Bank Z*(e.g., H_{SWA1}, L_{SWB1} and L_{SWC1} of *Bank 1*) is connected to an internal part of another *Bank Z* (e.g., H_{SWA2}, L_{SWB2} and L_{SWC2} of *Bank 2*). The capability to independently control each cell to obtain multi-level voltage and current is achieved by integrating each individual cell with an L-bridge. In addition, this stage leads to a possibility of accessing the deteriorated cells for maintenance or replacement without affecting the entire module or the system. A resistor (R) is added between the lower end of *GB* and *GC* to achieve a balancing current (I_b) between them, whereas the upper ends of *GB* and *GC* in *Bank 1* are connected.

B. OPERATING PRINCIPLE AND CELL DISTRIBUTION

The number of cells utilized in M is dependent on the switch status of the sub-modules in M, as illustrated in Fig. 2(a) and Table 1. Each M is directly connected to H_{SWA}, L_{SWB} and L_{SWC}; however, only one of them can utilize M depending on the status of SW_{Atz}, SW_{Btz} and SW_{Ctz}. Figs. 2(b)–2(d) demonstrate three scenarios in utilizing M_{11} in *Bank 1* by H_{SWA1}, L_{SWB1} and L_{SWC1}, respectively. The internal switch status of *Bank 1* in Fig. 2 is presented in Table 1, where the switches have two statuses, that is, either ON (1) or OFF (0).

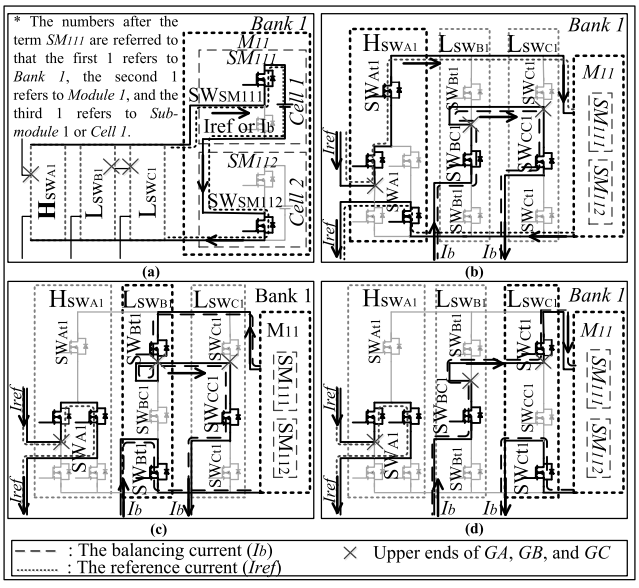

FIGURE 2. Three scenarios of the synchronized movement among the internal switches of *M11*, HswA1, LswB1 and LswC1. (a) Switch status of *SM111* and *SM112* in *M11*. (b) *M11* is only connected to HswA1. (c) *M11* is only connected to LswB1. (d) *M11* is only connected to LswC1.

In Fig. 2(a), two cells in M_{11} ($N = 2$) are connected in series. *Cell 1* of SM_{111} is ON because the L-bridge integrated with it (SW_{SM111}) is ON (1), whereas *Cell 2* of SM_{111} is OFF

TABLE 1. Internal switch status of *Bank 1* for Fig. 2.

Switches	State of switches			
	Fig. 2(a)	Fig. 2(b)	Fig. 2(c)	Fig. 2(d)
SW_{At1}	-	1	0	0
SW_{A1}	-	1 or −1	0	0
SW_{Bt1}	-	0	1	0
SW_{BC1}	-	1	0	1
SW_{Ct1}	-	0	0	1
SW_{CC1}	-	1	1	0
SW_{SM111} and SW_{SM112}	1, 0	1, 0	1, 0	1, 0

because the L-bridge integrated with it (SW_{SM112}) is OFF (0). Accordingly, the number of cells utilized in M depends on the switch status of its corresponding *SMs*. Only one of the terminal internal switches (SW_{Atz}, SW_{Btz} or SW_{Ctz}) of H_{SWAz}, L_{SWBZ} and L_{SWCZ}, respectively, can connect to M within the same *bank*, whereas the other two act as a short circuit (allowing the current to flow through them only without passing through the related cells) for their respective current loop (I_b or I_{ref}), as shown in Figs. 2(b)–2(d), respectively.

Two currents (i.e., I_b and reference current (I_{ref})) flow through the system simultaneously without overlapping. I_{ref} flows between the electrical grid and the cells, which are activated in *GA* through HswA, whereas I_b flows between the cells that have been selected in *GB/GC* through L_{SWB}/L_{SWC}. In Fig. 2(b), M_{11} in *Bank 1* is connected only to H_{SWA1} because its terminal switch (SW_{At1}) is ON (1) (I_{ref} flows through M_{11}), whereas the other terminal switches (i.e., SW_{Bt1} and SW_{Ct1}) of L_{SWB1} and L_{SWC1}, respectively, are OFF (0). The H-bridge integrated into H_{SWA1} is used to synthesize a sinusoidal voltage signal based on its switch status SWA1 as 1 for the positive side, −1 for the negative side or 0 for a short circuit (allows the current to flow through without passing through the related M). I_b flows through L_{SWB1} and L_{SWC1} in *Bank 1* without overlapping with I_{ref} or passing through M, where the center switches (i.e., SW_{BC1} and SW_{CC1}) are ON (1). Fig. 2(c) shows the second scenario, where M_{11} in *Bank 1* is connected only to L_{SWB1} (I_b flows through M_{11}). In addition, I_b flows through L_{SWC1} in the same bank (using the upper ends of *GB* and *GC*, as illustrated in Fig. 1) without overlapping with I_{ref} or passing through M, where its center switch (SW_{CC1}) is ON (1). H_{SWA1} is OFF (0) (short circuit). Fig. 2(d) shows the third scenario, where M_{11} in *Bank 1* is connected only to L_{SWC1}. The operating principle of Figs. 2(b) and 2(d) is similar. Accordingly, I_{ref} and I_b go through all the banks; however, only one of them can flow through a certain M at the same moment. In Fig. 3, a sample form for phase A of BESS after distributing the modules over three groups (i.e., *GA*, *GB* and *GC*) using H_{SWA}, L_{SWB} and L_{SWC} is presented. M_A, M_B and M_C refer to the modules that

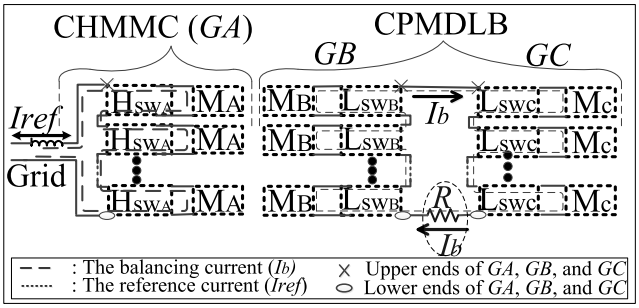

FIGURE 3. Sample form for phase A of a BESS after distributing the modules into three groups at any particular instant of BESS operation.

have been selected by balancing strategy algorithms to be utilized in *GA*, *GB* and *GC*, respectively. Each M is utilized into only one of the groups at each step of a stepped output voltage (V_{out}).

C. CELL SoC ESTIMATION

There are two approaches which are commonly used to implement cell balancing, either by using cell SoC or cell terminal voltages. The accuracy of SoC estimation plays an important role in cell balancing. Therefore, several methods have been proposed to obtain an accurate SoC estimation, as explained in [44]. In this paper, *Coulomb Counting* method is used to estimate cell SoC based on Equation (1), where SoC0, Qmax, and I(t) are initial SoC, maximum capacity of the cell, and current going in and out of a cell, respectively. This method has been described in [41].

$$\mathrm{SoC}\,(t) = \mathrm{SoC}_0 + \frac{1}{\mathrm{Q_{max}}} \int_0^t \mathrm{I}\,(t)\,\mathrm{dt} \tag{1}$$

III. BALANCING OF A BESS FOR THE PROPOSED TOPOLOGY USING CONTROL STRATEGY

Essentially, the operating principle of the balancing strategy depends on generating V_{out} to be as close as possible to a sinusoidal voltage signal (V_{ref}). Thus, the modules are distributed into three groups (i.e., *GA*, *GB* and *GC*) at each step of V_{out} via their switches (H_{SWAZ}, L_{SWBZ} and L_{SWCZ}), as presented in Fig. 2. The number of modules utilized in each group varies with time depending on the V_{out} used in MBS-CHMMC. The MBS-CHMMC and SBS-CPMDLB are proposed to achieve an SoC balancing convergence point among the cells/modules of a BESS. The MBS-CHMMC is applied on *GA*, which has terminals connected to the grid, whereas the SBS-CPMDLB is applied on *GB* and *GC*, which are connected together in parallel via their terminals, as illustrated in Fig. 1. Both balancing strategies work simultaneously on the same BESS of the phase if an SoC difference exists among the internal cells. Otherwise, the SBS-CPMDLB will be isolated and the system will remain working using the MBS-CHMMC alone, because the main objective of the SBS-CPMDLB is to have a fast SoC convergence among the cells. First, the MBS-CHMMC selects its related modules and then the SBS-CPMDLB.

The MBS-CHMMC operates all the time regardless of the SoC because it is connected to the grid. Cells are charged or discharged by the grid through the MBS-CHMMC while keeping them in balance. The MBS-CHMMC and SBS-CPMDLB work together when a BESS is ON-line (charged or discharged by the grid), whereas the SBS-CPMDLB can work by itself and reach the SoC balancing convergence point among the cells when a BESS is OFF-line (no charging or discharging occurs in the grid). The following section explains the MBS-CHMMC and SBS-CPMDLB of the proposed balancing strategy.

A. MBS USING CHMMC

The CHMMC consists of numerous active H_{SWAz}. Each H_{SWAz} (H-bridge integrated with one additional *MOSFET*) is integrated with a single *M*, as presented in Figs. 1 and 2(b). When SW_{Atz} is utilized (SW_{Btz} and SW_{Ctz} are unutilized), the cascaded H-bridge (SW_{Az}) will be connected directly to its corresponding modules, which will lead to the connection of all their internal cells in series. Each cell in *M* is integrated with an individual L-bridge. Accordingly, the proposed topology has high flexibility selecting and utilizes any cell determined by the balancing strategy. The fundamental idea of MBS is to utilize the cells/modules depending on SoC priority to achieve SoC balancing among all the cells/modules. Accordingly, MBS is designed to utilize its cells/modules depending on two levels of prioritizing SoC balancing. First, SoC balancing for the cells is prioritized before the modules, or the other way around. Therefore, the algorithms for a system with cell-prioritized MBS (CPMBS) and module-prioritized MBS (MPMBS) are proposed, as illustrated in Figs. 4 and 5, respectively. Second, the cells with high SoC are prioritized during discharging, whereas the cells with low SoC are prioritized during charging in CPMBS and MPMBS, as illustrated in Fig. 6, in addition to the benefits of operating the MBS-CHMMC.

In Fig. 4, the CPMBS algorithm is designed, such that the SoC difference among the modules is not considered to achieve SoC balancing among them, which is realized when the balancing convergence point among the cells is achieved. The MPMBS algorithm in Fig. 5 is designed to prioritize SoC balancing for the modules before the cells. The SBS-CPMDLB is enabled upon the cell/module selection in the MBS-CHMMC. The notations *a* and *b* in Figs. 4 and 5 refer to the positions of the cells and modules in SoC priority list, respectively. The fundamental idea of MBS and the benefit of using CHMMC are presented in Fig. 6 using six cells with a maximum SoC difference of 45 %, 30 %, 60 %, 40 %, 70 % and 55 %. *Cell 2* has the highest priority in term *a*, whereas *Cell 5* has the lowest priority in the charging status and vice versa. A seven-level output voltage (*t0* to *t12*) is generated during each half duty cycle (either the positive or negative side), as illustrated in Fig. 6(b). Thus, a different number of cells is utilized at each step of V_{out} where the total cell voltage (output voltage) must be as close as possible to V_{ref} (i.e., in Fig. 6(b), *Cell 2* is utilized at *t1* (Step 1),

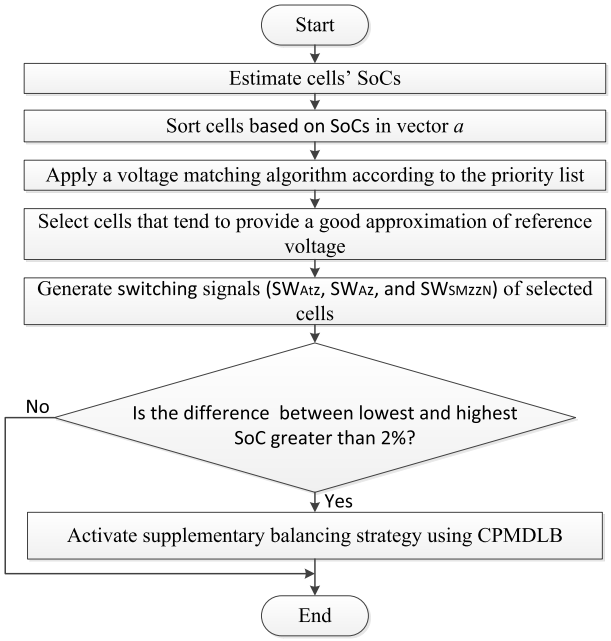

FIGURE 4. CPMBS algorithm.

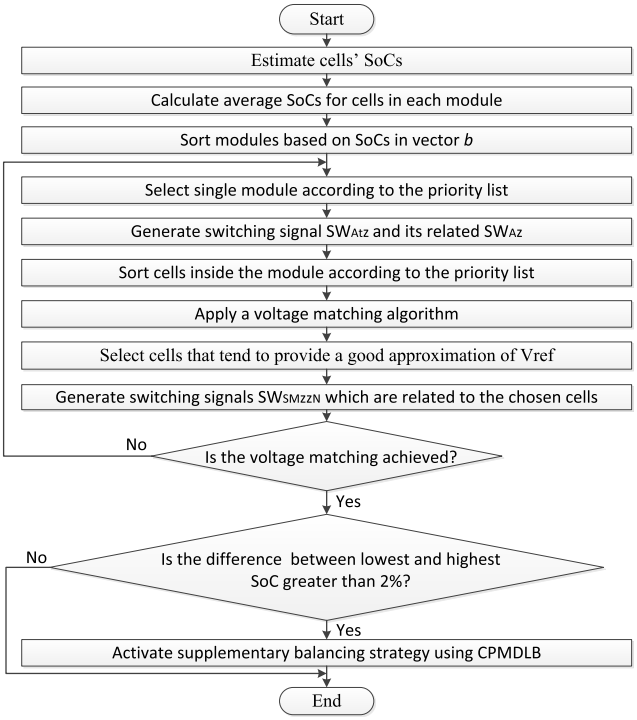

FIGURE 5. MPMBS algorithm.

whereas *Cells 2* and *4* are utilized at *t2* (Step 2), and so on). Accordingly, SoC balancing among the cells will be achieved over time (the fundamental idea of MBS is achieved). SoC balancing is achieved using CHMMC flexibility in selecting the cell determined by the MBS. In addition, V_{out} (positive or negative side) is generated by controlling the switches of cascaded L-bridge (SW_{SMZZN}), as presented in Fig. 6(a).

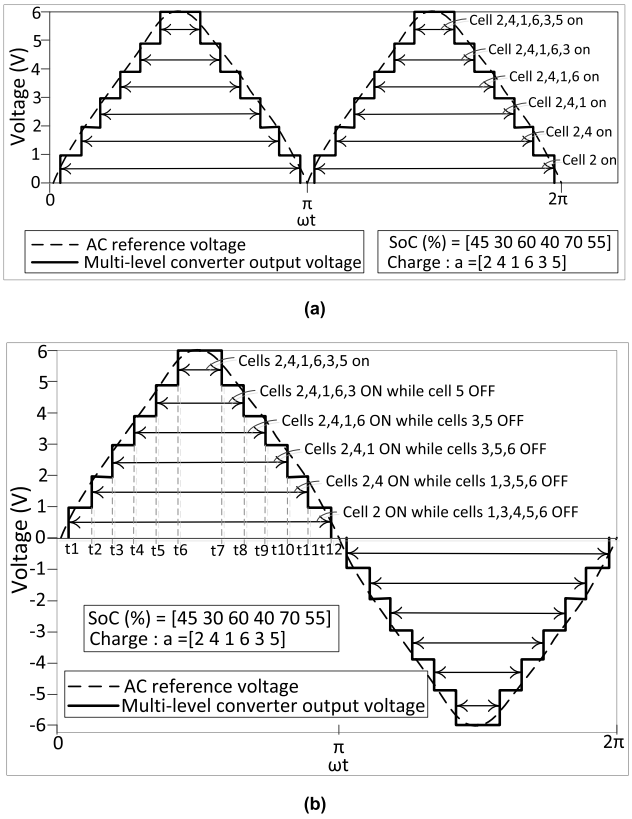

FIGURE 6. **(a) Sub-module's output voltage of a 7-level converter. (b) Stepped sinusoidal waveform of output voltage for a 13-level converter using CHMMC.**

Integrating each M with a H_{SWAZ} leads to the modification of V_{out} to be near to V_{ref} (positive and negative sides), as presented in Fig. 6(b).

B. SBS USING CPMDLB

1) OPERATING PRINCIPLES OF SBS-CPMDLB

The SBS-CPMDLB is enabled when MBS-CHMMC completes selecting its modules with at least two modules in the SBS-CPMDLB. The main objective of using SBS-CPMDLB is to minimize the duration of MBS-CHMMC in achieving SoC balancing convergence point in the entire system (Fig. 7). This objective can be achieved by using a large number of unutilized cells in the MBS at each step of V_{out} to be used in the SBS. Achieving V_{out} as close as possible to a grid voltage (V_{ref}) is necessary in any balancing strategy; thus, numerous cells are needed regardless of their SoC. However, the cells deteriorate in its deep discharging or overcharging states. To avoid this, BESS will be forced to stop operating when any cell reaches its 0 % or 100 % SoC even if the remaining cells have not reached their capacity. Nevertheless, stopping a BESS before reaching SoC balancing convergence point among the cells leads to the non-utilization of their available capacity. Accordingly, achieving SoC balancing convergence point quickly by using the SBS-CPMDLB is important and useful because it eliminates the aforementioned problems.

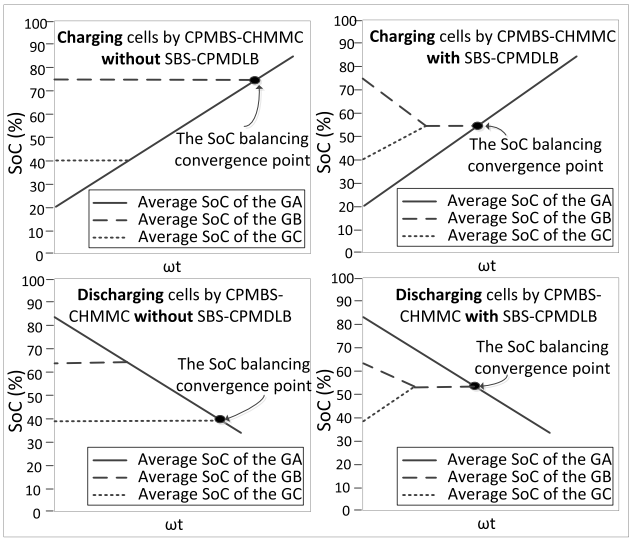

FIGURE 7. **Comparison between the duration needed to achieve SoC balancing convergence point for the cells by the CPMBS-CHMMC with and without the SBS-CPMDLB in charging and discharging statuses.**

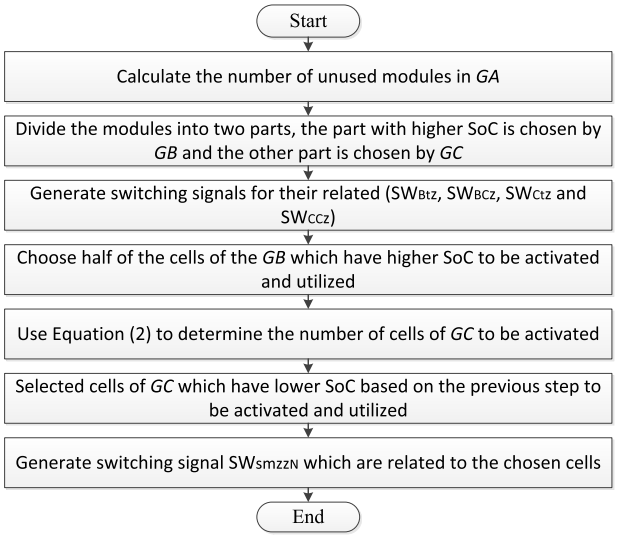

FIGURE 8. **SBS-CPMDLB algorithm.**

As a result, all the cells will reach their 0 % or 100 % SoC after reaching SoC balancing convergence point. Fig. 7 shows the fundamental idea of SBS-CPMDLB, which states that once the MBS selects its modules at each step of V_{out}, the remaining modules of BESS are distributed over two groups (i.e., *GB* and *GC*) depending on the SBS algorithm, as shown in Fig. 8. Fig. 8 shows that the modules with high SoC are selected in *GB* and modules with low SoC are selected in *GC*. Accordingly, the cells' energy in *GB* will be transferred to the cells in *GC* because they are connected in parallel. All the cells in *GB* are connected in series, and the same thing occurs for the cells in *GC*. The SBS-CPMDLB continues to transfer the energy from *GB* to *GC* until an SoC balancing convergence point is achieved among all the cells.

In Fig. 7, the average SoC of *GA* refers to the average SoC of all the cells utilized in the CPMBS-CHMMC, whereas each one of the average SoC of *GB* and *GC* refers to the average SoC of all the cells utilized in each part of SBS (the high SoC is for *GB*, and the low SoC is for *GC*). SoC balancing convergence point occurs when all the internal cells of BESS have the same SoC. During charging, the balancing convergence point is achieved at 75 % of SoC when the CPMBS-CHMMC is used without the SBS-CPMDLB, whereas SoC balancing convergence point is reduced to almost 57 % of SoC with the SBS-CPMDLB. Similarly, in discharging status, SoC balancing convergence point is reduced from 53 % to 40 % of SoC when the CPMBS-CHMMC is used with and without the SBS-CPMDLB, respectively. This finding indicates that a high balancing speed is achieved among the cells with the integration of the SBS-CPMDLB to the CPMBS-CHMMC compared with using the CPMBS-CHMMC by itself.

Unutilized cells in the MBS at each step of V_{out}, which will be used in the SBS, are expected to be present as a result of two sources; the first source of unutilized cells is ∼30 % of the total cells of BESS that are kept as a backup to ensure safe operation, where they will be utilized when BESS needs to operate at full capacity to achieve a grid demand or when some cells of the modules are taken out for replacement. Researchers have recommended using the batteries during the limited 20–80 % of its SoC to maintain a long lifespan [45]. Numerous cells of BESS have been used to generate a voltage or energy on a grid scale. The researchers in [41] used 2,835 of *Li-ion* cells to generate a 380 kWh. To reach a wide range of energy storage capacity of up to 100 MWh with high efficiency, the researchers suggested to use approximately 300,000 individual cells [46]. Accordingly, 30 % of the 300,000 cells are expected to be unutilized as previously mentioned, which will yield a large number of unutilized cells of approximately 90,000.

The second source of unutilized cells can be observed in Fig. 6(b). The cells enter the MBS-CHMMC one by one to generate (discharging) or receive (charging) a sinusoidal output/input voltage, where one cell is utilized at *t1*, then two cells are utilized at *t2*, and so on. Moreover, no cell is utilized at $t = 0$, π and 2π during each duty cycle. Therefore, a large number of the cells will be unutilized at all times during each duty cycle, which can be utilized in the SBS-CPMDLB. The proposed SBS-CPMDLB can reach all the unutilized cells and perform SoC balancing among them. The number of the unutilized cells will change with the time based on the cells that are selected in the MBS-CHMMC. The unutilized cells selected for SBS-CPMDLB strategy are divided into two equal parts as *GB* and *GC*. *GB* has the modules with high SoC, whereas *GC* has the modules with low SoC. Distributing the modules into *GB* and *GC* is achieved by controlling their corresponding switch status (i.e., ON or OFF). *GB* and *GC* terminals are connected in parallel with an additional *R* between them (Fig. 1). The control of the utilized cell number inside *GB* and *GC* is achieved by controlling the status of their switches (SW_{SMZZN}).

In certain cases, some of *GB* cells might have lower SoC than *GC* cells. Therefore, to ensure that the energy of the low SoC cells of *GB* is not transferred to *GC* cells, the number of utilized cells of *GB* is designed to be as half of the total number of the selected cells. The number of utilized cells of *GC* is calculated as follows:

$$\mathrm{cC} = \mathrm{bB} - ([\frac{\mathrm{bB}}{10}] + 1), \tag{2}$$

where *bB* and *cC* are the number of utilized cells in *GB* and *GC*, respectively; and [*bB*/10] refers to the greatest integer after dividing (*bB*) over 10. The algorithm for the SBS using CPMDLB is shown in Fig. 8. In Fig. 8, once module selection in the MBS is performed, the SBS-CPMDLB will start to take its modules and divide them into *GB* and *GC* based on their average SoC. The utilized cells of each one of them are selected based on the design proposed in this study, which will be described in the next section. Finally, the signals to control the switch status are generated.

2) DESIGN OF SBS-CPMDLB

The internal cells of *GB* are connected in series and in parallel with *GC*. Moreover, the internal cells of *GC* are connected in series and in parallel with *GB*, as shown in Fig. 9. When cells are connected in parallel, self-balancing will automatically occur among them over time based on their voltage difference, where the energy will be transferred from cells with high voltage to the cells with low voltage [47]. To control the energy transferred from the high-voltage cells to low-voltage cells, the corresponding I_b, which is drawn from the utilized cells of *GB* and provided to the utilized cells of *GC*, must be controlled. This situation can be achieved by obtaining a suitable voltage difference between *GB* and *GC*. I_b is given in Equation (3), which is calculated through the application of

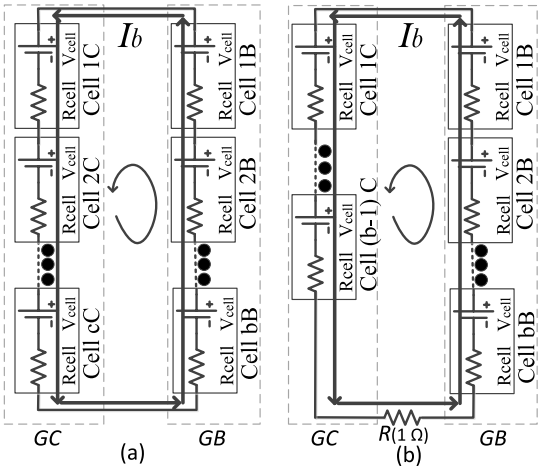

FIGURE 9. Schematic of the basic operating principle of SBS-CPMDLB, and direction of energy transfer. (a) Equal number of cells for *GB* and *GC* without *R*. (b) Unequal number of cells for *GB* and *GC* with *R*.

Kirchhoff's second law on the circuit of the SBS-CPMDLB presented in Fig. 9(a). *b* and *c* are the number of utilized cells into *GB* and *GC*, respectively.

$$\mathrm{I_b} = \frac{\sum_1^{\mathrm{b}} \mathrm{Vcell\ bB} - \sum_1^{\mathrm{c}} \mathrm{Vcell\ cC}}{\sum_1^{\mathrm{b}} \mathrm{Rcell\ bB} + \sum_1^{\mathrm{c}} \mathrm{Rcell\ cC}} \tag{3}$$

Manufactured batteries have many types; each type has a particular current limit (the maximum permissible current for the charging or discharging status), where the battery health will be deteriorated when the current exceeds its limit. Therefore, the value of I_b used in the SBS-CPMDLB must be below the limit. Furthermore, the benefit of using SBS-CPMDLB will continue to decline whenever I_b decreases. I_b status is considered dangerous when its value approaches 4.2 A and is considered to have no benefit when its value goes below 0.5 A, because the maximum permissible current of *Li-ion* cell is 4.2 A, as illustrated in Table 2. In this study, *Panasonic CGR18650CG Li-ion* cells are used based on the electrical model [48]; each cell consists of an internal cell voltage and a resistor connected in series. Table 2 presents the characteristics of the *Li-ion* cells [49]. Based on *Li-ion* cell characteristics, activating the same number of cells for *GB* and *GC* will lead to obtaining a small voltage difference between them, and accordingly, a small I_b will be achieved (no benefit). To overcome this, a different number of cells should be utilized inside *GB* and *GC* to increase the voltage difference between them. However, the small *Rcells* will lead to extremely high I_b. Therefore, $R = 1\ \Omega$ is added between *GB* and *GC* to ensure that I_b is operating within the safety margin and is beneficial (Fig. 9(b)). The new I_b for the SBS-CPMDLB is calculated as

$$\mathrm{I_b} = \frac{\sum_1^{\mathrm{b}} \mathrm{Vcell\ bB} - \sum_1^{\mathrm{b-1}} \mathrm{Vcell\ bC}}{\sum_1^{\mathrm{b}} \mathrm{RcellbB} + \sum_1^{\mathrm{b-1}} \mathrm{RcellbC} + vR}. \tag{4}$$

TABLE 2. Characteristics of *Li-ion* cells.

Characteristics of *Li-ion* cells	Value
Internal resistances (*Rcells*)	0.07–0.09 Ω
Internal voltages (*Vcells*) when the SoC is between 20 % and 80 %	3.3–3.6 V
Current limit	4.2 A

However, the number of utilized cells in *GB* and *GC* (i.e., *bB* and *cC*, respectively) and the difference between them (*bB*−*cC*) are the two main factors affecting I_b in the SBS-CPMDLB. Accordingly, a mathematical analysis of four sequential scenarios (each scenario overcomes the drawbacks in previous scenario) is used to derive Equation (5) (the best value for *cC* is obtained when *bB* is equal to half of the cells selected in *GB* based on the SBS algorithm), as presented in Table 3 and Fig. 10. I_b is calculated using Equation (4) with and without *R* for all scenarios. *Vcells* will almost be the same for SoC ranging from 20-80 %, as shown in Table 2. Therefore, two cases that the batteries can operate on are used, namely, *extreme*and *practical cases*. An *extreme case* occurs when the utilized cells of *GC* have SoC lower than 20 % and the utilized cells of *GB* have SoC higher than 80 %, which will lead to an extremely high voltage difference. The *practical case* occurs when all the cells have SoC between 20 % and 80 %, which will lead to a small voltage difference. The average voltage of each cell of *GB* and *GC* is 3.6 V and 3.3 V for *extreme* case and 3.48 V and 3.44 V for *practical case*, respectively. *Rcell* is assumed as 0.08 Ω for all cells, and *R* is assumed as 1 Ω.

For the SBS-CPMDLB to be significant, two conditions, namely, *useful* and *safe*, must be achieved in *extreme* and *practical* cases when choosing the number of utilized cells for *GB* and *GC*. As shown in Table 3 and Fig. 10, when $bB{-}cC = 0$ in a *practical case* (Scenario 1 in Fig. 10(a)), neither danger nor benefit is observed from the produced I_b. In *extreme case*, some cases where *useful* condition is not achieved are used. Moreover, *non-useful* and *dangerous* conditions will occur when the difference in the number of cells is more than one ($bB{-}cC = 2$ or 3; Scenario 2 in Fig. 10(b)). However, in *practical* and *extreme cases* when ($bB{-}cC = 1$) and when *R* is added (Scenario 3 in Fig. 10(c)), *useful* and *safe* conditions are achieved; thus, the SBS-CPMDLB is significant, whereas *dangerous* condition occurs for the same status without *R*. Moreover, when the number of utilized cells in *GB* and *GC* is increased (while $bB{-}cC = 1$ and *R* is added; Fig. 10(c)), the value of I_b decreases. As a result of the current reduction, the SBS-CPMDLB tends to be insignificant because one of the conditions might not be achieved. In Fig. 10(d) (Scenario 4), I_b has a value of 3.15 A for the *extreme* case and 2.84 A for the*practical case* when *bB* and*cC* are 2 and 1, respectively. In the *extreme case*, I_b is then reduced to 2.5 A when *bB* and *cC* are 10 and 9 and

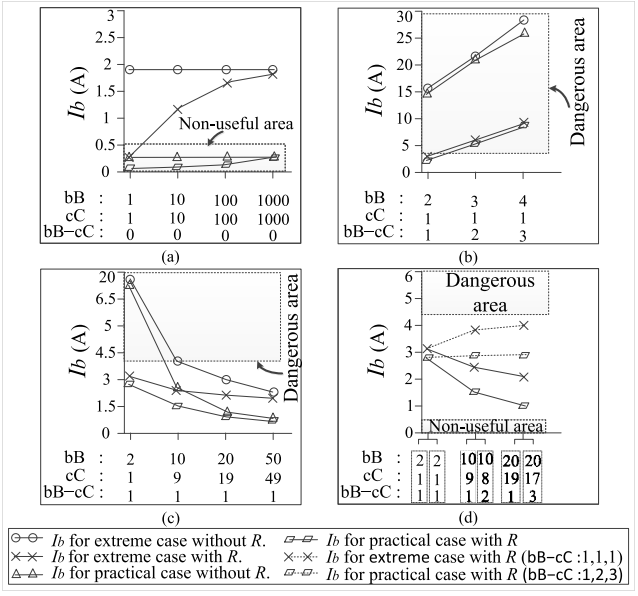

FIGURE 10. Four scenarios to choose different values of bB−cC and its effect on *Ib* value. (a) I_b for *extreme* and *practical cases* with and without *R* when (bB−cC = 0), (b) (bB−cC = 1, 2 and 3) and (c) (bB−cC = 1). (d) Comparing I_b when (bB−cC = 0) and (bB−cC = 1, 2 and 3) for *extreme* and *practical* cases with *R*.

TABLE 3. Effects of the Difference between the Numbers of Utilized Cells for *GB* and *GC* on *Ib* with and without *R*.

D	*Dangerous*	N	*Safe*			U	*Useful*			X	*Non-useful*					
Number of utilised cells in *GB* (*bB*)	Number of utilised cells in *GC* (*cC*)	*bB*–*cC*	*Extreme case*						*Practical case*							
			Ib without *R*			*Ib* with *R*			*Ib* without *R*			*Ib* with *R*		
1	1	0	1.88 A	N	U	0.26 A	N	U	0.25 A	N	X	0.03 A	N	X
10	10	0	1.88 A	N	U	1.15 A	N	U	0.25 A	N	X	0.15 A	N	X
100	100	0	1.88 A	N	U	1.77 A	N	U	0.25 A	N	X	0.24 A	N	X
1,000	1,000	0	1.88 A	N	U	1.86 A	N	U	0.25 A	N	X	0.25 A	N	X
2	1	1	16.25 A	D	X	3.15 A	N	U	14.7 A	D	X	2.84 A	N	U
3	1	2	23.44 A	D	X	5.7 A	D	X	21.9 A	D	X	5.3 A	D	X
4	1	3	27.75 A	D	X	7.93 A	D	X	26.2 A	D	X	7.4 A	D	X
10	9	1	4.15 A	D	X	2.5 A	N	U	2.56 A	N	U	1.52 A	N	U
10	8	2	6.67 A	D	X	3.93 A	N	U	5.06 A	D	X	2.98 A	N	U
20	19	1	2.98 A	N	U	2.26 A	N	U	1.36 A	N	U	1.03 A	N	U
20	17	3	5.37 A	D	X	4.02 A	N	U	3.76 A	N	U	2.81 A	N	U
50	49	1	2.31 A	N	U	2.05 A	N	U	0.68 A	N	X	0.61 A	N	X

reduced to 2.26 A when *bB* and *cC* are 20 and 19, respectively. In the *practical case*, I_b is then reduced to 1.52 A when *bB* and *cC* are 10 and 9 and reduced to 1.03 A when *bB* and *cC* are 20 and 19, respectively. However, in the *extreme case*, I_b increases to a suitable value of 3.93 A when *bB* and *cC* are changed to 10 and 8 and becomes 4.02 A when *bB* and *cC* are changed to 20 and 17, respectively. In the *practical case*, I_b increases to 2.98 A when *bB* and *cC* are changed to 10 and 8 and becomes 2.081 A when *bB* and *cC* are changed to 20 and 17, respectively. Accordingly, Equation (5) is used to prevent I_b from decreasing, which is due to the huge increase in *bB* and *cC*. [*bB*/10] refers to the greatest integer after dividing the number of utilized cells of *GB* (*bB*) over 10.

$$\mathrm{cC} = \mathrm{bB} - ([\frac{\mathrm{bB}}{10}] + 1) \tag{5}$$

A number of cells of up to 4,000 are tested the in SBS-CPMDLB to validate Equation (5). The calculated results of the modified method of determining the suitable number of cells are presented in Table 4 and Fig. 11. In Table 4 and Fig. 11, I_b has suitable values for *extreme* and *practical cases* with *R*, which confirms the validity of Equation (5) in determining the number of utilized cells in*GC* at each step of V_{out}, which makes the I_b values below the limit (below 4.2 A). Moreover, a *dangerous* condition will occur for the same strategy without *R*. The SBS-CPMDLB with *R* is shown to be significant, whereas the SBS-CPMDLB without *R* is not. The number of utilized cells of *GB* is designed to be half the total number of the selected cells. The number of modules, which are selected for the SBS-CPMDLB, is the same in *GB* and *GC*. Accordingly, for the 1,000 cells utilized in *GB* (Table 4), the total number of cells selected in the SBS-CPMDLB is 4,000 cells, apart from the number of cells selected by the MBS-CHMMC. This finding validates the practicality of this novel topology for a grid-scale BESS.

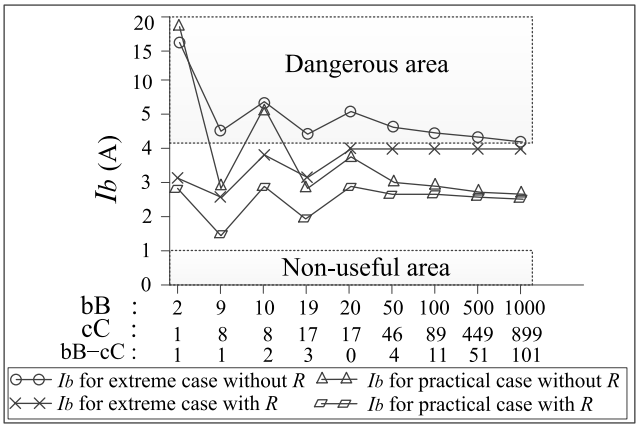

FIGURE 11. Comparing *Ib* values for extreme and practical cases with and without *R* while using a high number of cells in Equation (5).

IV. SIMULATION RESULTS OF THE PROPOSED SOC BALANCING STRATEGY WITH COMPARATIVE ANALYSIS

MATLAB Simulink software (*R2017b*) is used in this study to verify the operational feasibility and performance of the novel topology and the proposed balancing strategy. The proposed topology has four SoC balancing strategies (i.e., CPMBS, MPMBS, CPMBS-SBS and MPMBS-SBS). The simulation results validate that the CPMBS and the MPMBS can achieve SoC balancing for the cells/modules and keep them in balance during charging and discharging. In addition, the substantial improvement of their durations needed to achieve SoC balancing for the cells/modules are validated when integrating CPMBS and MPMBS with SBS, respectively. *Panasonic CGR18650CG Li-ion* cells are used in this study. Each *Li-ion* cell has a nominal voltage of 3.6 V and a standard capacity of 2250 mAh [49]. A simulation model for the proposed topology in Fig. 1 is implemented using the cell model in [48], [50] and the datasheet in [49]. *Coulomb Counting* method is used to estimate cell SoC. The proposed work consists of 12 cells, which are divided into six banks and six modules, where each module has two sub-modules.

The results obtained from the simulation model are presented in Figs. 12–20. The proposed SoC balancing strategy can use the MBS-CHMMC alone or integrated with SBS-CPMDLB. The MBS-CHMMC is divided into CPMBS and MPMBS, depending on whether cells or modules are

TABLE 4. Calculated results of *Ib* using the modified method.

D	*Dangerous*	N	*Safe*	U	*Useful*	X	*Non-useful*

Number of utilised cells in *GB* (*bB*)	Number of utilised cells in *GC* (*cC*)	*bB*–*cC*	*Extreme case*						*Practical case*					
			I_b without R			I_b with R			I_b without R			I_b with R		
2	1	1	16.25 A	D	X	3.15 A	N	U	14.7 A	D	X	2.84 A	N	U
9	8	1	4.41 A	D	X	2.54 A	N	U	2.79 A	N	U	1.6 A	N	U
10	8	2	6.67 A	D	X	3.93 A	N	U	5.06 A	D	X	2.98 A	N	U
19	17	2	4.27 A	D	X	3.17 A	N	U	2.65 A	N	U	1.97 A	N	U
20	17	3	5.37 A	D	X	4.02 A	N	U	3.76 A	N	U	2.81 A	N	U
30	26	4	4.96 A	D	X	4.05 A	N	U	3.34 A	N	U	2.73 A	N	U
40	35	5	4.75 A	D	X	4.07 A	N	U	3.13 A	N	U	2.69 A	N	U
50	44	6	4.63 A	D	X	4.08 A	N	U	3.01 A	N	U	2.66 A	N	U
100	89	11	4.38 A	D	X	4.11 A	N	U	2.77 A	N	U	2.6 A	N	U
500	449	51	4.19 A	D	X	4.13 A	N	U	2.57 A	N	U	2.54 A	N	U
1,000	899	101	4.17 A	N	U	4.14 A	N	U	2.55 A	N	U	2.53 A	N	U

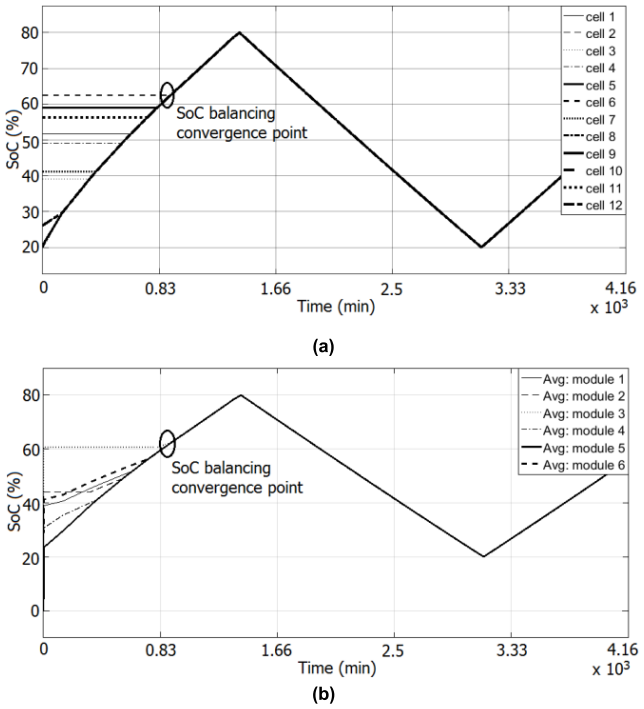

FIGURE 12. CPMBS-CHMMC works without SBS-CPMDLB. (a) Cell SoC balancing. (b) Module SoC balancing.

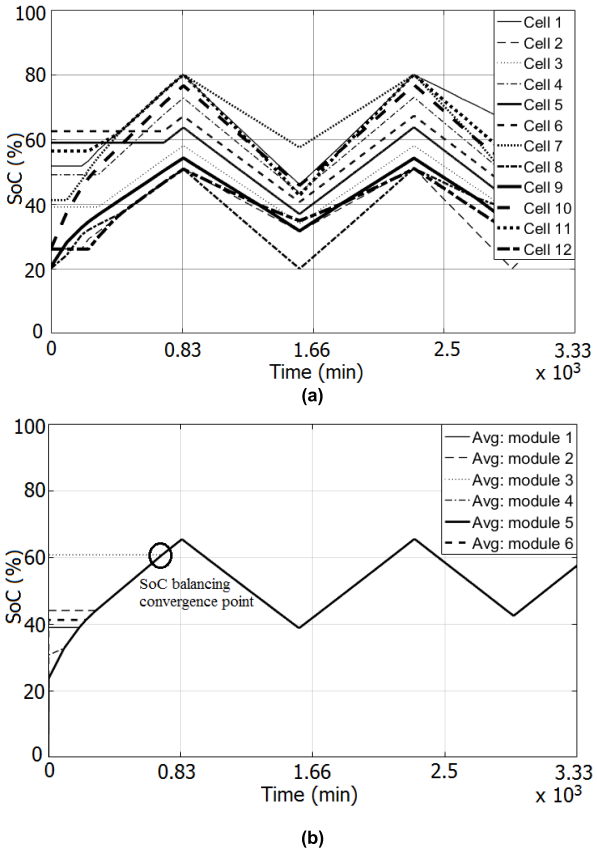

FIGURE 13. MPMBS-CHMMC works without SBS-CPMDLB. (a) Cell SoC balancing. (b) Module SoC balancing.

prioritized in the balancing of the cells, respectively. The results obtained from the proposed topology using the CPMBS-CHMMC (algorithm in Fig. 4) and the MPMBS-CHMMC (algorithm in Fig. 5) without the SBS-CPMDLB are presented in Figs. 12 and 13, respectively. A substantial improvement on the performance of the proposed topology is observed when the CPMBS-CHMMC and MPMBS-CHMMC are integrated with the SBS-CPMDLB (algorithm in Fig. 8), as presented in Figs. 14 and 15, respectively. Table 5 presents a comparison of the proposed topology with existing research in terms of the control complexity, applications, controlling and monitoring of each individual cell, feasibility in grid-scale BESS, SoC balancing method, and the main limitations. While a comparison between the proposed balancing strategies and the balancing strategy in [11] and [41] is presented in Table 6 to show the main advantages of the proposed balancing strategy. In Table 5, control complexity is evaluated depending on the necessity of cell voltage monitoring as well as the number of the control and sensing signals. Random initial SoC ranging from 20-65 % is also used, as shown in Figs. 12–15.

SoC balancing for cells/modules when the CPMBS-CHMMC works without the SBS-CPMDLB is presented in Figs. 12(a) and 12(b), respectively. SoC balancing for

TABLE 5. Comparison of the proposed topology with some existing research in literature.

Balancing strategy	Control complexity	Applications	Controlling and monitoring of each individual cell	Appropriate for execution in grid-scale BESS	SoC balancing method	Main limitations
Young et al. [13]	Medium	Medium/High Power	No	Appropriate	By controlling the modules' duty cycle	SoC estimation is inaccurate. High computational complexity (switching angle is achieved by *Newton-Raphson*)
Wang et al. [31]	High	Low/Medium Power	Yes	Inappropriate	Using DC/DC converter and an additional capacitor	Requires additional balancing circuit
Yang et al. [35]	High	Low/Medium Power	No	Inappropriate	Using an improved circuit of DC/DC converter with additional capacitors	Requires additional balancing circuit
Maharjan et al. [39]	High	Medium/High Power	No	Appropriate	Controlling the zero-voltage component of the output voltage and using the modules depending on their SoC	Requires battery management system to achieve a balancing among the cells
Ooi et al. [41]	Medium	Medium/High Power	Yes	Appropriate	Utilizing cells' energy depending on their SoC within a hierarchical control strategy	Using a high number of switches and taking a long duration for SoC balancing. Extra peak sharing algorithm is required.
Proposed topology	Medium	Medium/High Power	Yes	Appropriate	Utilizing cells' energy depending on their SoC and transferring the energy from the cells with higher energy to the cells with lower energy	Balancing between three phases is not addressed. SBS is not required once SoC balancing is achieved

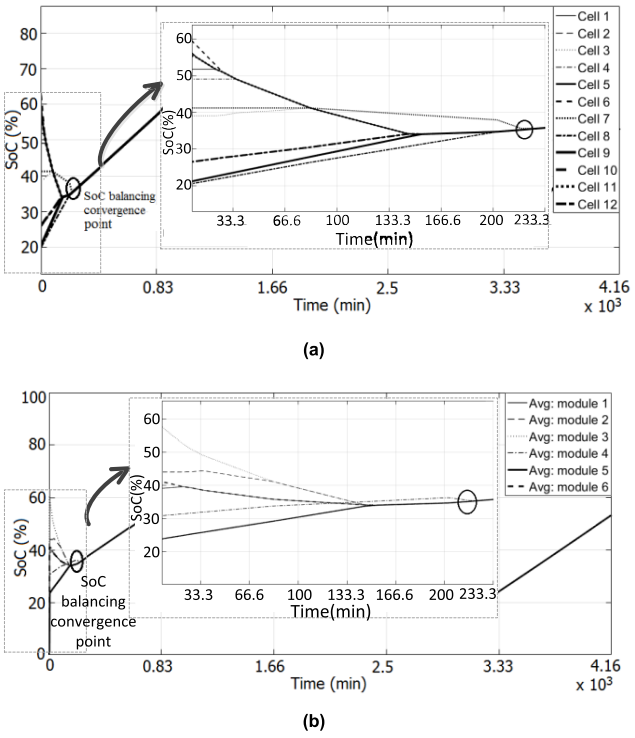

FIGURE 14. CPMBS-CHMMC works together with SBS-CPMDLB. (a) Cell SoC balancing. (b) Module SoC balancing.

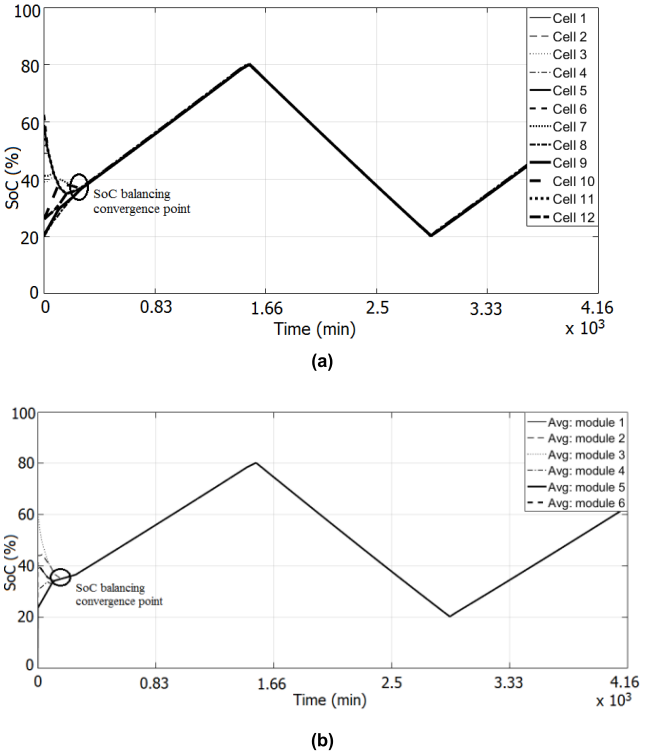

FIGURE 15. MPMBS-CHMMC works together with SBS-CPMDLB. (a) Cell SoC balancing. (b) Module SoC balancing.

cells/modules is achieved approximately 1,000 min after the start of the operation. The SoC of all cells stays the same even after the convergence point for charging and discharging. The same balancing strategy in [11] and [41] (prioritize SoC balancing for the cells before the modules) is employed in the CPMBS-CHMMC to achieve SoC balancing among the cells. Thus, the duration required to obtain SoC balancing among the cells using the CPMBS or the balancing strategy

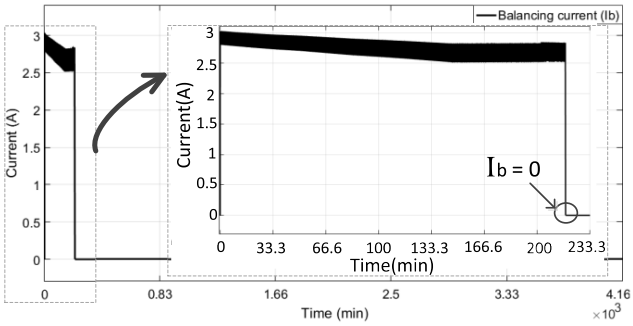

FIGURE 16. Balancing current of SBS-CPMDLB.

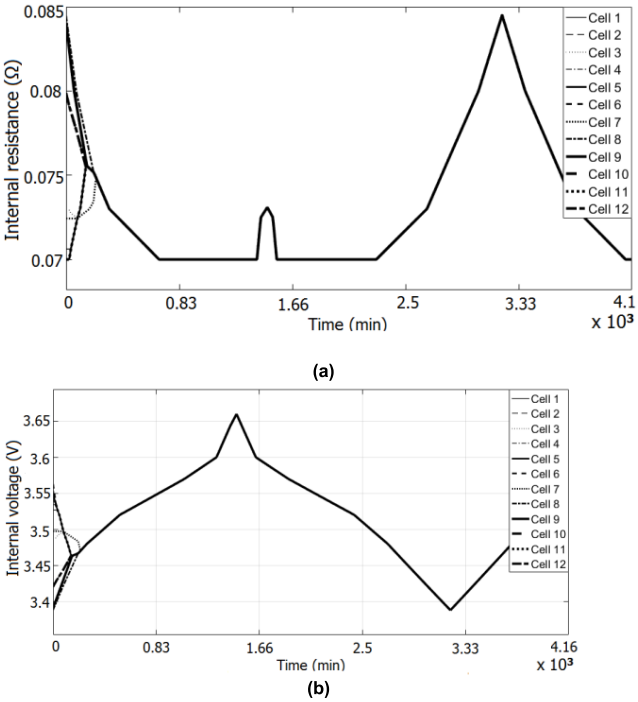

FIGURE 17. Relationship between the internal characteristics of *Li-ion* cells with their SoC. (a) Internal resistances. (b) Internal voltages.

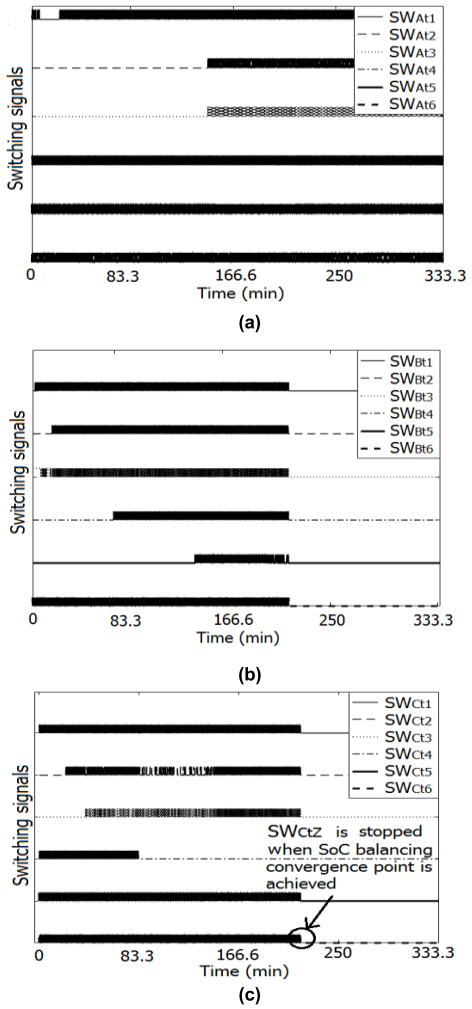

FIGURE 18. Switching signals. (a) SWAtZ, (b) SWBtZ and (c) SWCtZ.

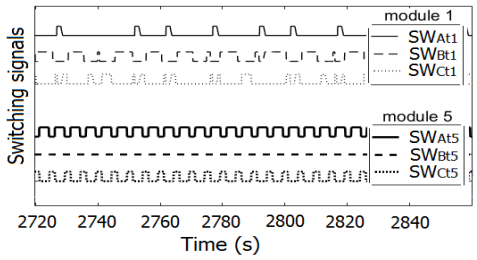

FIGURE 19. Comparison between the synchronized movement of the internal switches (SWAtZ, SWBtZ and SWCtZ) in *Modules 1* and 5.

in [11] and [41] will be similar as long as both topologies are operated with the same number of cells and V_{ref}.

SoC balancing for cells/modules when the MPMBS-CHMMC works without the SBS-CPMDLB is presented in Figs. 13(a) and 13(b), respectively. The MPMBS-CHMMC takes a longer time than the CPMBS-CHMMC to reach SoC balancing convergence point among the cells, as shown in Fig. 13(a). The MPMBS-CHMMC aims to achieve SoC balancing convergence point among the modules, and the SoC stays the same for charging and discharging (Fig. 13(b)). SoC balancing convergence point among the modules is achieved after approximately 666.6 min after the start operation, whereas SoC balancing convergence point among the cells is not achieved during the simulation time (4,166.6 min). In Fig. 13(a), the BESS switches from charging to discharging at 833.3 min before reaching SoC balancing convergence point among the cells, which leads to the non-utilization of their available capacity. Achieving SoC balancing convergence point among the modules early is preferable to increase the speed of realizing SoC balancing convergence point among the three phases. However, BESS still needs to obtain SoC balancing convergence point among the cells and the modules within a short duration.

SoC balancing for the cells/modules when the CPMBS-CHMMC works together with the SBS-CPMDLB is

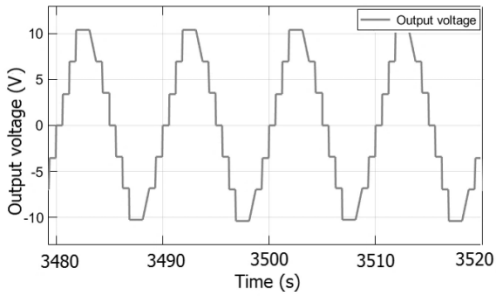

FIGURE 20. Generating a stepped sinusoidal waveform of output voltage (*Vout*) by CHMMC.

presented in Figs. 14(a) and 14(b), respectively. Some cells are charging (which are selected by *GA* and *GC* to operate within CPMBS and SBS, respectively), whereas the others (selected by *GB* to operate within SBS) are discharging for the same duration at the beginning of the operation. The charging and discharging statuses of the cells continue operating together until SoC balancing convergence point is achieved at 216.7 min. Accordingly, the CPMBS-CHMMC and SBS-CPMDLB are operating simultaneously, and the modules are divided into three blocks (i.e., *GA*, *GB* and *GC*), as explained in *Section II*. The SBS-CPMDLB stops operating when SoC balancing convergence point among the cells/modules is achieved, whereas CPMBS-CHMMC continues to operate for charging and discharging (from t = 216.7 min to t = 4,166.6 min) to maintain SoC balancing convergence point. When the CPMBS-CHMMC works together with the SBS-CPMDLB, SoC balancing convergence point among the cells/modules is achieved at the same duration at approximately 216.7 min, which is considered a significant improvement in the performance compared to working with the CPMBS-CHMMC alone. This phase takes approximately 1,000 min, as shown in Fig. 12 and Table 6.

TABLE 6. Comparison between the Proposed Balancing Strategies and Those in [11] and [41].

Balancing strategy	Features	
	Main elements required to balance *N cell* in *Z module*	Duration required to achieve SoC balancing among the cells/modules
Balancing strategy in [11] and [41]	4NZ + 4Z *MOSFET* switch	1,000 min for cells/modules
CPMBS-CHMMC (Fig. 12)	2NZ + 4Z *MOSFET* switch	1,000 min for cells/modules
CPMBS-CHMMC works together with SBS-CPMDLB (Fig. 14)	2NZ + 4Z +6Z *MOSFET* switch	216.7 min for cells/modules
MPMBS-CHMMC (Fig. 13)	2NZ + 4Z *MOSFET* switch	Was not achieved for cells; 666.6 min for modules
MPMBS-CHMMC works together with SBS-CPMDLB (Fig. 15)	2NZ + 4Z +6Z *MOSFET* switch	333.3 min for cells. 183.3 min for modules

SoC balancing for the cells/modules when the MPMBS-CHMMC and SBS-CPMDLB work together is presented in Figs. 15(a) and 15(b) respectively. The operating characteristics of the MBS and SBS are explained in Figs. 12–14. When the MPMBS-CHMMC works together with SBS-CPMDLB, SoC balancing convergence point among the cells/modules is achieved at approximately 333.3 min and 183.3 min after the start operation, respectively. This situation is considered a substantial improvement in the performance compared with operating with MPMBS-CHMMC alone, which is expected to take more than 4,166.6 min to achieve SoC balancing convergence point among the cells, as presented in Fig. 13 and approximately 666.6 min to achieve SoC balancing convergence point among the modules. Hence, achieving SoC balancing convergence point quickly is essential to ensure that the available capacity of the cells is fully utilized.

Clearly, a significant difference is not observed in terms of the duration required to obtain SoC balancing convergence point among the cells/modules when the CPMBS-CHMMC or MPMBS-CHMMC works together with the SBS-CPMDLB, as illustrated in Table 6. The SBS-CPMDLB can reach the unutilized cells during the operation of BESS, thereby achieving SoC balancing convergence point quickly. This condition potentially leads to SoC convergence among the three phases in a short time, thereby obtaining the stability in the electrical grid. The ratio of substantial improvement on the duration needed to achieve SoC balancing by CPMBS strategy or by the balancing strategy in [11] and [41] up to 73 % is achieved when the CPMBS-CHMMC works together with the SBS-CPMDLB (Table 6). In addition, it provides the capability to control and monitor each individual cell and direct the *DC–AC/AC–DC* grid interface.

Figs. 16–20 show the behavior of I_b and the switch status when the CPMBS-CHMMC works together with the SBS-CPMDLB (Fig. 14). I_b stops (Ib = 0) when SoC balancing convergence point among the cells is achieved at approximately 216.6 min. I_b ranging from 2.5 A to 3 A is recommended to ensure safe operation and preserve cell lifespan, as explained in *Section III*. I_b values confirm the validity of Equation (5) in determining the number of utilized cells in *GC* at each step of V_{out}, which makes the I_b values below the limit (below 4.2 A). The simulation of the relationship between the internal characteristics of *Li-ion* cells and respective SoC is presented in Fig. 17. At the beginning of the operation, a small difference among *Rcells* and *Vcells* is observed at approximately 0.015 Ω and 0.26 V, respectively, due to the SoC difference between them (Fig. 14); this difference becomes zero when SoC balancing convergence point is achieved, as presented in Figs. 17(a) and 17(b), respectively. The relationship among *Vcells* and *Rcells* with their SoC is nonlinear, as shown in Figs. 14 and 17, respectively.

In *Section II*, the proposed SoC balancing strategy in this study divides the modules into three groups (i.e., *GA*, *GB* and *GC*) by controlling their corresponding switches (SW_{AtZ}, SW_{BtZ} and SW_{CtZ}) as ON or OFF (Fig. 18).

TABLE 7. Characteristics of the *NiMH* cell.

Nominal voltage	Maximum charged voltage	Nominal capacity	Internal resistance	Cut-off voltage
1.2 V	1.5 V	2000 mAh	20 mΩ	0.95 V

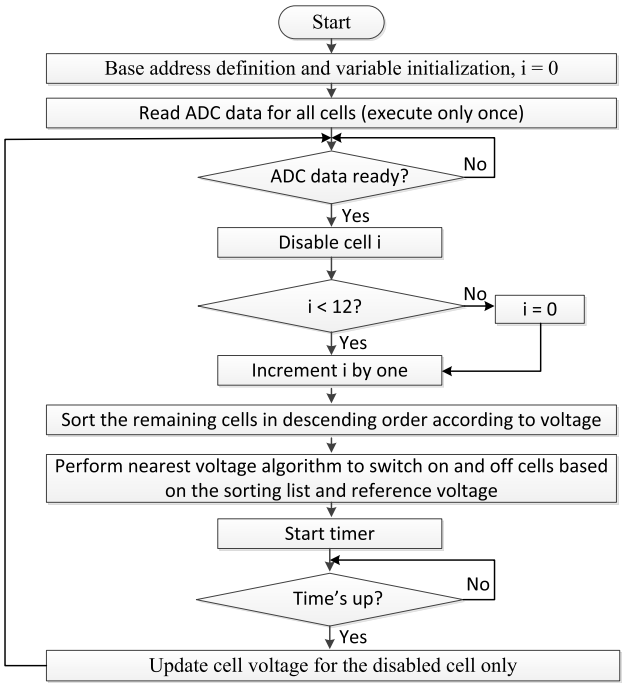

FIGURE 21. CPMBS flowchart based on *pseudo-OCV*.

SWAtZ continues operating all the time (Fig. 18(a)), whereas SWBtZ and SWCtZ are stopped (unutilized) when SoC balancing convergence point is achieved at approximately 216.6 min (Figs. 18(b) and 18(c), respectively). At any given time, each module can connect to a single switch, namely, SW_{AtZ}, SW_{BtZ} or SW_{CtZ}, as illustrated in Fig. 19 (inside the same module when any switch of SW_{AtZ}, SW_{BtZ} or SW_{CtZ} is ON and the other two of them is OFF). A semi-sinusoidal reference signal is generated by the MBS-CHMMC in Fig. 20. V_{out} of a seven-level converter is generated during each duty cycle using the CHMMC.

V. EXPERIMENTAL SET-UP

The experimental work is still going on. Accordingly, a general overview of the experimental set-up is presented in this paper. Since the main limitations for *Coulomb Counting* method are the inaccuracy of current sensor and accurate initial SoC is required [44], the pseudo-open circuit voltage (OCV) is used as the reference to *Coulomb Counting* method in the experimental set-up. Estimation using *pseudo-OCV* is straightforward where cell utilization is adjusted to achieve balancing without further adding complexity to the existing system. However, in order to obtain accurate OCV measurements, each cell has to be rested from any load for a period of time [44]. CPMBS itself based on

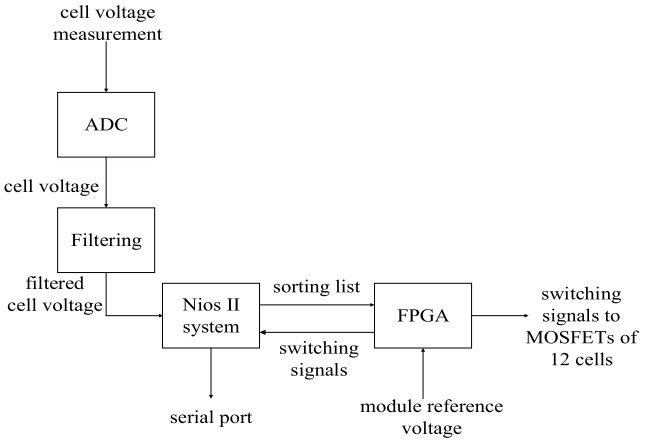

FIGURE 22. Block diagram of the experimental set-up.

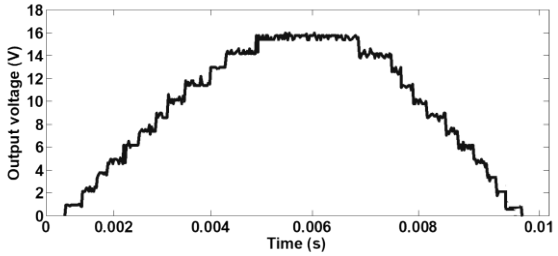

FIGURE 23. Output voltage of 25-level cascaded H-bridge multi-level converter.

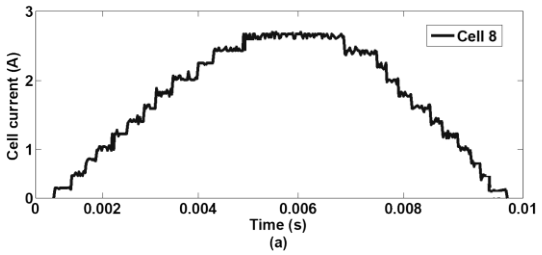

FIGURE 24. Cell current for cell 8.

pseudo-OCV is carried out as presented in Fig. 21. Compared with *Li-ion* cell, *NiMH* cell has good abuse tolerance such as it will not be permanently damaged when it exposed to overcharge status [51], [52]. Thus, a string of twelve *NiMH* cell is chosen to use in this early prototype. The characteristics of *NiMH* cells are presented in Table 7. The general block diagram of the experimental set-up is presented in Fig. 22. The results obtained from this prototype are presented in Fig. 23 and Fig. 24.

In Fig. 21, *Pseudo-OCV* measurement is employed to estimate SoC of each cell. In Fig. 22, before the balancing test, the OCV-SoC curve was measured using a 16-bits *ADC*. *Altera's Nios II* is a 32-bit soft processor, defined in a hardware description language, which can be implemented in *Altera's FPGA* (Field-Programmable Gate Array)

devices using *Quartus II* system. In this work, *VHSIC* (Very High Speed Integrated Circuit) Hardware Description Language (VHDL) is used as the hardware description language and *Terasic Cyclone IV DE0-Nano* development board is chosen as the *FPGA* device. Fig. 23 shows a 25-step sinusoidal output voltage generated by the 12 cell CHMMC. While the cell current for cell 8 is presented in Fig 24. It is shown that the maximum current drawn from any cell is around 2.8 A which is within the permissible limit.

VI. CONCLUSION

This study has proposed a novel topology in a grid-scale BESS where CHMMC and CPMDLB with MBS-CHMMC and SBS-CPMDLB have been implemented to achieve SoC balancing among all *ON/OFF-line* internal cells in a short duration. With L-bridge integration, the control and monitoring of an individual cell were made feasible. Moreover, the reduction in component count and the losses were achieved when integrating each individual cell into L-bridge compared with H-bridge. The advantages of MCHB were highlighted by the proposed topology by integrating each module with individual H-bridge to create a CHMMC. Direct *DC–AC/AC–DC* conversion was achieved using MBS-CHMMC. In this strategy, SoC balancing convergence point among the cells/modules was achieved. The SoC of all cells/modules stay the same even after the convergence point for charging and discharging by controlling their position based on a priority list. The use of MBS-CHMMC with SBS-CPMDLB has led to a significant improvement in the duration needed to achieve SoC balancing convergence point among the cells/modules compared with using the MBS-CHMMC alone. The SBS-CPMDLB can reach the unutilized cells in the MBS-CHMMC and transfer the energy among them, from the cells with high SoC to the cells with low SoC. The MBS-CHMMC with SBS-CPMDLB is active when BESS is *ON-line*, whereas SBS-CPMDLB can work by itself when BESS is *OFF-line*. A mathematical analysis and simulation modeling using *MATLAB* have been used to validate the proposed SoC balancing strategy. The simulation results have demonstrated a satisfactory performance of the proposed SoC balancing strategy where SoC balancing convergence point for the cells/modules has been achieved at approximately 1,000 min when the CPMBS-CHMMC has worked without SBS-CPMDLB and a reduction of 783.3 min has been observed when the CPMBS-CHMMC has worked together with SBS-CPMDLB. When the MPMBS-CHMMC has worked without the SBS-CPMDLB, SoC balancing convergence point for the cells has not been achieved, although it has been achieved for the modules after 666.6 min. Comparatively, when the MPMBS-CHMMC works together with the SBS-CPMDLB, SoC balancing convergence point for the cells/modules has been achieved after 333.3 min and 183.3 min, respectively. The practical value range of I_b of the SBS-CPMDLB is 2.5–3 A, which has led to obtaining a substantial improvement without posing any danger on the lifespan of cells. Accordingly, control complexity of a grid-scale BESS and slow SoC balancing among cells have been addressed by using the proposed circuit topology and its balancing strategy.

Future work will be focused on reducing control complexity, improving the proposed topology and its balancing strategy to add a new level of cell balancing to become three levels instead of two levels (balancing among the cells, modules, and three phases). Further work is required to improve the accuracy of SoC estimation. In addition, *State-of-Health* (SoH) will be included as the additional parameter in the existing balancing controller.

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