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GaN Integration Technology, an Ideal Candidate for High-Temperature Applications: A Review

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ABSTRACT In many leading industrial applications such as aerospace, military, automotive, and deep-well drilling, extreme temperature environment is the fundamental hindrance to the use of microelectronic devices. Developing an advanced technology with robust electrical and material properties dedicated for high-temperature environments represents a significant progress allowing to control and monitor the harsh environment regions. It may avoid using cooling structures while improving the reliability of the whole electronic systems. As a wide bandgap semiconductor, gallium nitride is considered as an ideal candidate for such environments, as well as in high-power and high-frequency applications. We review in this paper the main reasons that offer superiority to GaN devices over better-known technologies such as silicon (Si), silicon-on-insulator, gallium arsenide (GaAs), silicon germanium (SiGe), and silicon carbide (SiC). The theory of operation and main challenges at high temperature are discussed, notably those related to materials and contacts. In addition, the main limitations of GaN, including the technological (thermal and chemical) and intrinsic (current collapse and device self-heating) features are provided. In addition, the GaN devices recently developed for high-temperature applications are examined.

INDEX TERMS Extreme temperature applications, high-temperature electronics, gallium-nitride technology, wide-bandgap semiconductors.

I. INTRODUCTION

When the environmental temperature exceeds the limits of traditional electronic devices (more than 125°C), they are no longer able to fit application requirements. This limit of conventional technologies prevents their use in many significant industrial applications, such as deep-well drilling, and hot sectors of automotive and aerospace vehicles.

A possible solution is to provide cooling systems located outside the active high temperature medium to maintain the functionality of utilized technology. However, an additional cooling system introduces complexity and additional weight and size. Those overheads are not always acceptable, especially in critical industrial applications such as in aerospace vehicles, where the size, weight and reliability are extremely sensitive parameters that must be taken into consideration to obtain the required performance.

Despite these critical conditions, the number of installed sensors and microelectronic subsystems that control and monitor critical parameters in vital high temperature regions should increase if technology allows. This is compounded by efforts to replace all hydraulic subsystem and actuators by electrical and electronic functional equivalent components. Indeed, in general, the electrical approach yields more reliable, easier to maintain, and more compact systems than functionally similar systems composed of pumps, fluids and vacuum piping.

Aiming to reduce wiring and corresponding accessories which adversely affect system reliability, the distributed electronic system architecture is an accepted approach to support applications in aircrafts and automobiles. Modules in such systems require only two connections, power and communication. This contrasts with the central network system approach, where the power, control and monitor wires are installed throughout the airplane and automobile frame.

Note that even if high-temperature electronics is considered a niche market technology, it could strongly affect several modern industrial fields. For those reasons, there is a strong interest for microelectronic technologies that can be

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used at high temperatures. Developing such high-temperature electronics could offer great economic benefits significantly expanding the total market of present extreme electronics, which was estimated to be around US $17 billion in 2005 [1]. Significant as it is, the high-temperature electronics market is still modest compared to the worldwide market of conventional semiconductor technologies.

Commercially available semiconductor technologies dedicated for high-temperature applications such as silicon on insulator (SOI), gallium arsenide (GaAs) and silicon germanium (SiGe) are serving a rather narrow range of temperatures not exceeding 300°C, and are often associated with for limited operation time, due to fundamental physical limitations of these semiconductors at high temperature [2]. Many significant industrial applications have requirements far exceeding this limit. For example, in turbine engines, many sensors and electrical actuators should be located in 600°C ambient temperature. Similarly, in aerospace exploration, in addition to the extreme radiation environment that electronic must endure, the ambient temperature can exceed 500°C. This is the case for Venus and Mercury exploration. Moreover, in geothermal and automotive applications, telemetry devices and exhaust pipe sensors must sustain ambient temperatures above 500°C.

Wide bandgap (WBG) semiconductors are considered as main candidates in the foreseeable future to overcome the fundamental limits of available conventional electronics in high ambient temperature applications. Silicon carbide (SiC) and gallium nitride (GaN) are the best-known WBG devices offering attractive features suitable for high temperature conditions such as wide bandgap (3eV), high drift saturation velocity, high thermal conductivity, low intrinsic carrier concentration and large critical electric field [2]. By contrast, silicon-based technologies are more mature and generally less expensive for a given line-width.

In general, both GaN and SiC belong to the same WBG semiconductors family and share similar attractive properties. However, SiC have received a great deal of attention in the past decade, especially in the high temperature applications field. Although important advances have been made on SiC based ICs, most of the reported ICs were realized with either large areas or small number of devices, having low device density integration [3]. In addition, no commercially available SiC integrated devices and circuits operating at temperature higher than 300ř C were found [4]. The direct temperature dependence of carrier concentration, due to the bulk nature of the active region in SiC devices, is considered as a common shortcoming [5] in addition to the crystal dislocations that degrade junction leakage, particularly at the highest temperature levels.

III-Nitride and primarily GaN technologies exhibit substantial performance improvement over SiC semiconductor with respect to response speed and operating temperature limits [6]. In addition, the temperature stability of electron concentration in the HEMT channel makes GaN devices more stable at high temperature. The recent research on GaN technology in Europe is summarized in [7] showing incremental progress to establish an independent GaN supply chain in Europe. In addition, [8], [9] summarize some major recent trends of semiconductor research toward mature GaN technology that goes beyond the conventional limits of silicon. These papers discuss means to offer higher blocking voltages, wider range of operational temperature and better energy conversion efficiency.

In this review paper, the theory of operation of GaN devices is presented in section II, including the basic principle of GaN technology and the reasons why this semiconductor is superior the other known materials. In section III we discuss the challenges of GaN devices in terms of materials and contacts, along with the corresponding limitations at high temperature. The most known GaN technologies are examined in section IV, in addition to the recent published results in this field. Section V summarizes our main findings.

II. OPERATION OF GaN SEMICONDUCTOR

The III-nitride semiconductors possess large bandgaps varying from 0.7eV for InN, 3.4eV for GaN, up to 6.2eV for AlN. Profiting from their wide range of energy bandgap, these materials can be utilized to emit light in various visible ranges (violet, blue and green) in addition to be used in high frequency and high-power applications [10]–[12]. A great deal of research focused on GaN and its alloys like AlGaN and InGaN. These alloys were investigated for their special properties, such as low resistivity and high voltage capability. Obtaining good substrate material for GaN remains challenging due to the difficulty of providing a good quality GaN substrate layer. Other alternatives are utilized such as sapphire, SiC and silicon substrates, which are available at lower cost. These substrate materials are thermally compatible with GaN and have proper lattice matching.

A. GaN BASIC PRINCIPLE

The thermodynamic stability of GaN is due to its wurzite crystal structure and bandgap energy of 3.4eV, which make it capable of sustaining high temperature. Growing GaN layers is typically done by molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD) and hybrid vapor phase epitaxy (HVPE). These various methods open a wide variety of epilayers quality and surface roughness.

The first GaN epitaxial layer grown on sapphire substrate was reported in 1969 [13]. Due to the high n-type background carrier concentration of GaN layers and the lack of p-doping, GaN could not be used rapidly in electronic devices and its adoption was very limited until the 1980s. Hetero-epitaxy problems could be eliminated by utilizing GaN substrates, giving better control of stress, dopant concentration, polarity, lattice constant mismatch and thermal expansion coefficient mismatch. However, the difficulty of obtaining large GaN wafers and their costly fabrication further hindered its adoption. With the availability of large sapphire (Al_2O_3) wafers that provide perfect electrical insulation, that offer high quality, excellent temperature stability and low fabrication cost,

TABLE 1. Physical properties of substrates considered for GaN technologies.

Properties	Substrate			
	GaN	Al_2O_3	SiC	Si
Thermal expansion coefficient (10^{-6} K^{-1})	5.59	6.9	2.77	2.6
Lattice mismatch (%)	-	-16	+3.5	-17
Thermal conductivity (W/cmK)	1.3	0.5	3.8	1.5
Wafer size (inches)	2	6	3	12
Cost	high	low	High	low
Resistivity	high	high	High	mediate
Temperature stability (°C)	>900	>1600	1700	900

this material was considered as a candidate substrate for GaN. Unfortunately, using sapphire substrates leads to high defect density, because of low thermal conductivity and large lattice mismatch to GaN.

Silicon carbide (SiC) and silicon (Si) offer higher thermal conductivity and smaller lattice mismatch to GaN and combining them gives good candidate solutions for high temperature applications. However, the disadvantages of SiC substrates are their small area, intermediate quality and high price. These disadvantages of SiC play in favor of silicon as a substrate of choice for GaN epitaxy with its good thermal conductivity, low cost and availability of larger wafers, in addition to the possibility of integrating GaN devices with mature silicon devices. On the other hand, the high thermal expansion coefficient mismatch and large lattice mismatch between Si and GaN favor the appearance of cracks on the surface. Table 1 summarizes the physical properties of several substrates considered for GaN.

The attention with GaN has focused on HEMTs (High Electron Mobility Transistors), which are also called HFETs (Heterostructure Field Effect Transistors). To explain the theory of operation of GaN HEMT devices, AlGaN/GaN will be used [14]. These devices are the dominant GaN HEMT structure. When an AlGaN alloy is deposited on a thick GaN layer, an AlGaN/GaN heterostructure is formed. A band bending happens due to the difference in bandgap energies between the two semiconductors, and a two-dimensional electron channel is created in the upper side of GaN layer (Fig. 1a).

The wurtzite structure of GaN is tetrahedrally coordinated with a lack of symmetry in the c-direction [15]. A spontaneous polarization along the c-direction takes place because of this lack of symmetry and the large iconicity of the covalent bond in the GaN structure. The lattice mismatch between AlGaN and GaN induces a piezoelectric polarization oriented in the same direction of spontaneous polarization. The total polarization charge is the combination of both the piezoelectric effect and difference of spontaneous polarization. Therefore, a positive polarization charge appears at the lower interface between AlGaN and GaN due to the superiority of AlGaN polarization over the GaN layer.

To compensate this positive charge, electrons are attracted to form a 2DEG (Two-Dimensional Electron Gas) dropping

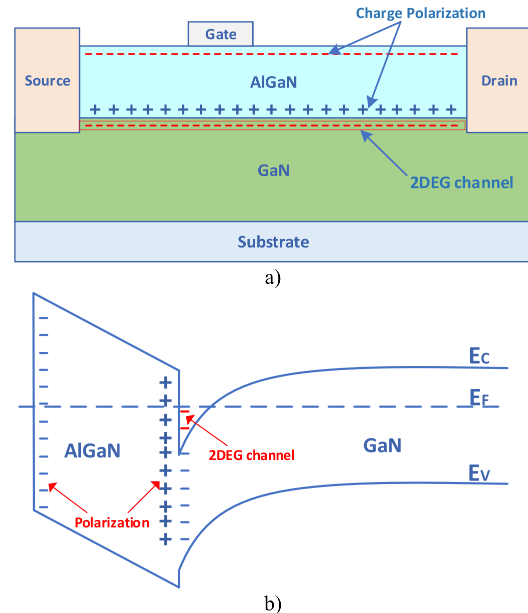

FIGURE 1. AlGaN/GaN based HEMT: a) Physical structure and b) Band structure.

below the Fermi Level E_F. This creates a triangular quantum well at the AlGaN/GaN interface as shown in Fig. 1(b). Even without doping the AlGaN layer, the 2DEG can be produced due to the strong piezoelectric and spontaneous polarization effects in nitrides, resulting in high electron density and high drift mobility. The carrier concentration is limited by the strain relaxation of the top layer. The AlGaN layer thickness, as well as the Al concentration have a direct effect on the maximum sheet charge. A positive polarization is formed in Ga-faced structures. A negative polarization will take place in the case of N-faced structures, which will be compensated by holes instead of electrons, and these charges are accumulated at the AlGaN/GaN interface.

Electron trapping may occur due to the presence of impurities in the lattice structure or at the interface between the heterostructure layers, which produces a current collapse that in turn deteriorates the device performance. After applying drain-source voltage, the trapped carriers remain, even when removing this voltage, leading to degeneration of the device output power. This can be compensated by light illumination on the device, giving enough energy to the trapped carriers to be released. There are various scattering mechanisms that affect the total mobility of the 2DEG channel, such as polar optic scattering, ionized impurity scattering, piezoelectric scattering and acoustic phonon scattering.

A simplified cross-sectional representation of a typical GaN HEMT structure is depicted in Fig. 2. The substrate layer could be one of several materials like silicon, silicon carbide or sapphire as discussed previously. The nucleation layer is very important to ensure better growth quality of the following layers and to allow a good polarity of the upper buffer layer. Usually, AlN and GaN are utilized as nucleation

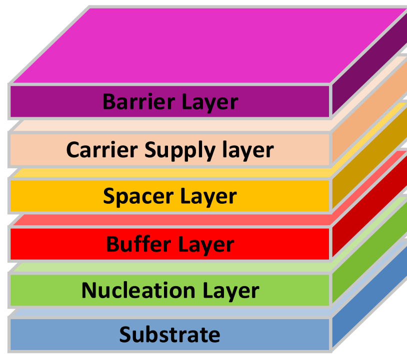

FIGURE 2. Schematic drawing of a typical GaN HEMT layer structure.

layers. The buffer layer ensures device isolation and improves the material quality. A thick GaN layer is taking place and at the upper side the 2DEG is located. A thin undoped AlGaN layer (AlGaN/GaN case) acts as a spacer for carriers injected into the 2DEG by the carrier supply layer. The carrier supply layer could be Si-doped GaN layer or an undoped AlGaN layer supplying the 2DEG with electrons. The main purpose of the barrier layer is to maintain an effective barrier for the Schottky contact typically placed over this layer.

By default, when a positive voltage is applied to the drain, a current flows between the drain and the source through the 2DEG sheet. This current can be controlled by the applied gate voltage, which, in turn, controls the space charge of the two- dimensional conductive channel. The quality of the 2DEG sheet depends on various parameters such as the substrate material, the method used to grow the layers composing the device and the doping level of carrier supply layer. With negative gate voltage values, the space charge under the gate area expands toward the 2DEG loaded with electrons gradually depleting this channel until the 2DEG sheet is pinched off.

B. GaN ADVANTAGES

To understand the superiority of GaN technology over conventional devices at high temperatures, it is very important to identify the main factors that affect the physical limits and operation of semiconductors at high temperature.

1) INTRINSIC CARRIERS

All semiconductors have thermal electron and hole carriers in their crystals. The intrinsic carrier concentration (ni) varies exponentially with semiconductor temperature [16] following equation (1), where k is the Boltzmann constant.

$$ni = \sqrt{NcNv}e^{-EG/2kT} \quad (1)$$

In (1), E_G, N_C and N_V are respectively the energy bandgap and the effective electron and hole density of the semiconductor that vary only slowly with the device temperature (T) when compared to the ($e^{-EG/2KT}$) term that grows exponentially with temperature. Consider the temperature dependence of the intrinsic carrier concentration [17], the ni of silicon at

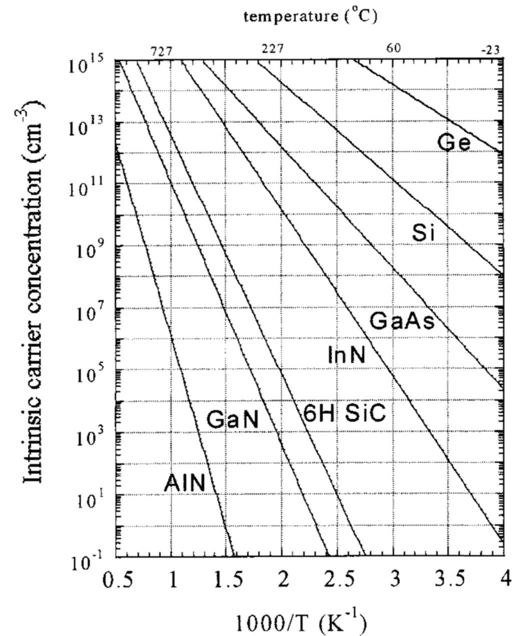

FIGURE 3. Semiconductor intrinsic carrier concentration versus temperature [18].

room temperature is around 10^{10} cm^{-3}. This concentration is almost negligible if it is compared to the device doping level around 10^{15}. However, when the temperature exceeds 300°C, this concentration becomes higher than the dopant carriers' concentration in typical doped silicon semiconductor. This undesirably affects the electrical properties of this device that is supposed to be controlled by well-designed doping levels.

On the other hand, the GaN intrinsic carrier concentration, with its wide bandgap (around 3eV), is much lower than the one observed in silicon, even at higher temperatures beyond 600°C. This prevents problems due to excessive intrinsic carrier concentration. As shown in Fig. 3 [18], at any temperature, the intrinsic carrier concentration (and consequently, the intrinsic leakage current) is around 12 orders of magnitude lower in WBG semiconductors than in the more common ones such as silicon.

2) LEAKAGE CURRENT OF P-N JUNCTIONS

The leakage current of p-n junctions is the reverse current passed through the equivalent diode of this junction when a reverse bias voltage is applied. This reverse current must be negligible particularly in power applications where high switching frequency is needed at high applied voltage [19]. The mobile carriers, which are depleted at the junction area, form the depletion region of p-n junction. The p-type junction is positively charged with hole carriers and the n-type junction is negatively charged with electron carriers. The I-V characteristic of a p-n junction diode is given by (2) when the p-type doping is larger than n-type doping [20].

$$I = qAni[ni/ND\sqrt{DP}/\tau \left(e^{qVA/kT} - 1\right) + W/2\tau \left(e^{qVA/2kT} - 1\right)] \quad (2)$$

At applied voltage VA, the depletion region width is W and τ is the lifetime of effective minority carrier in seconds. The minority carrier diffusion current is represented in the first exponential term in (2), while thermal generation appears in the second exponential term. By applying few tens of reverse bias voltage V_A at high temperature less than 1000°C, equation (2) can be simplified to (3)

$$I = -qAni[ni/ND\sqrt{DP}/\tau + W/2\tau] \tag{3}$$

where it is obvious that the leakage current of the reversed biased p-n junction is substantially related to the intrinsic carrier concentration ni. Therefore, a harmful leakage current on the device and operation system is from the reversed biased junction which increases with applied temperature. In GaN semiconductor devices, this leakage current is orders of magnitude lower than in silicon devices, due to their lower intrinsic carrier concentration ni. Thus, GaN and all wide bandgap semiconductors are much better candidates for applications where the temperature exceeds 600°C.

3) CARRIER EMISSION LEAKAGE CURRENT

Another type of leakage current that can affect device operation is the carrier emission leakage current. When the carriers gain sufficient energy to pass through an energy barrier, this process is called emission and is directly related to the temperature which is considered as the source of thermal energy. This mechanism appears in Schottky barrier contact rectifying metal-semiconductor diodes. The carrier emission current can be expressed by:

$$I = AK^*T^2e^{-q\Phi_B/kT}\left(e^{qVA/kT} - 1\right) \tag{4}$$

where Φ_B is the Schottky barrier height (effective potential barrier height). For a significant reverse bias voltage V_A, the current in (4) can be simplified to:

$$I = -AK^*T^2e^{-q\Phi_B/kT} \tag{5}$$

where the carrier emission leakage current decreases according to an exponential relation in Φ_B. It is easy to see that the leakage current can be controlled by the effective potential barrier height. Although this Φ_B depends on the junction formation, the semiconductor and the metal, it cannot be larger than the device bandgap and, in most cases, less than 75% of the bandgap energy. Therefore, the Schottky barrier heights are limited to 0.9V for silicon device (1.1eV bandgap), whereas the barrier heights in GaN semiconductors ($<$3.3eV) are twice larger. This advantage in wide bandgap devices reduces the junction leakage current by several orders of magnitude at any operating temperature, thus enabling the implementation of devices operating at high voltage and high temperature where conventional semiconductors are no longer applicable.

4) POWER APPLICATIONS

In power applications, there exist several sources of power dissipation. Large currents flowing through power semiconductor devices always imply significant dissipated power in the device resistance. In addition, considerable instantaneous dynamic power dissipation appears during on-off switching of power devices. Also, a large amount of power dissipation is induced by off-state leakage currents flowing while the power devices block high voltages. In case of high ambient temperature, the influence of those power dissipation sources becomes more serious and increases the internal temperature of power devices significantly beyond the surrounding temperature, which typically results in undesired interaction between power dissipation and device temperature.

However, the special properties of GaN devices, including their wide bandgap, high-drift saturation velocity, thermal conductivity (SiC substrate), high-breakdown electric field and low-intrinsic carrier concentration, put them as leading candidates for high-power applications [10], [11], [21]–[23]. Table 2 presents the most important electrical properties of GaN compared with GaAs, silicon and SiC (wide bandgap semiconductor family) [24].

TABLE 2. Comparison of selected semiconductor material properties [24].

Property	Silicon	GaAs	4H-SiC	6H-SiC	2H-GaN
Bandgap energy (eV)	1.1	1.42	3.2	3.0	3.4
Relative dielectric constan	11.9	13.1	9.7	9.7	9.5
Breakdown electric Field at $N_D = 10^{17}$ cm^{-3} (MV/cm)	0.6	0.6	3.0	3.2	2-3
Intrinsic carrier Concentration (cm^{-3})	10^{10}	1.8 x 10^{6}	~10^{-7}	~10^{-5}	~10^{-10}
Electron mobility at $N_D = 10^{16}$ cm^{-3} (cm^2/V.s)	1200	6500	800	60- 400	900
Hole mobility at $N_A = 10^{16}$ cm^{-3} (cm^2/V.s)	420	320	115	90	200
Saturated electron velocity (10^7 cm/s)	1.0	1.2	2	2	2.5
Thermal conductivity (W/m.K)	150	55	400	480	130

III. GaN CHALLENGES AND LIMITATIONS

A. CHALLENGES

In spite of the promising properties of GaN devices as great candidates for extreme temperature applications, there still exist major technical challenges that must be surmounted before their beneficial properties can be fully leveraged in high temperature electronic systems.

1) MATERIALS

The material quality and crystal growth of GaN and III-Vs devices remain inherent hinders that should be overcome to enable these devices to withstand high temperature conditions. The heteroepitaxial growth of GaN devices is typically performed on foreign substrates such as SiC and sapphire instead of single crystal GaN wafer. The I-V characteristics of p-n junctions are undesirably affected by the crystal dislocation defects in GaN semiconductor inducing leakage currents greater than estimated in (3), which may hinder the merits of GaN in high temperature applications due to specific types and density of defects. For high power GaN devices, material

defects have large effects because of the large junction area and high electric field [11], [22].

Moreover, the device efficiency can be also adversely affected by surface morphological defects and variations of thickness across the wafer. Therefore, more improvements in material quality and crystal growth are still required to enable effective use of GaN devices in high temperature environments. Although demonstration of GaN devices operation at high temperature between 300°C and 600°C has been successful [25], long-term reliable functionality is still unachievable and more fundamental technological adjustments are needed.

2) CONTACTS

Due to the absence of metal contacts with suitably low barrier with the semiconductor, it becomes difficult to produce ohmic contact to GaN wide bandgap semiconductor. For that reason, a low resistance ohmic contact is obtained by doping heavily the semiconductor region close to the metal interface.

Ideally, the Schottky contacts that constitutes the gate should possess a high breakdown voltage and low leakage current. Generally, Ni and Au are the common metallic Schottky contact materials, with high work function conducting to high Schottky barrier heights. It is of interest that Ni offers excellent adhesion to nitride, while Au offers an excellent thermal stability.

The conductive contacts functionality at high temperature is not less important than that of the semiconductor itself. The reliability of contacts metallization and interconnects between the on-chip devices presents a substantial challenge for GaN operation at high temperature, particularly for applications beyond 400°C. The self-heating generated during normal operation combines to the surrounding high temperature to cause contact degradation and limit the long-term reliability of GaN devices.

The metal-semiconductor ohmic and Schottky contacts of n-type and p-type layers must have thermal stability during the device lifetime. The conductive n-type are more easily obtained than p-type doping layers due to the difference of acceptor and donor dopant ionization energies. Thus, n-type contacts are more mature than p-type contacts and they offer better performance. Understanding the electrical characteristics and reaction kinetics of metal/GaN interface are the main focus of several researchers who also study diffusion barriers in case of multilayer metallization. Although hermetic packaging is a good solution to protect the contacts at high temperature, developing contacts that are thermally stable at high ambient temperature leads to simpler and less expensive packaging.

The Ti/Al/Ni/Au low resistance ohmic contact has been studied in [26] between 25°C and 600°C for n-type GaN. On the other hand, various Schottky contacts such as n-GaN Ni/Au, Ni/Pt/Au, Pt/Ni/Au and Pt/Ti/Au have been investigated in [27] for temperatures going up to 400°C. In parallel, a novel Mo/Al/Mo metal stack is introduced in [5] to improve the robustness of ohmic contacts at high temperature reaching 500°C. A high-K dielectric is deposited to provide Schottky contacts showing stable dielectric permittivity and reduced leakage over a wide temperature range. However, it offered a decreasing lower breakdown voltage with temperature due to the ionization of deep traps in the dielectric material.

Due to the difficulties of realizing conductive p-type GaN layers, obtaining highly stable contacts of this material has presented serious challenges so far. Additionally, more studies are still needed to investigate the reliability of GaN ohmic contacts in presence of electromigration and chemical reactions with applied electrical bias at oxidizing high temperature above 400°C. Thus, significant challenges related to GaN contacts must be surmounted to enable this device to support long-term operation in real environment and at temperatures higher than 600°C.

B. LIMITATIONS

The GaN HEMT limitations can be separated into two types: 1) technological, such as barrier scaling, thermal limitations and chemical limitations, and 2) intrinsic associated with current collapse and device self-heating.

1) TECHNOLOGICAL LIMITATIONS

The output power is proportional to the barrier thickness. On the other hand, this barrier thickness is inversely proportional to the device cut off frequency. This conflict could be resolved with several techniques such as using a thin barrier with a low surface potential and high polarization discontinuity as well. For example, an AlN barrier layer can be applied [28] and the break down voltage could be maximized by utilizing slanted gates [29]. Optimizing the buffer layer growth with an extremely insulating materials would reduce the buffer leakage current [30]. It is very important to suppress the leakage current of Schottky contacts on the Mesa edge to improve the mesa isolation. Reducing of gate source resistance by shortening the gate source distance and contact resistance would decrease the knee voltage which directly affects power devices. The influence of tunneling of ohmic contact could be minimized by contact recess [31], selective doping [32] or re-growth of ohmic contact region [33].

In addition, the so-called recessing process avoids undesired kink effects and prevents R_C (contact resistance) and gm (transconductance) nonlinearities [34]. A piezoelectric polarization is also related to the Al concentration, which leads to a drop in the electron mobility and increases the barrier strain and strain relaxation [35]. Additionally, stress in the barriers hinders the growth of thick barriers to prevent cracking and defects.

Additional challenges can appear when the recessing process is applied on thick barriers. One of the challenges is damage of the heterostructure polarization by discriminatory etching [36]. Another type of faults that can result from physical defects is an increase of gate leakage currents, which are dominated by the tunneling mechanism, especially when the junction is forward biased. The leakage current can be shrunk by raising the Schottky barrier height through some higher

metal barrier or by modifying the surface potential with wet chemical or plasma treatments [37], [38]. Another alternative is a gate dielectric approach forming a MOSHEMT [39] or an InGaN cap layer on the barrier layer [40].

Chemical limitations appear when the GaN HEMT device is utilized in chemical applications [41], [42]. In this case, a stable passivation layer is required to protect the free surfaces of the device. And the thermal limitations present when the device operates in high temperature environment or during high power operation causing self-heating effects. In such conditions, the heterostructure may suffer degradation or surface decomposition [43] if materials reach their chemical stability limit. Thermal management is a key solution when dealing with self-heating, but in high temperature applications, the device, the passivation material, and the contact metallization should be thermally stable.

A promising solution is to overgrow a diamond layer over the HEMT devices, taking advantage from its high thermal conductivity to obtain an efficient heat management system. However, this approach is not applicable to all GaN HEMT devices, because of the harsh growth environment conditions which could degrade the GaN device [44].

2) INTRINSIC LIMITATIONS

The previous technological limitations can be avoided by selecting a suitable heterostructure and proper device design. On the other hand, the intrinsic limitations discussed here are of prime interest when considering the device reliability because they cannot be prevented. For instance, the dispersion effect (lag effects) that can induce the current collapse phenomenon is inherent in all GaN heterostructures. Dispersion is due to the polarization counter charge on the top surface. Current collapse can degrade power performance and DC characteristics of GaN devices, even before the predicted theoretical values.

In planar GaN HEMT devices, a high-breakdown voltage can be obtained by removing the surface donor charge localized in the area between the gate and drain. On the other side, this will induce drain-lag current collapse if the injected charges are not able to track the swing frequency of the applied voltage. This phenomenon is observed when the device operates at high power, but it does not appear in small signal operation and it does not affect the cutoff frequency and the fmax. Several experimental techniques can be used to detect current collapse, such as large signal pulsing, switching operation and dual gate methods. In addition, current collapse effects can be observed by combining DC characteristics with dynamic load lines at RF operation.

Current collapse effects can be controlled by regulating the injected lateral charge. To do that, a passivation layer could be added to prevent the injected charges from running on the surface [45]. In this case, charges will concentrate in the passivation layer, far away from the surface. This is obtained with suitable surface treatment and passivation type. With an efficient passivation, the impact of virtual gate effects can be reduced very significantly.

Moreover, a lossy dielectric can be used to augment the injected charges mobility shifting the current collapse to higher operation frequencies. Additionally, this effect can be reduced by using gate recess and the field plate mechanism. Eventually, controlling the charge and discharge of surface traps traveling between the gate and drain is an essential factor to reduce current collapse. This can be done by controlling the device fabrication steps and the passivation deposition.

The most common passivation to reduce the current collapse of GaN HEMT devices are MOCVD Si_3N_4 [46] and PCVD (plasma chemical vapor deposition) Si_3N_4 [47], in addition to combinations of gate dielectric and passivation ALD-Al_2O_3 [48], [49] and high dielectric constant oxides such as MgO, HfO_2 and ZrO_2 [50], [51].

Self-heating represents a major factor that can limit the reliability and performance of GaN HEMTs. Indeed, the device temperature increases with the dissipated power. This self-heating affects the device high-frequency operation and output power due to the reduction in drift velocities and mobility respectively [52]. In addition, higher device temperatures accelerate electromigration and aging of device metallization that can affect reliability and induce device failure [53]. Therefore, an effective heat dissipation management is necessary to get a reliable device, especially in power applications.

The device temperature could be estimated by several techniques such as scanning thermal microscopy [54], photocurrent measurements [55], microphotoluminescence [56], micro-Raman spectroscopy and infrared thermography [57]. It was reported that efficient device design and packaging have a significant impact on thermal management. Notably, the substrate has a major role as it is the main heat removal path connecting the device to the package heat sink. Thus, for more efficient heat management, a higher thermal conductivity substrate is required. For that reason, SiC is considered the most appropriate substrate material when compared to Si and Sapphire since it has a superior thermal conductivity. However, extraction of heat can also be done from the top of the device by coating it with high-thermal conductivity materials such as diamond [58].

IV. HIGH TEMPERATURE GaN GENERATIONS

As they already provide reliable contacts, interconnections and packaging, the III-N semiconductors are suitable candidates for high ambient temperature. However, the major obstruction of these devices is represented by charge trapping effects. The latter is a function of operation temperature and adversely affects the electrical characteristics of the device. Although junction devices (p-junctions) are possibly reliable for high temperature, the Insulated-Gate Field Effect Transistors (IGFETs) are favorable for practical electronic system implementation.

To obtain reliable high temperature IGFETs, gate insulating material should maintain adequate insulation and interfacial characteristics at the targeted high-temperatures (300°C-600°C) and high-electric field stress. However, such

properties high quality insulating materials are extremely difficult to obtain with III-N semiconductors.

While the high-temperature operation of III-N IGFETs exceeding 600°C has been demonstrated [59], long-term operation at such operation temperature still demands more improvements in the gate insulation ability due to two essential defections. The first one is the insufficient insulation properties which lead to undesirable charge leakage from the device channel. This leakage may change the threshold voltage (V_T) of the IGFET by creating traps in the insulator. Adding the degradation mechanism to insulator carrier leakage, these two defects are undesirably accelerated with higher operation temperature. Secondly, in case of GaN device, the undesirable electric charges at the interface of the semiconductor and insulator have higher densities negatively leading to fragile channel mobility (μ). This, in terms, damages the electrical performance of the IGFET [17].

Aiming to improve the III-N IGFET devices, research efforts have focused on alternative insulation materials and improved processing. However, compared to the advanced reliability and performance of Si/SiO_2 MOSFET devices even at low operation temperature, massive challenges should be overcome until the III-N IGFETs can be considered as acceptable devices with proper functionality for operation ambient temperature well beyond 500°C.

A. GaN HBT

Compared with FET devices, GaN based HBTs provide better options for RF applications. They offer significant advantage from the IC manufacturing point of view. They rely on uniform turn on characteristics and are convenient for current amplification and impedance matching for high-power applications. Also, GaN HBTs offer important benefits in harsh environments subject to high total dose of radiation, corrosive and particularly extreme temperature applications.

Many researches focused on AlGaN/GaN HBTs aiming to provide junction transistors [60], [61]. However, only marginal improvements were reported. The limited success appears related to the unavailability of low resistance base layers, combined with limited fabrication techniques, and shortage in high crystalline quality epitaxial structures and low defect density substrates. Moreover, a fundamental factor in GaN HBT devices is the low free hole concentration in p-type epitaxial GaN layers that introduces serious emitter crowding effect. This deficiency is treated in GaN/InGaN HBTs by utilizing InGaN base layer aiming to minimize the resistances of base sheet and p-type contacts [62].

Some researchers have tried to reduce etching deteriorations in the base layer by using an epitaxial regrowth approach in npn GaN/InGaN HBTs [63]. The response of GaN HBT was studied between room temperature and 250°C to investigate the performance of this device at high temperature [64]. This Double Heterojunction Bipolar Transistor (DHBT) was grown on a Free State (FS) 40×40 μm^2 GaN substrate. When the temperature increases from room temperature to 250°C, the device gain current is reduced from 115 to 43 respectively

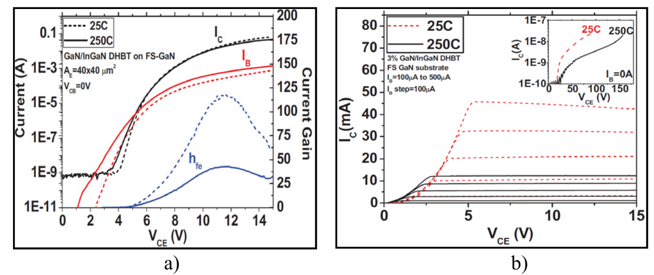

FIGURE 4. DHBT grown on a GaN substrate, a) Gummel plot, b) Common-emitter characteristic [64].

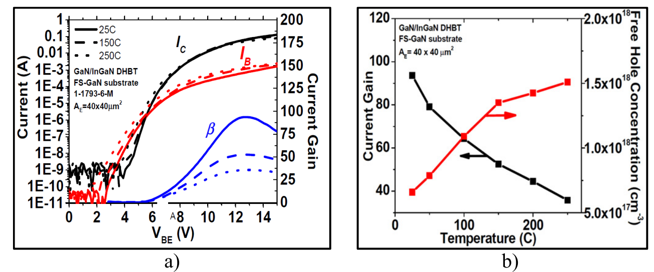

FIGURE 5. a) A measured Gummel plot of the DHBT at different temperatures, b) Measured current gain (β = IC / IB) and free hole concentration (p) calculated from 1/C^2 v.s. V_{BE} curve fittings at different temperatures from 25 to 250 °C [66].

as shown in Fig. 4(a). The current reduction was related to a reduced emitter injection efficiency and a higher recombination rate introduced by Mg ionization and free-hole concentration in the base.

Similarly, the $I_C - V_{CE}$ characteristics in Fig. 4(b) show a drop in the knee voltage from 5.2V to 2.75V for I_B = 500μA in addition to a reduction of the offset voltage from 0.8 to 0.3V. The knee voltage and offset voltage reduction are due to the drop in base resistance at high temperature. Moreover, as the temperature increases to 250°C, the breakdown voltage BV_{CEO} is shifted from 90 to 157V, which highlights the dominant role of the impact ionization process on GaN/InGaN HBTs. In the case of pnp AlGaN/GaN HBTs, it is reported that these devices can endure operating temperatures of 590°C with current gain = 3 [65]. Considered globally, these results confirm that GaN HBTs can operate at extreme operating temperatures.

A high performance of InGaN npn HBTs has been reported in [66]. This device was grown on a sapphire substrate by MOCVD and it showed high collector current density (J_C), low knee voltage (V_{knee}), low offset voltage (V_{offset}) and high BV_{CEO} characteristics. In the same work, another InGaN HBT was grown on free-standing GaN substrate. This device showed reduction in peak current gain from 93 at 25°C to 35 at 250°C (see Fig. 5(a)) in addition to higher free-hole concentration as shown in Fig. 5(b) leading to base resistance and V_{knee} reduction.

B. RECENTLY DEVELOPED DEVICES

The fabrication processes and the characterization of AlGaN/GaN HEMT devices (depicted in Fig. 6a) are

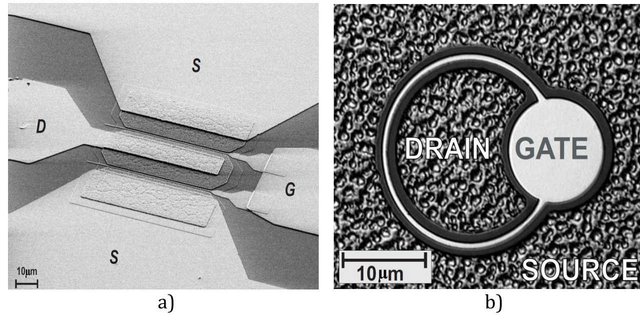

FIGURE 6. a) Photograph of a AlGaN/GaN HEMT. Three ohmic contacts (drain D and source S) and two finger Schottky contacts (gate G) at the top of the mesa are placed, b) Simple RoundHEMT layout with ohmic contacts (source and drain) and Schottky contact (gate) [15].

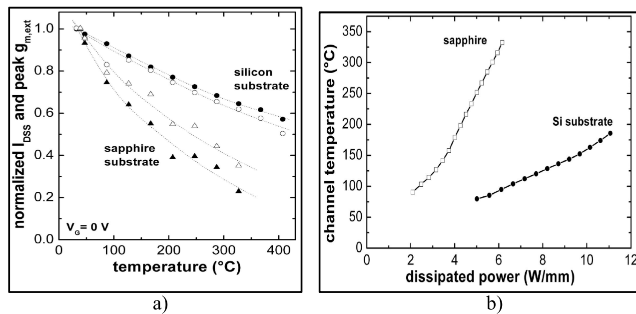

FIGURE 7. AlGaN/GaN HEMTs on Si and sapphire substrates: a) Temperature dependence of I_{DSS} and peak of $g_{m,ext}$ normalized to their room temperature values, b) Dissipated power-to-channel temperature transfer characteristics [15].

discussed in [15]. These processes used sapphire and silicon substrates. The ohmic contacts reported in that work are multilayered Ti/Al/Ni/Au contacts annealed at 900°C and the Schottky contacts are Ni/Au metal layers. Three etching techniques are investigated: RIE ECR (reactive ion etching with electron cyclotron resonance), photochemical etching and Ion beam etching. The latter, using Ar+ ion sputtering, is more reliable and leads to a better controlled process, smooth surfaces, sharp edges, well defined sidewalls and an etching rate of 30nm/min. The HEMT on sapphire substrate was optimized by RoundHEMT technology (depicted in Fig. 6b).

As plotted in Fig. 7(a), the degradation of maximum saturation drain current (I_{DSS}) and peak extrinsic transconductance ($g_{m,ext}$) increase with temperature increase for both sapphire and silicon substrate devices. In parallel, the study of self-heating effects shows higher temperature dissipation in the channel of sapphire substrate device when compared to the one observed in devices built over silicon substrates as plotted in Fig. 7(b).

In addition, the influences of doping density of an AlGaN carrier supply layer combined with an AlGaN barrier layer or various thickness are studied in [15] along with their impacts on the electrical properties. By reducing the gate length and source to drain distance, the device performance is improved due to the reduction in source and gate resistance. However, due to its poor thermal conductivity, the sapphire substrate is not suitable for high power and high temperature applications. The AlGaN/GaN RoundHEMTs (depicted in Fig. 6b) on silicon substrate shows better performance at higher temperature (320°C) and high power (6W/mm). The DC and RF performance of this device increased with the doping density. It was observed that Si_3N_4 passivation has better impact than SiO_2. It improved the DC and RF performance, the 2DEG concentration and the output power density.

A novel AlInN/GaN HEMT is presented in [67] as an alternative of AlGaN/GaN. The performance of this device with 0.25μm and 0.15μm gate lengths is discussed. The reported measurements indicate a surface more stable than in AlGaN/GaN devices in addition to high-chemical stability at temperatures of 1000°C in vacuum as shown in Fig. 8. The key solution, as depicted in Fig. 9, is to insert a thin AlN interfacial layer between a thick GaN buffer and a thick undoped AlInN barrier layer resulting in high mobility, low sheet resistance and high sheet charge density. The device is grown using an AIXTRON Metalorganic Vapor Phase Epitaxy system on 2-inch diameter sapphire substrate. The ohmic contacts with this technology are obtained from a Ti/Al/Ni/Au metal sequence annealed at 890°C. Ni/Au Schottky gates and contacts are defined by e-beam lithography.

Between 2009 and 2011, the MORGaN project [68] was an extension of UltraGaN project launched in 2005 under the FP6 (FET-IST) program [69]. MORGaN focused on InAlN/GaN as a candidate for extreme environment applications [70]–[75]. Investigating the availability of GaN growth on polycrystalline diamond and Si substrates, MORGaN provided the first European demonstration of 2-inch wafers. Moreover, the same team had already demonstrated the first AlGaN/GaN HEMT with direct growth on '111' single crystal diamond, in addition to the first InAlGaN HEMT grown on 2-inch free standing wafers using a substrate combining 2μm of '111' silicon grown over a 70μm polycrystalline diamond layer. Also, they had successfully developed diffusion barriers for Ti/Al ohmic contacts dedicated to HEMTs and harsh environments (800°C). Multilayer structures of TiN/TiSiN (Cu mounting layer coverage) and ZrN/ZrB_2 (Au mounting coverage layer) were investigated and realized.

In [58], significant work on fabrication and characterizion of InAlN/GaN HEMT devices was reported. A nanocrystalline diamond (NCD) coated lattice matched (LM) InAlN/GaN technology is proposed to solve the self-heating device problem. Due to the high lattice mismatch, AlN suffers serious limitations with respect to mechanical stability that makes it unfavorable for NCD overgrowth. However, InAlN possesses better matching of grown lattice over a GaN buffer layer with 83% of Al content. This avoid mechanical stability issues and preserve a high density of the 2DEG taking into account the larger polarization discontinuity with the buffer layer. Investigating the performance and limitations of the LM-InAl/GaN HEMT, the results showed an interesting high thermal stability of the device. This leads to accept uncommon treatment of HEMT inherent limitations

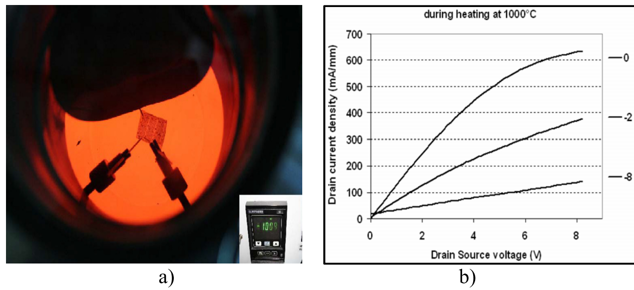

FIGURE 8. 0.25×50 μm^2 AlIn/GaN HEMT device tested at 1000°C: a) Sample under test, b) I-V characteristics where V_{GS} is swept from -8V to 0V by steps of 4V [67].

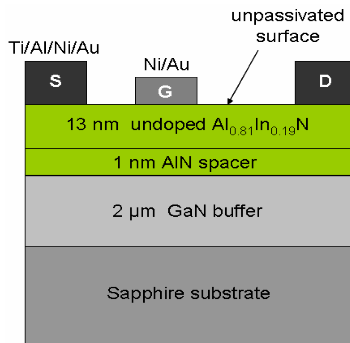

FIGURE 9. Schematic cross section of an AlInN/GaN HEMT structure [67].

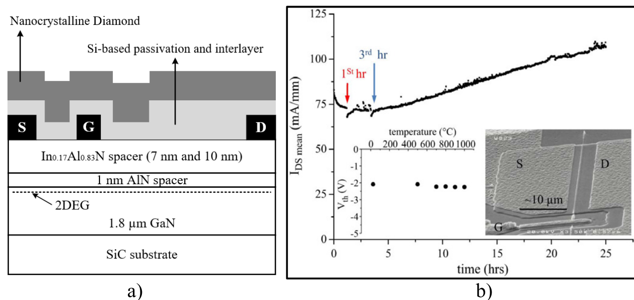

FIGURE 10. a) Cross section of NCD overgrown $In_{0.17}Al_{0.83}N$/GaN HEMT [75], b) Evolution of the mean drain–source current ($I_{DS,mean}$) with test time. (Inset left) Evolution of threshold voltage (V_{th}) from RT up to 1000°C. Small changes above 600°C can be attributed to a slight increase in the gate diode leakage current. (Inset right) SEM picture of the device, SiN passivation removed, after 25 h testing at 1000°C. No visible damage can be observed [74].

such as current collapse and gate leakage by utilizing thermal oxidation of the LM-InAlN which, in terms, appears as a perfect surface passivation component.

Preliminary testing at 800°C ensures the compatibility of NCD growth with the HEMT capability while observing degradation in metallization and passivation. The optimization is done by Diamond growth process developing Diamond coated HEMT devices (Fig. 10a) capable for continuous operation at 1000°C (Fig. 10b). Additional improvement can be achieved with this HEMT structure to sustain higher temperature. The observed degradations were not in the transistors but only in other peripheral elements such as metallization and passivation.

Aiming to increase NCD films thickness, the overgrowing was performed with no other changes besides the omission of Cu from ohmic contacts that was used as gate metal only. At storage temperature of 1000°C, Cu diffuses into the Si_3N_4 passivation layer, thus inducing conduction paths on the surface that eventually lead to short circuits between contacts.

To solve the situation, Mo or Pt replaced the Cu and the deposition conditions of PCVD Si_3N_4 was regulated. The following step was the deposition of the bias enhanced nucleation (BEN) interlayer system and a NCD layer approximately 3μm thick obtained after 28 hours of growth at 750°C. After that, in-situ Si_3N_4 was used as an alternative to the PCVD Si_3N_4 showing convenience for high power GaN devices.

Another alternative was the utilization of an Al_2O_3 layer obtained by atomic layer deposition (ALD) that showed high thermal stability. This passivation layer is good in MOSHEMT as it allows improving the gate diode stability at high ambient temperature by considerably lowering the gate leakage. As proposed future work, the single crystal Diamond substrate can be integrated with the top NCD coating layer leading to Diamond encapsulated GaN HEMT devices with exceptional heat extraction capability and durable surface.

A homojunction vertical GaN PIN rectifier was characterized at various temperatures [76]. The device was fabricated on a free-standing GaN substrate and tested from room temperature up to 175°C with free carrier concentration of 2×10^{16} cm^{-3}. The positive impact of a thin layer of Gd_2O_3 gate dielectric on an AlGaN/GaN MOSHEMT was demonstrated in [77]. The device was grown on a silicon substrate and tested at 500°C, where reported results show lower gate leakage current and stable DC performance when compared with conventional AlGaN/GaN HEMTs. Moreover, it was concluded that the thermal stability of GaN with this Gd_2O_3 dielectric layer could be enhanced by a soft thermal annealing process.

C. GaN IMPLEMENTATION

Despite the suitability of GaN technology for HT environment, limited integrated circuits and sensors are implemented based on GaN devices for HT applications [5], [78], [79]. In [79], a 31-stage ring oscillator, frequency dividers, several logic gates, and a comparator as shown in Fig. 11 have been implemented based on GaN/AlGaN HFET device and tested at 300°C. Another work [78] presents an AlGaN/GaN-based inverter grown on sapphire substrate by MOCVD and integrated with depletion mode HEMT and enhanced mode MOSFET. The inverter is characterized at high temperature between room temperature and 300°C. The relative variations of voltage swing, threshold voltage, logic-low noise margin and logic-high noise margin are respectively 2.2%, 5.7%, 12.9% and 4.9% from RT to 300°C. Novel AlInN/GaN integrated circuits had been demonstrated in [5] operating at 500°C. The fabricated inverter and differential amplifier (shown in Fig. 12) were tested at 500°C showing stable performance with internal response time 45 ns and unit-gain bandwidth above 1MHz. High-K passivation/gate dielectrics and new metallization scheme sustainable at high opera-

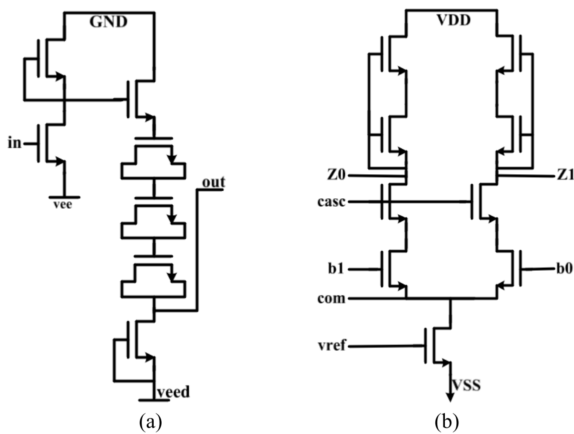

FIGURE 11. Schematic of GaN HFET-based digital circuits. (a) Inverter block used in ring oscillator, and (b) Comparator [79].

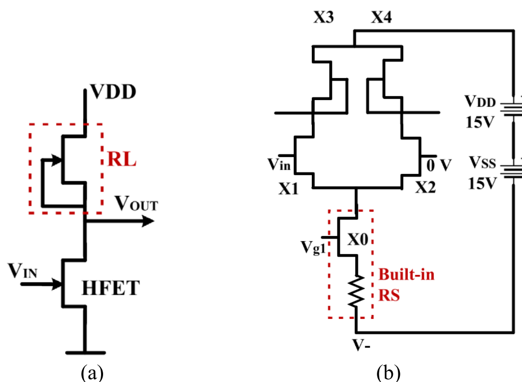

FIGURE 12. Schematic of GaN HFET-based integrated circuits. (a) Inverter, and (b) Differential amplifier [5].

tion temperature are the main advancements in that work. Mo/Al/Mo ohmic metal stack was utilized to solve the problems of Ti/Al/Ti/Au ohmic contact and Ti/Au interconnect at high operation temperature of 500°C.

Recently, a team at the Polystim Neurotechnologies Laboratory [80] is investigating the possibility to develop microelectronic systems for harsh environment based on AlGaN/GaN HEMT [81]–[84]. Some preliminary results showed relatively stable characteristics of GaN devices tested at temperatures ranging from room temperature to 400°C. By completing the development of robust models for the desired GaN device, the next step is directed towards implementing wireless power and data transmission systems dedicated to aerospace harsh-environment applications.

V. CONCLUSION

The electrical and material properties of GaN semiconductors make them excellent candidates for high temperature applications. In spite of GaN superiority over other known conventional devices, there are still many challenges with GaN based technologies, including material, ohmic and Schottky contacts. These challenges should be overcome before the exceptional ability of GaN to function at extreme temperature exceeding 600°C can be fully leveraged. We reviewed in this paper technological and intrinsic limitations of GaN, including thermal, chemical, current collapse and device self-heating limitations.

This review also summarized several significant recent developments of GaN devices as well as their use in harsh environments. In spite of the significant reported recent developments, the maturity of GaN technologies still limit their use in systems that must withstand harsh environments. On the road to maturity, further work is required to obtain integrated devices that are reliable at high temperature. Significant efforts are required to characterize and improve GaN fabrication processes.

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