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A Resonant Gate Driver for Silicon Carbide MOSFETs

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ABSTRACT In this paper, a resonant gate driver for silicon carbide power MOSFET is proposed. This resonant gate driver contains four N-MOSFETs, a resonant inductor, and a capacitor. The proposed gate driver recycles the energy which is stored in the gate capacitor of the SiC MOSFET. The gate drive losses of the resonant gate driver are reduced greatly, and the switching frequency can reach MHz. The design and the loss analysis are introduced in this paper. Finally, the simulation model and the experimental platform of the resonant gate driver are built to validate the theoretical analysis. Both the simulation and experiment results are provided to verify the feasibility and high performance of the proposed resonant gate driver.

INDEX TERMS SiC MOSFET, resonant gate driver, gate drive losses, high frequency.

I. INTRODUCTION

Recently, SiC MOSFET has been widely used on motor driving, switching power supply and grid-tied inverter due to the performances of high thermal conductivity, high voltage pressure and lower on-state resistance ($R_{DS(on)}$) [1]–[5]. The SiC MOSFET may work under extremely high frequency and the switching frequency can reach MHz. However, the gate drive losses of the SiC MOSFET cannot be ignored and serious consequences such as overheating might happens to the gate drive circuit under certain high frequency applications, since the gate drive losses are proportional to switching frequency. Then the design of gate driver for the SiC MOSFET is quite important to widen and promote the applications of the wide-band power devices.

The power losses of the gate driver can be expressed as

$$P_{gate} = Q_g(|V_{CC}| + |V_{EE}|)f_s \tag{1}$$

where, Q_g is the total gate charge of the SiC MOSFET, f_s is the switching frequency, V_{CC} and V_{EE} are the gate voltage of the SiC MOSFET during turn-on and turn-off, respectively.

The conventional gate driver of the SiC MOSFET is shown in Figure 1, where the gate drive energy is consumed on the gate resistor R_g [6], [7]. In order to reduce the gate drive losses, many schemes have been proposed using auxiliary components to recover gate energy [6]–[20]. Resonant gate driver has been put forward by using an inductor which is connected in series in drive circuit to recycle the energy [8]–[13]. This resonant gate driver can reduce the drive losses, but only positive voltage is provided and then this driver cannot switch off the SiC MOSFET reliably, especially in high frequency applications. In [14], a resonant gate driver with gate voltage feedback loop is given and can keep the gate voltage stable, but it only provides positive voltage also. The resonant gate driver with full-bridge configuration, which provide both positive and negative voltage are proposed in [15], [16]. However, the negative voltage is equal to the positive voltage, and it is not suitable to the SiC MOSFET since it only needs small negative voltage to turn off the device.

To meet the drive requirements of the SiC MOSFET, a voltage level shifting circuit is proposed in [17], where the voltage of resonant gate driver is adjusted to suitable value of the gate voltage for the SiC MOSFET. However, the gate voltage will be distorted under high switching frequency. The resonant gate drivers in [7] and [18], [19] have dual power supply, and can provide suitable drive voltage during turn-on or turn-off process for the SiC MOSFET. In [20], a capacitor is used to replace negative power supply and provide negative drive voltage. In this paper a new resonant gate driver is proposed for the SiC MOSFET, which can achieve high efficiency especially in high frequency applications.

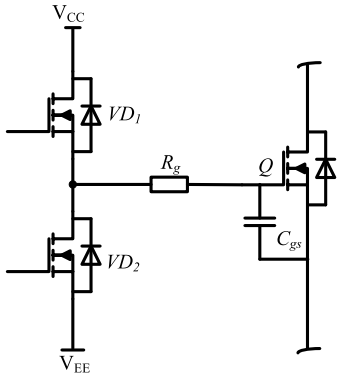

FIGURE 1. The conventional gate driver of SiC MOSFET.

In this paper, the resonant gate driver is put forward and the operation principle is introduced in section II. The design and loss analysis of the resonant gate driver are discussed in section III. Section IV and Section V present the simulations and experimental validations, respectively. Finally, the conclusions are given in section VI.

II. RESONANT GATE DRIVER

The circuit structure of the proposed resonant gate driver for the SiC MOSFET is shown in Figure 2. It contains four N-MOSFETs S_1-S_4, resonant inductor L_r and capacitor C_r. Here dual power supply is adopted which is similar as [7] and [18], [19], however less reactive component is used than [7] and [18]–[20].

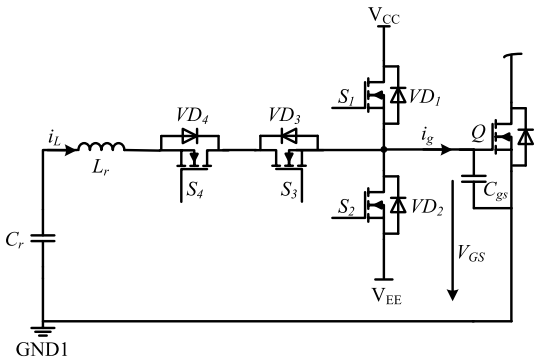

FIGURE 2. The proposed resonant gate driver.

The main waveforms in resonant gate driver are shown in Figure 3. By switching the auxiliary MOSFET S_1-S_4 sequentially, the effective driving of SiC MOSFET can be realized. Figure 4 shows the operation modes of the resonant gate driver, where total 8 modes are shown during a switching cycle. Eight modes appear in sequence according to the order of time t_0-t_7, as shown in Figure 4(a)-(h). The details of these modes are discussed as follows.

Mode 1 [t_0-t_1]: Prior t_0, S_2 is on and S_1 is off. At that time, the gate voltage of the SiC MOSFET (V_{GS}) is clamped at V_{EE}. At t_0, S_3 turns on under zero current switching (ZCS). C_r begins to pre-charge L_r as a stable voltage source. The current path is C_r-L_r-VD_4-S_3-S_2. The current (i_L) in L_r increases linearly, and gate voltage V_{GS} is equal to V_{EE}, then the SiC MOSFET is off.

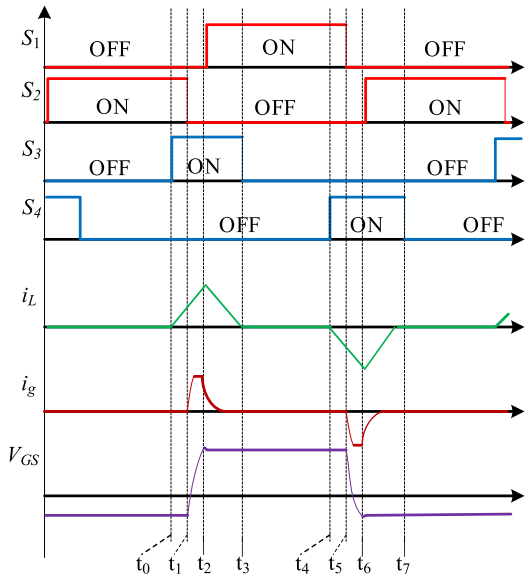

FIGURE 3. The timing sequence of resonant gate driver.

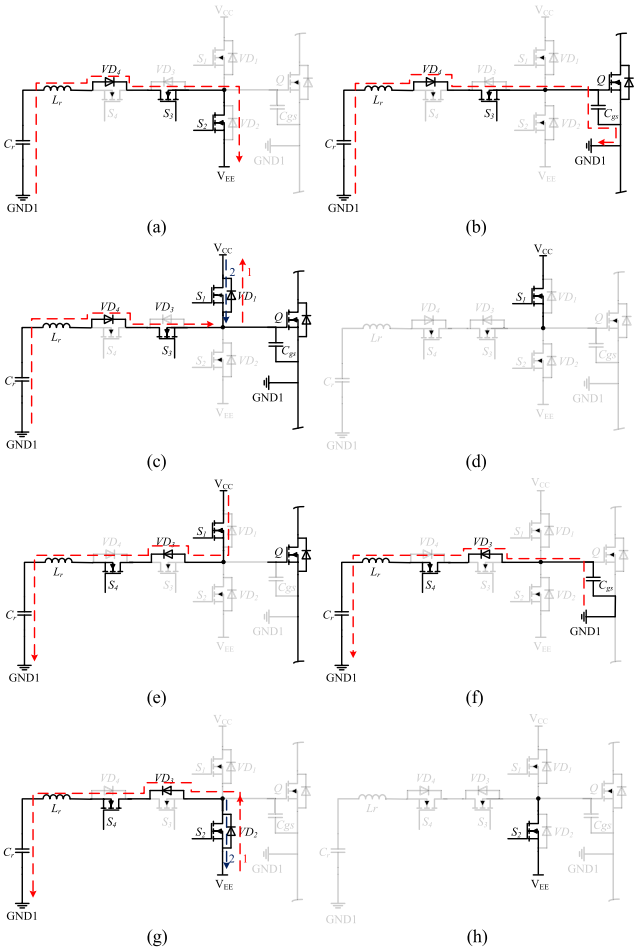

FIGURE 4. Operation modes of resonant gate driver. (a) Mode 1, t_0-t_1. (b) Mode 2, t_1-t_2. (c) Mode 3, t_2-t_3. (d) Mode 4, t_3-t_4. (e) Mode 5, t_4-t_5. (f) Mode 6, t_5-t_6. (g) Mode 7, t_6-t_7. (h) Mode 8, t_7-t_8.

Mode 2 [t_1-t_2]: S_2 turns off under zero voltage switching (ZVS) at t_1, then inductor current i_L per-charge the gate capacitor C_{iss} which equals the sum of gate-to-source capacitor C_{gs} and gate-to-drain capacitor C_{gd}. The gate current i_g is approximately constant and equivalent to constant current source driver. The current path is C_r-L_r-VD_4-S_3-C_{iss}, and the gate voltage rises.

Mode 3 [t_2-t_3]: At t_2, the V_{GS} rises up to V_{CC}, and the VD_1 turns on when the V_{GS} over V_{CC}. The gate voltage $V_{GS} = V_{CC} + V_D$ (V_D is the forward bias voltage of diode VD_1), S_1 turns on under ZVS at this time. The inductor current i_L is decreased and the energy stored in L_r is fed back to power source.

Mode 4 [t_3-t_4]: At t_3, S_3 turns off under ZCS. The gate of SiC MOSFET is connected to V_{CC} and the SiC MOSFET turns on reliably.

Mode 5 [t_4-t_5]: At t_4, S_4 turns on under ZCS, and the inductor current i_L rises in reverse. The current path is V_{CC}-S_1-VD_3-S_4-L_r-C_r, and the SiC MOSFET is still on.

Mode 6 [t_5-t_6]: At t_5, S_1 turns off under ZVS. C_{iss} begin to discharge, and the path is C_{iss}-VD_3-S_4-L_r-C_r. The energy stored in the gate is fed back to the inductor, and the gate voltage decreases.

Mode 7 [t_6-t_7]: At t_6, VD_2 turns on and the inductor current i_L freewheeling through VD_2.

Mode 8 [t_7-t_8]: At t_7, S_4 turns off under ZCS. The gate of the SiC MOSFET is connected to negative voltage V_{EE} and gate voltage is clamped at V_{EE}. The SiC MOSFET turns off reliably.

So the advantages of the proposed resonant gate driver are:

(1) The pre-charging stage and pre-discharging stage accelerate the turn-on and turn-off moments which can improve the switching frequency.
(2) The inductor L_r is resonant with the gate capacitor C_{iss} and recycles the energy stored in the gate of MOSFET, which can reduce the gate losses.
(3) S_1 and S_2 are under ZVS, and S_3 and S_4 are under ZCS, which reduces the switching loss of auxiliary switches.

Comparisons between the proposed resonant gate driver and other resonant gate drivers are provided in Table 1.

TABLE 1. Comparison of different resonant gate drivers (RGD).

RGD proposed in	suitable negative voltage	complexity degree	very high frequency operation	noise immunity
this paper	√	**easy**	√	√
[7]	√	difficult	√	√
[11]	none	easy	√	none
[14]	none	difficult	√	√
[17]	√	middle	none	none
[18]	none	difficult	none	none

It is shown in Table 1 that the proposed resonant gate driver do not have the disadvantages of other resonant gate drivers, and it is suitable for high frequency applications.

III. DESIGN AND LOSS ANALYSIS

The losses are the main consideration for design of the resonant gate driver. The selection of L_r and C_r is most important during the design process which will affect the performance and be related to the losses of the gate driver.

A. SELECTION OF L_r AND C_r

Assuming that the pre-charging time of inductor is t_M, the voltage across the inductor is (V_{Cr}-V_{EE}), as shown in Figure 4(a). t_N is the time interval where energy stored in L_r is fed back to power source, and the voltage across the inductor is (V_{CC}-V_{Cr}), which is shown in Figure 4(c). According to the volt-second balance characteristics of the inductor, the following equation can be obtained.

$$(V_{Cr} - V_{EE}) \cdot t_M = (V_{CC} - V_{Cr}) \cdot t_N \tag{2}$$

Assuming $t_M = t_N$, the voltage of C_r can be obtained from (2). Then it has

$$V_{Cr} = \frac{V_{CC} + V_{EE}}{2} \tag{3}$$

During the inductor pre-charging stage, the ripple of the capacitor voltage can be calculated by

$$\Delta V_{Cr} = \frac{1}{C_r}\int_0^{t_M} \frac{V_{Cr} - V_{EE}}{Lr} \cdot tdt = \frac{V_{Cr} - V_{EE}}{2C_r \cdot L_r} \cdot t_M^2 \tag{4}$$

So C_r is determined by (4). It is

$$C_r \geq \frac{V_{Cr} - V_{EE}}{2\Delta V_{Cr} \cdot L_r} \cdot t_M^2 \tag{5}$$

Then the resonant inductor L_r in (5) can be calculated by

$$L_r = \frac{V_{CC} \cdot t_{res}}{Q_g}\left(\frac{t_{res}}{4} + t_M\right) \tag{6}$$

where t_{res} is the rise time of V_{GS}. At the same time, the inductance of L_r should be selected to make the turn-on speed (t_r) of SiC MOSFET less than 3% of the total switching period (T). Then it has

$$t_r \approx \pi\sqrt{L_r C_{iss}} \tag{7}$$

$$\frac{t_r}{T} \leq 0.03 \tag{8}$$

where C_{iss} is the gate capacitor of the SiC MOSFET. Thus, L_r should be designed as following equation.

$$L_r = \frac{t_r^2}{\pi^2 C_{iss}} \leq \frac{(0.03T)^2}{\pi^2 C_{iss}} = \frac{0.03^2}{\pi^2 f^2 C_{iss}} \tag{9}$$

According to (6) and (9), the resonant inductor L_r in proposed gate driver is determined.

B. LOSS ANALYSIS

The losses of gate drive can be calculated according to the selected parameters of L_r and C_r. The total gate drive losses of resonant gate driver (P_g) consists of the drive losses of S_1-S_4 (P_{gs}), conduction losses in drive circuit (P_{cond}), switching losses of S_1-S_4 (P_{sw}) and the losses of L_r (P_{Lr}).

Drive losses of $S_1 \sim S_4$ can be calculated as

$$P_{gs} = (Q_{g-S_1} + Q_{g-S_2} + Q_{g-S_3} + Q_{g-S_4})V_{gs_s} - f_s \quad (10)$$

where Q_{g-S1}, Q_{g-S2}, Q_{g-S3} and Q_{g-S4} are the total gate charge of S_1 to S_4 respectively, V_{gs-s} is the gate voltage of S_1-S_4. Here same type switches are adopted for S_1-S_4 in this paper, so the drive losses of $S_1 \sim S_4$ are equal.

The conduction losses in drive circuit are related to inductor current i_{Lr}. When the circuit is operated in mode 1, mode 3, mode 4, mode 5, mode 7 and mode 8, i_{Lr} in resonant gate driver can be expressed as

$$i_{L_r}(t) = \frac{V_{CC}}{R_{eq}} + (I_{L_r0} - \frac{V_{CC}}{R_{eq}})e^{-\frac{R_{eq}}{L_r}t} \quad (11)$$

When the circuit is in mode 2 and mode 6, i_{Lr} in resonant gate driver can be expressed as

$$i_L(t) = \frac{V_{CC} - V_{gs0} - 0.5R_{eq}I_{L_r0}}{\omega L_r} e^{-\frac{R_{eq}}{2L_r}} \sin(\omega t) + I_{L_r0} e^{-\frac{R_{eq}}{2L_r}} \cos(\omega t) \quad (12)$$

where ω is angular frequency of the current and can be express as

$$\omega = \frac{\sqrt{4L_r C_{iss} - R_{eq}^2}}{2L_r C_{iss}} \quad (13)$$

The R_{eq} in (11) and (12) are $2R_{ds}$ and $R_g + R_{ds}$ respectively. R_{ds} is the on-resistance of S_1-S_4. R_g is the internal gate resistance of the SiC MOSFET.

Conduction losses in drive circuit (P_{cond}) contain two parts. One part is the loss of equivalent resistance R_{eq} (P_{Req}), the other is the loss of Diode (P_D). Then it has

$$P_{cond} = P_{R_{eq}} + P_D \quad (14)$$

The loss of R_{eq} can be expressed as

$$P_{R_{eq}} = R_{eq} f_s \int_0^{T_s} i_{L_r}^2(t)\, dt \quad (15)$$

The loss of P_D can be express as

$$P_D = V_D f_s \int_0^{T_s} \left| i_{L_r}(t) \right| dt \quad (16)$$

where, T_s is the period of switching cycle. V_D is the positive conduction voltage of diode.

S_1 and S_2 are operated under ZVS, while S_3 and S_4 are operated under ZCS. So the switching losses of S_1-S_4 (P_{sw}) can be ignored in this paper.

The losses of L_r contain copper loss (P_{cop}) and core loss (P_{cor}). They are

$$P_{L_r} = P_{cop} + P_{cor} \quad (17)$$

where copper loss can be calculated by

$$P_{cop} = I_{L_r\_RMS}^2 R_{ac} \quad (18)$$

where R_{ac} is resistance of L_r, I_{Lr_RMS} is RMS value of inductor current.

The core loss of L_r can be obtained from

$$P_{cor} = K_1 f^x B^y V_e \quad (19)$$

where, K_1 is the core material constant, f is the frequency, B is the peak magnetic flux density, x is the index of frequency, y is the index of magnetic flux density, V_e is the effective core volume.

So the total gate drive losses P_g can be express as

$$P_g = P_{gs} + P_{cond} + P_{sw} + P_{L_r} \quad (20)$$

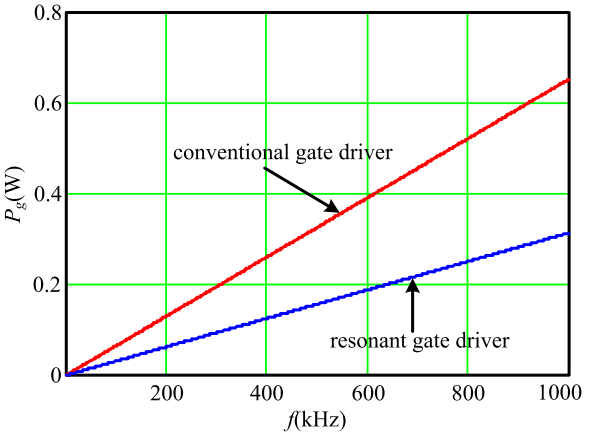

FIGURE 5. The losses of resonant gate driver and conventional gate driver.

The losses of resonant gate driver and conventional gate driver are calculated and compared, as shown in Figure 5. Comparing to the conventional gate driver, the losses of the resonant gate driver are reduced obviously. As the frequency increases, the losses increase in both driver, however about 50% losses are reduced in the resonant gate driver.

IV. SIMULATIONS

To verify the validity and feasibility of the resonant gate driver proposed in this paper, the simulations are carried out, where Pspice software is used. By using the design of the circuit introduced in section III. The parameters of resonant gate driver adopted in simulations are listed in Table 2.

TABLE 2. The parameters of resonant gate driver.

parameter	value	parameter	value
SiC MOSFET	SCT3080KL	V_{CC}	20 V
S_1~S_4	IRLR2703	V_{EE}	-4 V
L_r	120 nH	t_M	25 µs
C_r	1 µF	t_{res}	35 µs

The simulation results of the resonant gate driver are shown in Figure 6. It contains the gate voltage of S_1-S_4, inductor current i_L, the gate current (i_g) of the SiC MOSFET. It shows that the results agree with theoretical analysis well.

Figure 7 shows the gate voltage V_{GS} of the SiC MOSFET, where the rise time and fall time of the gate voltage are both

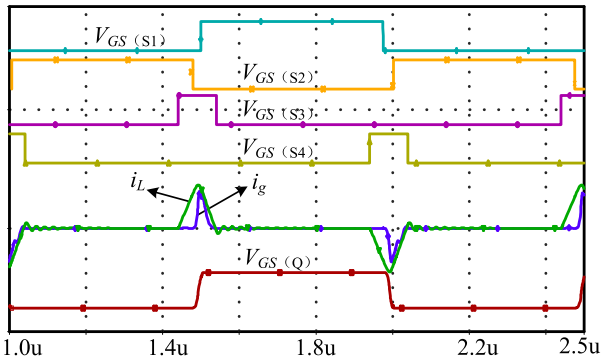

FIGURE 6. The simulation results of resonant gate driver.

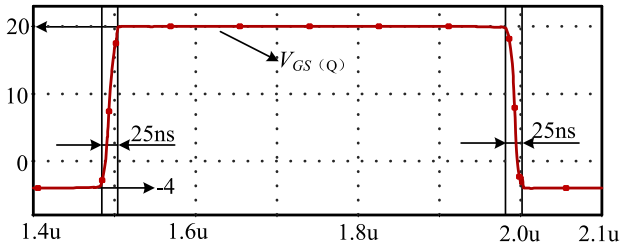

FIGURE 7. The simulation result of V_{GS} of SiC MOSFET.

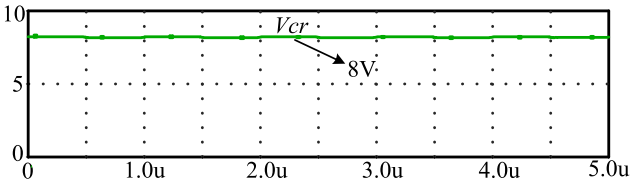

FIGURE 8. The simulation result of voltage across capacitor.

25 ns, and then high frequency drive for the SiC MOSFET might be realized. The gate voltage of the SiC MOSFET is 20 V for turn-on process and −4 V for turn-off process. Then the SiC MOSFET can be turned on and turned off reliably.

Figure 8 shows the simulation results of the voltage across the capacitor, where V_{Cr} is the voltage across the capacitor C_r. V_{Cr} can keep voltage balance during the one period of switching cycle, and the value of voltage is the same as that calculated in (3).

Figure 9 shows the waveforms of V_{GS} and I_D of S_1 and S_2. It shows that S_1 and S_2 can be operated under ZVS at both turn-on and turn-off process. So, the drive losses can be greatly reduced.

V. EXPERIMENTAL VALIDATIONS

Based on the simulations, the experimental platform of the resonant gate driver is built, as shown in Figure 10. It contains DSP controller, resonant gate driver, external power supply and isolated power supply for the SiC MOSFET. External power supply provides power for optocoupler and isolated power supply. Isolated power supply can generate positive

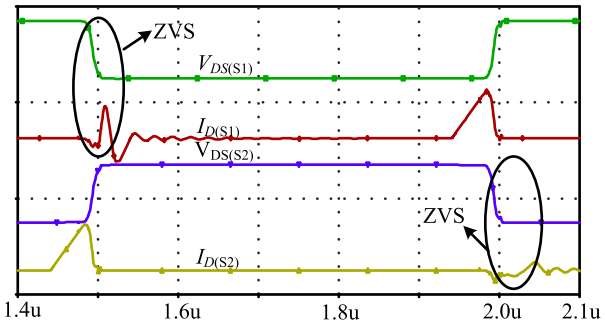

FIGURE 9. The V_{DS} and I_D of the S_1 and S_2.

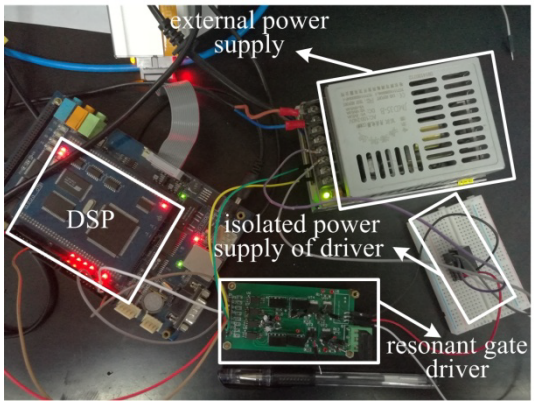

FIGURE 10. The experimental platform of resonant gate driver.

voltage V_{CC} and negative voltage V_{EE} for the resonant gate driver.

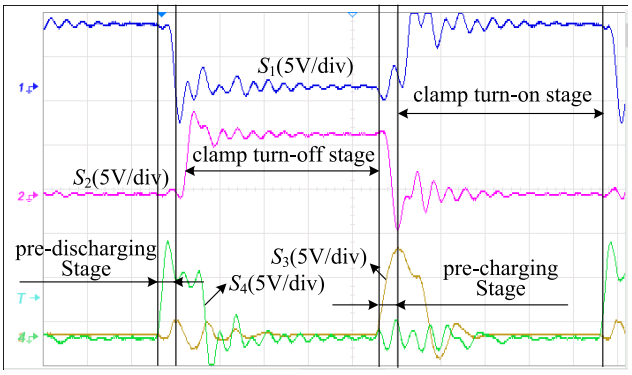

FIGURE 11. The experiment waveforms of V_{GS} of MOSFET $S_1 \sim S_4$.

Figure 11 shows the drive pulses of S_1-S_4. The drive signal of the SiC MOSFET is mainly divided into four stages: pre-discharging stage, clamped turn-off state, pre-charging stage and clamped turn-on stage.

Figure 12 shows the waveforms of V_{GS} and I_g in the SiC MOSFET. Due to the presence of stray inductance on the driving circuit, the gate voltage has spikes and oscillations under 1MHz. The gate drive current in experiment is 2 A, and it meets the requirement of the SiC MOSFET.

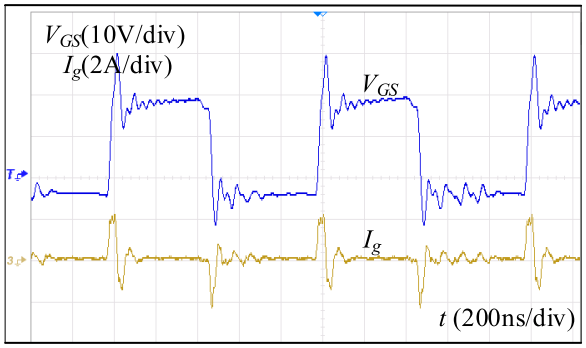

FIGURE 12. The V_{GS} and I_g of SiC MOSFET.

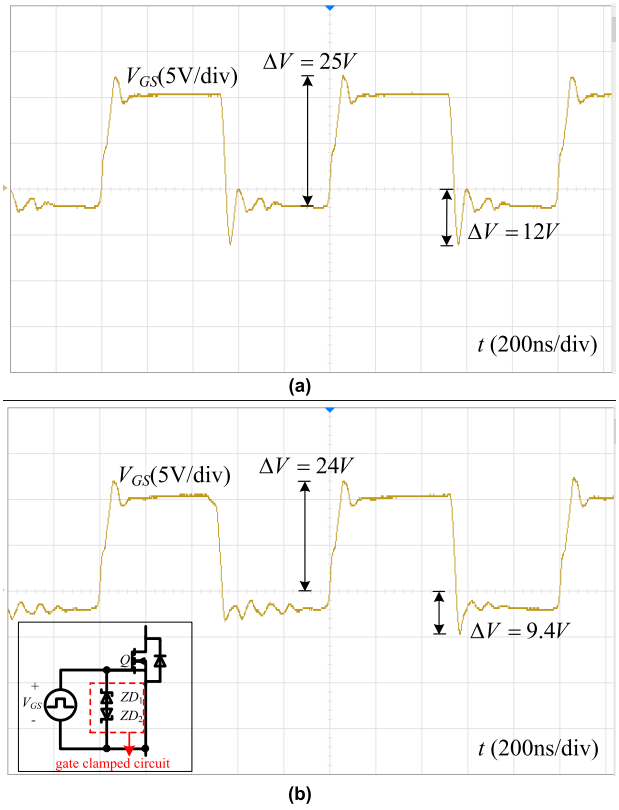

FIGURE 13. The gate voltage of SiC MOSFET. (a) without gate clamped circuit. (b) with gate clamped circuit.

In order to reduce the voltage spikes of the gate voltage, the gate clamped circuit can be parallel connected to the gate of the SiC MOSFET. The gate clamped circuit may be composed of Zener diodes with reverse polarity. The experiment results with gate clamped circuit in Figure 14 show that the forward gate voltage is reduced from 25 V to 24 V and the reverse gate voltage is reduced from 12 V to 9.4 V. So the drive voltage is optimized by parallel connecting the gate clamped circuit to the gate of the SiC MOSFET.

Figure 14 shows the output voltage of conventional gate driver at 150 kHz and 1 MHz. The experiment results show that conventional gate driver works effectively at 150 kHz.

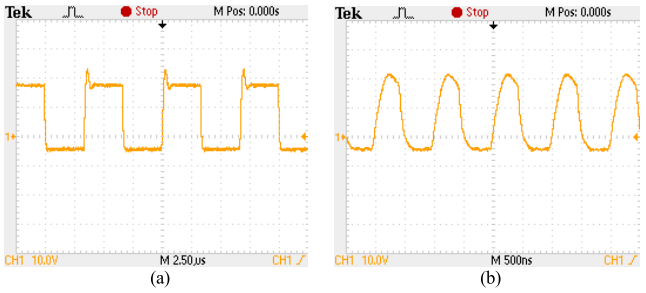

FIGURE 14. The output voltage (V_{GS}) of conventional gate driver. (a) 150 kHz. (b) 1 MHz.

However, the drive pulse of the SiC MOSFET is distorted when the switching frequency reaches 1 MHz. The gate drive signal is no longer a rectangular wave and cannot meet the basic requirements of the SiC MOSFET.

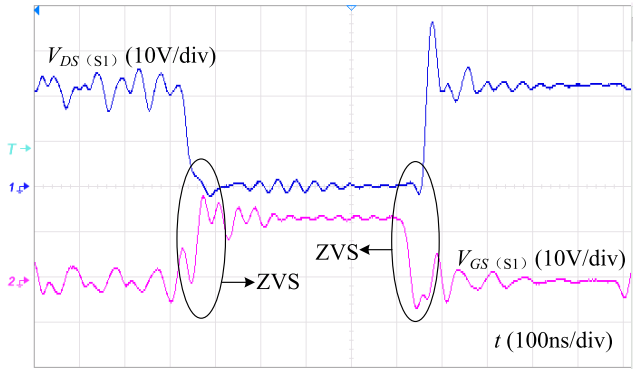

FIGURE 15. The V_{GS} and V_{DS} of S_1.

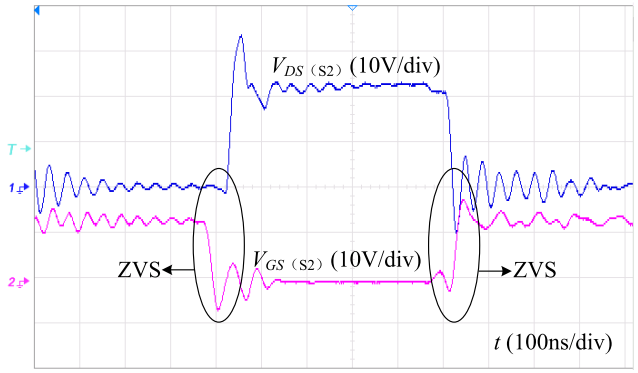

FIGURE 16. The V_{GS} and V_{DS} of S_2.

Figure 15 and Figure 16 show the gate-to-source voltage V_{GS} and drain-to-source voltage V_{DS} of S_1 and S_2, respectively. The voltage oscillations are normally existed during the switching period because of high frequency and stray inductance. The MOSFET S_1 and S_2 can achieve the ZVS operation during turn-on and turn-off process.

Figure 17 shows measured power losses of the resonant gate driver and the conventional gate driver under 1 MHz.

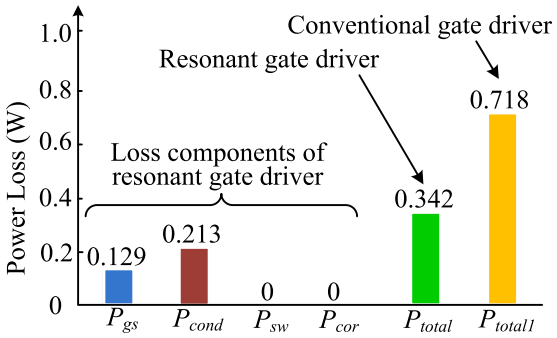

FIGURE 17. Power Losses of Resonant Gate Driver and Conventional Gate Driver under 1 MHz.

Here the core losses and switching losses are neglected due to the air core inductor is used and soft switching operation of S_1-S_4 is realized. The total power losses of the resonant gate driver are reduced to 0.342W, which improves the efficiency of gate driver greatly.

The experiment results show that the resonant gate driver proposed in this paper has good performances in high frequency and owns higher efficiency than the conventional gate driver.

VI. CONCLUSION

In this paper, a new resonant gate driver for the SiC MOSFET is proposed, which may provide suitable negative gate voltage and operate with high noise immunity and high frequency. The resonant inductor is used to recover the energy which is stored in the gate capacitor of the SiC MOSFET. The operation principle of the resonant gate driver is introduced. The design of main circuit devices is discussed and the drive losses of the gate driver are analyzed. The simulations and experimental validations are carried out to verify the performances of the proposed resonant gate driver. The proposed resonant gate driver has many advantages, such as higher operation frequency and reduced gate drive losses.

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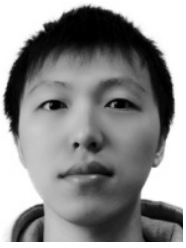

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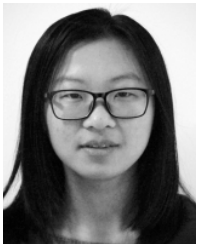

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