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A 3.2 Gb/s 16-Channel Transmitter for Intra-Panel Interfaces, With Independently Controllable Output Swing, Common-Mode Voltage, and Equalization

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ABSTRACT The use of coupled-bias common-mode feedback allows a low-voltage differential signaling driver, implemented in a deep-submicron process, to adjust its output common-mode voltage, as well as the output swing and equalization strength independently. This form of differential signaling driver has been incorporated in a 16-channel transmitter for the timing controller of an intra-panel interface. The flexibility of its output characteristics allows it to accommodate the range of channel characteristics commonly found in the intra-panel interface of an ultra-high-definition display. Fabricated in a 28-nm bulk CMOS process, our 16-channel transmitter occupies 1.39 mm^2. Its total power consumption is 203.2 mW with a supply voltage of 1.05 V, running at 3.2 Gb/s with the maximum output swing. Measurements confirm that the transmitter can operate from 0.8 to 3.2 Gb/s with channels that replicate those encountered in an intra-panel interface. The maximum controllable range of the output swing, the output common-mode voltage, and equalization are 216–1072 mV_{diff}, 291–604 mV, and 0–14.6 dB, respectively.

INDEX TERMS Low-voltage differential signaling, driver, transmitter, intra-panel interface, timing controller.

I. INTRODUCTION

Televisions (TVs) are currently in transition from full-high-definition (FHD) to ultra-high-definition (UHD) resolution. An ultra-high-definition display has a resolution of 3840×2160, and usually supports a refresh rate of 120Hz and a color depth of 10 bits. This requires a pixel clock frequency of about 1.1GHz, and thus 10-bit source drivers, which receive the data and control signals from a timing controller through an intra-panel interface and generate an analog signal that sends to the TV panel, must provide a data-rate of at least 2.7Gb/s. Therefore, the intra-panel interface, which has 16 differential signal pairs between the timing controller and the source driver, needs to support a data-rate of 3.0Gb/s or even higher with a 10% margin [1].

Fig. 1 shows the configuration of the timing controller and the source driver in an ultra-high-definition display which supports the point-to-point differential signaling generally used in intra-panel interfaces [2]–[4]. The channels of this interface consist of a connector, a flexible flat cable (FFC), and a long trace on the printed circuit board (PCB). Since the lengths of the channels are not equal, the characteristics of each channel, and hence the signal loss, will not

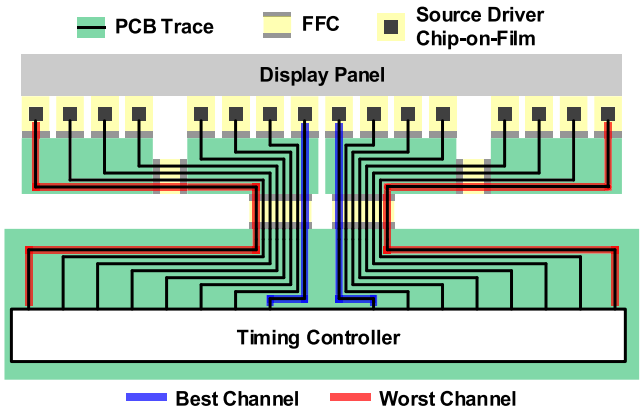

FIGURE 1. Configuration of multi-channel intra-panel interfaces for ultra-high-definition displays.

be uniform. These inequalities between channels are exacerbated by increases in data-rate [5], [6], and electromagnetic interference (EMI) and jitter also get worse [7], eventually leading to severe degradation of the quality of the transmitted signal. It is possible to compensate for differences between channels by adjusting the output swing and the strength of equalization [8], [9]. The common-mode voltage of the output signal should also be controllable, independent of both the output swing and equalization [10], [11], to cope with a variety of the channel, and to reduce the power consumption and design complexity of the source driver [12], [13].

Independent controllability of the output characteristics in the transmitter depends on the output driver topology. A current-mode driver [14] and voltage-mode drivers [15], [16], incorporated with the transmitter for multi-standard interfaces, provide independently controllable output swing and equalization in each channel. However, they are hard to control the common-mode voltage separately from the output swing.

To alleviate this issue, alternative designs [11], [17] employ an output driver together with a supply-voltage regulator and a ground-voltage regulator. This structure can control the output swing and the common-mode voltage independently by adjusting the level of the supply and ground voltages generated by the two regulators, but the increased power consumption and area of the voltage regulator are a significant disadvantage of this design. The common-mode voltage can be controlled independently without using a voltage regulator by introducing a low-voltage differential-signaling (LVDS) driver, and this approach has been incorporated into a 4-channel multi-standard transceiver [18]. However, a replica circuit and a buffer are required to control the common-mode voltage, and this increases the power consumption and the area of the circuit. In yet another design [10], a 12-channel transmitter for the timing controller can assert independent control of the output swing and equalization, and uses an LVDS driver with common-mode feedback to also control the common-mode voltage. However, this design can cause variations in the output swing with the adjustment of the common-mode voltage, and it needs additional bias generators to provide a stable current and voltage for the LVDS driver. This causes multiple current and voltage paths to deliver this bias current and voltage to each channel, again increasing the design complexity and the area.

In this paper, we present a 3.2Gb/s 16-channel transmitter that incorporates an LVDS driver with coupled-bias common-mode feedback, designed for the timing controller of intra-panel interfaces, which addresses these issues. Our LVDS driver can control the output swing and equalization separately. It also provides common-mode voltage control independently of the output swing and equalization by adjusting the bias voltage of current sources by the same amount in the same direction, without much requirement for additional bias generator and control circuitry. This approach can improve the signal quality of a transmitter which has to drive disparate channels in an intra-panel interface, potentially reducing the power consumption or the design complexity of the source driver.

II. LOW-VOLTAGE DIFFERENTIAL SIGNALING DRIVER WITH COUPLED-BIAS COMMON-MODE FEEDBACK

A. PRIOR ARTS

An LVDS driver is a type of push-pull current-mode driver for low-voltage signal transmission in point-to-point interfaces. It provides a power-efficient way of transmitting differential signals with low EMI and crosstalk [18].

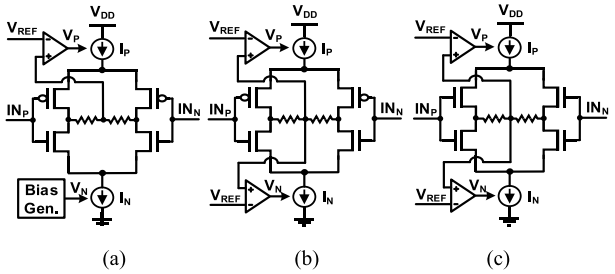

FIGURE 2. Previous LVDS drivers (a) [10], [19], (b) [20], and (c) [21].

Fig. 2 shows three previous LVDS driver topologies [10], [19]–[21]. The driver [10], [19] shown in Fig. 2(a) adjusts its output common-mode voltage by varying the reference voltage V_{REF} in the common-mode feedback loop. A common-mode feedback loop in [10] only adjusts the amount of V_P by adjusting the reference voltage V_{REF}. A shift of V_P moves the output common-mode voltage, but this can vary the output swing. Therefore, in this design, an additional bias generator (Gen.) should also be controlled to adjust the output swing and the output common-mode voltage independently. In [19], the bias generator is integrated with the amplifier in common-mode feedback, forming two common-mode feedback loops to adjust both V_P and V_N. However, each operation of these separate two loops can cause the variation of the output swing. In the design [20] shown in Fig. 2(b), complementary current sources and common-mode feedback loops have been introduced to save additional circuits, reduce simultaneous switching noise, and improve noise immunity; but these loops also increase power consumption and circuit area overhead, and the output swing can be affected by the common-mode adjustment. In the third design [21], as shown in Fig. 2(c), PMOS switches are replaced by NMOS switches to reduce loading of the input MOS of the LVDS driver. However, the reduction in process and supply voltage limits the overdrive voltage and reduces the noise margin.

B. PROPOSED DRIVER TOPOLOGY

Fig. 3 shows how our LVDS driver uses the coupled-bias common-mode feedback. There are 24 output driver cells, a coupled-bias common-mode feedback loop, a resistor digital-to-analog converter (DAC), and an output termination R_{TERM}. The differential output signals from the driver, OUT_P and OUT_N, are divided by large resistors R_{CM} to obtain the common-mode voltage V_{CM}. The resistor DAC

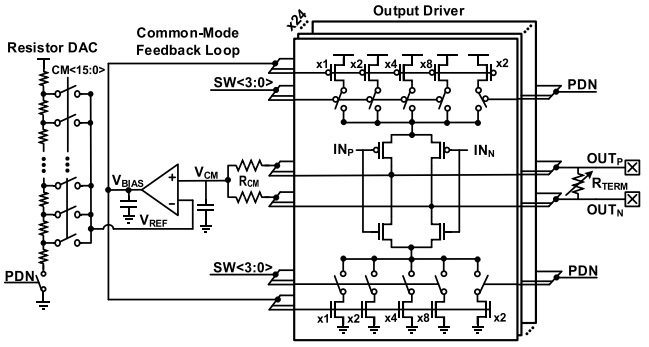

FIGURE 3. LVDS output driver with coupled-bias common-mode feedback.

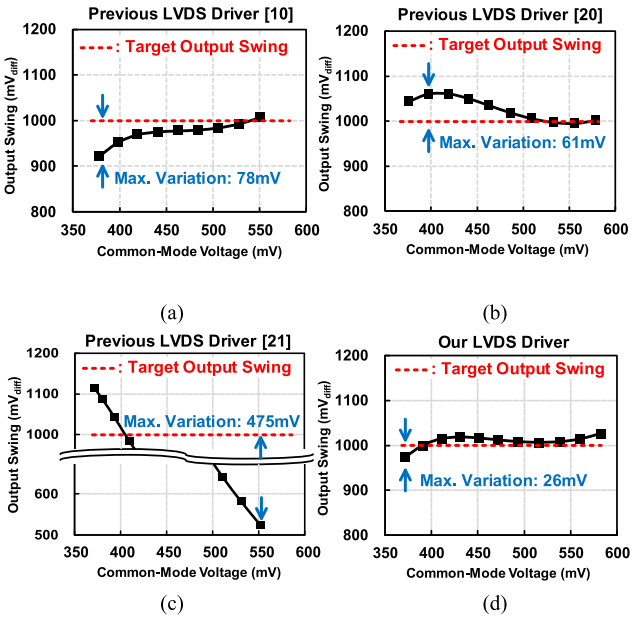

FIGURE 4. Simulated variations in output swing produced by adjustment of the common-mode voltage in previous LVDS drivers (a) [10], (b) [20], (c) [21], and (d) our LVDS driver.

generates 16 voltages, one of which is selected by the control signal CM<16:0> to be the reference voltage V_{REF} which determines the common-mode voltage of the output signal. An error amplifier in the common-mode feedback loop receives V_{CM} and V_{REF} and generates the output voltage V_{BIAS} from their relationship. In turn, V_{BIAS} adjusts the current sources in the LVDS driver to make the output common-mode voltage V_{CM} equal to V_{REF}. This coupled-bias common-mode feedback adjusts the single bias voltage used for the upper and lower current source, by the same amount in the same direction. It allows for independent control between the output swing and the common-mode voltage by reducing the variation in the output swing due to the common-mode voltage regulation. It also saves the bias generator, the amplifier, and the additional circuit.

The output swing of the output driver is determined by the control signal SW<3:0>, which switches current sources on or off, producing different currents. It varies the total amount of currents in the upper and lower current source equally. It is also possible to adjust equalization independently by changing the ratio of the number of unit drivers assigned to the main-tap and the post-tap. The output termination resistance R_{TERM} is also controllable in 5 steps with an open circuit and values of 300, 150, 100, and 75Ω.

To assess the effectiveness of coupled-bias common-mode feedback, we performed a simulation of the differential output swing produced by adjusting the output common-mode voltage in our LVDS driver and in the previous drivers shown in Fig. 2(a), (b), and (c). Fig. 4(a) shows what happens to an LVDS driver with a bias generator [10]. Varying the common-mode voltage from 378mV to 550mV changes the output swing from $922mV_{diff}$ to $1007mV_{diff}$, a maximum difference of 78mV from the target output swing. This is caused by the way in which V_P is changed while V_N stays constant in this circuit. The simulated result for an LVDS driver with complementary current sources and common-mode feedback loops [20] is shown in Fig. 4(b). Changing the control code moves the output common-mode voltage from 376mV to 579mV. The differential output swing varies from $995mV_{diff}$ to $1061mV_{diff}$, a maximum difference of 61mV from the target output swing. In this structure, the common-mode voltage is regulated by moving V_P and V_N. This regulates the common-mode voltage, but two separate common-mode feedback loops can adjust V_P and V_N to different amounts, thereby affecting the output swing. Fig. 4(c) shows the simulated result for an LVDS driver, in which PMOS switches are replaced by NMOS switches [21]. Controlling the common-mode voltage from 371mV to 552mV changes the output swing from $1115mV_{diff}$ to $524mV_{diff}$, a maximum difference of 475mV from the target output swing. Fig. 4(d) shows the simulated result for our LVDS driver. While the common-mode voltage of output signal adjusted from 372mV to 583mV, the output swing varies from $974mV_{diff}$ to $1026mV_{diff}$, a maximum difference of 26mV from the target output swing. Compared to the previous two structures, our LVDS driver with coupled-bias common-mode feedback has the least influence on the output swing by the regulation of the common-mode voltage, because V_P and V_N are adjusted by the same amount in the same direction. Therefore, our structure is suitable for controlling the output swing and the common-mode voltage independently.

The simulated ranges of the common-mode voltage are from 261mV to 579mV, from 239mV to 550mV, and from 356mV to 552mV respectively, for previous drivers in Fig. 2(a), (b), and (c). The corresponding range is from 281mV to 583mV for our LVDS driver.

Fig. 5 shows the results of 1000 runs of a Monte-Carlo simulation of the common-mode voltage and swing of the output signal of our LVDS driver when it is set to maintain a common-mode voltage of 450 mV and an output swing of $1000mV_{diff}$. The mean and standard deviation of the distribution of common-mode voltages are 451.4mV and 11.4mV respectively, and the mean and standard deviation of the distribution of output swings are $1016.3mV_{diff}$ and $46.4mV_{diff}$.

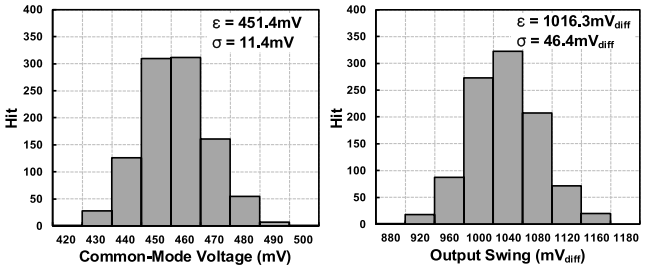

FIGURE 5. Results of 1000 runs of a Monte-Carlo simulation showing the variations of the output common-mode voltage and the output swing of our LVDS driver, when the common-mode voltage is 450mV and the output swing is 1000mV$_{diff}$.

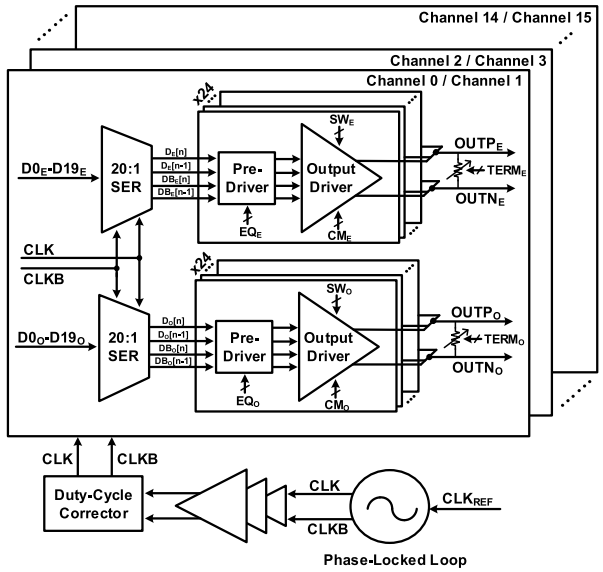

FIGURE 6. Architecture of the 16-channel transmitter for the timing controller.

It demonstrates that the common-mode voltage and output swing maintain the desired value well.

III. TRANSMITTER ARCHITECTURE

Fig. 6 shows the architecture of the 16-channel transmitter in the timing controller. This transmitter consists of a phase-locked loop (PLL), a clock distribution tree that includes a clock buffer and a duty-cycle corrector (DCC), and the data paths of 16 channels, each of which contains a 20:1 serializer, a pre-driver, and an output driver.

The PLL, which generates the differential clock signals CLK and CLKB within a frequency range of 0.4 to 1.6GHz, is located at the center of the transmitter. Spread-spectrum clock generation (SSCG) is used in the PLL to reduce EMI. The CLK and CLKB signals are distributed to each channel through the clock distribution tree, which has a duty-cycle corrector to compensate for errors in the duty-cycle of the signals.

The timing controller of the intra-panel interface should be designed so that there is little timing skew between adjacent channels. Thus each channel consists of a pair of symmetrical structures to limit the skew of its differential output signals OUTP/N$_E$ and OUTP/N$_O$. A 20:1 serializer in each channel converts the 20-bit parallel data to 1-bit full-rate serial data, while achieving 2-tap feed-forward equalization (FFE) by outputting the previous data bits D[n-1] and DB[n-1] as well as the current data bits D[n] and DB[n]. The pre-driver then transmits this serial data to the output driver, which has an LVDS driver structure with coupled-bias common-mode feedback to obtain independent control of the output swing, the output common-mode voltage, and equalization. This driver is composed of 24 identical driver cells, each of which outputs data by selecting either the current bit or the previous bit, as specified by the equalization control code EQ<6:0>, which adjusts the equalization strength. The output swing, the output common-mode voltage, and the termination resistance are independently controlled, as specified by the signals SW<3:0>, CM<15:0>, and TERM<3:0>.

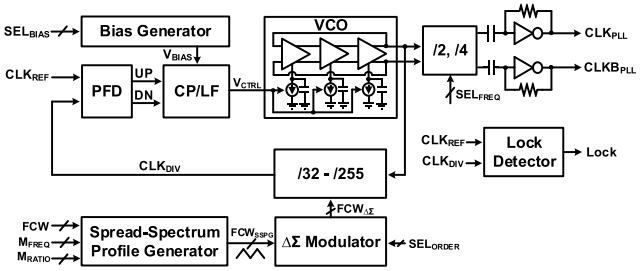

FIGURE 7. Block diagram of the phase-locked loop with spread-spectrum clock generation.

IV. CIRCUIT IMPLEMENTATION

A. PHASE-LOCKED LOOP

Fig. 7 is a block diagram of the PLL that generates the differential clock signals CLK$_{PLL}$ and CLKB$_{PLL}$ using in the transmitter of the timing controller. This PLL consists of a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LF), a bias generator (Gen), a voltage-controlled oscillator (VCO), a clock buffer, a programmable divider, a delta-sigma ($\Delta\Sigma$) modulator, a spread-spectrum profile generator, and a lock detector. It is an integer-N PLL, and generates an output clock signal with a frequency range between 400MHz and 1.6GHz from an input reference clock signal CLK$_{REF}$ which ranges from 20MHz to 100MHz.

The phase-frequency detector generates UP and DN signals by comparing the phase and frequency of the divided output clock signal CLK$_{DIV}$ and CLK$_{REF}$. These signals cause the charge pump to vary the current supplied to the loop filter, which in turn generates V$_{CTRL}$ to control the phase and frequency of the voltage-controlled oscillator. The charge pump uses a sub-threshold current bypass technique to compensate for the leakage current present in a deep submicron process [22]. Since the PLL has to operate over a wide frequency range, it is necessary to correct the loop bandwidth. Thus we arrange for the current going to the loop filter to be

adjusted under control of the signal SEL_{BIAS}, causing the bias generator to apply a voltage V_{BIAS} which modifies the output of the charge pump. In the default setting of the bias generator, the loop bandwidth of the PLL is 2MHz.

The VCO, which consists of a 3-stage ring oscillator, generates a clock signal with a frequency between 1.6GHz and 3.2GHz. It is controlled by the current generated from the tail current source, and voltage fluctuations at the drain of this current source are responsible for most of the noise coming from the oscillator. This phase noise is reduced by introducing a capacitor in parallel to the current source. The frequency of the clock signal produced by the VCO is reduced by an output divider controlled by the SEL_{FREQ} signal, and the frequency of the output clock signal can be varied from 400MHz to 1.6GHz. The clock buffer in the final stage increases the signal bandwidth and corrects any errors in the duty-cycle. The lock detector based on the digital counter [23] compares the values of rising edge counts in CLK_{REF} and CLK_{DIV}. When the frequencies of CLK_{REF} and CLK_{DIV} are the same, their count values become equal, and then the lock signal Lock is issued.

Our PLL uses the spread-spectrum technique to reduce the EMI produced by the clock signals [24]. This is particularly important in large display panels which require long channels. The SSCG scheme that has been implemented uses modulation frequencies between 30kHz and 33kHz, and a modulation ratio of 0.5%. Our SSCG is implemented by adjusting the dividing ratio of the programmable driver in the feedback loop, as specified by $FCW_{\Delta\Sigma}$ signal. The spread-spectrum profile generator receives the FCW signal, which informs it of the output frequency, the M_{FREQ} signal, which determines the modulation frequency, and the M_{RATIO} signal, which determines the modulation ratio. It transmits the FCW_{SSCG} signal, modulated with a triangular profile, to the delta-sigma modulator. This delta-sigma modulator performs noise shaping that moves the quantization noise generated by the SSCG to higher frequencies. The SEL_{ORDER} signal determines the order of the delta-sigma modulator, which can be 1st, 2nd, or 3rd order.

B. DUTY-CYCLE CORRECTOR

The duty-cycle corrector is implemented, as shown in Fig. 8, by modifying an existing the structure [25], and it is located at the output node of the PLL and at the input of each data path. A duty-cycle detector contains a low-pass filter which converts the duty-cycle error information to voltages V_{CLK} and V_{CLKB}. An error amplifier generates output voltages V_P and V_N by the difference between V_{CLK} and V_{CLKB}. This modifies the bias voltages supplied to the duty-cycle adjusters (DCAs), so as to correct the duty-cycle errors. Duty-cycle adjusters are used to compensate for a wide range of duty-cycle errors. If the duty-cycle of the CLK_{OUT} signal is larger than 50%, and the duty-cycle of $CLKB_{OUT}$ signal is less than 50%, the error amplifier in the feedback loop increases V_P and reduces V_N to restore the duty-cycle to 50%.

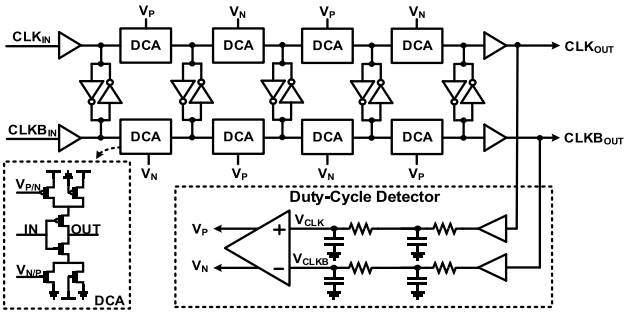

FIGURE 8. Block diagram of the duty-cycle corrector.

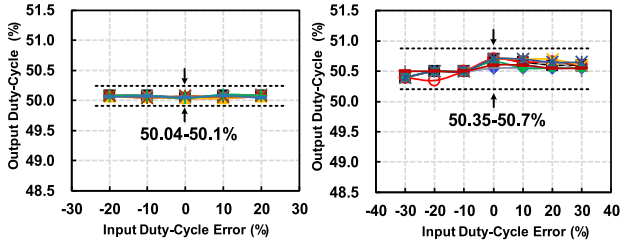

FIGURE 9. Results of a post-layout simulation of duty-cycle correction over 16 channels at (a) 400MHz and (b) 1.6GHz.

Fig. 9 shows the results of a post-layout simulation of this duty-cycle corrector with 16 channels. At 400MHz, the error in the duty-cycle at the output is kept within 0.1% when the duty-cycle of the input clock is varied over ±20% range. At 1.6GHz, the duty-cycle error is corrected to within 0.7% when the variation in the duty-cycle of the input clock signal is ±30%.

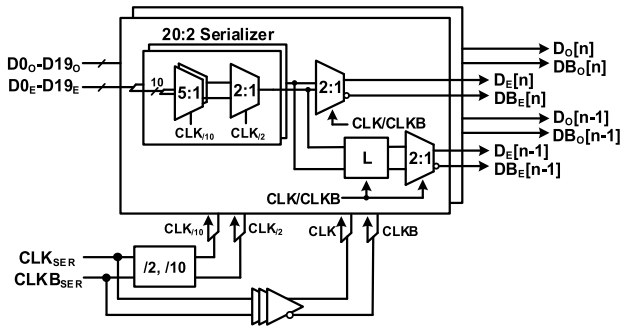

FIGURE 10. Block diagram of a pair of the 20:1 serializers between two adjacent channels.

C. 20:1 SERIALIZERS

Fig. 10 is a block diagram of the pair of 20:1 serializers located between two adjacent channels of the data path. The frequencies of the differential input clock signals CLK_{SER} and $CLKB_{SER}$ are divided by 2 and 10, and these slower clock signals $CLK_{/2}$ and $CLK_{/10}$ and buffered input clock signals CLK and CLKB are distributed to each block in the 20:1 serializer. This consists of a 20:2 serializer, which includes two

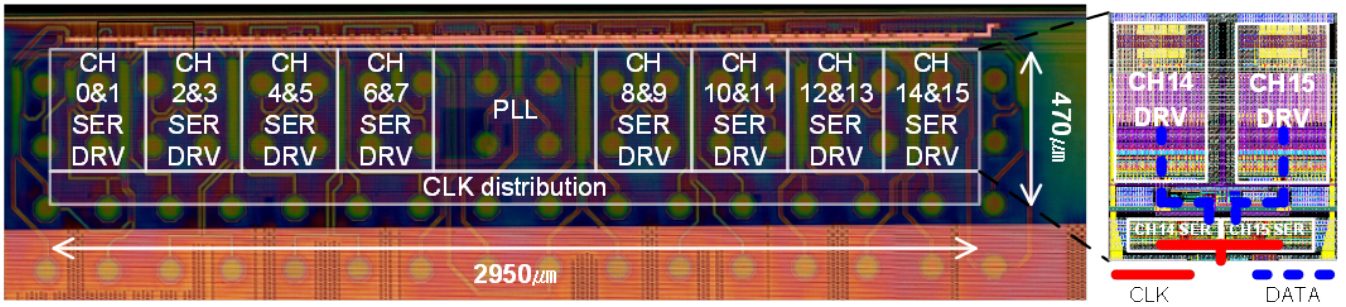

FIGURE 11. Microphotograph of our transmitter for a timing controller, and the layout of the symmetric driver and 20:1 serializer pair which reduce the data skew between adjacent channels.

5:1 serializers and a 2:1 serializer, a latch L, and a final 2:1 serializer which generates full-rate serial data. The latch and a further 2:1 serializer output the data corresponding to the one preceding unit interval (UI) to enable 2-tap FFE in the output driver. The serializers in each pair are symmetrically placed to reduce skewing of the clock and output data signals in adjacent channels, and the clock tree in the serializer is arranged symmetrically for the same reason. This placement also facilitates the delivery of clock signals to both sides of the circuit, and the receivers in the adjacent channels of the source driver can both be sampled with a single recovered clock signal obtained from a clock recovery circuit. This reduces receiver-side power and area requirements.

V. EXPERIMENTAL RESULTS

A prototype chip has been implemented in a 28nm bulk CMOS process, and the back-gate bias of NMOS and PMOS is the ground and supply voltage. Fig. 11 is a microphotograph of our 16-channel transmitter for the timing controller, which has an area of 1.39mm^2. This figure also shows how the symmetric output driver and 20:1 serializer pair are laid out to reduce skewing of the output data between adjacent channels.

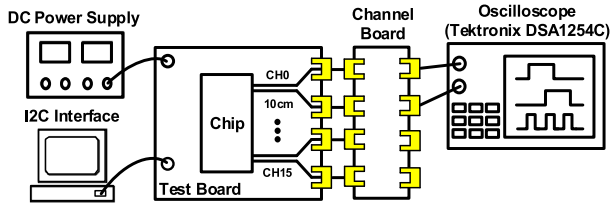

FIGURE 12. Measurement setup using a channel board.

Fig. 12 shows the measurement setup, which consists of a test board and a channel board. The latter can provide a range of environments to replicate the channels of the intra-panel interface. The signals output by the transmitter were displayed on an oscilloscope.

Fig. 13(a) shows the measured lock time of the PLL. Recall that the PLL generates a 1.6GHz output clock signal $CLK_{PLL,OUT}$ from a 20MHz reference clock signal CLK_{REF}. The lock signal $LOCK_{PLL}$ is issued 76.4μs after

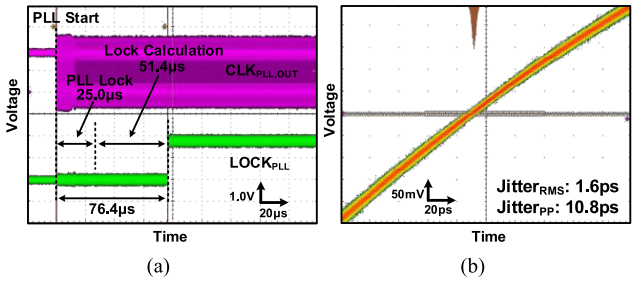

FIGURE 13. Measured (a) lock time of the PLL at 1.6GHz and (b) jitter of the output clock signal divided by 40.

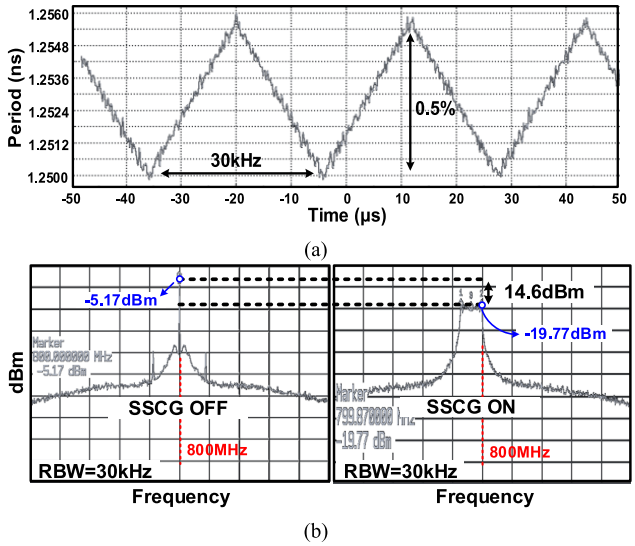

FIGURE 14. Measured (a) SSCG modulation profile and (b) power spectrum, at 800MHz.

the PLL starts; the lock time is 25.0μs, and it is determined that the lock occurred after 1028 cycles of CLK_{REF} on the counter, and it takes 51.4μs. Fig. 13(b) shows the jitter of the output clock signal of the PLL divided by 40. The RMS jitter and peak-to-peak jitter are 1.6ps and 10.8ps respectively.

The performance of the SSCG was assessed by forcing the LVDS driver to output a "0011" data pattern, which corresponds to an 800MHz clock signal. Fig. 14(a) shows

the resulting modulation profile of the SSCG. The triangular waveform produced by modulation appears to be clean, and the modulation ratio and modulation frequency are 0.5% and 30kHz respectively. Fig. 14(b) shows the measured power spectrum at 800MHz with and without the SSCG. When the SSCG is enabled, the measured peak power is reduced from −5.17dBm to −19.77dBm at a resolution bandwidth (RBW) of 30kHz, corresponding to a reduction of 14.6dBm.

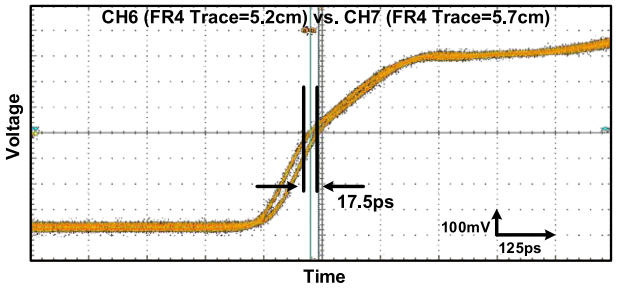

FIGURE 15. Measured adjacent channel skew (CH6 vs. CH7).

Fig. 15 shows measurements of output data skew between adjacent channels CH6 and CH7, when the transmitter is operating at 3.2Gb/s. The lengths of FR4 trace corresponding to CH6 and CH7 on the test board are 5.2cm and 5.7cm respectively. The maximum output skew is 17.5ps, which is 5.6% of a unit interval. The lengths of FR4 trace are different, so this result is acceptable.

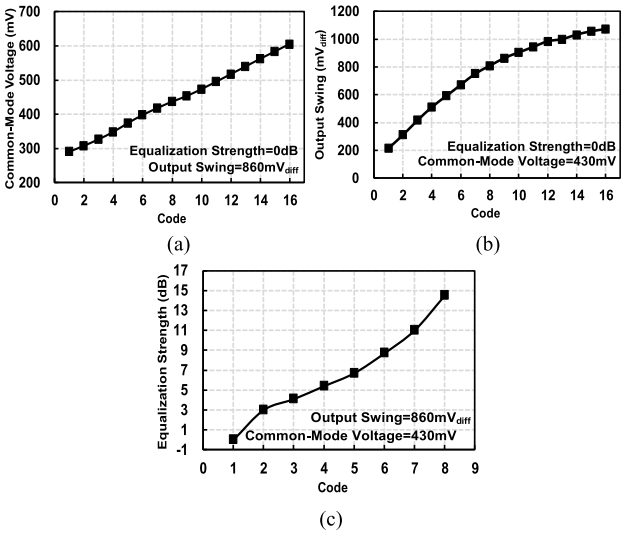

FIGURE 16. Response of the driver to control codes: (a) output common-mode voltage, (b) differential output swing, and (c) equalization strength.

Fig. 16(a) shows the measured common-mode voltage as it is adjusted in 16 nominally equal steps from 291mV to 604mV while keeping the equalization strength and differential output swing constant at 0dB and 860mV$_{diff}$ respectively. Fig. 16(b) shows the measured differential output swing as it is adjusted in 16 steps from 216mV$_{diff}$ to 1072mV$_{diff}$, while keeping the equalization strength and output common-mode voltage at 0dB and 430mV respectively. Fig. 16(c) shows the measured equalization strength, as it is adjusted over 8 steps from 0dB to −14.5dB. Each output characteristic is independently controlled its own control code.

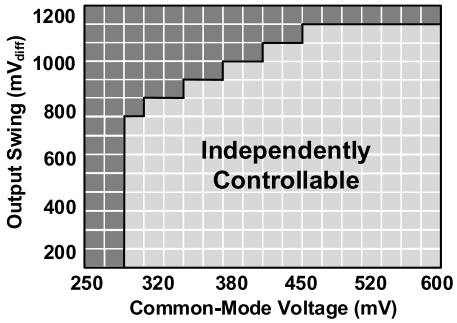

FIGURE 17. Controllability of the output swing and the output common-mode voltage, from a post-layout simulation.

Fig. 17 presents the results of a post-layout simulation which shows the range over which the output swing and the output common-mode voltage can be independently adjusted: When the output swing is above 800mV, the range of achievable common-mode voltages is reduced. This is because it is difficult to obtain a low common-mode voltage when the output swing is large due to the saturation condition in the MOS devices of the LVDS driver.

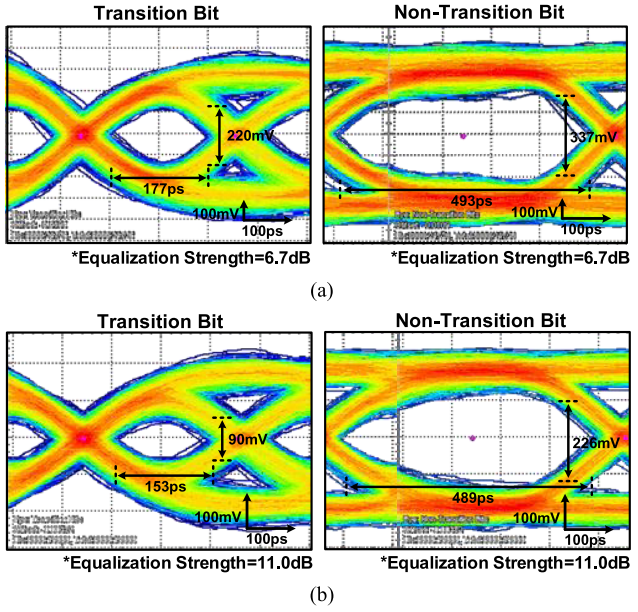

FIGURE 18. Eye diagrams for transition bit and non-transition bit, of a 3.2Gb/s output signal when the FR4 trace on the channel board in (a) 50cm and (b) 100cm.

Fig. 18 shows measured eye diagrams for transition bit and non-transition bit [26], of the output signal with the PRBS10 pattern at 3.2Gb/s. When equalization strength of 6.7dB is applied for a channel with a 50cm FR4 trace, whose insertion loss is −11.04dB at 1.6GHz, the height and the width of the

TABLE 1. Performance summary and comparison with other recent transmitter designs with controllable output characteristics.

	This Work	[10]	[11]	[14]	[16]	[17]
Process	28nm bulk CMOS	28nm bulk CMOS	16nm FinFET	16nm FinFET	65nm bulk CMOS	130nm bulk CMOS
Supply Voltage	1.05V	1.0V	0.9/1.2V	0.9V	1.5/1.1V	N/A
Data-Rate	0.8-3.2Gb/s	2.1Gb/s	0.5-32.75Gb/s	0.5-16.3Gb/s	5-32Gb/s	2.0Gb/s
Number of Channels	16	12	1	4	2	8
Driver Type	LVDS	LVDS	Voltage-Mode	Current-Mode	Voltage-Mode	LVDS
Equalization	2-tap FFE (Controllable)	[a] 3-tap PE 2-tap FFE (Controllable)	3-tap FFE (Controllable)	3-tap FFE (Controllable)	2-tap FFE (Controllable)	No
Independent Controllability of Output Swing (Range)	Yes (216-1072mV$_{diff}$)	Yes (126-1256mV$_{diff}$)	Yes (250-900mV$_{diff}$)	Yes (N/A)	Yes (400-1300mV$_{diff}$)	Yes (200-600mV$_{SE}$)
Independent Controllability of Common-Mode Voltage (Range)	Yes (291-606mV)	Yes (117-686mV)	Yes (N/A)	No (N/A)	No (N/A)	No (N/A)
Power Consumption/Channel	12.7mW @3.2Gb/s	12.7mW @2.1Gb/s	120.8mW @32.75Gb/s	[b] 219mW @16.3Gb/s	87.68mW @32Gb/s	N/A
Energy Efficiency/Channel	3.9pJ/bit @3.2Gb/s	6.05pJ/bit @2.1Gb/s	3.69pJ/bit @32.75Gb/s	[b] 13.44pJ/bit @16.3Gb/s	2.74pJ/bit @32Gb/s	N/A
Active Area/Channel	0.087mm^2	[c] 0.112mm^2	[d] 0.22mm^2	[b] 1.085mm^2	0.173mm^2	N/A

[a] PE: Phase domain equalization [b] Transceiver power and area [c] Includes the area of I/O PAD [d] Without the area of PLL

eye are 220mV and 177ps for the transition bit. For the non-transition bit, the height of the eye is 337mV and its width is 493ps. The height and the width of the eye are 90mV and 153ps for the transition bit when equalization strength of 11.0dB is applied for a channel with a 100cm FR4 trace, whose insertion loss is −17.63dB at 1.6GHz. The height of the eye is 226mV and its width is 489ps, for the non-transition bit.

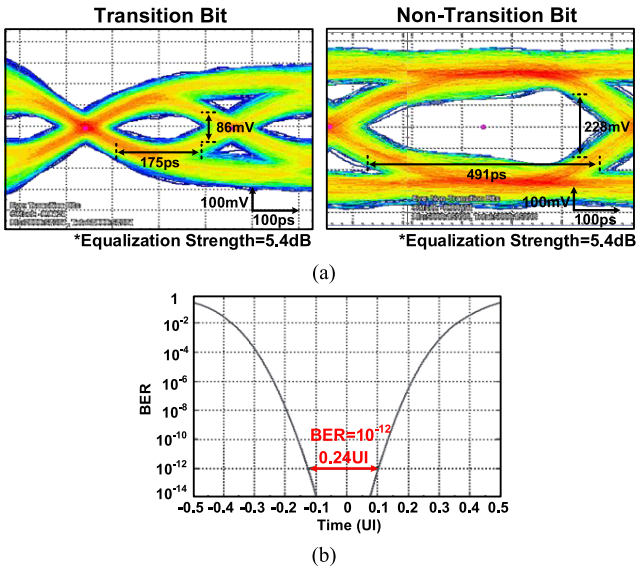

FIGURE 19. (a) Eye diagrams for transition bit and non-transition bit, and (b) bathtub curve, of a 3.2Gb/s output signal passing through a 7cm SMA to FFC board, a 50cm FFC, and the display panel test board.

Fig. 19(a) shows measured eye diagrams for transition bit and non-transition bit, of a PRBS10 pattern at 3.2Gb/s, which is passed through the 7cm SMA-to-FFC conversion board, the 50cm FFC, and the display panel test board. These channel environments mimic the intra-panel interface, and the insertion loss is −15.57dB at 1.6GHz. With equalization strength of 5.4dB, the eye for the transition bit has a height of 86mV and a width of 175ps. For the non-transition bit, the height of the eye is 228mV and its width is 491ps. Fig. 19(b) shows the measured bathtub curve at 3.2Gb/s for this channel. Our transmitter has a bit-error-rate (BER) of 10^{-12} with a timing margin of 0.24UI.

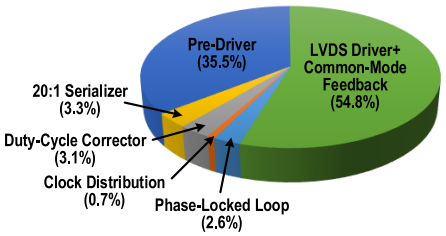

FIGURE 20. Power breakdown per channel in our transmitter at 3.2Gb/s.

Fig. 20 provides a power breakdown per channel for the components in our transmitter. At a data-rate of 3.2Gb/s, most of the power is consumed by the LVDS driver with common-mode feedback, and its power consumption is 9.4mW when the differential output swing is 1050mV$_{diff}$. Compared to the power efficiency of previous LVDS drivers [10], [19]–[21], our LVDS driver has better quantitative efficiency due to the simple common-mode feedback circuit, reduced supply voltage, and improved CMOS process.

In Table 1, the performance of our design is summarized and compared with those of other recent transmitter designs with the controllability of the output characteristics. While independently adjusting the output swing and the output common-mode voltage, our transmitter has more channels and a higher data-rate and achieved a better energy efficiency

than the other transmitters [10], [17] designed to operate in the timing controller of an intra-panel interface. The advantage of our design over the multi-standard transmitters [14], [16], is that it can control both the output swing and the common-mode voltage independently, allowing it to cope with a range of channel characteristics, potentially simplifying the design of the receiver. Compared to the previous transmitter [11] with independent controllability of output characteristics, for use in a field-programmable gate array (FPGA), our design has a wide-range of controllability and can save the area in a multi-channel architecture because it does not need a voltage regulator. The scaled threshold voltage in 28nm bulk CMOS process can extend the bandwidth of the circuit at low supply voltages, reducing the number of buffers required to transmit clock and data signals in a multi-channel design. Therefore, our design can balance the tradeoff between the high-speed and low-power design.

VI. CONCLUSION

We have presented a 16-channel transmitter for use in the timing controller of an intra-panel interface in an ultra-high-definition display. The output common-mode voltage, as well as the output swing and equalization strength are all independently controllable using an LVDS driver with coupled-bias common-mode feedback to cope with the disparate channels to be found in an intra-panel interface. This structure offers potential savings in the area and design complexity of the output driver. A PLL generates differential clock signals over frequencies from 400MHz to 1.6GHz, and a duty-cycle corrector corrects errors in the duty-cycle of the clock signal which are likely to be introduced by the long clock distribution tree. A symmetrical 20:1 serializer reduces the timing skew between adjacent channels.

Implemented in a 28nm bulk CMOS process, our transmitter has been shown to operate successfully from 0.8 to 3.2Gb/s in channel environments replicating those found in an intra-panel interface. The area of the transmitter is 1.39mm^2, and its power consumption is 203.2mW at a supply voltage of 1.05V, operating at 3.2Gb/s operation with the maximum output swing. The output swing, output common-mode voltage, and equalization respectively range from 216 to 1072mV$_{\text{diff}}$, from 291 to 604mV, and from 0 to −14.6dB.

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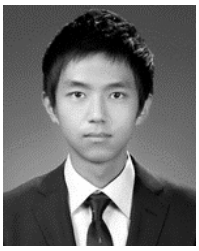

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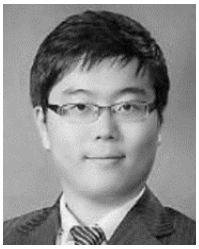

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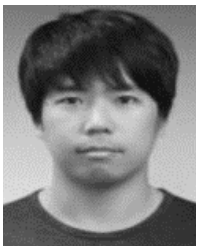

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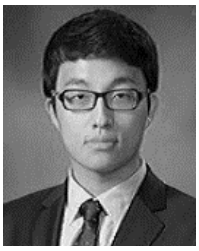

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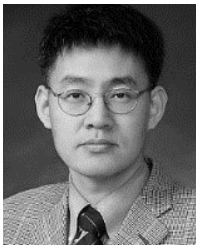

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