IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received November 3, 2018, accepted November 22, 2018, date of publication November 29, 2018,
date of current version December 27, 2018.

Digital Object Identifier 10.1109/ACCESS.2018.2884036

A Compact Passive Equalizer Design for Differential Channels in TSV-Based 3-D ICs

KAI FU[1], WEN-SHENG ZHAO[1,2], (Senior Member, IEEE), DA-WEI WANG[3], GAOFENG WANG[1], (Senior Member, IEEE), MADHAVAN SWAMINATHAN[4], (Fellow, IEEE), AND WEN-YAN YIN[3], (Fellow, IEEE)

[1]Key Lab of RF Circuits and Systems of Ministry of Education, School of Electronics and Information, Hangzhou Dianzi University, Hangzhou 310018, China
[2]State Key Lab of Millimeter Waves, Southeast University, Nanjing 210096, China
[3]Key Lab of Advanced Micro-Nano Electronic Devices and Smart Systems of Zhejiang Province, College of Information Science and Electronic Engineering, Innovative Institute of Electromagnetic Information and Electronic Integration, Zhejiang University, Hangzhou 310018, China
[4]School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332, USA

Corresponding authors: Wen-Sheng Zhao (wsh.zhao@gmail.com) and Gaofeng Wang (gaofeng@hdu.edu.cn)

This work was supported in part by the National Natural Science Foundation of China under Grant 61874038, Grant 61504033, Grant 61411136003, and Grant 61431014, in part by the Talent Project of the Zhejiang Association for Science and Technology under Grant 2017YCGC012, and in part by the Open Research Fund of the State Key Lab of Millimeter Waves, Southeast University, under Grant K201910.

ABSTRACT In this paper, a compact passive equalizer for differential transmission channel is designed in TSV-based three-dimensional integrated circuits (3-D ICs). The compact size of the equalizer is achieved by a square shunt metal line. Three simplified odd-mode half circuit models are proposed for ground-signal-signal-ground (G-S-S-G) type TSVs, differential on-interposer interconnects, and differential channels, respectively. Those simplified models merely consist of frequency-independent elements and can accurately predict the differential insertion losses up to 20 GHz. Moreover, the electrical parameters of the proposed serial resistance-inductance (*RL*) type equalizers are derived from the system transfer functions and optimized by virtue of the time-domain inter-symbol interference cancellation technique. Further, the geometrical parameters of the *RL* equalizers are calculated by using a genetic algorithm based multi-objective optimization method. Finally, the performance of the designed *RL* equalizer is validated by both frequency- and time-domain simulations for 20 Gb/s high-speed differential signaling.

INDEX TERMS Passive equalizer, through-silicon vias (TSVs), on-interposer interconnects, three-dimensional integrated circuits (3-D ICs), peak distortion analysis.

I. INTRODUCTION

Through-silicon via (TSV) based three-dimensional integrated circuits (3-D ICs), which can realize high-density packaging and heterogeneous integration, have attracted intense interests in recent years [1], [2]. TSV interposer is developed to satisfy the system bandwidth requirements in high-speed applications. It can reduce the length of chip-to-chip interconnect and increase the number of input/output (I/O) connections [3]. In particular, the differential on-interposer interconnects can effectively improve channel bandwidth due to its immunity to common-mode noise and good electromagnetic interference performance [4]–[10].

However, as the operating frequency increases, the inherent frequency-dependent loss of the silicon substrate limits the high-speed data transmission and results in degradation of the channel bandwidth [10]. These signal integrity problems lead to the occurrence of inter-symbol interference (ISI) and the degraded quality of eye diagram. More importantly, the ISI of the channels is hardly relieved by differential signaling. Hence, unavoidable bandwidth degradation of the differential channels would be caused as the data rate rises [4].

To date, several types of passive equalizers have been developed to counteract the bandwidth problems as well as overcome the limitations of the active equalizers. In [12], an ohmic contact based passive equalizer was proposed to reduce the ISI of TSV interconnects using an intentional direct current (DC) attenuation method. Based on the body contact effect, an equalizer was developed in [13], and it can alleviate the crosstalk and distortion of TSV interconnects by closing the effective virtual ground plate of TSV

capacitance. However, both of these two equalizers have low adjustability for channel loss compensation due to the limitation of TSV design. A wideband on-interposer equalizer was designed and measured for 30-Gb/s serial data transmission in [3]. It is innovative and valid but has a relatively large size and cannot be applied to the differential channels. A compact on-interposer equalizer for high-speed differential signaling was developed and verified experimentally in [4]. However, the design process is quite time-consuming in practical applications, as the parasitic inductance of equalizer needs to be extracted by 3-D full-wave electromagnetic simulation (e.g., ANSYS Q3D) rather than an analytic method. From the fast design perspective, the equalizer design theories in [14] for single-ended channels and in [15] for differential channels were developed. The design theories of resistance-capacitance (*RC*) type equalizer are based on a simplified circuit model. But the metal-insulator-metal capacitor of such equalizer requires significant process support and is area-consuming [16]. Therefore, a compact passive equalizer with a complete design method for high-speed differential channels is highly desirable.

This paper proposes a systematic design method of a compact passive equalizer for differential channels in TSV-based 3-D ICs. The resistance-inductance (*RL*) type equalizer is chosen since it can be realized by a relatively simple manufacturing process and satisfies the compact size requirement by using the square coil-shaped shunt metal line [17]. The electrical parameters of the *RL* equalizer are primarily deduced by the system transfer function based on a simplified odd-mode half circuit model. And the overcompensation effects for some possible circumstances are eliminated by the time-domain ISI cancellation technique [18]. To meet the real application requirement, the physical structure of proposed *RL* equalizer is designed, and the geometrical parameters are calculated by using a genetic algorithm based multi-objective optimization method. The whole design procedure of the equalizer is based on a set of closed-form equations, with the transfer function obtained by circuit model rather than 3-D full-wave electromagnetic simulation.

The rest of this paper is organized as follow. In Section II, the equivalent circuit models of the differential channels are presented, and the derived simplified odd-model half-circuit models are validated up to 20 GHz by comparing with 3-D full-wave electromagnetic simulator (e.g., ANSYS HFSS). Based on the circuit model, a complete passive equalizer design method, which consists of system transfer function deduction, time-domain ISI cancellation technique, physical structure and geometry parameters establishment, is proposed in section IV. Finally, some conclusions are drawn in Section V.

II. EQUIVALENT CIRCUIT MODEL

The schematic diagram of a differential transmission structure is depicted in Fig. 1, with the definitions and default values of the geometrical parameters listed in Table 1. This structure contains a set of Ground-Signal-Signal-Ground (GSSG) type TSVs and an array of differential on-interposer interconnects. The GSSG type TSVs are buried in the silicon substrate and surrounded by the dielectric layers (usually SiO_2) for DC isolation. The differential on-interposer interconnects are connected with the GSSG type TSVs for differential signaling transmission in horizontal direction. In addition, the inter-metal-dielectric (IMD) layer is caught between the on-interposer interconnects and the silicon substrate for separating them as well as for DC isolation. In this paper, the depletion regions surrounding the TSV dielectric layers are not taken into account as the silicon substrate is assumed as unbiased [1]. The silicon permittivity ε_{Si} $11.9\varepsilon_0$ (where ε_0 is the permittivity of vacuum) and the default value of silicon conductivity σ_{Si} is 10 S/m.

TABLE 1. Structural parameters with their Symbols (Unit: μm).

Symbol	Value	Definition
w_{int}	30	Interconnect width
s	120	Interconnect separation
t_{int}	5	Interconnect thickness
l_{int}	500	Interconnect length
t_{IMD}	9	IMD thickness
h_{sub}	110	Silicon substrate height
d_{TSV}	30	TSV diameter
t_{ox}	0.7	Oxide layer thickness
P	150	Pitch of adjacent TSVs
h_{TSV}	119	TSV height

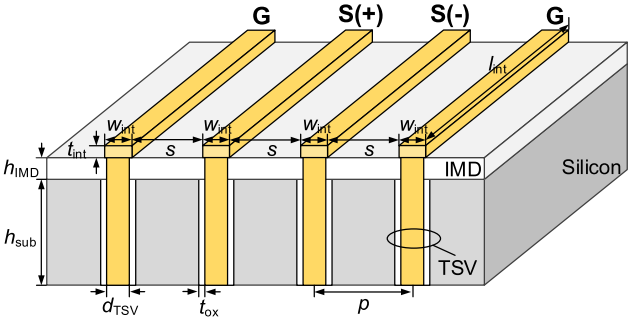


FIGURE 1. Schematic diagram of a differential transmission structure, which consists of GSSG type TSVs and on-interposer interconnects.

The equivalent circuit models for the GSSG type TSVs and the on-interposer interconnects are primarily presented in subsections II-A and II-B, respectively. Then, the simplified odd-mode half circuit models, which merely consist of frequency-independent elements, are developed and verified against the HFSS simulation results. The equivalent circuit model of the whole differential channel is developed by combining the simplified models proposed in subsections II-A and II-B.

A. EQUIVALENT CIRCUIT MODEL OF GSSG TYPE TSVs

Fig. 2(a) shows the equivalent circuit model of the GSSG type TSVs, in which the *RLCG* parameters can be extracted analytically. According to the conductance-frequency chart [19], the wave propagation on GSSG type TSVs is in the

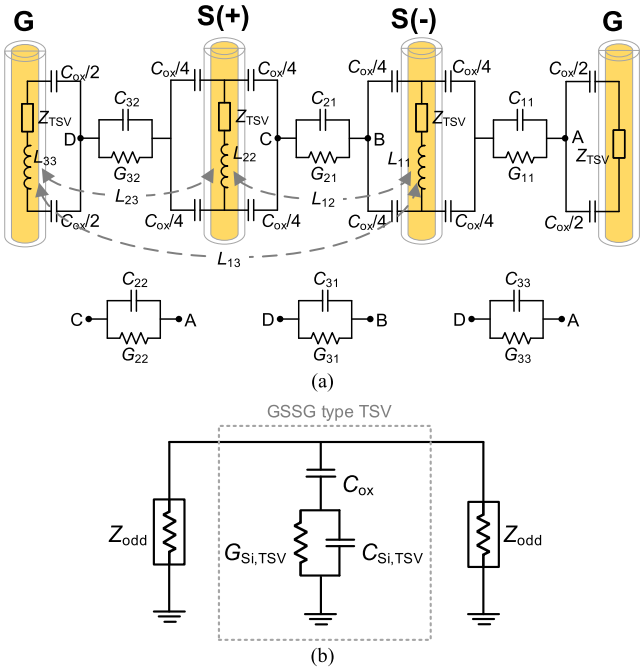


FIGURE 2. (a) Equivalent circuit model and (b) simplified odd-mode half circuit model of GSSG type TSVs.

slow-wave mode and the quasi-TEM dielectric mode. Therefore, the magnetic field of TSVs is not affected by the lossy silicon substrate (i.e., the eddy current effect can be ignored [20]). For an isolated TSV, the internal impedance can be calculated as

$$Z_{TSV} = \frac{h_{TSV}}{\pi d_{TSV}} \frac{I_0(0.5 d_{TSV}\sqrt{j\omega\mu_0\sigma_{Cu}})}{I_1(0.5 d_{TSV}\sqrt{j\omega\mu_0\sigma_{Cu}})} \sqrt{\frac{j\omega\mu_0}{\sigma_{Cu}}} \tag{1}$$

where σ_{Cu} is the conductivity of copper, $I_0(\cdot)$ and $I_1(\cdot)$ are the modified Bessel functions of order zero and one, respectively, and h_{TSV} $(= h_{sub} + h_{IMD})$ is the TSV height.

The external inductance can be extracted using the multiconductor transmission line (MTL) method [21], [22]. Without loss of generality, the leftmost TSV is herein assumed as the reference (#0-TSV), and the other TSVs are presented as #1 to #3-TSV counted from left to right side. The self-loop inductance of #i-TSV can be obtained as [19]

$$L_{ii} = \frac{\mu_0 h_{TSV}}{\pi} \ln\left(\frac{2p_{i0}}{d_{TSV}}\right) \tag{2}$$

The mutual-loop inductance between #i-TSV and #j-TSV can be given by

$$L_{ij} = \frac{\mu_0 h_{TSV}}{2\pi} \ln\left(\frac{2p_{i0}p_{j0}}{p_{ij}d_{TSV}}\right) \tag{3}$$

where p_{i0} ($i = 1$, 2, and 3) represents the pitch between #i-TSV and #0-TSV, and p_{ij} ($i, j = 1$, 2, and 3, and $i \neq j$) is the pitch between #i-TSV and #j-TSV.

The oxide capacitance C_{ox} of TSVs can be calculated as [23]:

$$C_{ox} = \frac{2\pi h_{sub}\varepsilon_{ox}}{\ln\left(d_{ox}/d_{TSV}\right)} \tag{4}$$

where ε_{ox} $(= 3.9\varepsilon_0)$ is the permittivity of the SiO_2 layer and d_{ox} $(= d_{TSV} + 2t_{ox})$ is the outer diameter of SiO_2 layers. It is worth noting that the height used here is h_{sub} rather than h_{TSV}, because only a part of TSV (with a height of h_{sub}) is surrounded by the dielectric layer (see Fig. 1).

The silicon capacitance and conductance between the outer edges of the SiO_2 layers can be calculated by using the same method as the calculation of the capacitance matrix of ribbon cables [19], [24]. By replacing d_{TSV} with d_{ox} in (2) and (3), another inductance matrix $[\boldsymbol{L_{Si}}]$ is introduced to deduce the silicon capacitance matrix $[\boldsymbol{C_{Si}}]$ and the conductance matrix $[\boldsymbol{G_{Si}}]$ as follows:

$$[\boldsymbol{C}_{Si}] = \mu_0\varepsilon_{Si}h_{TSV}^2[\boldsymbol{L}_{Si}]^{-1} = \begin{bmatrix} \sum_{j=1}^{3} C_{1j} & -C_{12} & -C_{13} \\ -C_{21} & \sum_{j=1}^{3} C_{2j} & -C_{23} \\ -C_{31} & -C_{32} & \sum_{j=1}^{3} C_{3j} \end{bmatrix} \tag{5}$$

$$[\boldsymbol{G}_{Si}] = \frac{\sigma_{Si}}{\varepsilon_{Si}}[\boldsymbol{C}_{Si}]^{-1} \tag{6}$$

Furthermore, an odd-mode half circuit model of the GSSG type TSVs is derived from the circuit model in Fig. 2(a) by inserting a perfect electric conductor plane at the symmetric plane of the differential TSV pair [24]–[26]. Using the same method proposed in [14] and [15], the simplified odd-mode half circuit model of the GSSG type TSVs, which merely consists of three frequency independent elements, is realized as shown in Fig. 2(b). Herein, the characteristic impedance Z_{odd} equals to 50 Ω. The simplified silicon capacitance $C_{Si,TSV}$ and silicon conductance $G_{Si,TSV}$ are formed by the shunt of silicon admittances:

$$C_{Si,TSV} = C_{20} + C_{32} + 2C_{21} \tag{7}$$

$$G_{Si,TSV} = G_{20} + G_{32} + 2G_{21} \tag{8}$$

Fig. 3 shows the differential insertion loss obtained by the simplified model and the HFSS simulation with various geometric parameters: oxide thickness t_{ox}, TSV diameter d_{TSV}, silicon conductivity σ_{Si}, and TSV height h_{TSV}. It is evident that these results agree well with each other, implying the proposed simplified circuit model can accurately predict the transmission coefficients of GSSG type TSVs up to 20 GHz. Moreover, there are three factors that have major impacts on the differential insertion loss.

1) Oxide capacitance C_{ox}: it can be observed in Fig. 3(a) that the differential insertion loss reduces as the t_{ox}

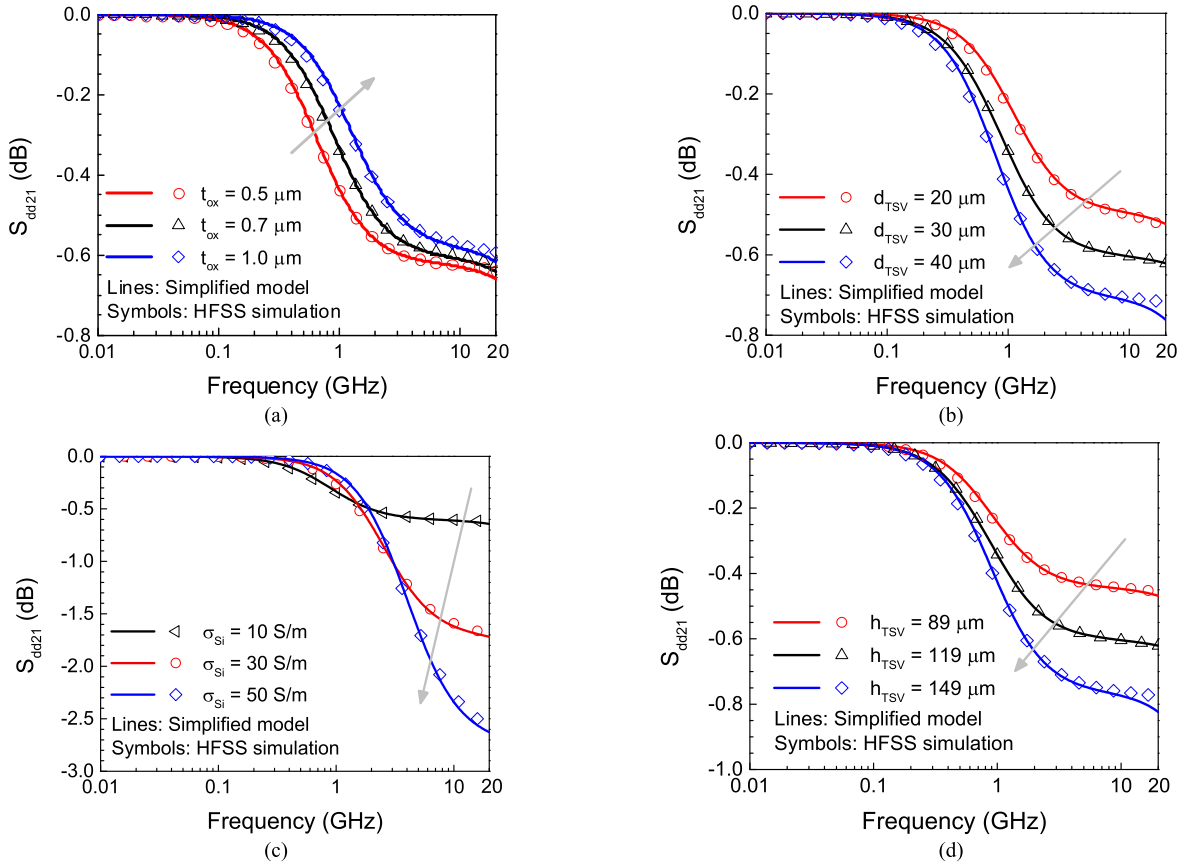


FIGURE 3. Differential insertion losses of the GSSG type TSVs with different (a) t_{ox}, (b) d_{TSV}, (c) σ_{Si}, and (d) h_{TSV}.

increases. That is caused by a smaller C_{ox} that shows an inverse correlation with t_{ox} according to (4).

2) Silicon capacitance C_{Si}: with a constant p of adjacent TSVs, the separation between the outer edges of any two TSVs decreases with the enlarging d_{TSV}, thereby leading to a larger C_{Si} and an increased differential insertion loss, as shown in Fig. 3(b).
3) Silicon conductance G_{Si}: it is evident that a larger G_{Si}, which is directly proportional to σ_{Si}, can cause more differential insertion loss as shown in Fig. 3(c).

Moreover, the increased h_{TSV} can augment all three factors mentioned above thereby leading to an increased differential insertion loss as shown in Fig. 3(d). The differential insertion loss has a negative correlation with t_{ox} whereas keeps positive correlations with d_{TSV}, σ_{Si}, and h_{TSV}.

B. EQUIVALENT CIRCUIT MODEL OF ON-INTERPOSER INTERCONNECTS

In the previous study [8], an equivalent circuit model of differential on-interposer interconnects has been established, with the impedance extracted using partial element equivalent circuit (PEEC) method. And the proposed model was verified against the HFSS simulation up to 100 GHz. Fig. 4(a) shows the equivalent circuit model of the differential on-interposer interconnects, where the inductance and AC resistance are omitted for simplicity. In the figure, R_{int} represents the DC resistance of the on-interposer interconnects, which can be calculated as

$$R_{int} = \rho_{int}\frac{l_{int}}{A_{int}} = \rho_{int}\frac{l_{int}}{w_{int}\cdot t_{int}} \tag{9}$$

where ρ_{int} is the resistivity of the conductor. The coupling capacitances in odd-mode and even-mode (C_{odd} and C_{even}) can be extracted by the conformal mapping technique [26]. Then, the signal-signal and signal-ground coupling capacitances can be calculated using the Veyers-Fouad Hanna approximation [8],

$$C_{ss} = \frac{(C_{odd} - C_{even})}{2} \tag{10}$$

$$C_{sg} = C_{even} \tag{11}$$

As described earlier, an IMD layer needs to be fabricated between interconnects and silicon substrate. The corresponding IMD capacitance C_{IMD} can be calculated based on conformal mapping technique [27],

$$C_{IMD} = \varepsilon_{ox} l_{int}\left[\frac{w_{int}}{t_{IMD}} + \frac{K(k)}{K(k')}\right] \tag{12}$$

where $K(\cdot)$ is the complete elliptic integral of the first kind, and the coefficients k and k' can be expressed as

$$k = \sqrt{1 - \left(1 + \frac{t_{\text{int}}}{t_{\text{IMD}}}\right)^{-2}} \tag{13}$$

$$k' = \sqrt{1 - k^2} \tag{14}$$

The silicon capacitance C_{Si} and the conductance G_{Si} between the interconnects and the silicon substrate can be calculated as [28]

$$C_{\text{Si}} = \varepsilon_{\text{Si,eff}} l_{\text{int}} \frac{w_{\text{int}}}{h_{\text{eff}}} \tag{15}$$

$$G_{\text{Si}} = \frac{\sigma_{\text{Si,eff}}}{\varepsilon_{\text{Si,eff}}} C_{\text{Si}} \tag{16}$$

where the effective permittivity $\varepsilon_{\text{Si,eff}}$, the effective conductivity $\sigma_{\text{Si,eff}}$, and the effective thickness h_{eff} are obtained by

$$\varepsilon_{\text{Si,eff}} = \frac{\varepsilon_{\text{Si}} + \varepsilon_0}{2} + \frac{\varepsilon_{\text{Si}} - \varepsilon_0}{2\sqrt{1 + 10\frac{h_{\text{TSV}}}{w_{\text{int}}}}} \tag{17}$$

$$\sigma_{\text{Si,eff}} = \frac{1}{2} + \frac{1}{2\sqrt{1 + 10\frac{h_{\text{TSV}}}{w_{\text{int}}}}} \tag{18}$$

$$h_{\text{eff}} = \frac{w_{\text{int}}}{2\pi} \ln\left(8\frac{h_{\text{TSV}}}{w_{\text{int}}} + \frac{w_{\text{int}}}{4h_{\text{TSV}}}\right) \tag{19}$$

Generally speaking, in comparison with the admittance, the impedance of on-chip interconnects has less impact on the performance at relatively low frequencies, and can be neglected [14], [15]. Therefore, a simplified odd-mode half circuit model of on-interposer differential interconnects can be obtained by replacing an equipotential surface with a ground plane, as shown in Fig. 4(b). Herein, the total coupling capacitance C_c equals to

$$C_{\text{c}} = 2C_{\text{ss}} + C_{\text{sg}} \tag{20}$$

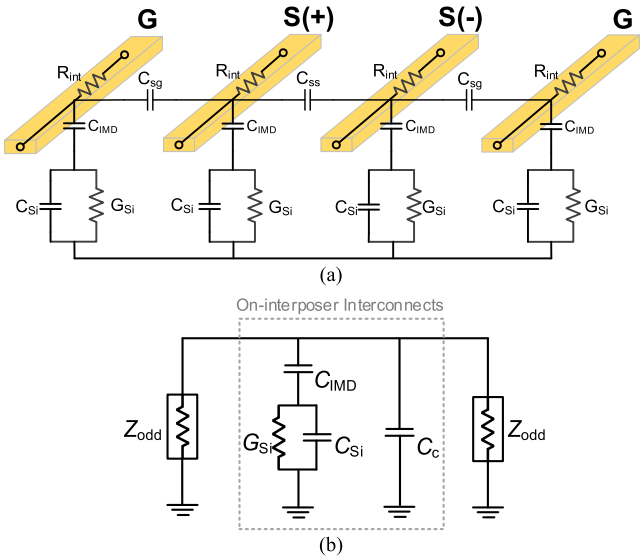


FIGURE 4. (a) Equivalent circuit model and (b) odd-mode half circuit model of differential on-interposer interconnects.

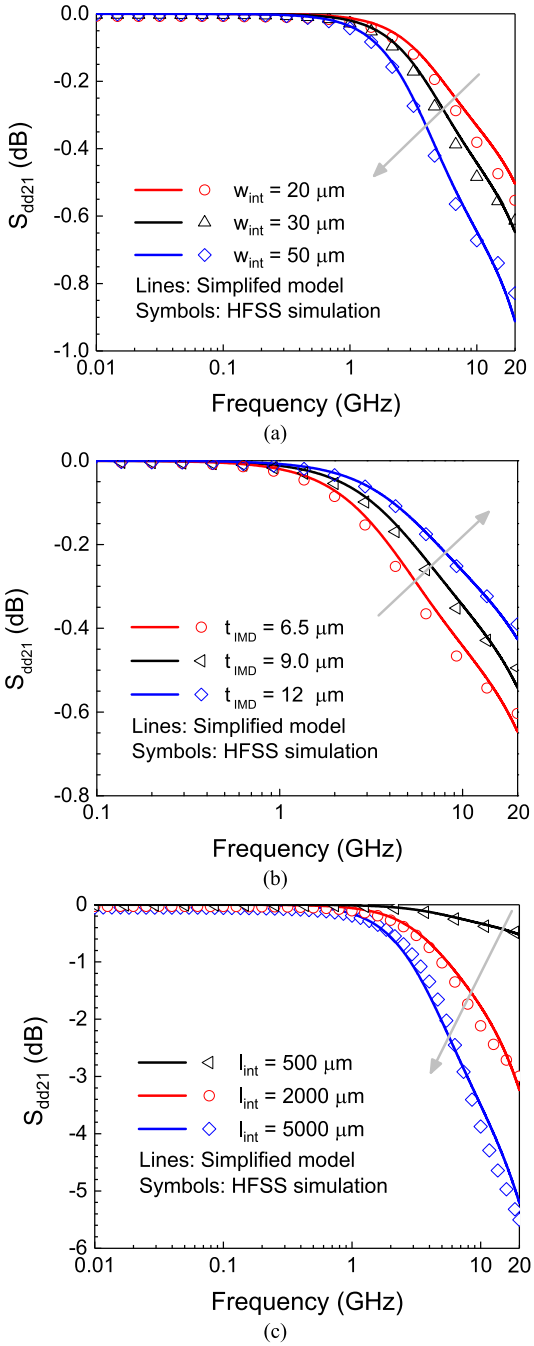


FIGURE 5. The differential insertion loss of on-interposer interconnects with different (a) w_{int}, (b) t_{IMD}, and (c) l_{int}.

Fig. 5 shows the differential insertion loss of differential on-interposer interconnects obtained by the simplified model and the HFSS simulation. Good agreements can be observed between these results, and some observations can be drawn as follows:

1) With increasing w_{int}, the coupling capacitance C_c increases on account of the decreasing separation between each two interconnects, whereas C_{IMD} increases due to augmentation of the metal plate areas

according to (12). Therefore, the differential insertion loss increases as shown in Fig. 5(a).

2) Fig. 5(b) shows that the differential insertion loss decreases with the increased t_{IMD}. This is mainly caused by the reduction of C_{IMD} according (10).
3) It can be observed from Fig. 5(b) that the differential insertion loss increases on account of the augmentation of all *CG* parameters which are proportional to l_{int}.

C. EQUIVALENT CIRCUIT MODEL OF WHOLE DIFFERENTIAL STRUCTURE

The simplified odd-mode circuit model of an integrated differential transmission structure can be obtained by combining the circuit models of GSSG type TSVs and differential on-interposer interconnects, as shown in Fig. 6. The coupling between TSVs and on-interposer interconnects is neglected. The parameters of each electrical component can be exacted as explained in the preceding subsections.

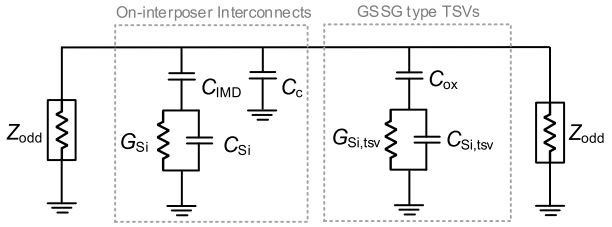


FIGURE 6. Simplified odd-mode half circuit model of the differential transmission structure which consists of GSSG type TSVs and On-interposer interconnects.

Fig. 7 shows the differential insertion loss of the whole structure with various interconnect width w_{int}, height of the silicon substrate h_{sub}, interconnects length l_{int}, and silicon conductivity σ_{Si}. It is evident that the differential insertion loss exacted from the simplified model agrees well with that of the HFSS simulation up to 20 GHz. Some observations can be drawn as follows:

1) With an augmented w_{int} (as well as d_{TSV}), the differential insertion loss increases as shown in Fig. 7(a). This is because a stronger coupling is caused by the narrower separation between each two channels. In other words, the increased $G_{Si,TSV}$, $C_{Si,TSV}$ and C_c (according to (5), (6), and (20)) cause this phenomenon.
2) Fig. 7(b) illustrates that the differential insertion loss increases with a larger h_{sub}. This is because stronger current leakage is caused by the increases of C_{ox}, $C_{Si,TSV}$ and $G_{Si,TSV}$, due to larger TSV height h_{TSV}.
3) Fig. 7(c) reveals that the differential insertion loss increases as l_{int} augments. This is mainly caused by the increases of C_{IMD}, C_{Si}, and G_{Si}, which are in direct proportion to l_{int}.
4) With augmented σ_{Si}, the differential insertion loss increases, as shown in Fig. 7(d). This is because stronger current leakage is caused by the augmentation of $G_{Si,TSV}$ and G_{Si}, which are in direct proportion to σ_{Si} according to (6) and (16).

In summary, the proposed simplified models can accurately predict the differential insertion loss of three types of differential transmission channel up to 20 GHz. As the circuit components of simplified models are frequency-independent, the related system transfer functions are straightforward and thus have a significant benefit for the design of passive equalizers, which will be as discussed in Section III.

III. DESIGN METHOD OF PASSIVE EQUALIZER

A design method of passive equalizer will be carried out in this section based on the inherent transmission property of differential channels in 3-D ICs. The passive equalizer acts as a high-pass filter to render the overall response as flat as possible, thereby mitigating the ISI and enhancing the quality of eye diagram [14], [17]. The *RL* type equalizer is herein chosen since it can be realized by a square coil-shaped shunt metal line [17]. The *RL* parameters of the equalizer are obtained based on the system transfer function and optimized by using the time-domain ISI cancellation technique [18]. In the view of the real-world applications of 3-D ICs, the physical structure of the *RL* equalizer for the whole differential transmission structure is designed using a genetic algorithm based multi-objective optimization method.

A. PASSIVE EQUALIZER FOR GSSG TYPE TSVs

Fig. 8 illustrates the odd-model half circuit model of the GSSG type TSVs with a serial *RL* equalizer, and the corresponding system transfer function can be expressed as

$$\begin{aligned} H_{TSV}(s) &\approx 2\frac{V_{out}}{V_{in}} \\ &= \frac{2}{2+Z_{odd}\left[\frac{sC_{ox}(G_{Si,TSV}+sC_{Si,TSV})}{G_{Si,TSV}+s(C_{Si,TSV}+C_{ox})}+\frac{1}{R_{eq}+sL_{eq}}\right]} \\ &= \frac{2}{2+Z_{odd}\left(\frac{a_1}{b_1}\right)} \end{aligned} \tag{21}$$

where s denotes the complex frequency, and a_1 and b_1 are two polynomial functions of s that can be expressed as

$$\begin{aligned} a_1 = {} & s^3 C_{Si,TSV}C_{ox} + s^2\left(\frac{C_{ox}C_{Si,TSV}R_{eq}}{L_{eq}} + C_{ox}G_{Si,TSV}\right) \\ & + \frac{s\left(C_{Si,TSV}+C_{ox}+C_{ox}R_{eq}G_{Si,TSV}\right)}{L_{eq}} + \frac{G_{Si,TSV}}{L_{eq}} \end{aligned} \tag{22}$$

$$\begin{aligned} b_1 = {} & s^2\left(C_{Si,TSV}+C_{ox}\right) + s\left(R_{eq}\frac{C_{Si,TSV}+C_{ox}}{L_{eq}} + G_{Si,TSV}\right) \\ & + \frac{R_{eq}G_{Si,TSV}}{L_{eq}} \end{aligned} \tag{23}$$

It is worth noting that the cubic-term of a_1 could be neglected, as the cubic-term coefficient (i.e., $C_{Si}C_{ox}$) is nearly 14 orders of magnitude smaller than that of the quadratic-term (i.e., $C_{ox}G_{Si} + C_{ox}C_{Si}R_{eq}/L_{eq}$). Therefore, the polynomial terms with s in (21) can be eliminated when

$$\frac{a_1}{b_1} = \frac{1}{R_{eq}} \tag{24}$$

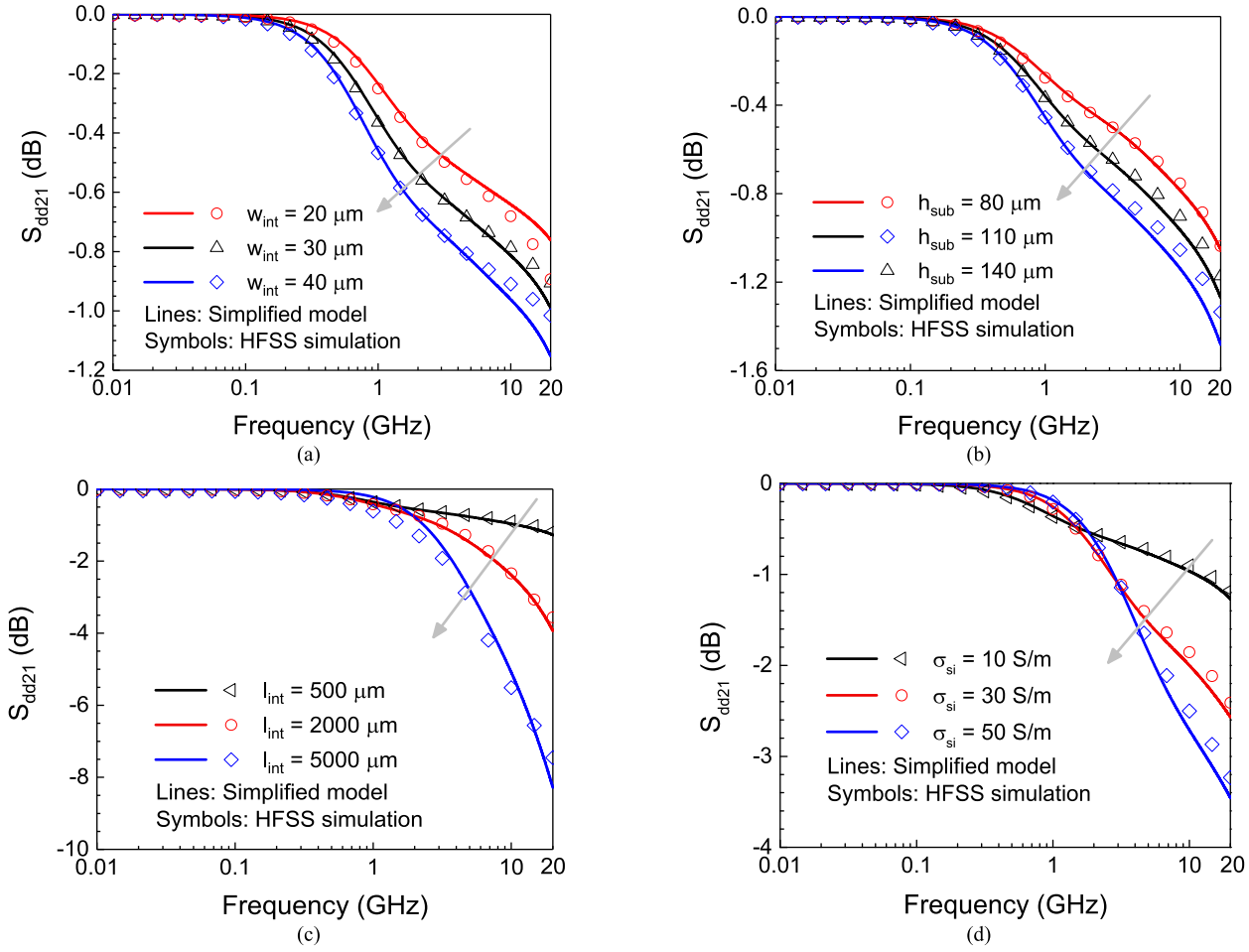


FIGURE 7. Differential insertion loss of the transmission structure with different (a) w_{int}, (b) h_{sub}, (c) l_{int}, and (d) σ_{Si}.

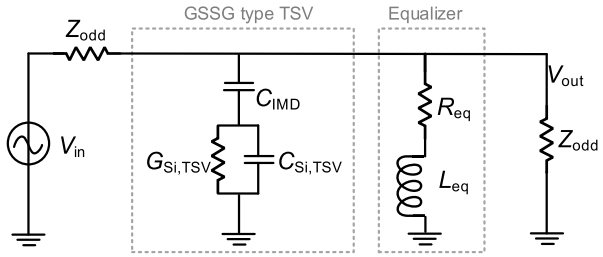


FIGURE 8. Odd-mode half circuit of equalized GSSG type TSVs.

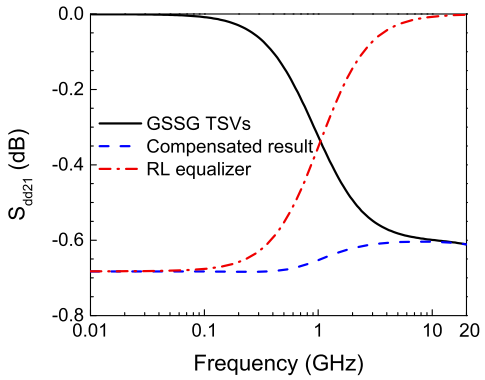


FIGURE 9. Simulated differential insertion loss of original and compensated GSSG type TSVs with geometrical parameters listed in TABLE 1.

In other words, the correlation between the system transfer function and the complex frequency is nearly non-significant when the *RL* parameters of the equalizer are set as

$$R_{eq} = 1/G_{Si} \tag{25}$$

$$L_{eq} = C_{ox}R_{eq}^2 \tag{26}$$

Fig. 9 shows the simulated differential insertion loss of the GSSG type TSVs with configuration parameters listed in Table 1. The *RL* equalizer acts as a high-pass filter and compensates the loss effect of GSSG type TSVs. The compensated S_{dd21} is flat in the frequency region from DC to 1 GHz but has a small discrepancy from the ideally flat response. That is because the *RL* equalizer parameters are derived based on the simplified circuit model and also the cubic-term of the system transfer function in (21) is

neglected. When the frequency rises up to 1 GHz, the cubic-term of a_1 is nearly the same order of magnitude as the quadratic-term. Despite the imperfection of the *RL* equalizer, the eye-diagram which signifies the transmission quality of high-speed digital signal still has an improvement.

The transient simulations are performed in advanced design system (ADS) to obtain the eye diagram. The input signal source is a time-domain pseudo-random bit sequence (PRBS) of $2^8 - 1$, with a 20 Gb/s data rate, 20 ps rising/fall edge, 10 ns simulation time length, 0.01 ps step, and the voltage swing from −1 V to 1 V. Fig. 10 shows the eye diagram of the signal through the GSSG type TSVs with and without the *RL* equalizer. It can be seen that the eye-opening improves from 1.773 V to 1.850 V and the eye-width improves from 49 ps to 50 ps. Moreover, the peak to peak timing jitter (Jitter PP) is reduced from 1 ps to 0.05 ps.

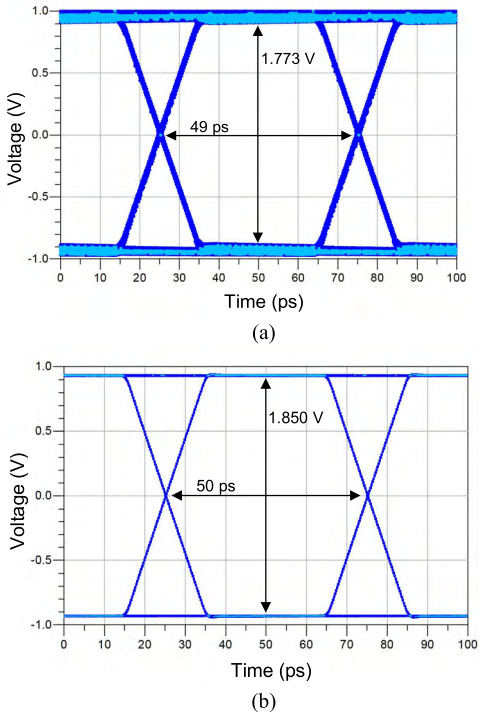


FIGURE 10. Comparisons of eye diagram of signal through GSSG type TSVs presented in TABLE 1 (a) without and (b) with equalizer.

The improvement is relatively slight because the TSV itself with the geometry parameters in Table 1 is a low-loss transmission channel, as shown in Fig. 9, and the eye diagram of the TSV channel without the *RL* equalizer has a relatively high quality in Fig. 10(a). However, there are generally several numbers of stacked dies in the real-world 3-D ICs system applications. As the number of stacked dies increases, the loss effects of the GSSG type TSVs become significant and the eye diagrams appear inferior in quality.

Fig. 11 shows the simulated differential insertion loss of ten-stacked GSSG type TSVs. In the simulation, the full circuit model in Fig. 2(a) is cascaded ten times and connected with the corresponding *RL* equalizer designed

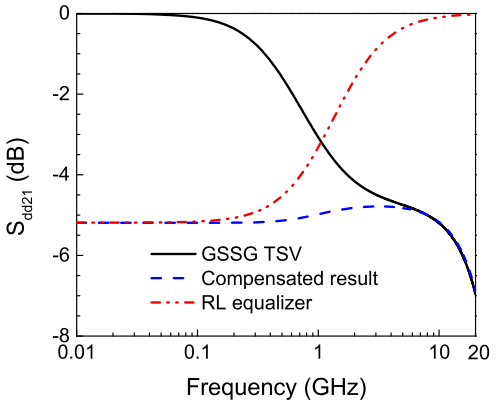


FIGURE 11. Simulated differential insertion loss of original and compensated ten-staked GSSG type TSVs.

by (25) and (26). It is evident that there is a relatively significant loss effect when the frequency increases. The compensated S_{dd21} is nearly flat in the frequency region from DC to 5 GHz and has the same tendency as that of the original GSSG type TSVs beyond 5 GHz.

An inevitable DC attenuation that reduces the signal voltage swing is caused by the *RL* equalizer as shown in Fig. 9 and Fig. 11. The DC drop augments as the number of stacked dies increases, and can be found from the low-frequency limit of the differential insertion loss [14]

$$|S_{dd21}|_{DC} = \frac{2}{2 + N \cdot G_{Si,TSV} Z_{odd}} \tag{27}$$

where N is the number of stacked dies. Taking the ten-stacked GSSG type TSVs as an example, the calculated DC S_{dd21} equals to −5.189 dB, which is matched well with Fig. 11.

Fig. 12 depicts the eye diagrams of the signal through the ten-stacked GSSG type TSVs with and without the *RL* equalizer. There is a huge improvement of the eye-opening and eye-width when the *RL* equalizer is applied. It is evident that the eye-opening has a 74.6% improvement from 0.634 V to 1.107 V and the eye-width has a 33.1% improvement from 37 ps to 49.25 ps. In addition, the Jitter PP is reduced from 14 ps to 0.75 ps. Therefore, the proposed *RL* equalizer is effective especially for a multi-stacked GSSG type TSVs transmission channel.

B. PASSIVE EQUALIZER FOR ON-INTERPOSER INTERCONNECTS

Fig. 13 illustrates the odd-model half circuit model of differential on-interposer interconnects with a serial *RL* equalizer, and the corresponding system transfer function can be expressed as

$$\begin{aligned} H_{int}(s) &\approx 2\frac{V_{out}}{V_{in}} \\ &= \frac{2}{2 + Z_{odd}\left[\frac{sC_{IMD}(G_{Si}+sC_{Si})}{G_{Si}+s(C_{Si}+C_{IMD})} + sC_c + \frac{1}{R_{eq}+sL_{eq}}\right]} \\ &= \frac{2}{2 + Z_{odd}\left(\frac{a_2}{b_2}\right)} \end{aligned} \tag{28}$$

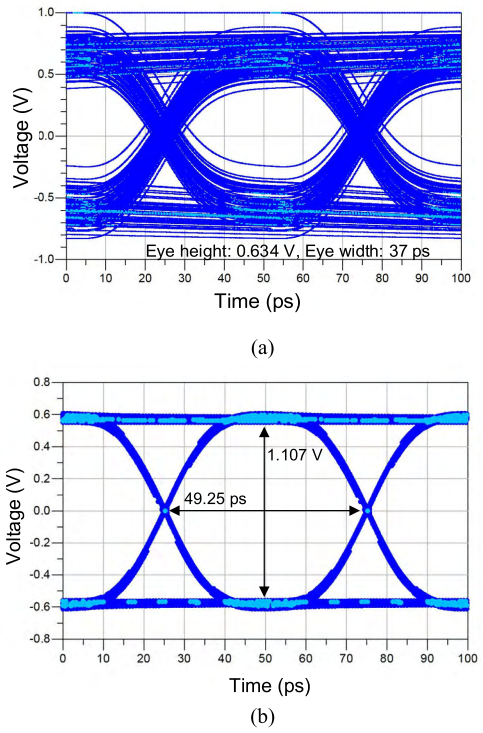


FIGURE 12. Comparisons of eye diagram of signal through ten-staked GSSG type TSVs (a) without and (b) with equalizer.

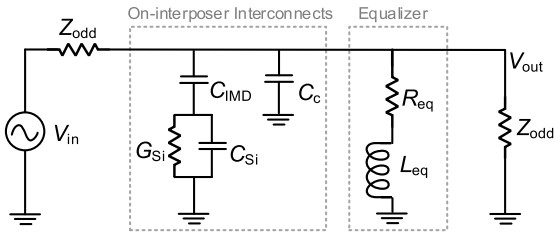


FIGURE 13. Odd-mode half circuit of equalized differential on-interposer interconnects.

where the polynomial functions a_2 and b_2 are given as

$$a_2 = s^3 \left[C_{\rm Si}C_{\rm ox} + C_{\rm c}\left(C_{\rm Si} + C_{\rm ox}\right)\right] + s^2\left\{C_{\rm ox}\left(C_{\rm Si}\frac{R_{\rm eq}}{L_{\rm eq}} + G_{\rm Si}\right) + C_{\rm c}\left[\left(C_{\rm Si} + C_{\rm ox}\right)\frac{R_{\rm eq}}{L_{\rm eq}} + G_{\rm Si}\right]\right\} + \frac{s\left(C_{\rm Si} + C_{\rm ox} + \left(C_{\rm ox} + C_{\rm c}\right)R_{\rm eq}G_{\rm Si}\right)}{L_{\rm eq}} + \frac{G_{\rm Si}}{L_{\rm eq}} \quad (29)$$

$$b_2 = s^2\left(C_{\rm Si} + C_{\rm ox}\right) + s\left(R_{\rm eq}\frac{C_{\rm Si} + C_{\rm ox}}{L_{\rm eq}} + G_{\rm Si}\right) + \frac{R_{\rm eq}G_{\rm Si}}{L_{\rm eq}} \quad (30)$$

By using the same frequency domain-based method discussed in the preceding subsection, the *RL* parameters of the passive equalizer can be obtained as

$$R_{\rm eq} = \frac{C_{\rm IMD}^2}{G_{\rm Si}\left(C_{\rm IMD} + C_{\rm c}\right)^2} \quad (31)$$

$$L_{\rm eq} = \left(C_{\rm ox} + C_{\rm c}\right)R_{\rm eq}^2 \quad (32)$$

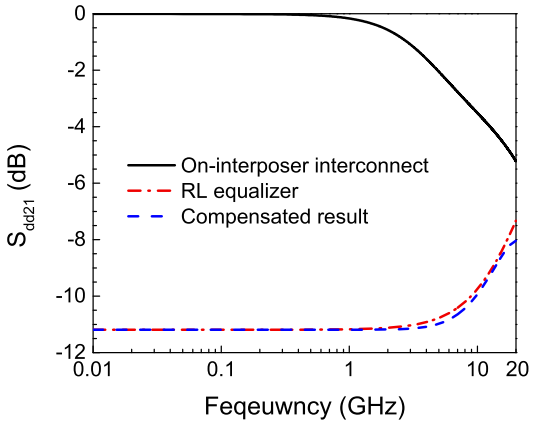


FIGURE 14. Overcompensation phenomenon of simulated differential insertion loss of differential on-interposer interconnects with equalizer (31) and (32).

The on-interposer interconnects with 5 mm length and other parameters listed in Table 1 are herein used in the design example. Fig. 14 shows the simulated differential insertion loss of the differential on-interposer interconnects. In the simulation, the full circuit model in Fig. 3(a) is connected with the corresponding *RL* equalizer specified by (31) and (32) in parallel. It can be found that the compensated $S_{\rm dd21}$ is nearly flat in the frequency region from DC to 5 GHz, but a severe overcompensation phenomenon appears. As shown in Fig. 14, the overcompensation causes an excessive DC attenuation in the transmission channel and damages the quality of the differential transmission signal, thereby leading to a worse eye diagram.

Fig. 15 shows eye diagrams of the signal passing through the differential on-interposer interconnects with and without the *RL* equalizer. The deterioration of eye diagram is significant: the eye-opening declines from 1.155 V to 0.508 V although the eye-width increases from 47.25 ps to 50 ps. The reason of this phenomena is that the on-interposer interconnect is a relative low-loss transmission channel and the DC drop with *RL* equalizer is determined by [14]

$$|S_{\rm dd21}|_{\rm DC} = \frac{2}{2 + G_{\rm Si}Z_{\rm odd}} \quad (33)$$

With a relatively low value of $G_{\rm Si}$, the calculated DC $S_{\rm dd21}$ (i.e., −11.20 dB) is far less than the that of original on-interposer interconnects at 20 GHz (i.e., −5.22 dB), as shown in Fig. 14.

In order to settle the matter of overcompensation, the proposed *RL* equalizer is improved by using the optimization method based on the time-domain ISI cancellation technique proposed in [18]. ISI, a form of a signal distortion, is the interference between digital signals where the current bit distorts the subsequent and pervious bits. It can be extracted using the peak distortion analysis (PDA), which is based on the single pulse response of transmission channel [32].

For the differential on-interposer interconnects, the time-domain single-bit response $y(t)$ can be obtained by the

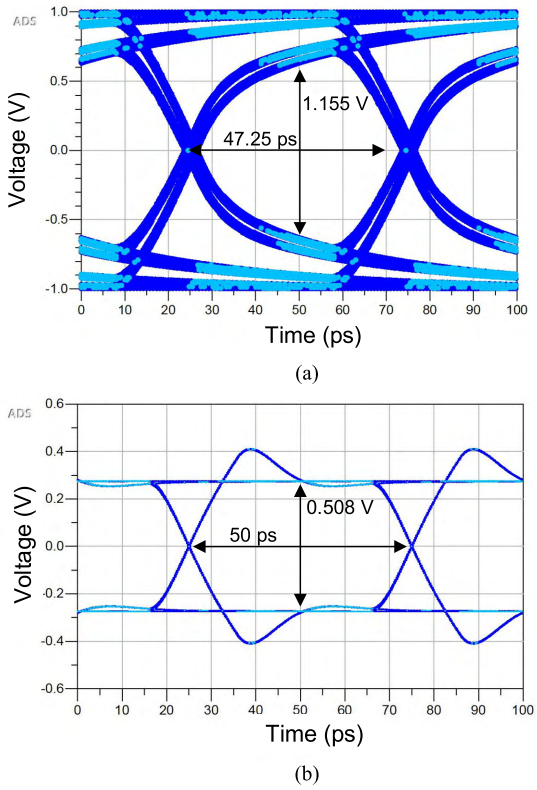


FIGURE 15. Eye diagram of signal through differential on-interposer interconnects (a) without and (b) with equalizer (31) & (32).

electrical circuit models in Fig. 4 and Fig. 13. Herein, the transient simulation is employed with a 20 Gb/s impulse voltage source whose amplitude is from 0 V to 1 V with both the rising and falling times of 20 ps. The corresponding output single-bit response can be obtained by

$$Y(\omega) = H_{\text{int}}(\omega) P(\omega) \tag{34}$$

where ω is the angular frequency, $P(\omega)$ is the frequency-domain response of the impulse voltage source, and $H_{\text{int}}(\omega)$ can be calculated by (28).

Assuming that $y(t)$ has the maximum at $t = 0$, the positive and negative ISIs can be calculated using the following equation [18]:

$$\text{ISI}_+ = \sum_{\substack{k=n_{\text{pre}} \\ k\neq 0}}^{n_{\text{post}}} y(t-kT)\,|_{y(t-kT)>0} \tag{35}$$

$$\text{ISI}_- = \sum_{\substack{k=n_{\text{pre}} \\ k\neq 0}}^{n_{\text{post}}} y(t-kT)\,|_{y(t-kT)<0} \tag{36}$$

where n_{pre} and n_{post} are integers of the pre- and post-cursor, and the single-bit period T, which equals to 0.05 ns, is the inverse of digital bit rate 20 Gb/s. Therefore, the total ISIs (ISI_{sum}) and the worst case eye-opening y_{EO} can be obtained.

In order to cancel ISI_{sum}, a recursive process is employed by enforcing the DC response of another equalizer $H'_{\text{eq}}(\omega)$ that equals to $y(0)/P(0)$ [18]. Herein, the transfer function of the *RL* equalizer is calculated by omitting the circuit of the on-interposer interconnects in Fig. 13:

$$H_{\text{eq}}(\omega) = \frac{2}{2 + \frac{Z_{\text{odd}}}{R_{\text{eq}} + j\omega L_{\text{eq}}}} \tag{37}$$

The recursive process starts with an initial condition that R_{eq} equals to Z_{odd}, and the initial single-bit response $y(t)$ is imported into MATLAB. The optimized value of L_{eq} is determined by sweeping from 0.1 nH to 10 nH with a 0.1 nH step when y_{EO} reaches the maximum in each recursion.

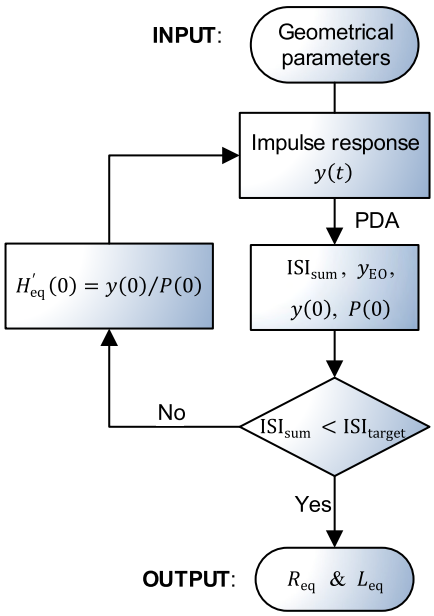


FIGURE 16. Optimization flow for equalizer parameters.

The overall optimization flow is depicted in Fig. 16. The recursive process finished if the obtained ISI_{sum} reaches the target amount $\text{ISI}_{\text{target}}$, which is set as one third of the original ISI. The optimized *RL* parameters are 44.5 Ω and 1.1 nH, respectively. Fig. 17 shows the time-domain single-bit response and the differential insertion loss of the on-interposer interconnects by using the equalizer optimization method. The simulated S_{dd21} is flattened by the *RL* equalizer up to 10 GHz (i.e., the Nyquist frequency of the data rate of 20 Gb/s). Due to the DC power consumption caused by the passive equalizer, a 0.26 V decline of the peak voltage occurs in Fig. 17(a). In the perspective of frequency domain, the DC S_{dd21} decreases from 0 dB to −3.89 dB, as shown in Fig. 17(b). Therefore, the overcompensation phenomenon in Fig. 14 is eliminated successfully with a suitable DC drop, which is contributed by the optimized *R*. Fig. 18 shows the simulated eye diagram of signal through on-interposer interconnects with the optimized equalizer. There is an obvious improvement of the quality of eye diagram compared with Fig. 15(a). The eye-opening enlarges from 1.155 V to 1.276 V and the eye-width increases from 47.25 ps to 50 ps.

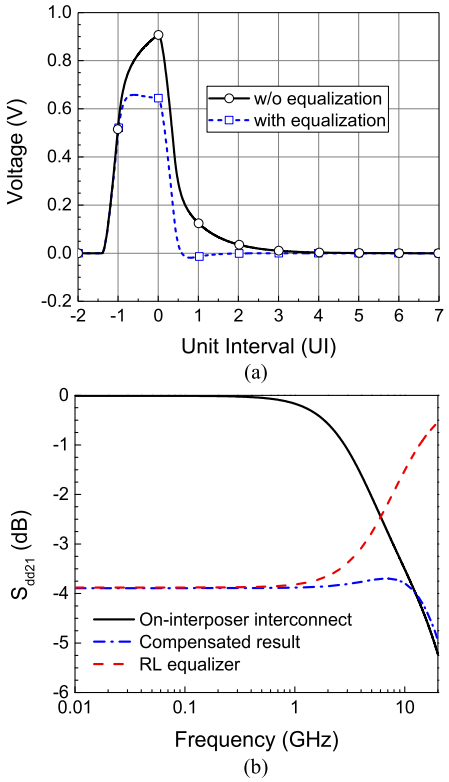


FIGURE 17. (a) Time-domain single-bit output and (b) frequency-domain response of the on-interposer differential interconnects with equalizer optimization method.

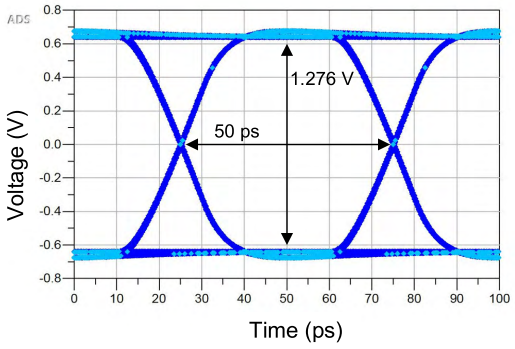


FIGURE 18. Eye diagram of signal through 5 mm-length on-interposer differential interconnects with the optimized equalizer.

More importantly, the Jitter PP reduces from 2.75 ps to 0.5 ps by applying the proposed equalizer.

C. PASSIVE EQUALIZER FOR DIFFERENTIAL TRANSMISSION STRUCTURE

The differential transmission structure, consisting of both the GSSG type TSVs and on-interposer interconnects, is commonly used in the real-world applications of 3-D IC. The odd-model half circuit model of the differential transmission structure with the *RL* equalizer is depicted in Fig. 19, and the corresponding system transfer function can be

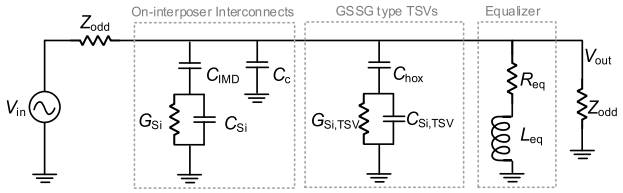


FIGURE 19. Simplified odd-mode half circuit of equalized differential transmission structure.

expressed as

$$H(s) \approx 2\frac{V_{out}}{V_{in}} = \frac{2}{2 + Z_{odd}\left(Y_{TSV} + Y_{int} + Y_{eq}\right)} = \frac{2}{2 + Z_{odd}\left(\frac{a_3}{b_3}\right)} \tag{38}$$

where

$$Y_{TSV} = \frac{sC_{ox}(G_{Si,TSV} + sC_{Si,TSV})}{G_{Si,TSV} + s\left(C_{Si,TSV} + C_{ox}\right)} \tag{39}$$

$$Y_{int} = \frac{sC_{IMD}(G_{Si} + sC_{Si})}{G_{Si} + s\left(C_{Si} + C_{IMD}\right)} + sC_c \tag{40}$$

$$Y_{eq} = \frac{1}{R_{eq} + sL_{eq}} \tag{41}$$

It is worth noting that $H(s)$ is more complicated than $H_{TSV}(s)$ and $H_{int}(s)$, thereby leading to a pair of sophisticated polynomial functions a_3 and b_3. It is difficult to derive the *RL* parameters using the frequency item elimination method presented in subsection III-A. Hence, the *RL* parameters for the whole differential transmission structure are directly obtained by the time-domain ISI cancellation technique.

The time-domain single-bit response $y(t)$ is obtained by the simplified odd-mode half circuit model shown in Fig. 19. Then, the optimization flow depicted in Fig. 16 is carried out and the obtained R and L parameters equal to 43.93 Ω and 1.6 nH, respectively.

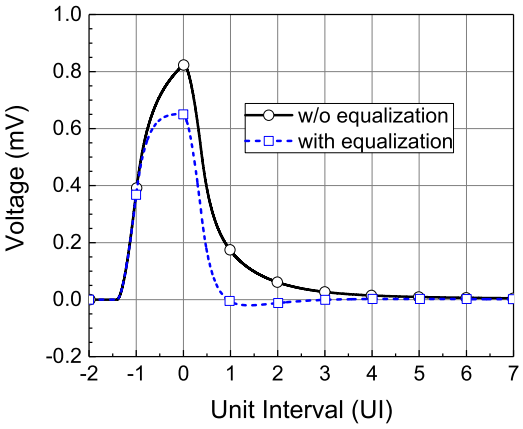


FIGURE 20. Time-domain single-bit output of the differential transmission structure.

Fig. 20 shows the simulated time-domain single-bit response of the whole transmission structure without and

with the *RL* equalizer. It can be observed that the peak-to-peak voltage decreases from 0.82 V to 0.65 V because of the DC power consumption caused by the passive equalizer. Moreover, the simulated eye diagrams of the whole structure without and with the *RL* equalizer are shown in Fig. 21. Even though there is an inevitable voltage decline, the quality of eye diagram has an obvious improvement, as shown in Fig. 21(b). Specifically, the eye-opening enlarges from 0.799 V to 1.092 V, the eye-width increases from 42.75 ps to 49 ps, and the Jitter PP is suppressed from 7.25 ps to 1 ps.

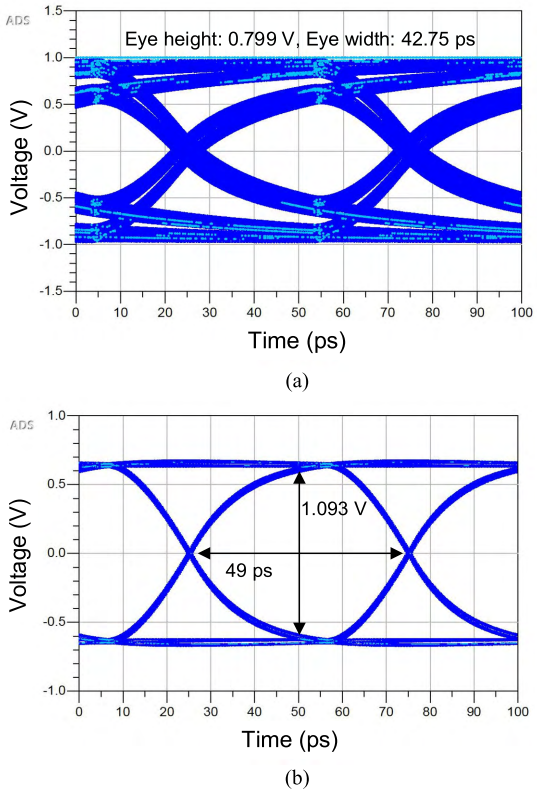


FIGURE 21. Comparisons of the eye diagrams of signal through the differential transmission structure (a) without and (b) with equalizer.

In the real-world applications of 3-D IC, the whole differential transmission structures are commonly used. Therefore, it is necessary to implement the physical structure design of the *RL* equalizer. Fig. 22 shows the top cross-sectional view of the whole transmission channel with the *RL* equalizer. With a similar structure depicted in [4] and [17], the proposed *RL* equalizer is constituted by a pair of symmetric square coil-shaped metal lines, which are located on a metal layer above the metal layer where the on-interposer interconnects are manufactured. And the compact size of *RL* equalizer can be designed by using the narrow metal width and gap space, thereby enhancing the amount of parasitic inductance [4].

Form the rapid design perspective, the parasitic resistance of the *RL* equalizer is approximately calculated by DC resistance [4]:

$$R_{eq} \approx \rho_{\mathrm{Cu}} \frac{l_{\mathrm{coil}}}{w_{\mathrm{coil}} \cdot t_{\mathrm{coil}}} \tag{42}$$

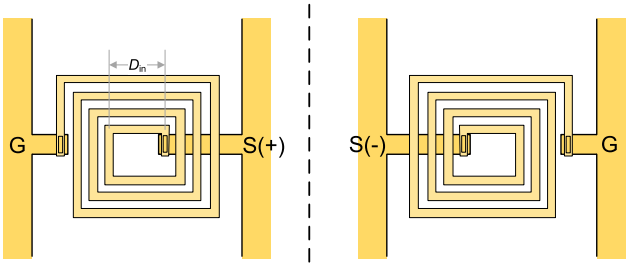


FIGURE 22. Partial top cross-sectional view of the whole structure with *RL* equalizers that are constituted by a pair of symmetric square coil-shaped metal lines.

where ρ_{Cu}, w_{coil}, and t_{coil} are the resistivity, width, and thickness of the *RL* equalizer, respectively. The total length l_{coil} of the square coil-shaped structure can be calculated by

$$l_{\mathrm{coil}} = (4n+1)\, D_{in} + (4N_i^2 + N_i)\,(w_{\mathrm{coil}} + s_{\mathrm{coil}}) \tag{43}$$

where D_{in} is the inner diameter, n is the number of turns, N_i is the integer part of n, and s_{coil} is the space between the metal lines of the coil-shaped structure.

To enhance the calculating efficiency, Snezana Jenei formula is used to calculate the low-frequency inductance of the square coil-shaped structure [29], [32]. The total inductance mainly consists of three parts: self-inductance L_{self}, negative mutual inductance L_{neg}, and positive mutual inductance L_{pos}. Herein, L_{self} of the square coil-shaped structure can be expressed as [32] and [33]:

$$L_{\mathrm{self}} = \frac{\mu_0}{2\pi} l_{\mathrm{coil}} \left(\ln \frac{2l_{\mathrm{av}}}{w_{\mathrm{coil}} + t_{\mathrm{coil}}} + \frac{1}{2} \right) \tag{44}$$

where l_{av} is the average length of the square coil-shaped structure, which is specified as

$$l_{\mathrm{av}} = \frac{l_{\mathrm{coil}}}{4n} \tag{45}$$

The negative mutual-inductance, which is caused by the anti-parallel segments, can be expressed as

$$L_{\mathrm{neg}} = 0.47n \frac{\mu_0}{2\pi} l_{\mathrm{coil}} \tag{46}$$

The positive mutual-inductance, which is due to the interactions among the parallel segments on the same side of a square, can be calculated by

$$L_{\mathrm{pos}} = \frac{\mu_0}{2\pi} l_{\mathrm{coil}} (n-1) \left[\ln \left(\sqrt{1 + \left(\frac{l_{\mathrm{coil}}}{4nd_{\mathrm{av}}} \right)^2} + \frac{l_{coil}}{4nd_{\mathrm{av}}} \right) \right] + \frac{\mu_0}{2\pi} l_{\mathrm{coil}} (n-1) \left[\frac{4nd_{\mathrm{av}}}{l_{\mathrm{coil}}} - \sqrt{1 + \left(\frac{4nd_{\mathrm{av}}}{l_{\mathrm{coil}}} \right)^2} \right] \tag{47}$$

where d_{av} indicates the average distance for the constituting factor of L_{pos}, which is specified as

$$d_{\mathrm{av}} = (w_{\mathrm{coil}} + s_{\mathrm{coil}}) \frac{(3n - 2N_i - 1)(N_i + 1)}{3(2n - N_i - 1)} \tag{48}$$

Finally, the total inductance of the *RL* equalizer can be calculated as [29] and [34]

$$L_{\text{eq}} = L_{\text{self}} - L_{\text{neg}} + L_{\text{pos}} \tag{49}$$

In order to achieve the target *RL* parameters, the appropriate physical parameters should be determined. Without loss of generality, the thickness of the *RL* equalizer is set as 0.5μm, and the value of s_{coil} is set as the same as w_{coil}. Therefore, the problem formulation can be written as

$$\begin{aligned} &\min\ F(x) = \left[R(x) - R_{target}, L(x) - L_{target}\right] \\ &\text{s.t.} \begin{cases} 0.01\ \mu m \le w_{\text{coil}} \le 1\ \mu m \\ s_{\text{coil}} = w_{\text{coil}} \\ t_{\text{coil}} = 0.5\ \mu m \\ n = [1.5, 2.5, 3.5, 4.5, 5.5] \\ 20 \le D_{\text{in}} \le 45 \end{cases} \end{aligned} \tag{50}$$

The relation between the cost function and the variables in (50) can be regarded as a dual-objective optimization problem. It can be solved using a genetic algorithm based multi-objective optimization method [35]. The obtained structural parameters of the *RL* equalizer are summarized in TABLE 2. Moreover, the *RL* equalizer is simulated by HFSS to verify the accuracy of the closed-form function, and the *RL* parameters can be derived by the *Y* parameters as follows [30], [31]:

$$L = \frac{\text{Imag}\left(\frac{1}{Y_{11}}\right)}{\omega} \tag{51}$$

$$R = \text{Real}\left(-\frac{1}{Y_{12}}\right) \tag{52}$$

The percentage errors of the calculated *R* and *L* parameters are, respectively, about 6% and 0.7% by comparison with the simulated results from the HFSS simulation.

TABLE 2. Structural parameters of RL equalizer.

Symbol	Value
w_{coil}	$0.57\ \mu m$
s_{coil}	$0.57\ \mu m$
t_{coil}	$0.5\ \mu m$
D_{in}	$30\ \mu m$
n	4.5

The differential insertion loss of the entire differential transmission structure without and with the *RL* equalizer is shown in Fig. 23. Due to the time-domain DC consumption, the low-frequency S_{dd21} decreases from 0 dB to −3.91 dB. The *RL* equalizer acts as a high-pass filter and the compensated S_{dd21} is nearly flat in the frequency region from DC to 4 GHz. It is worth noting that a small discrepancy exists beyond 4 GHz between the results obtained by the circuit model and the HFSS simulation. That is mainly caused by:

1) Skin effects: this is caused by the metallic materials of the *RL* equalizer; the serial resistance R_{eq} increases due to the skin effects, thereby leading to a decreasing S_{dd21} in 4 GHz.
2) Parasitic capacitance: there exists a parasitic capacitance between the *RL* equalizer and the silicon substrate, thereby leading to the decrease of the frequency response in the high-frequency range [4].

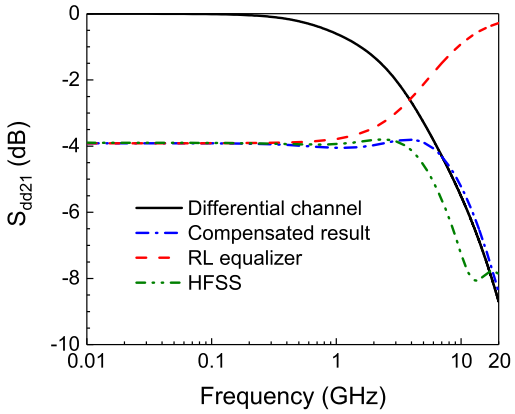


FIGURE 23. Differential insertion losses of the transmission structure, *RL* equalizer and compensated results simulated by ADS and HFSS.

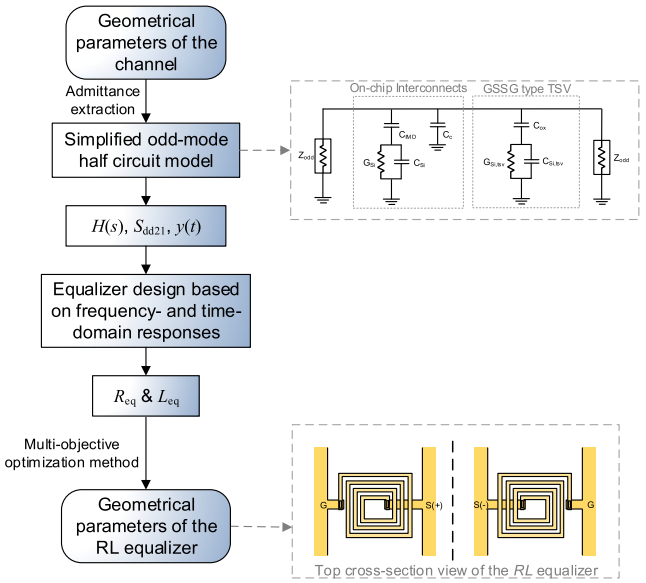


FIGURE 24. Overall procedure for the proposed equalizer design method.

In summary, the flow chart of the equalizer design method for differential channels in TSV-based 3-D ICs is presented in Fig. 24. The proposed method starts with the initially tentative geometrical parameters of the differential transmission structure as inputs. Based on the simplified odd-mode half circuit model, the system transfer function $H(s)$ could be expressed as a closed-form function such as (21), (28), and (38). In addition, the differential insertion loss S_{dd21} and the single-bit response $y(t)$ could be derived. Then, the target *RL* parameters (R_{eq} and L_{eq}) of the equalizer can be calculated based on the frequency- and time-domain responses. Finally, based on a set of closed-form functions, the geometrical parameters

of the *RL* equalizer can be obtained by a multi-objective optimization method. The proposed design method is fast and effective since it is all based on the simplified models and the closed-form functions.

IV. CONCLUSION

A complete design method of the compact *RL* type passive equalizer for differential transmission channels in TSV-based 3-D ICs was introduced. Three simplified odd-mode half circuit models were proposed and validated for the GSSG type TSVs, on-interposer interconnects, and differential channels up to 20 GHz. The *RL* parameters of the equalizer for GSSG type TSVs can be straightly derived based on the system voltage transfer function, whereas the equalizer parameters for on-interposer interconnects and differential channels can be optimized by the time-domain ISI cancellation technique. Based on a set of closed-form functions, the geometrical parameters of the practical equalizer structures can be obtained by a genetic algorithm based multi-objective optimization method. Simulated results show that the compensated differential insertion losses for all the three types of transmission channels are flat in the frequency region from DC to several GHz. The eye heights for three types of transmission channels improve 74.6%, 10.5%, and 36.8%, respectively, whereas their eye widths enlarge 24.9%, 5.82%, and 14.6%, respectively. More importantly, the jitter PP can be effectively reduced by applying the proposed *RL* equalizers.

ACKNOWLEDGMENT

The authors would like to thank Prof. Eakhwan Song at Kwangwoon University for his helpful assistances with the time-domain ISI cancelation technique.

REFERENCES

[1] M. Koyanagi, T. Fukushima, and T. Tanaka, "High-density through silicon vias for 3-D LSIs," *Proc. IEEE*, vol. 97, no. 1, pp. 49–59, Jan. 2009.

[2] A. Rahman and R. Reif, "System-level performance evaluation of three-dimensional integrated circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 8, no. 6, pp. 671–678, Dec. 2000.

[3] H. Kim *et al.*, "A wideband on-interposer passive equalizer design for chip-to-chip 30-Gb/s serial data transmission," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 5, no. 1, pp. 28–39, Jan. 2015.

[4] H. Kim *et al.*, "Design and measurement of a compact on-interposer passive equalizer for chip-to-chip high-speed differential signaling," in *Proc. 9th Int. Workshop Electromagn. Compat. Integr. Circuits*, Nara, Japan, Dec. 2013, pp. 5–9.

[5] J. Kim *et al.*, "High-frequency scalable modeling and analysis of a differential signal through-silicon via," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 4, pp. 697–707, Apr. 2014.

[6] Q. Lu, Z. Zhu, Y. Yang, and R. Ding, "Electrical modeling and characterization of shield differential through-silicon vias," *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1544–1552, May 2015.

[7] W. S. Zhao, J. Zheng, F. Liang, K. Xu, X. Chen, and G. Wang, "Wideband modeling and characterization of differential through-silicon vias for 3-D ICs," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1168–1175, Mar. 2016.

[8] W.-S. Zhao *et al.*, "High-frequency modeling of on-chip coupled carbon nanotube interconnects for millimeter-wave applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 6, no. 8, pp. 1226–1232, Aug. 2016.

[9] K. Fu, W.-S. Zhao, G. Wang, and M. Swaminathan, "Modeling and performance analysis of shielded differential annular through-silicon via (SD-ATSV) for 3-D ICs," *IEEE Access*, vol. 6, pp. 33238–33250, 2018.

[10] K. Cho *et al.*, "Signal integrity design and analysis of differential high-speed serial links in silicon interposer with through-silicon via," *IEEE Trans. Compon., Packag., Manuf. Technol.*, to be published. [Online]. Available: https://ieeexplore.ieee.org/abstract/document/8398473

[11] M. Horowitz, C.-K. K. Yang, and S. Sidiropoulos, "High-speed electrical signaling: Overview and limitations," *IEEE Micro*, vol. 18, no. 1, pp. 12–24, Jan. 1998.

[12] J. Kim *et al.*, "Through silicon via (TSV) equalizer," in *Proc. IEEE 18th Conf. Elect. Perform. Electron. Packag. Syst.*, Portland, OR, USA, Oct. 2009, pp. 13–16.

[13] K. Mohamed, A. Elrouby, Y. Ismail, and H. Ragai, "Body contact based TSV equalizer," in *Proc. IEEE 6th Int. Design Test Workshop (IDT)*, Beirut, Lebanon, Dec. 2011, pp. 114–117.

[14] R.-B. Sun, C.-Y. Wen, and R.-B. Wu, "Passive equalizer design for through silicon via with perfect compensation," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 11, pp. 1815–1822, Nov. 2011.

[15] K. Fu, W.-S. Zhao, G. Wang, and M. Swaminathan, "A passive equalizer design for shielded differential through-silicon vias in 3-D IC," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 9, pp. 768–770, Sep. 2018.

[16] C. H. Ng, C.-S. Ho, S.-F. S. Chu, and S.-C. Sun, "MIM capacitor integration for mixed-signal/RF applications," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1399–1409, Jul. 2005.

[17] Y. Jeon, H. Kim, J. Kim, and M. Je, "Design of an on-silicon-interposer passive equalizer for next generation high bandwidth memory with data rate up to 8 Gb/s," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 7, pp. 2293–2303, Jan. 2018.

[18] E. Song, J. Kim, and J. Kim, "A passive equalizer optimization method based on time-domain inter-symbol interference (ISI) cancellation technique," *IEEE Trans. Electromagn. Compat.*, vol. 60, no. 3, pp. 807–810, Jun. 2018.

[19] A. E. Engin and S. R. Narasimhan, "Modeling of crosstalk in through silicon vias," *IEEE Trans. Electromagn. Compat.*, vol. 55, no. 1, pp. 149–158, Feb. 2013.

[20] C. Xu, H. Li, R. Suaya, and K. Banerjee, "Compact AC modeling and performance analysis of through-silicon vias in 3-D ICs," *IEEE Trans. Electron Devices*, vol. 57, no. 12, pp. 3405–3417, Dec. 2010.

[21] C. Qu, R. Ding, X. Liu, and Z. Zhu, "Modeling and optimization of multi-ground TSVs for signals shield in 3-D ICs," *IEEE Trans. Electromagn. Compat.*, vol. 59, no. 2, pp. 461–467, Apr. 2017.

[22] J. Jin, W.-S. Zhao, D.-W. Wang, H.-S. Chen, E.-P. Li, and W.-Y. Yin, "Investigation of carbon nanotube-based through-silicon vias for PDN applications," *IEEE Trans. Electromagn. Compat.*, vol. 60, no. 3, pp. 738–746, Jun. 2018.

[23] W.-S. Zhao, J. Zheng, S. Chen, X. Wang, and G. Wang, "Transient analysis of through-silicon vias in floating silicon substrate," *IEEE Trans. Electromagn. Compat.*, vol. 59, no. 1, pp. 207–216, Feb. 2017.

[24] C. R. Paul, "Prediction of crosstalk in ribbon cables: Comparison of model predictions and experimental results," *IEEE Trans. Electromagn. Compat.*, vol. EMC-20, no. 3, pp. 394–406, Aug. 1978.

[25] Y.-J. Cheng, H.-H. Chuang, C.-K. Cheng, and T.-L. Wu, "Novel differential-mode equalizer with broadband common-mode filtering for Gb/s differential-signal transmission," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 9, pp. 1578–1587, Sep. 2013.

[26] R. N. Simons, *Coplanar Waveguide Circuits, Components, and Systems*. New York, NY, USA: Wiley, 2001.

[27] F. Stellari and A. L. Lacaita, "New formulas of interconnect capacitances based on results of conformal mapping method," *IEEE Trans. Electron Devices*, vol. 47, no. 1, pp. 222–231, Jan. 2000.

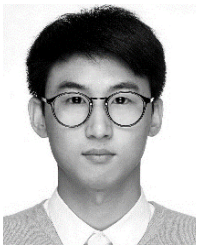
[28] Y. Eo and W. R. Eisenstadt, "High-speed VLSI interconnect modeling based on S-parameter measurements," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. 16, no. 5, pp. 555–562, Aug. 1993.

[29] S. Jenei, B. K. J. C. Nauwelaers, and S. Decoutere, "Physics-based closed-form inductance expression for compact modeling of integrated spiral inductors," *IEEE J. Solid-State Circuits*, vol. 37, no. 1, pp. 77–80, Jan. 2002.

[30] J. Zheng, D.-W. Wang, W.-S. Zhao, G. Wang, and W.-Y. Yin, "Modeling of TSV-based solenoid inductors for 3-D integration," in *Proc. IEEE MTT-S Int. Microw. Workshop Adv. Mater. Process RF THz Appl. (IMWS-AMP)*, Jul. 2015, pp. 1–3.

[31] C. B. Sia, B. H. Ong, K. W. Chan, K. S. Yeo, J.-G. Ma, and A. V. Do, "Physical layout design optimization of integrated spiral inductors for silicon-based RFIC applications," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2559–2567, Dec. 2005.

[32] B. K. Casper, M. Haycok, and R. Mooney, "An accurate and efficient analysis method for multi-Gb/s chip-to-chip signaling schemes," in *Proc. Int. Symp. IEEE VLSI Circuits*, Jun. 2002, pp. 54–57.
[33] F. W. Grover, *Inductance Calculations*. New York, NY, USA: Dover, 1946.
[34] T. Luo *et al.*, "A new accurate and fast arithmetic for on-chip spiral inductors," in *Proc. IEEE Int. Conf. Inf. Acquisition*, Aug. 2006, pp. 545–549.
[35] A. J. Chipperfield and P. J. Fleming, "The MATLAB genetic algorithm toolbox," in *Proc. IEEE Colloquium Appl. Control Techn. MATLAB*, 1995, pp. 1–8.



KAI FU received the B.E. degree in electronic and information engineering from Hangzhou Dianzi University, Hangzhou, China, in 2017, where he is currently pursuing the M.E. degree with a focus on interconnect design and modeling for 3-D integration.

WEN-SHENG ZHAO (S'09–M'13–SM'18) received the B.E. degree from the Harbin Institute of Technology, Harbin, China, in 2008, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 2013.

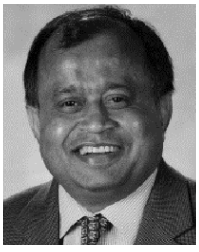
He was a Visiting Ph.D. Student with the National University of Singapore, Singapore, from 2010 to 2013, and a Visiting Scholar with the Georgia Institute of Technology, Atlanta, GA, USA, from 2017 to 2018. He is currently an Associate Professor at Hangzhou Dianzi University, Hangzhou, China. He has published one book, three book chapters, and over 80 papers in refereed journals and conference proceedings (including over 30 IEEE journal papers). His research interests include signal integrity and EMC, carbon nanoelectronics, microwave sensor, multiphysics simulation, and machine learning applications in the electronic design.

DA-WEI WANG received the B.E. degree in communication engineering from Jilin University, Changchun, China, in 2010, and the M.E. degree in communication and information system from the China Academy of Telecommunication Technology, Beijing, China, in 2013. He is currently pursuing the Ph.D. degree in electronic science and technology with Zhejiang University, Hangzhou, China.

His current research interests include computational electromagnetics, signal integrity analysis, and multiphysics simulation.

GAOFENG WANG (S'93–M'95–SM'01) received the Ph.D. degree in electrical engineering from the University of Wisconsin–Milwaukee, Milwaukee, WI, USA, in 1993, and the Ph.D. degree in scientific computing from Stanford University, Stanford, CA, USA, in 2001.

He was a Scientist with Tanner Research Inc., Pasadena, CA, USA, from 1993 to 1996. He was a Principal Researcher and Development Engineering with Synopsys Inc., Mountain View, CA, USA, from 1996 to 2001. In 1999, he served as a Consultant with Bell Laboratories, Murray Hill, NJ, USA. He was the Chief Technology Officer (CTO) at Intpax, Inc., San Jose, CA, USA, from 2001 to 2003. He was the CTO at Siargo Inc., Santo Clara, CA, USA, from 2004 to 2010. He was a Professor and the Head of the CJ Huang Information Technology Research Institute, Wuhan University, Wuhan, China, from 2004 to 2013. He was a Chief Scientist with Lorentz Solution, Inc., Santa Clara, CA, USA, from 2010 to 2013. He is currently a Distinguished Professor with Hangzhou Dianzi University, Hangzhou, China. He has over 220 journal articles and held 35 patents. His current research interests include integrated circuit and microelectromechanical system design and simulation, computational electromagnetics, electronic design automation, and wavelet applications in engineering.



MADHAVAN SWAMINATHAN (M'95–SM'98–F'06) received the M.S. and Ph.D. degrees in electrical engineering from Syracuse University in 1989 and 1991, respectively. He is currently the John Pippin Chair Professor in microsystems packaging & electromagnetics with the School of Electrical and Computer Engineering (ECE) and also the Director of the Center for Co-Design of Chip, Packages, System, Georgia Institute of Technology (Georgia Tech.), Atlanta, GA, USA. He formerly held the position of Joseph M. Pettit Professor in Electronics in ECE and the Deputy Director of the NSF Microsystems Packaging Research Center, Georgia Tech. Prior to joining Georgia Tech., he was with IBM working on packaging for supercomputers. He is the author of over 450 refereed technical publications, holds 29 patents, primary author and co-editor of three books, founder and co-founder of two start-up companies (E-System Design and Jacket Micro Devices) and the Founder of the IEEE Conference Electrical Design of Advanced Packaging and Systems, a premier conference sponsored by the CPMT society on Signal Integrity in the Asian Region. He has served as the Distinguished Lecturer for the IEEE EMC Society.

WEN-YAN YIN (M'99–SM'01–F'13) received the M.Sc. degree in electromagnetic field and microwave technique from Xidian University, Xi'an, China, in 1989, and the Ph.D. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, in 1994.

He is currently a Distinguished Professor with Zhejiang University, Hangzhou, China. His current research interests include passive and active RF and millimeter-wave device and circuit modeling, ultrawideband interconnects and signal integrity, nanoelectronics, EMC and electromagnetic protection of communication platforms, and computational multiphysics and its application.

Dr. Yin is an Associate Editor of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY and the IEEE JOURNAL OF MULTISCALE AND MULTIPHYSICS COMPUTATIONAL TECHNIQUES. He was an IEEE EMC Society Distinguished Lecturer from 2011 to 2012 and the General Co-Chair of the IEEE EDAPS in 2011 and 2017, respectively.