Novel Integrated Class F Power Amplifier Design for RF Power Infrastructure Applications

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ABSTRACT This paper presents a comprehensive study of the impact of resistive harmonic loading on the design of integrated Class-F power amplifiers (PAs). The proposed time-domain waveform-based analysis allows for an evaluation of the performance of Class-F PAs while controlling both second and third harmonics simultaneously. The voltage mapping is presented to include the impact of the resistive second harmonic impedance in the design of Class-F PAs. Besides, drain current formulations as a function of conduction angle are used to evaluate the harmonic coefficients under the impact of resistive third harmonic impedance. As such, the combination of resistive second and third harmonics is modeled to study its impact on efficiency and optimum impedance in the Class-F PAs. For practical validation, the derived knowledge is applied to propose a novel integrated Class-F PA that absorbs the output capacitance into the match while maintaining a purely resistive load at the fundamental frequency. The output match is fabricated on a highly integrated NXP Laterally Diffused MOSFET (LDMOS) process. At 1.8 GHz, using NXP 5-mm LDMOS die, the integrated Class-F achieves a drain efficiency ranging from 52% to 61% at 5-W output power based on two different design topologies. Both prototypes demonstrate excellent isolation at the second and third harmonics. Measurement results confirm the theoretical framework reported in this paper.

INDEX TERMS Active load pull, Class-F, harmonic tuned, integrated, LDMOS, power amplifier, quality factor, resonating structures, resistive harmonics.

I. INTRODUCTION

Massive Multiple Input and Multiple Output (mMIMO) based radio frequency (RF) base stations demand high-efficiency Power Amplifiers (PAs) to meet the expectation of next-generation wireless infrastructure, now called 5G. With improved signal quality, higher data rates, lower latency, and increased power efficiency, the 5G solutions demand efficient solutions on various fronts. For enablement of the next-generation RF circuitry, the PA continues to be the critical element for base station solutions. The road to successful implementation of MIMO based RF solutions involves lowering the DC consumption and minimizing the RFPA circuitry footprint, which remains the focus of researchers in this domain.

The harmonically tuned amplifier topologies classified as Class E, Class F, Class F^{-1}, and Class J are widely investigated to achieve high efficiency [1]–[14]. The ideal Class F

shapes voltage waveform to the square and current to half sinusoidal leading to theoretical 100% power conversion efficiency when infinite harmonics are considered for waveform shaping. However, in practice, the higher frequencies and device output parasitic limit the waveform shaping upto three harmonics [7]–[14]. When controlling up to three harmonics, class F demonstrates a theoretical drain efficiency (DE) of 90.6% [14], with second harmonic and third harmonic impedances tuned to exact short and open loads, respectively.

Thus far, there has been no comprehensive study that quantified the efficiency degradation due to the resistivity of individual harmonics or their combinations under class-F operation. The works reported in [15] and [16] are attempted to solve the problem of matching network design while taking into account the quality factor of passives but limited to fundamental impedance solutions. Some works have attempted to demonstrate the operation of Class-F PAs under resistive

operation [22], [23] but there is a gap between practical implementation and a proposed theory. For instance, [22] introduces resistive class-F operation using waveform engineering theory and measurements that are not validated with load-pull measurements. In addition, the variation in fundamental loading condition and efficiency degradation has not been reported while accounting for the resistive behavior of second and third harmonic impedance simultaneously. Besides, most of previously reported Class-F PA designs are often implemented using off-chip matching networks synthesis on printed circuit boards [17]–[23], which increases the circuit footprint and limits application of these PAs in mMIMO based RF base stations that require compact form factor.

This work provides a novel, fully integrated solution for Class-F PA design, which can be applied in industrial mMIMO infrastructure systems. The unique topology satisfies the Class F harmonic loading terminations by absorbing the device output capacitance while maintaining a purely resistive fundamental impedance transformation, unlike previous works where purely resistive termination at the fundamental frequency is not guaranteed. In addition, this work provides a methodology that addresses the operation of class-F PAs under losses and resistivity of second and third harmonic using the large-signal time-domain waveform analysis. This study reveals that the resistive second and third harmonic will impact the optimum load resistance at fundamental frequency as a combination of both harmonic impedances. The practical validation of this work addresses the design of two integrated Class-F PA prototypes.

In this manuscript, Section II discusses details of voltage and current mapping in Class F PAs. The generalized time domain waveforms are presented as a function of conduction angle and resistive harmonic terminations, which helps to evaluate the performance degradation arising because of resistivity of harmonics. The mathematical formulation presented in Section II are extended in Section III to derive the optimum load resistance and evaluate theoretical performance. Using the analysis, a novel integrated Class-F topology is proposed and implemented in Section IV.

II. GENERALIZED CLASS-F PA
A. VOLTAGE MAPPING IN CLASS F PAs
When controlling up to first three harmonics, the generalized drain voltage (V_{DS}) is given by

$$V_{DS}(k_2, k_3, \delta, \theta) = V_{dc} - \delta(k_2, k_3)(V_{dc} - V_k)$$
$$\times [\cos\theta - k_2 \cos 2\theta - k_3 \cos 3\theta] \quad (1)$$

where δ is the voltage gain function, V_k is the knee voltage of the device, V_{dc} is the dc drain voltage, k_2 and k_3 are second and third harmonic voltage coefficients, respectively and θ is the angular frequency [2]. The voltage gain function is defined as the ratio of the altered fundamental component due to harmonic manipulation, to the un-manipulated case wherein second and third harmonic impedances are both short circuited [2]. The magnitude of δ is in fact dependent on the selection of second, third or combination of both impedances. Using (1), the drain voltage can be normalized with respect to dc voltage and δ as

$$\overline{V_{DS}(k_2, k_3, \delta, \theta)} = \cos\theta - k_2 \cos 2\theta - k_3 \cos 3\theta \quad (2)$$

In order to maximize the fundamental voltage swing, using [2], the voltage gain function can analytically be written as

$$\delta(k_2, k_3) = \frac{-1}{\left| \frac{\partial V_{DS}(k_2,k_3,\theta)}{\partial\theta} \right|_{\theta_{min}}} \quad (3)$$

$$\theta_{min,1} = 0 \quad (5)$$

$$\theta_{min,2} = \pi \quad (6)$$

$$\theta_{min,3} = \left| \cos^{-1}\left(\frac{-1}{4k_2}\right) \right| \quad if\ k_3 = 0,\ k_2 \neq 0 \quad (7)$$

$$\theta_{min,4} = \cos^{-1}\left(\frac{1}{2}\sqrt{\frac{3k_3-1}{3k_3}}\right) \left| \begin{array}{l} if\ k_2 = 0, k_3 \neq 0 \\ \frac{3k_3-1}{3k_3} > 0,\ \left|\frac{1}{2}\sqrt{\frac{3k_3-1}{3k_3}}\right| < 1 \end{array} \right.$$
$$\theta_{min,5} = \cos^{-1}\left(\frac{-1}{2}\sqrt{\frac{3k_3-1}{3k_3}}\right) \quad (8)$$

$$\theta_{min,6} = \cos^{-1}\left(\frac{-\left(k_2+\sqrt{k_2^2-3k_3+9k_3^2}\right)}{6k_3}\right) \left| \begin{array}{l} if\ k_2^2-3k_3+9k_3^2 > 0 \\ -1 < \frac{-\left(k_2+\sqrt{k_2^2-3k_3+9k_3^2}\right)}{6k_3} < 1 \end{array} \right.$$
$$\theta_{min,7} = \cos^{-1}\left(\frac{-\left(k_2-\sqrt{k_2^2-3k_3+9k_3^2}\right)}{6k_3}\right) \left| \begin{array}{l} -1 < \frac{-\left(k_2-\sqrt{k_2^2-3k_3+9k_3^2}\right)}{6k_3} < 1 \end{array} \right. \quad (9)$$

By applying the first derivate on (2) and equating (3) to zero, minima θ_{min} can be evaluated as

$$
\overline{\frac{\partial V_{DS}(k_2, k_3, \delta, \theta)}{\partial \theta}}
= (1 - 3k_3 + 4\cos\theta(k_2 + 3k_3\cos\theta))(\sin\theta) = 0 \quad (4)
$$

Since the generalized voltage is a multi-variable system, it is not possible to find a closed form solution for θ_{min}. However, by applying different boundary conditions on second and third harmonic, the voltage map can be divided into different regions. Thus, the θ_{min} can be evaluated based on the selection of different values of k_2 and k_3. For the different boundaries of k_2 and k_3, given in (5) − (9), as shown at the bottom of the previous page, δ can be plotted as a function of k_2 and k_3 as shown in Fig. 1. In particular, for Class-F mode with $k_2 = 0$ (since second harmonic impedance is short circuited) and $k_3 = -1/6$ (for maximum delta) δ is evaluated using voltage map as $2/\sqrt{3}$. By substituting the values of k_2, k_3 and δ in (1), Class-F drain voltage (V_F) waveform is expressed as

$$
V_F(\theta) = V_{dc} - (V_{dc} - V_k)\left(\frac{2}{\sqrt{3}}\cos\theta - \frac{1}{3\sqrt{3}}\cos 3\theta\right) \quad (10)
$$

Fig. 2(b) shows voltage waveforms for different values of k_2 including the Class-F voltage with $k_2 = 0$. The variation in k_2 results in different voltage waveforms with high crest distortions as shown in Fig. 2(b).

B. CURRENT FORMULATION IN CLASS F PAs

The Class-F PA mode requires an infinite third harmonic impedance; and, as a result, the intrinsic current waveform is manipulated by removing the third harmonic current component $i_3(\theta) = \gamma_3 \cos 3\theta$, where γ_3 is a real component of third harmonic current. The generalized drain current (I_F) under Class-F PA operation can be expressed as function of
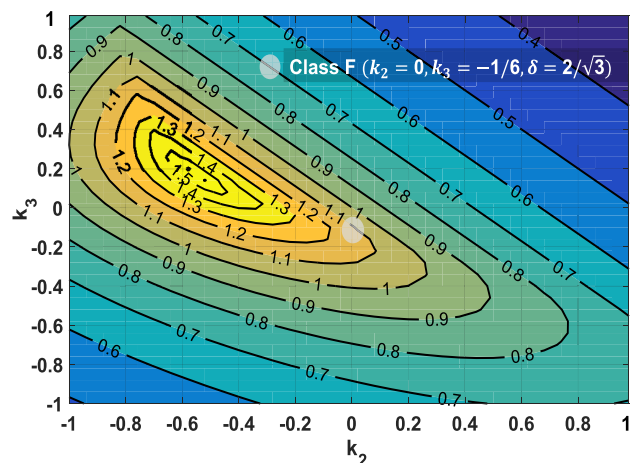

FIGURE 1. The generalized voltage gain function (δ) as a function of second (k_2) and third harmonic voltage coefficient (k_3).
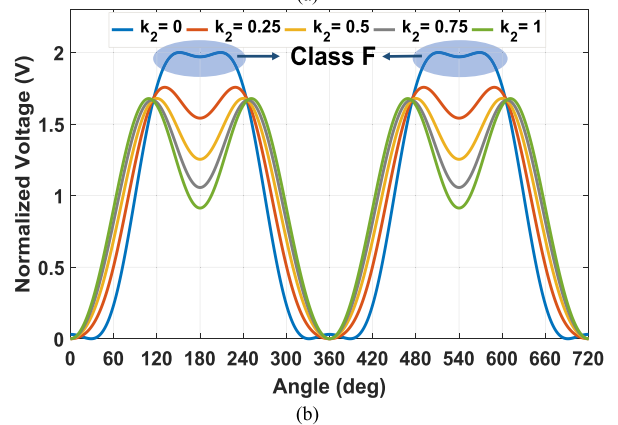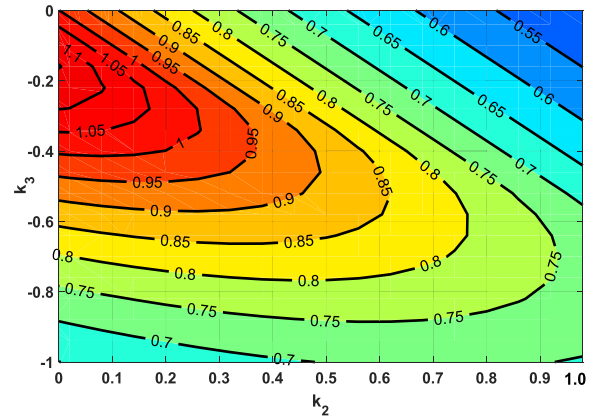
FIGURE 2. (a) The voltage gain function (δ) under resistive second harmonic impedance region. (b) Normalized drain voltage under resistive second harmonic termination for class F amplifiers.

conduction angle (β), peak drain current (I_m) and θ as

$$
I_F(\theta) = \frac{I_m + \gamma_3(\beta, I_{F,3})}{1 - \cos\left(\frac{\beta}{2}\right)}\left[\cos\theta - \cos\left(\frac{\beta}{2}\right)\right] - i_3(\theta);
$$

$$
-\frac{\beta}{2} < \theta < \frac{\beta}{2}
$$

$$
0; \quad -\pi < \theta < -\frac{\beta}{2}, \quad \frac{\beta}{2} < \theta < \pi \quad (11)
$$

Since Class F tunes third harmonic to open circuit condition, the drain current should contain no third harmonic component ($I_{F,3}$) and can be computed by forcing third-order Fourier expansion of (11) to zero as

$$
I_{F,3}(\beta, \gamma_3)
$$

$$
= \frac{1}{\pi}\int_{-\frac{\beta}{2}}^{\frac{\beta}{2}} I_F(\theta)\cos 3\theta \, d\theta = \left(I_m\left(\frac{\sin\frac{\beta}{2} + 2\sin\beta + \sin\frac{3\beta}{2}}{6\pi}\right)\right.
$$

$$
\left. + \frac{\gamma_3\left(\sin\frac{\beta}{2} + 3\sin\beta + \sin\frac{3\beta}{2} - 3\beta - 4\sin\beta\cos^2\beta\right)}{6\pi}\right)
$$

$$
= 0 \quad (12)
$$

By applying the Fourier expansion on (11) while accounting for (12), the dc ($I_{F,dc}$), fundamental ($I_{F,1}$), and second har-

monic ($I_{F,2}$) current components can be derived as a function of $\rho(\beta, I_{F,3})$ as

$$I_{F,dc}(\beta, \rho)$$
$$= \frac{1}{2\pi} \int_{-\beta/2}^{\beta/2} I_F d\theta = \frac{I_m}{6\pi \left(\cos \frac{\beta}{2} - 1\right)} \left(\left(3\beta \cos \frac{\beta}{2} - 6 \sin \frac{\beta}{2}\right)\right.$$
$$\left. - \rho I_m \left(\sin 2\beta + 6 \sin \frac{\beta}{2} - 2 \sin \frac{3\beta}{2} - 3\beta \cos \frac{\beta}{2} + \sin \beta\right)\right) \tag{13}$$

$$I_{F,1}(\beta, \rho)$$
$$= \frac{1}{\pi} \int_{-\frac{\beta}{2}}^{\frac{\beta}{2}} I_F \cos \theta d\theta = \frac{I_m \sin \frac{\beta}{2}}{\pi} - \frac{\rho I_m \sin \frac{\beta}{2}}{\pi}$$
$$\times \left(2\cos^3 \frac{\beta}{2} - 1\right) + \frac{I_m (1 + \rho) \left(2 \sin \frac{\beta}{2} - \beta\right)}{2\pi \left(\cos \frac{\beta}{2} - 1\right)} \tag{14}$$

$$I_{F,2}(\beta, \rho)$$
$$= \frac{1}{\pi} \int_{-\frac{\beta}{2}}^{\frac{\beta}{2}} I_F \cos 2\theta d\theta = \frac{I_m}{3\pi} \left(2 \sin \frac{\beta}{2} + \sin \beta\right)$$
$$+ \frac{I_m \rho}{\pi} \left(\frac{\sin \beta - \sin \frac{\beta}{2}}{3} - \frac{\sin \frac{5\beta}{2}}{5}\right) \tag{15}$$

where

$$\rho = \frac{\gamma_3}{I_m} = -\frac{\left(\sin \frac{\beta}{2} + 2 \sin \beta + \sin \frac{3\beta}{2}\right) - 6\pi \frac{I_{F,3}}{I_m}}{4\sin^3 \beta - \sin \beta - 3\beta + \sin \frac{\beta}{2} + \sin \frac{3\beta}{2}} \tag{16}$$
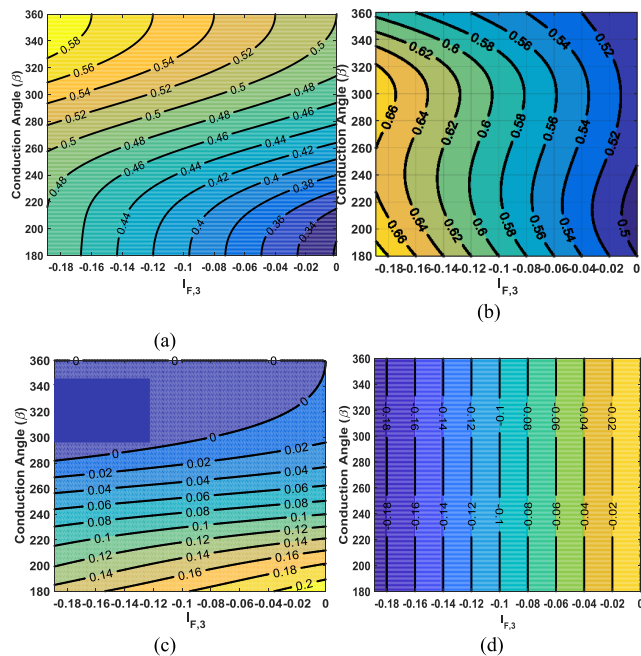

FIGURE 3. Normalized intrinsic drain components as a function of conduction angle (β) and third harmonic current. (a) DC component ($I_{F,dc}$) (b) Fundamental component ($I_{F,1}$) (c) Second component ($I_{F,2}$) (d) Third component ($I_{F,3}$).

The dc, fundamental, second and third harmonic drain current components are plotted and shown in Fig. 3(a) (d). For the $\beta = \pi$, and third harmonic impedance at open, current components can be computed using (13)–(16) as

$$\begin{bmatrix} I_{F,dc} & I_{F,1} \\ I_{F,2} & I_{F,3} \end{bmatrix} = \begin{bmatrix} I_m/\pi & I_m/2 \\ 2I_m/3\pi & 0 \end{bmatrix}, \tag{17}$$

which corresponds to well-known Class-F harmonic current components.

III. SECOND AND THIRD HARMONIC ENGINEERED CLASS-F PA

A. VOLTAGE AND CURRENT FORMULATION

In practice, maintaining an ideal harmonic short or open circuit condition is difficult because of losses involved in the package, wire bonds, and the printed circuit board. Any resistive harmonic impedance alters the voltage and current components thereby impacting the power efficiency of the PA. The resistive harmonic impedance and its corresponding harmonic voltage and current coefficients are inter-dependent on each other. The variation in harmonic coefficients determines the respective harmonic impedance and vice versa i.e. change in harmonic impedance determines the variation in harmonic voltage or current components. The impact and formulation of resistive second and third harmonic impedance are explained in the following section.

The half sinusoidal Class-F drain current exhibits even harmonic current components with no existence of third order component. As a result, for a positive resistive second harmonic to exist, an out-of-phase voltage component must exist. This drain-voltage requirement is satisfied for $0 \leq k_2 \leq 1$, thus leading to the choice of a negative second harmonic voltage-component. As illustrated in Fig. 2(a), for a fixed $k_3 = -0.16$, a resistive second harmonic impedance space can be exploited for $0 \leq k_2 \leq 1$, which in turn degrades δ from 1.15 to 0.55 For an open third harmonic condition, i.e. $I_{F,3} = 0$ ($k_3 = -0.16$), the second harmonic impedance ($Z_F, 2$) in a resistive Class-F mode can be computed using (1) and (9) as

$$Z_F, 2(\delta, k_2, k_3, \beta, \rho)$$
$$= \frac{\delta (k_2 \neq 0, k_3 = -1/6) \times (V_{dc} - V_k) \times k_2}{I_{F,2}(\beta, \rho, I_{F,2} = 0)} \tag{18}$$

On the other hand, the third harmonic resistive impedance is caused by an alteration in the third harmonic drain current component ($I_{F,3}$). For a short second harmonic condition, i.e. $k_2 = 0$, and $k_3 = -0.16$, the third harmonic impedance, ($Z_F, 3$), can be calculated as a function of varying third harmonic drain current as

$$Z_F, 3(\delta, k_2, k_3, \beta, \rho)$$
$$= \frac{\delta (k_2 = 0, k_3 = -0.16) \times (V_{dc} - V_k) \times k_3}{I_{F,3}(\beta, \rho)} \tag{19}$$

To have a precise and more practical study of the impact of harmonics, the resistive sweep of the reflection coefficient over second is restricted starting from short condition
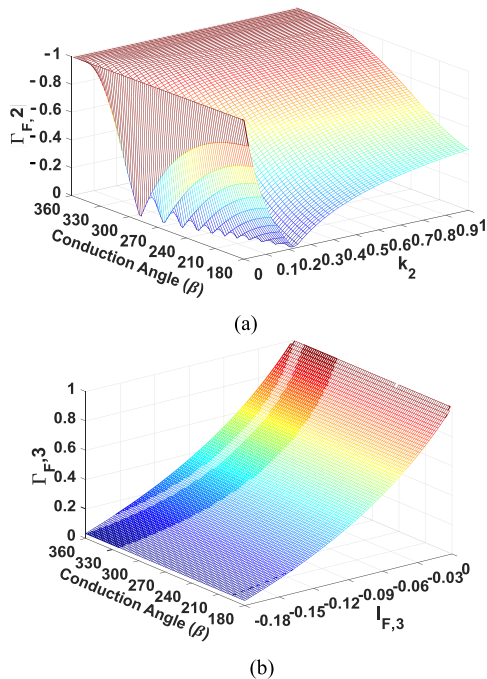
(a)

(b)

FIGURE 4. (a) Variation of $\Gamma_F, 2$ as function of conduction angle (β) and second harmonic voltage coefficient (k_2) (b) Variation of $\Gamma_F, 3$ as a function of conduction angle (β) and third harmonic current component ($I_{F,3}$).

($\Gamma_F, 2 = -1$) to the center of Smith chart ($\Gamma_F, 2 = 0$). Likewise, the third harmonic sweep of the reflection coefficient is restricted from an open circuit ($\Gamma_F, 3 = 1$) to the center of Smith chart ($\Gamma_F, 3 = 0$) and is given by

$$0 \leq \Gamma_{F,n} = \left| \frac{Z_{F,n}(\delta, k_2, k_3, \beta) - Z_o}{Z_{F,n}(\delta, k_2, k_3, \beta) + Z_o} \right| \leq 1 \quad (20)$$

where n = 2 or 3 designates the harmonic order and Z_o is characteristic impedance. In this work, a value of 50 Ω was used since that is the system impedance of the measurement apparatus used for verification. Class-F amplifiers have an in-phase third harmonic voltage component. As a result, an out-of-phase third harmonic current must be realized for a real impedance to exist. Based on (20) and sweeping $I_{F,3} < 0$, the drain current components can be computed using (13) − (16). By imposing the condition (20), the region of sweep for k_2 and $I_{F,3}$ can be delimited for any β which are plotted in Fig. 4(a) and (b), respectively. Using the boundary on $I_{F,3}$, the dc, fundamental, second and third harmonic currents are plotted for different conduction angles in Fig. 3. The plots are limited to $I_{F,3} = -0.188$, and it can be inferred that that any change in third harmonic current impacts all the other current components at the drain of the device. For $\beta = 180°$, i.e. Class-B bias condition, both $I_{F,dc}$ and $I_{F,1}$ increases with a sweep in $I_{F,3}$. However, the change is dc current is higher than the change in the fundamental current component.

B. DESIGN SPACE AND PERFORMANCE EVALUATION
The resistive second harmonic impacts the fundamental voltage component and resistive third harmonic impacts fundamental current thereby changing the optimum load at the

current generator of the device. The fundamental load ($Z_F, 1$), can be expressed as

$$Z_{F,1}(\delta, k_2, k_3, \beta, \rho) = \frac{\delta(k_2, k_3) R_{opt}}{I_{F,1}(\beta, \rho)} \quad (21)$$

where R_{opt} is the Class-B optimum impedance given as $(V_{dc} - V_k)/(I_m/2)$. For Class-B conduction angle, $\beta = 180°$ and the second harmonic at short and third harmonic at open, $Z_F, 1$ can be computed as $1.15 \times R_{opt}$ as seen in Fig. 5(a), which is in fact same as Class-F fundamental impedance reported in previous works [9]. For a fixed open third harmonic impedance, $Z_F, 1$ decreases from $1.15 \times R_{opt}$ to $0.94 \times R_{opt}$ with the resistive second harmonic. Likewise, for a short second harmonic impedance, $Z_{F,1}$ changes from $1.15 \times R_{opt}$ to $0.84 \times R_{opt}$ with resistive third harmonic. With both $Z_F, 2$ and $Z_F, 3$ at the center of Smith chart ($\Gamma_F, 2 = 1$, $\Gamma_F, 3 = 1$), $Z_F, 1$ decreases to $0.72 \times R_{opt}$. Since the fundamental impedance changes with any variation at second and third harmonics, this in turn impacts the output power and drain efficiency (DE) in Class F. Using the DC power (P_{dc}) and delivered RF power (P_{RF}), the generalized drain efficiency can be expressed using (10), (12)–(14) as

$$\eta_F(\delta, k_2, k_3, \beta) = \frac{\left(1 - \frac{V_k}{V_{dc}}\right) I_{F,1}(\beta, \rho) \delta(k_2, k_3)}{2 I_{F,dc}(\beta, \rho)} \quad (22)$$

The DE is plotted as a function of $\Gamma_F, 2$ and $\Gamma_F, 3$ in Fig 5(b). It can be inferred from the plot that DE of 90.6% is achieved for a Class-F amplifier. For the second harmonic impedance at short, DE decreases from 90.6 to 83% for $0 \leq \Gamma_F, 3 \leq 1$. Furthermore, for a fixed third harmonic at open ($\Gamma_F, 3 = 1$), the DE decreases from 90.6 to 73% under the impact of resistive second harmonic. Since the resistive nature of both harmonics impacts the performance of the amplifier, it is noteworthy that the drop-in efficiency for a resistive third harmonic is 7% on contrary to second harmonic which drops efficiency by 18%. In fact, this also highlights the importance of prioritizing termination of second harmonic over the third harmonic in the design process.

IV. NOVEL INTEGRATED CLASS F POWER AMPLIFIER DESIGN
A. ACTIVE LOAD PULL-BASED RESISTIVE HARMONIC MAPPING
The experimental validation of this work is divided into two steps, one based on the active load-pull and another based on the integrated PA design and fabrication. The active load-pull (ALP) is carried out using Maury's active system [24] as shown in Fig. 6(a). The objective of ALP is to quantify the maximum achievable efficiency under resistive second and third harmonic impedance under Class-F operation. For an NXP LDMOS 4.8 mm die, the ground-signal-ground (GSG) launch effects are extracted using the thru measurements. The impedances are intrinsically reengineered from 50 Ω to open circuit for third harmonic and from 50 Ω to short circuit for second harmonic impedance. Thereafter, the linear
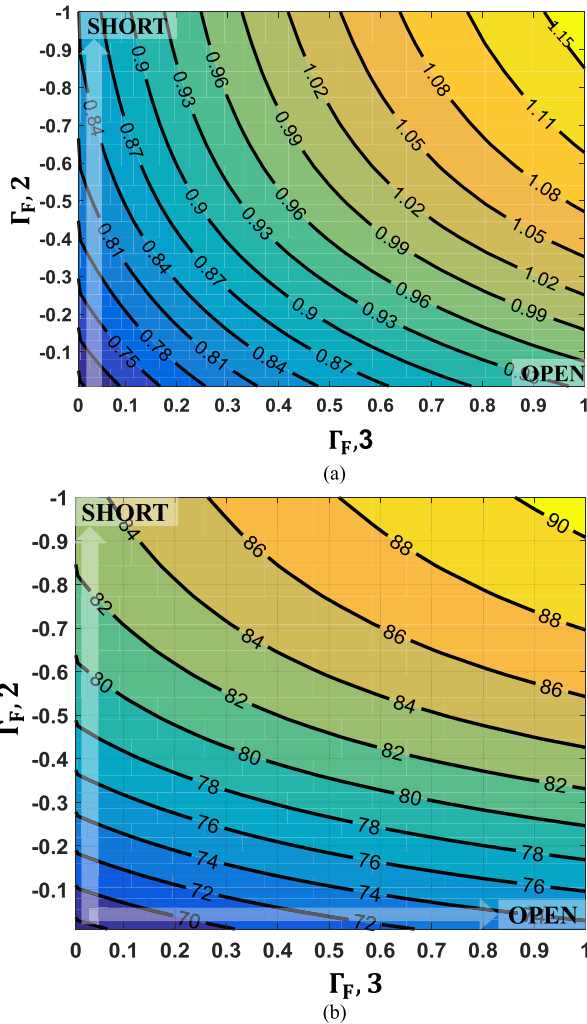
FIGURE 5. Impact of resistive second (Γ_F, 2) and third harmonic (Γ_F, 3) as a function of β on (a) Fundamental optimum impedance (Z_F, 1) normalized to R_{opt} (b) Theoretical drain efficiency of class F PA.

FIGURE 6. (a) Active load pull measurement set up with reengineered harmonic and fundamental impedance (b) Measured drain efficiency as function of resistive second and third harmonic impedance for 4.8 mm LDMOS die at 1.8 GHz.

approximated output capacitance along with GSG effects is embedded to determine the second and third harmonic impedance at the probe pad as shown in Fig. 6(a). For the combination of each second and third harmonic resistive impedance, a fundamental load-pull is performed at P3 dB gain compression.

The drain efficiency is plotted as a function of Γ_F, 2 and Γ_F, 3 in Fig. 6(b). For an ideal Class F condition i.e. Γ_F, 3 = 1Γ_F, 2 = −1, drain efficiency of 74.5 % is measured using an active load pull system. For Γ_F, 3 = 1 (Z_F, 3 open circuited), the DE varies from 74.5 to 69% for resistive second harmonic sweep i.e. −1 ≤ Γ_F, 2 ≤ 0. Likewise, for Γ_F, 2 = −1 (Z_F, 3 short-circuited), the DE drops from 74.5 to 68.5 %. Similar to the theoretical predictions, the measured drop in efficiency at the second harmonic impedance and third harmonic is critical for output matching network design. Due to component losses at high frequencies, it is very challenging to maintain the third harmonic in an open circuit condition.
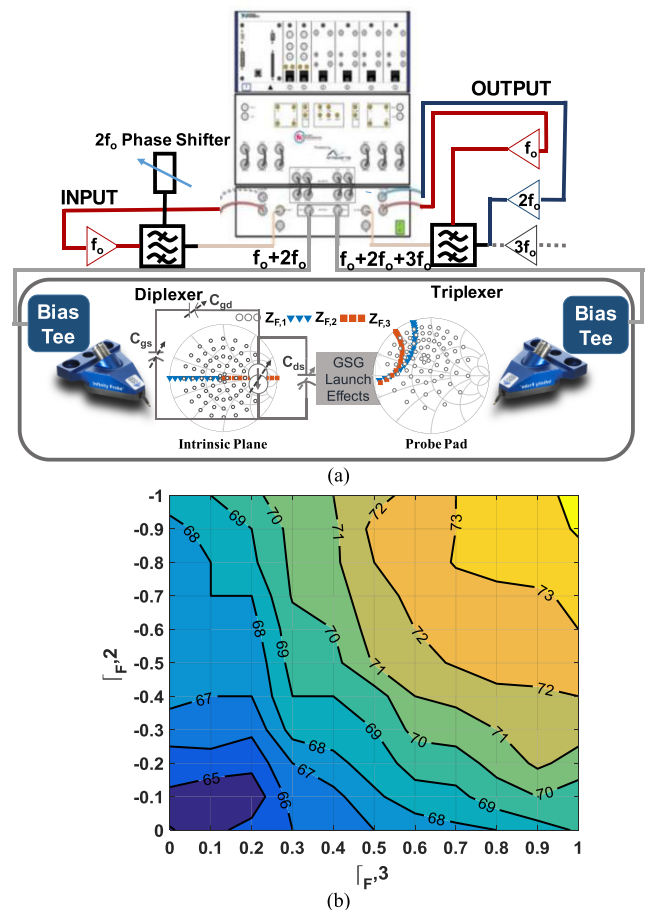
As a result, the second harmonic impedance match is very crucial for controlling the overall efficiency of the integrated Class F PA and is given a higher priority in design over third harmonic.

B. INTEGRATED NOVEL CLASS-F PA TOPOLOGY

This work proposes a novel topology of Class F shown in Fig. 7. This unique topology satisfies the Class F harmonic load terminations up to the third harmonic while maintaining a purely resistive fundamental impedance at the current generator plane of the device. The topology uses the output capacitance (C_{DS}) as part of the output match, i.e. it uses the linear representation of the active cell's output capacitance to resonate with other circuit components in the matching network [25]. This method of C_{DS} resonance is similar to the method used in [26], with the difference being that the proposed method provides a fundamental impedance matching to a purely resistive load, which cannot be achieved using the topology reported [26]. The different resonating blocks, are selected in such a manner that current generator plane sees an almost-ideal short at second, open at third and a real
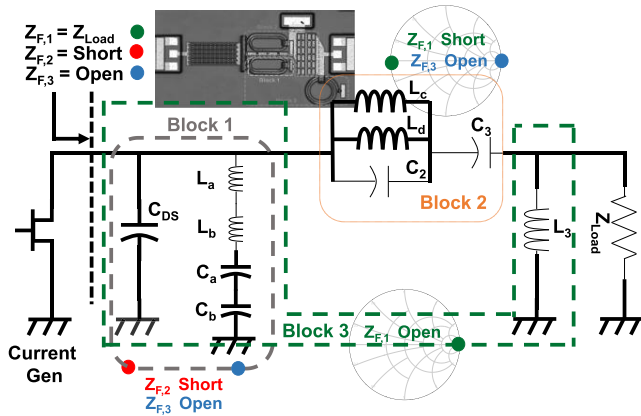
FIGURE 7. Proposed integrated Class-F topology using lumped elements.

fundamental impedance. Although the circuit can be tuned such that the fundamental impedance may reach the real axis, the design equations shown in [26] do not guarantee fundamental impedance at the current source and the impedance transformation. In some instances, the circuit transformation ratio may be less than 1. In our manuscript, a 1:1 impedance transformation ratio exists from the Z_{load} to the current source of the active cell. The topology depicted in Fig. 7 is divided into three major blocks, accounting for fundamental and harmonic resonances. Block 1 creates a short at second and an open resonance at third harmonic, which satisfies Class-F harmonic loading. Block 2 creates a short resonance at fundamental and open resonance at third harmonic. Likewise, Block 3 creates an open circuit resonance at fundamental frequency making a transparent circuity at fundamental frequency thus having a Z_{Load} impedance at current generator plane. Furthermore, any change in fundamental impedance at extrinsic plane does not impact harmonic terminations thereby isolating harmonics and fundamental match which was not possible in previous topologies.

1) FUNDAMENTAL FREQUENCY OPERATION
Referring to Fig. 7, at the fundamental frequency (f_0), components C_2 and L_d resonate to create a high impedance in parallel with component L_c. If L_c and C_3 are also designed to resonate at f_0, a low impedance is generated effectively shorting the two ports of Block 2 leading to relation given by

$$2\pi f_0 = \frac{1}{\sqrt{L_d C_2}}, \quad 2\pi f_0 = \frac{1}{\sqrt{L_c C_3}}, \quad L_2 = \frac{L_c L_d}{L_c + L_d} \quad (23)$$

Components L_a, L_b, and C_a are designed to form a series LC branch that resonates to leave C_b in parallel with C_{DS} and L_3. The three remaining shunt elements, C_{DS}, L_3 and C_b form a parallel LC resonator providing an open shunt impedance as shown in block 3 of Fig.7. This resonance condition can be mathematically derived as a function of f_0 and is given as

$$\frac{1}{\sqrt{L_1 C_a}} = 2\pi f_0, \quad \frac{1}{\sqrt{L_3(C_{DS} + C_b)}} = 2\pi f_0, \ L_1 = L_a + L_b \quad (24)$$

In effect, these resonances allow a 1:1 impedance transformation ratio from Z_{Load} to the current source of the active cell.

2) HARMONIC FREQUENCY OPERATION
At the second harmonic ($2f_0$), the series LC shunt branch of L_a, L_b, C_a, and C_b resonates to create a low impedance path to ground. Block 1 of Fig.7 is shorted, isolating the other elements in the circuit from the FET. Shorting the FET at the second harmonic satisfies the second harmonic $2f_0$ resonance condition and is mathematically formulated as

$$\frac{1}{\sqrt{L_1 C_1}} = 4\pi f_0, \quad C_1 = \frac{C_a C_b}{C_a + C_b} \quad (25)$$

Likewise, at the third harmonic ($3f_0$), capacitor C_2 resonates with the parallel combination of L_c and L_d. This creates a high impedance path between the FET drain and the load. Components L_b, C_a, and C_b form a series LC resonator which then enables a parallel LC resonator between C_{DS} and L_a. When C_{DS} and L_a resonate, a high impedance is realized between the drain and ground. An open circuit loading the drain at third harmonic satisfies the $3f_0$ Class-F harmonic termination and is mathematically given as

$$6\pi f_0 = \frac{1}{\sqrt{L_b C_1}}, \quad 6\pi f_0 = \frac{1}{\sqrt{L_a C_{DS}}}, \quad 6\pi f_0 = \frac{1}{\sqrt{L_2 C_2}} \quad (26)$$

The required resonances put constraints on the various component values and allow for easy closed-form calculation. Equations (22)−(26) can be used to determine five of the six unknown component values; the last component can be selected based upon RF bandwidth and implementation considerations. The five dependent components are determined from the output capacitance of the device (C_{ds}) and the capacitor C_2. The final design equation can be simplified using (27)−(32) as a function of C_{ds} (which is available from device periphery), user selected capacitance C_2 and device radial frequency ($w_o = 2\pi f_0$) as

$$L_1 = \frac{1}{5 C_{ds} w_o^2} \quad (27)$$

$$C_1 = \frac{5}{4} C_{ds} \quad (28)$$

$$L_2 = \frac{1}{9\, C_2 w_o^2} \quad (29)$$

$$C_2 \ \text{independent} \quad (30)$$

$$L_3 = \frac{3}{8\, C_{ds} w_o^2} \quad (31)$$

$$C_3 = 8 C_2 \quad (32)$$

C. INTEGRATED CIRCUIT IMPLEMENTATION AND PA MEASUREMENTS
The integrated Class-F PA was implemented using a 4.8 mm LDMOS die at a frequency of 1.8 GHz (for GSM 1800) using a 28 V LDMOS process. The implementation of the integrated circuit topology presented in section IV (B) has been carried out using two different designs. Design 1 is

Class F full Integrated Circuit (IC) shown in Fig. 7, and design 2 is the partial IC, which are elaborated in detail in section C.1 and C.2, respectively. The small signal and large signal PA measurements are performed using a vector network analyzer with the on-wafer active load-pull system. The characterization of the proposed output matching topology has also been carried out by de-embedding the GSG and device capacitances and is reported in the following sections.

1) DESIGN CASE I: FULLY INTEGRATED CIRCUIT
The fully integrated design uses the process consisting of several layers of metal, metal insulator metal (MIM) capacitor capability, and thick copper top metal. The ground-signal ground metallization has been added to the circuit to allow for an easy on-wafer characterization. An additional bond pad was added between C_2 and C_3 to allow for the drain biasing of the active transistor. To realize the expected termination at the current-source plane of the device, the effects of output capacitance are included in the plots based on estimated linear Cds of the active device technology. The simulated versus measured intrinsic impedances for the integrated Class-F design are shown in Fig. 8(a). As one can infer, the fundamental impedance is at device R_{opt}, second near short and third harmonic is resistive due to substrate losses. The simulation and measured impedance agree quite well which

can be further seen in Fig. 8(a). The intrinsic square voltage with a swing of $2 \times V_{dd}$ and half-sinusoidal current waveforms confirms the Class-F PA operation as seen in Fig. 8(b). For the large signal measurements, the device is biased at a drain supply-voltage of 28 V with a quiescent current of 40 mA. The fully integrated PA using the LDMOS 4.8 mm die exhibits a drain efficiency of 54% with an output power of 36.4 dBm and a gain of 15 dB at 1.8 GHz. As explained in section IV (a), the resistivity of harmonics degrades the achievable efficiency. The on-chip inductor introduces losses which degrade achievable output power and efficiency and its impact is studied using a segmented integrated circuit design.

2) DESIGN CASE II: PARTIAL INTEGRATED CIRCUIT
The design 2 was also implemented according to Fig.7 with the exception that the L_3 component was neglected in design 2. The removal of L_3 in Design 2 results in partial integration of the Class-F impedance matching, and allows for an assessment of its impact on efficiency as compared to Design 1.

The load termination of Designs 1 and 2 share the same harmonic response except at the fundamental frequency due to the lack of L3 shunt inductor in design 2. For PA measurements, the device was biased at a drain supply voltage of 28 V and bias quiescent current of 40 mA. The partial IC was measured at a frequency of 1.8 GHz using on wafer active load pull system. Under this configuration, the Class-F PA exhibits a DE of 61% at an output power level of 5 watts with a gain of 15 dB at 3-dB gain compression as seen in Fig 9 (a). Furthermore, at 5-W output power, design 1 and design 2 show over 30 dBc second harmonic suppression compared to fundamental power. At the third harmonic, harmonic power is isolated over 15 dBc for both design 1 and 2 and is plotted in Fig. 9(b).

The obtained results were also benchmarked against the existing works in high-efficiency harmonic tuned PA design. Not many attempts have been made for integrated Class-F PA design in literature so far. The comparison is reported in Table 1 where the performance of this PA in terms of PAE
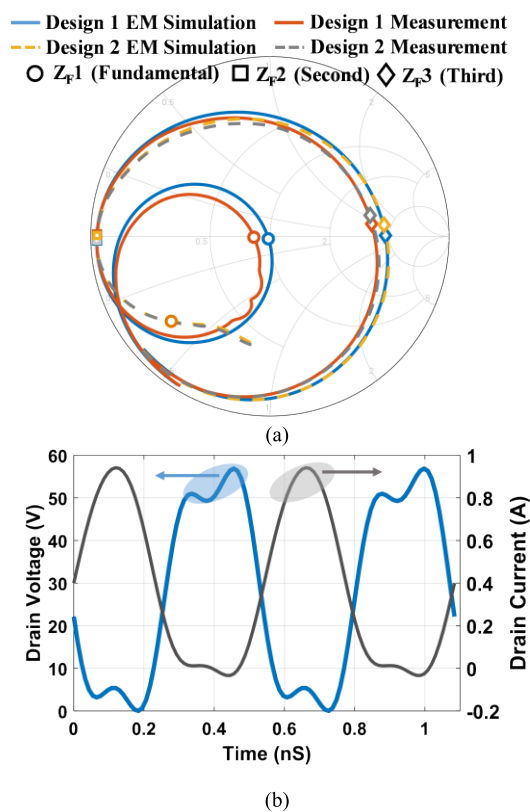
FIGURE 8. Measured s-parameters augmented with estimated output capacitance (b) Drain voltage and current waveforms using larger signal model terminated with measured on wafer output termination.

TABLE 1. Performance comparison with state-of-the-art high-efficiency PAs.

Ref	f (GHz)	P_{out} (W)	DE (%)	PAE (%)	FE (%)	Class
[27]	2.6	0.5	58	50.36	64	J (GaN)
[28]	6	3.4	31	26	40.8	CSCG (GaN)
[29]	2.4	0.1	38	34.2	42.5	F (SiGe)
[30]	2.4	0.15	44	NA	NA	F (CMOS)
[31]	1.2	0.29	49	48	50.2	F (CMOS)
[32]	3.8	1.38	24.3	18	25	AB (LDMOS)
	3.9	2.2	10.5	9.17	13	
[33]	1.9	0.2	55	43	50.4	F (CMOS)
This Work	1.8	5	54	52.2	61	Design 1 (LDMOS)
		5	61	60	69	Design 2 (LDMOS)

f: Frequency, DE: drain efficiency, P_{out}: output power, PAE: Power added efficiency, FE: frequency weighted efficiency $(GHz)^{0.25}$ x PAE.
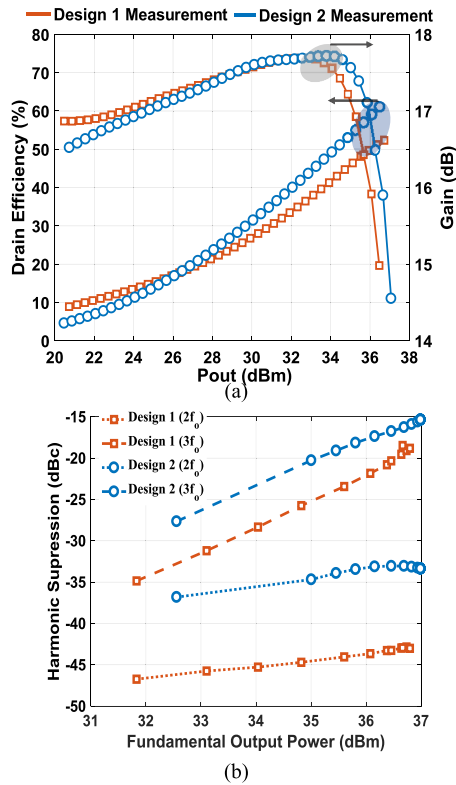
FIGURE 9. Measured gain and DE versus output power at a frequency of 1.8 GHz. (b) Class F harmonic suppression in dBc relative to fundamental output power.

and frequency weighted efficiency is among the very best of different technologies including LDMOS, SiGe, CMOS, and GaN.

V. CONCLUSIONS

In this paper, a detailed analysis of the impact of resistive harmonics and their combination on the design of Class-F power amplifiers was presented. A novel Class-F integrated topology was then introduced. The proposed output match absorbs the active devices' output capacitance thereby allowing for harmonic short and open circuit conditions at the current source reference plane. In addition, the topology maintains a purely resistive termination at the fundamental frequency. To support 5G miniaturization activities and to enable compact m-MIMO transmitter systems, two Class F PA prototypes were fabricated and tested. At 1.8 GHz, using NXP 5mm LDMOS die, the fabricated Class-F PAs achieve a frequency weighted efficiency of 61 % and 69% at 5 W output power under full integration and partial integration, respectively.

ACKNOWLEDGMENT

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