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Differential Phase Measurement Accuracy of a Monobit Receiver

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ABSTRACT Differential phase measurements using two receiver channels are used to calculate the angle of arrival of a target signal. A monobit receiver architecture is a desirable receiver type due to its low hardware complexity, sampling rate, and power efficiency. The application motivating this paper benefits from the use of automatic gain control circuitry and sensitivity offered by the monobit architecture. However, the one-bit sampling of the input signal introduces undesirable non-linear effects. This paper analyzes the effects of a monobit receiver architecture on the differential phase accuracy. Simulated results are compared to measurement data collected from prototype monobit receiver hardware. The measured data had good agreement with the simulated results. At a high-input signal-to-noise ratio of 30 dB, the differential phase measurement sigma was approximately 0.66° for input phase shifts of 0°, 45°, and 90°. While the differential phase measurement accuracy is less than predicted by the Cramer–Rao lower bound, it is sufficient for the low cost, power, and size constrained sensor application motivating this paper.

INDEX TERMS Monobit ADC, signal processing, radar, receiver, phase.

I. INTRODUCTION

Radar sensors have traditionally been applied to applications such as defense, weather monitoring, air traffic control and satellite imaging. The nature of these applications have afforded complex and costly solutions to meet the required radar sensor performance. Advances in technology have enabled the development of low cost high performance microwave and electronic integrated circuits (ICs) that have encouraged development of radar sensors for low cost portable applications. Even with advances in microwave and electronic integrated circuit technology analog-to-digital converters are a limiter to system power efficiency and overall system complexity [1]. The pairing of a digital monobit receiver architecture is a desirable solution for applications that have cost, size/volume and power limitations such as those found in consumer, portable and space/airborne systems [2]. The concept of a monobit receiver has application to GPS [3], ultra-wideband (UWB) systems [4], communications [5], electronic warfare [2], [6], and radar [7]. The digital instantaneous frequency measurement (IFM) receiver is used to measure a received signal [8], [9]. Monobit sampling can be paired with an IFM core to make frequency and chirp rate measurements of a received signal as described in [10].

The majority of the published literature found on the monobit receiver architecture focuses on the effects of the quantization on the output frequency spectrum. The following discussion examines the magnitude, but also extends the analysis to a consideration of the phase, particularly the effects on the measurement of phase between two monobit receiver channels. In the notional RF sensor the measurement of the differential phase between two channels is used to calculate the direction of arrival of a signal. A sinusoidal tone was selected as the signal of interest to provide a straightforward interpretation of the differential phase accuracy.

The advantages of a monobit receiver are due to its simplicity. Limiting RF amplifiers and high speed comparators form the basic building blocks of the monobit receiver. These simple microwave and electronic components can operate at extremely high rates and in high input signal power environments.

A monobit architecture provides system simplicity and power efficiency to an RF receiver. It also provides system flexibility when paired with a modern field programmable gate array (FPGA) used for the digital signal processing. However, the monobit receiver is not without drawbacks, it has inherently low dynamic range due the single bit sampling and as a result has difficulty processing strong and weak signals simultaneously [11]. The low dynamic range of the monobit receiver does not always make it suitable as a replacement for a digital channelized receiver approach [11]. However, in specialized applications where a dominant strong signal is of interest or applications where the elimination of

complex automatic gain control mechanisms is necessary the monobit receiver architecture is a suitable solution [11], [12].

The work discussed in this paper is motivated by an interest in using a monobit receiver architecture for a power constrained and size limited application that requires differential phase measurements in addition to measuring the signal frequency. The application requires the RF sensor to measure the direction to an RF beacon transmitting a continuous wave signal with a high signal-to-noise ratio (SNR). A two channel digital monobit receiver was selected for the application due to the low hardware complexity and signal measurement performance.

In the sections that follow a low complexity digital monobit receiver containing two channels for measuring the differential phase of received signals is examined. Other estimation techniques of the phase of a sinusoid and time delay exploiting monobit approaches include those using multiple antenna beams [11] and signal correlation and coherence techniques [13], [14] were considered.

The research discussed clearly demonstrates a prototype monobit receiver can be constructed that is capable of providing highly accurate differential phase measurements that can be used for a direction finding. The nonlinear behavior of the simulated monobit receiver accurately reflects the prototype hardware and can be used to predict its performance.

The approach that is used in this work to evaluate the monobit receiver is to examine a simulation of an ideal architecture and compare performance to an un-quantized system. Measurements from a prototype monobit receiver are also presented and compared with the modeled receiver. The effects of the 1-bit quantization on the magnitude and phase of the sample signal are examined with regard to the input signal-to-noise, frequency and quantization of the signal.

II. BACKGROUND

A simplified monobit receiver is shown in Fig. 1. The input signal (s(t)), and Gaussian noise (n(t)) are combined to form the signal x(t) which is then passed through a hard limiter. The hard limiter performs the sampling and quantization of the signal.

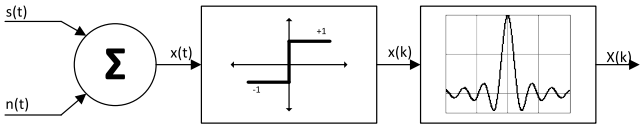

FIGURE 1. Monobit Receiver Architecture.

The signal, x(k), output from the hard limiter is a stream of -1 and $+1$ values that encode the signal. The encoded signal is then passed through a narrow band filter to form X(k). The simplified monobit receiver shown in Fig. 1 does not show an analog prefilter that would be necessary in a practical realization to limit strong out of band interference.

The architecture in Fig. 1 is used in [15] and [16] to examine the effect of a hard limiter followed by a narrowband analog filter on the SNR. The previous work discussed in [15] and [16] focused on the analog processing of hard limited signals. The implementation of Fig. 1 discussed in this work passes the output of the hard limiter, x(k), through a filter bank of narrowband digital filters in the form of a Fast Fourier Transform (FFT).

Utilizing FFT processing of the time domain samples provides sufficient sensitivity and dynamic range in both under sampling [7] and over sampling [4] monobit digital receiver applications. The monobit architecture analyzed and discussed in this paper is modified slightly from the architecture discussed in [3], specifically the kernel used to calculate the FFT is not limited to a one-bit kernel. The increase in the complexity of the kernel function provides improved performance to the digital monobit receiver and was proposed as a possible improvement in [3]. A multi-bit FFT kernel can be implemented in modern field programmable gate arrays (FPGAs) without an excessive burden on its resources [17], [18]. It is also important to note that the concept of oversampling the input signal by the one-bit analog-to-digital converter as discussed in [4], [5], [19], and [20] is utilized in this analysis.

The monobit receiver architecture introduces nonlinear effects through the hard limiter that make it difficult to perform a theoretical performance analysis [21]. However, even with the undesired non-linear effect introduced, research has been conducted to analyze the performance loss of a monobit architecture versus a multi-bit quantizer [22]. Studies such as [23] show that in low signal-to-noise (SNR) conditions the performance loss of the monobit quantizer is approximately 2 dB less than an ideal quantizer. It has also been shown that by oversampling a signal the performance loss due to the single bit quantization can be improved [19].

Much research has been conducted on the development of specialized integrated circuits for the implementation of digital monobit receivers [7], [24], [25]. The system model developed and discussed in this paper is used to evaluate the performance of a digital monobit receiver that is targeted for implementation on an FPGA, which offer flexible, high performance processing options for digital channelized receivers [18].

The sections that follow examine the effects of the monobit sampling approach on the SNR to verify the behavior of the proposed system. The impact of the digital monobit receiver architecture on the phase accuracy versus input SNR, frequency and quantization is considered. Measurement data from a hardware implementation are provided that support the results obtained from the simulated receiver model.

The digital monobit receiver system analyzed in this paper is shown in Fig. 1. It consists of a hard limiter followed by a bank of narrow band filters implemented by a FFT. The output of the FFT of a complete real-time receiver would likely be processed using a threshold and peak search algorithm to locate any spectral peaks which would then be used to estimate parameters of the received signal. In both the simulated monobit receiver analysis of section three and measurement data analysis in section four of this paper the frequency bin of the input signal is known and a thresholding and peak search

algorithm is not required to identify the spectral peaks. The placement of the signal in a known bin was done to simplify the analysis discussed here. In an actual implementation of a sensor a signal detection and peak finding algorithm would be employed at the output of the FFT to dynamically identify signals throughout the operating frequency band for processing. Identifying the FFT bin the signal peak falls in should provide sufficient accuracy for measuring the differential phase of the input.

The discussion and results that follow were generated using a moderately sized FFT of 1024 points. The number of FFT points have been found to impact the performance of the digital monobit receiver [2]. A high input SNR of 30 dB is used to generate the signals and corresponding figures unless otherwise noted by the x-axis of the plot. A SNR of 30 dB was chosen based upon the simulation results to give consistent behavior between the fundamental and harmonic signals output from the monobit receiver. The analysis of the simulated monobit receiver presented in section three utilizes a 0 dBm input signal, and the noise is scaled appropriately to obtain the desired input signal-to-noise. The measurement data discussed in section four achieves the desired input signal-to-noise by scaling the input signal level rather than the noise. The noise level of the RF signal generator and noise figure of the RF frontend of the prototype monobit receiver were used along with the signal generator output power level to calculate the input SNR for the data collection. The sampling frequency used to process the data throughout the analysis is 1200 MHz and the sampling frequency was chosen to oversample the input signal. The frequency of the continuous wave (CW) sinusoidal tone is placed at the center of bin 120 of the output FFT.

The modeled and hardware implementations of the digital monobit receiver discussed in this paper both consist of two identical channels of the form shown in Fig. 1. One of the channels is used as a reference channel, and the other channel is used to measure the phase shift applied to the signal. The complex output of the FFT bin containing the input signal in both the reference and phase shifted channel is used to compute the differential phase of the signal.

A. SIGNAL MODEL

The signal input to the receiver is of the form,

$$s(t) = A \cdot cos(2\pi ft + \phi). \tag{1}$$

Where s(t) is the real portion of a continuous time complex signal with amplitude A in volts, frequency f in Hertz and phase offset of φ in radians. Zero mean white Gaussian noise is added to the signal to form the input to the monobit receiver and scaled to the appropriate SNR. Equation (2),

$$x(t) = s(t) + n(t), \tag{2}$$

gives the expression for the real portion of the signal plus noise.

The sign of x(t) is used to form the monobit samples,

$$x(k) = sign\{x(t)\} \tag{3}$$

Where, x(k) represent the hard limited samples output from a comparator of the time domain signal, x(t). A threshold of zero is used and all inputs above zero result in a $+1$, all inputs below 0 result in a -1, providing the monobit quantization of the signal.

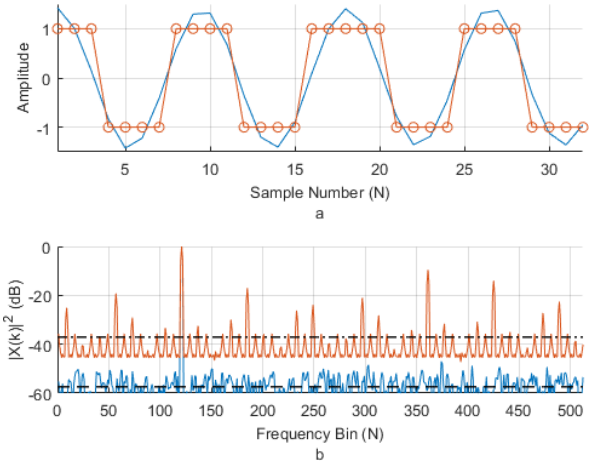

FIGURE 2. Simulated monobit receiver 30 dB SNR input and output signals (a) time domain input (b) Frequency Domain.

Fig. 2a shows a time domain representation of the input signal plus noise (blue) and a 1-bit quantized version of the signal plus noise (red). The FFT of the monobit bipolar signal, x(k), is calculated and shown in Fig. 2b. Fig. 2b contains the output of the FFT for the un-quantized signal plus noise (blue) and the monobit quantized signal (red).

The spectra of signals plotted in Fig. 2b illustrates the effects of the monobit sampling on the signal at high input signal to noise ratios ($+30$ dB). The FFT provides integration gain of $10log_{10}\left(\frac{N_{fft}}{2}\right)$, which in this case is 27 dB. The noise floor of both the monobit sampled signal plus noise (red) and the un-quantized signal plus noise (blue) are plotted as black dashed lines. The integration gain along with the input SNR of $+30$ dB result in the $+57$ dB of SNR observed in the blue trace of Fig. 2b. The introduction of additional signal harmonic components is clearly observable in the plot of the monobit FFT output (red). The increase in the noise floor of the 1-bit quantized signal above the noise floor level of the un-quantized signal is referred to as the excess noise floor. With the high SNR input shown in Fig. 2b the excess noise floor is approximately $+20$ dB.

Fig. 3 contains the time domain input and FFT output for a 0 dB SNR (Fig. 3a and Fig. 3c, respectively) and -10 dB SNR input (Fig. 3b and Fig. 3d, respectively). These plots are shown to illustrate the behavior of the output of the monobit receiver FFT at moderate and low SNR inputs. In the 0 dB SNR input case of Fig. 3a and Fig. 3c both the un-quantized and 1-bit quantized signals have approximately the same SNR of $+27$ dB. In this case the peak of the fundamental signal is clearly distinguishable for both the un-quantized and 1-bit quantized signals. The SNR of the FFT output is minimally degraded by the excess noise floor. The -10 dB

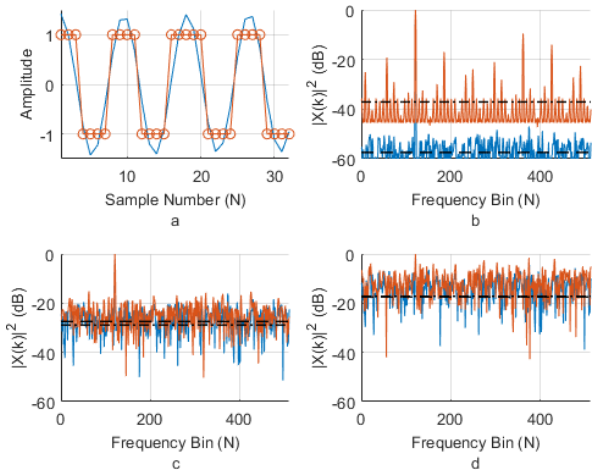

FIGURE 3. Simulated monobit receiver input and FFT ouput (a) 0 dB SNR time domain input, (b) −10 dB SNR time domain signal (c) 0 dB SNR FFT output, (d) −10 dB SNR FFT output.

SNR input shown in Fig. 3b and Fig. 3d. At this input SNR level the fundamental has become more difficult to identify from other noise spikes in the FFT output. The behavior of the un-quantized and 1-bit quantized signals show the same behavior, with no indication of any effect due to the excess noise floor. The three signal input cases illustrate that the impact of the excess noise floor varies with the input SNR.

Table 1 contains the fundamental peak along with the first three harmonics. The third harmonic is approximately −9.5 dBc below the normalized fundamental peak frequency as predicted in [2] and [6].

TABLE 1. FFT spectrum peaks of interest.

	Frequency (MHz)	Folded Frequency (MHz)	FFT Bin (N)	Mag (dBc)
Fundamental	140.625	-	120	-
3rd Harmonic	421.875	-	360	-9.5
5th Harmonic	703.125	496.875	424	-14.0
7th Harmonic	984.375	215.625	184	-17.0

The complex values of the FFT, (X(k)) are used to compute the phase, $(\varphi_{X(k)})$ of the signal using the expression,

$$\varphi_{X(k)} = \tan^{-1}\left\{\frac{Im\{X(k)\}}{Re\{X(k)\}}\right\}. \tag{4}$$

As an example, the complex values of the fundamental peak, bin 120, shown in Fig. 2b are used to calculate the absolute phase of the fundamental signal in each channel using (4). Then the differential or delta phase between channels is calculated using the expression,

$$\Delta\varphi_{21} = \varphi_{X2(k)} - \varphi_{X1(k)}. \tag{5}$$

Where, $\varphi_{X2(k)}$ is the absolute phase of the fundamental frequency in Channel 2, $\varphi_{X1(k)}$ is the absolute phase of the fundamental frequency of Channel 1 and $\Delta\varphi_{21}$ represents the differential or delta phase between the two channels.

B. DIFFERENTIAL PHASE MEASUREMENT ACCURACY

The Cramer- Rao Lower Bound (CRLB) represents the best case theoretical limit of the differential phase measurement (sigma) as a function of the input SNR. The expression for the CRLB for the estimation of phase in a long baseline interferometer is derived in [26] and is given by

$$CRLB = \frac{1}{2N}\left(\frac{1}{SNR_1} + \frac{1}{SNR_2}\right). \tag{6}$$

In this expression, N is the number of samples, SNR1 is the signal-to-noise ratio at the input of receiver channel 1 and SNR2 is the signal to noise ratio at the input of receiver channel 2. In the system considered here, the SNR inputs are similar, therefore it is assumed SNR1 = SNR2,

$$CRLB = \frac{1}{N}\left(\frac{1}{SNR}\right). \tag{7}$$

Substituting the number of FFT points, N_{fft} used to calculate the phase of the signal in each channel into (7) and taking the square root to obtain sigma results in

$$\sigma = \sqrt{\frac{1}{N_{fft} * SNR}}. \tag{8}$$

Where, σ represents the differential phase measurement accuracy, SNR is the input SNR and N_{fft} is the number of points in the FFT computation.

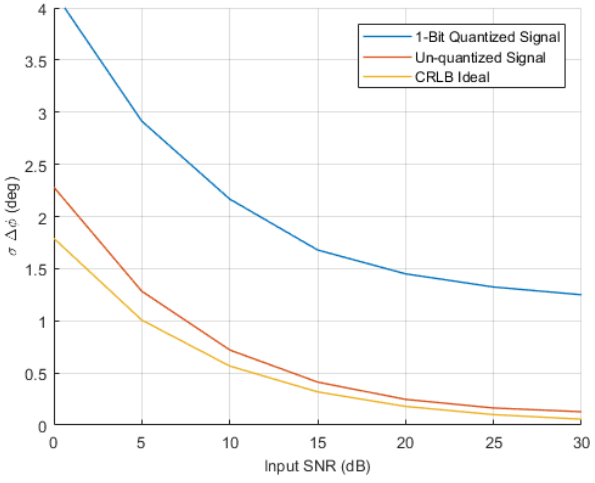

FIGURE 4. Simulated monobit receiver differential phase measurement accuracy (CRLB) versus input signal-to-noise.

Fig. 4 contains a plot of the differential phase measurement accuracy simulated for the 1-bit quantized and un-quantized signals along with the CRLB given in (8). In order to generate the curves of Fig. 4 the input SNR was swept over the range of 0 to 30 dB, in 5 dB steps. At each input SNR a sinusoidal tone with a phase shift of 45° between channels was swept through all of the frequency bins of the FFT. The variance of the differential phase error between the channels was then calculated.

The simulated 1-bit quantized signal (blue), has a sigma that is approximately 4 degrees at 0 dB SNR and converges

to a measurement accuracy of approximately 1.25 degrees at 30 dB SNR in Fig. 4. The simulated un-quantized signal (red) has a sigma of approximately 2.25 degrees at 0 dB input SNR and approaches a measurement floor of 0.2 degrees 30 dB input SNR. The theoretical CRLB predicts a sigma of approximately 1.75 degrees for an input SNR of 0 dB that converges to a value of approximately 0.1 at 30 dB of input SNR. The differential phase measurement accuracy of the 1-bit quantized signal (blue) is significantly less than the measurement accuracy predicted by the CRLB (yellow) computed using (8) and the differential phase measurement accuracy for the un-quantized signal (red). The differential phase measurement accuracy of the un-quantized signal shows good agreement with the theoretical CRLB calculation. Both of the simulated results have a similar shape as the theoretical CRLB and have greater values of sigma (less measurement accuracy) than predicted by the CRLB as expected.

The measurement floor to which the 1-bit quantized signal converges to is attributed to the excess noise introduced by the 1-bit sampling process. Fig. 5 shows the simulated behavior of the fundamental signal, third harmonic and excess noise floor for a signal in bin 120. Fig. 5 provides insight into the behavior of the differential phase measurement sigma shown in Fig. 4. In the 1-bit quantized case as SNR is increased, the excess noise floor introduced by the 1-bit sampling increases. This additional noise offsets the additional signal input resulting in the measurement floor that is observed in the modeled receiver output.

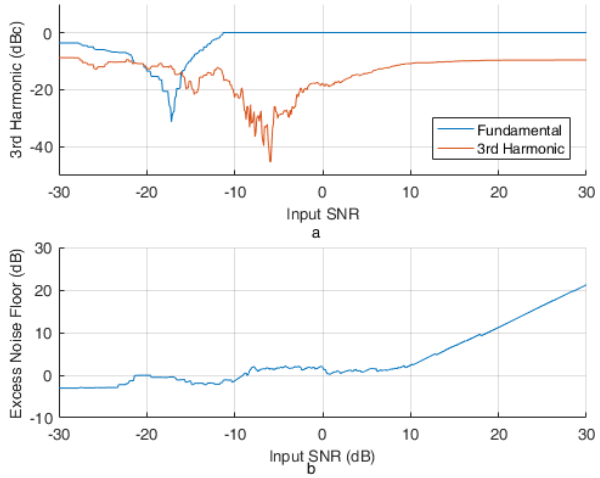

FIGURE 5. Simulated monobit receiver response to input signal-to-noise (a) fundamental and third harmonic, (b) excess noise floor.

C. DIFFERENTIAL PHASE MEASUREMENT ACCURACY VS INPUT SIGNAL PHASE SHIFT

The differential phase between two simulated monobit receiver channels was calculated at a constant input SNR (+30 dB) over the frequency range 0 to $\frac{f_s}{2}$ for phase shifts of 0°, 22.5°, 45°, 67.5° and 90°. The results of these calculations are shown in Fig. 6. The red trace represents the differential phase calculated for an un-quantized signal and

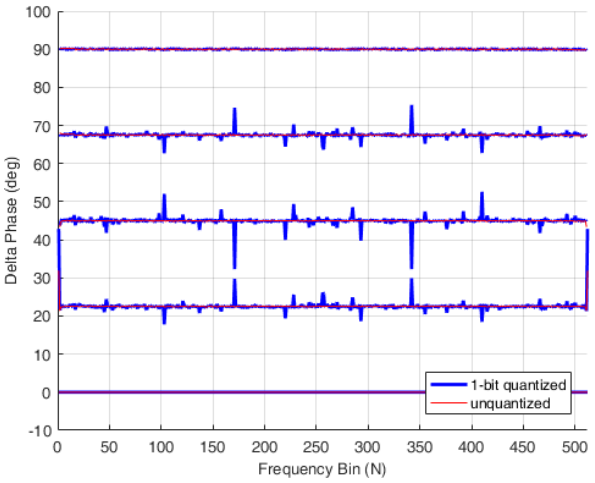

FIGURE 6. Simulated monobit receiver fundamental frequency input effect on differential phase measurement.

the blue trace represents the 1-bit quantized signal. The plot shows variation in the differential phase with frequency bin. Symmetry observed about bin number 256 in the differential phase data shown in Fig. 6. The differential phase data shown in Fig. 6 indicates that the delta phase variation is at a minimum at 0 degrees of phase shift between signals. As the phase shift increases to 45° the error increases to a maximum. As the phase shift is increased beyond 45° the differential phase measurement variation decreases toward a minimum at a phase shift of 90°. The variation in the phase measurement is due to perturbations in the SNR by the folding of the undesired sampling products introduced by the 1-bit sampling. The phase shift applied to the input signal changes how these products constructively and destructively add during the delta phase computation.

III. MEASURED PERFORMANCE

In order to evaluate the utility and performance of a monobit architecture receiver, a prototype circuit was designed and fabricated. The prototype architecture has two receiver channels. Each receiver channel consists of an RF frontend that amplifies, filters and down converts an S-band input RF of 3.250 GHz to an IF of 140 MHz. The IF output is then oversampled at 1200 MHz using a high speed comparator as a 1-bit analog-to-digital converter. The comparator output is intended to be input to a signal processor implemented in an FPGA. Any phase errors introduced by differences in the amplifiers, filters and mixers of each receive channel are not calibrated out in this analysis.

In order to inform the future development of the FPGA signal processing, the monobit output of the comparator was captured using a high speed oscilloscope and processed using MATLAB in order to evaluate the performance of the prototype hardware and verify the monobit receiver performance that was predicted in the simulation. A single, fixed frequency sinusoidal tone in bin 120 was used as the input signal to each receiver channel for generating the data set. A phase shift of

0°, 45° and 90°, (units of electrical degrees) was applied to the signal input to each channel. The input SNR was also varied from −30 dB to +30 dB in 10 dB steps. At each input SNR and phase shift a data set of 102400 samples were collected. The samples were then processed into 100 measurements using the FFT. The experiment has been repeated more than ten times. The results from these repeated trials were stable, within the expected noise of the measurement setup.

The measurement setup used to collect data from the prototype monobit receiver is shown in Fig. 7.

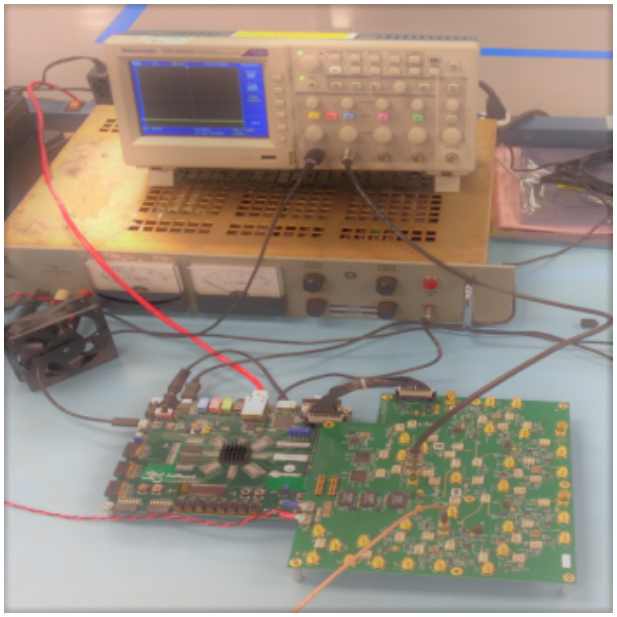

FIGURE 7. Prototype monobit receiver measurement setup.

A. CHANNEL MAGNITUDE MEASUREMENTS

Fig. 8 and Fig. 9 contain data collected from the prototype monobit receiver at low input SNR (−6 dB) and high input SNR (+33 dB), respectively. Monobit data was collected from the two receiver channels and FFT processed. One of the FFT calculations for channel 1 (blue) and channel 2 (red) are shown in Fig. 8 and Fig. 9. Subplots (a), (b), (c) and (d) of Fig. 8 and Fig. 9 contain the FFT output for no signal inputs, and signal inputs with phase shifts of 0, 45 and 90 electrical degrees, respectively. The expression given in (4) is used to calculate the phase of the peak in bin 120 of each channel. Once the phase information of the individual channels was calculated the differential phase was computed using (5).

Fig. 8a contains a plot of the FFT output with no RF input signal. The plot has the distinctive shape due to the input IF filter. Channels 1 and 2 are not phase shifted with respect to one another in the noise only input case. Fig. 8b, c and d show the expected normalized fundamental frequency occurring in bin 120. The FFT output has an expected SNR of +21 dB, (−6 dB input SNR + 27 dB FFT integration gain). The third harmonic component is located in bin 360 of the FFT and is at a level of approximately −20 dBc. The monbit

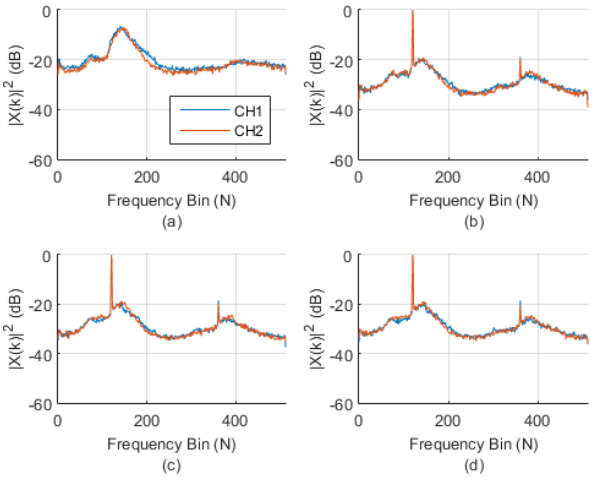

FIGURE 8. Measured monobit receiver output at −6 dB SNR Input (a) Noise Only Input (b) 0° phase shift (c) 45° phase shift (d) 90° phase shift.

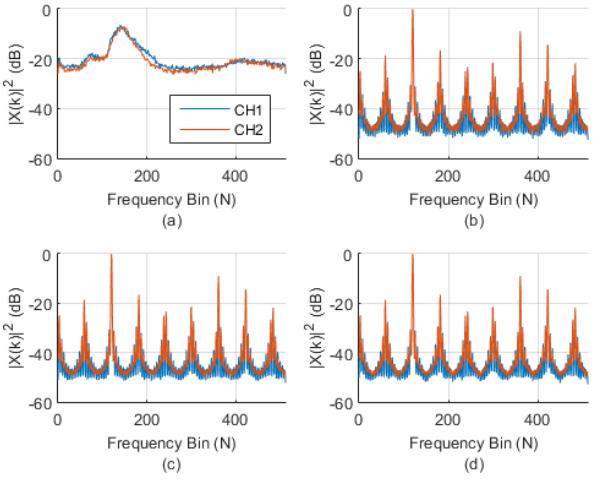

FIGURE 9. Measured monobit receiver output at +33 dB SNR Input (a) Noise Only Input (b) 0° phase shift (c) 45° phase shift (d) 90° phase shift.

data a low input SNR (−6 dB) contains the expected signal (bin 120) and third harmonic (bin 360) but does not contain other undesired sampling harmonics. The third harmonic is examined because of the limitations it places on the dynamic range of the monobit receiver.

Fig. 9a contains a plot of the FFT output with no RF input signal. The plot of Fig. 9a shows the same behavior as the noise only input case in Fig. 8a, as expected. The plot in Fig. 9a shows the distinctive shape of the input IF filter. Channels 1 and 2 are not shifted with respect to one another in the noise only input case. Fig. 9b, c and d show the expected normalized fundamental frequency occurring in bin 120. The plots of Fig. 9 show a similar behavior to the simulated monobit receiver output in Fig. 2. The magnitude of the harmonic peaks to the fundamental peak show the same ratio. The third harmonic component is located in bin 360 of the FFT. In addition to the third harmonic that was observed

in Fig. 8, additional harmonic components and folded sampling artifacts due to the 1-bit quantization of the signal are clearly observable in the FFT output.

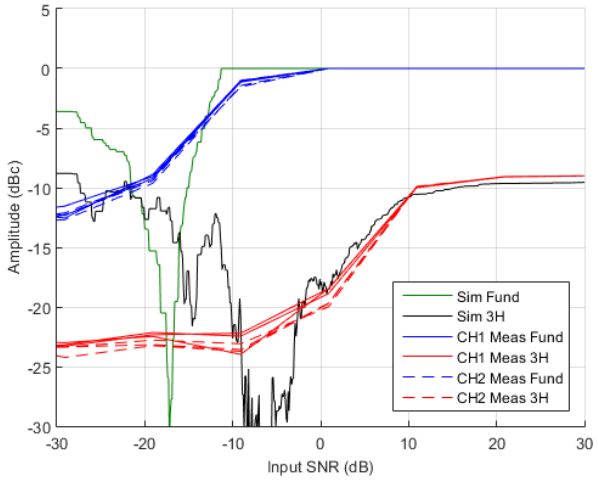

FIGURE 10. Measured and simulated monobit receiver fundamental and third harmonic versus input signal-to-noise.

The fundamental and third harmonic peaks, located in FFT bins 120 and 360 respectively, were calculated using the complex values extracted from each channel of the data set for each phase shift and input signal-to-noise ratio level. The mean of the measurement peaks at each input condition was taken and used to plot Fig. 10. The color in the plot is used to identify the signal and harmonic, blue and red respectively. The solid lines indicate the data is collected from channel 1, while the dashed lines indicates the data is collected from channel 2. The solid green and black lines represent the fundamental and third harmonic signal predicted by the simulated monobit receiver.

The plots in Fig. 10 show that the fundamental signal in bin 120 begins to become apparent at an input of −10 dB SNR and has become the dominant peak by 0 dB input SNR. The observation is also supported by the spectrum plots shown in Fig. 8. Fig. 10 also shows that the third harmonic has reached a constant magnitude of −10 dBc once the input SNR reaches +10 dB. The limited dynamic range of the monobit receiver is also apparent in both the simulated and measured data of Fig. 10.

The measured data shown in Fig. 10 shows good agreement between channels and with the simulated data. The maximum difference (delta) between the measured peak data in each channel is summarized in Table 2. The results in Table 2 show less than one dB of variation of the signal located in bin 120 (peak location) data across the range of input SNR and phase shifts. The largest variation occurs at low input SNR, −30 dB in this case, as expected.

The peak and third harmonic measurement data have a generally similar shape to that of the simulated monobit receiver. The agreement is apparent at higher input SNR. At low input SNR there is a greater difference between the simulated and the measured monobit receiver performance.

TABLE 2. Channel Variation of Measured Peak Data.

Channel	Delta (dB)	Input SNR (dB)	Max (dB)	Min (dB)
CH1	0.94	-30	-11.54	-12.53
CH2	0.56	-30	-12.12	-12.68

The difference is due to differences in behavior/distribution of the noise in the simulation versus the prototype hardware. One difference that exists between the simulated and prototype receivers is the IF filter. It is likely that a more accurate representation of the analog IF filter would result in better agreement between the simulated and prototype hardware at low input SNR.

B. CHANNEL NOISE MEASUREMENTS

Fig. 11 contains a plot of the noise power calculated for the simulated and prototype receiver. The noise power for the simulated receiver (red) shows good agreement, in both shape and the magnitude with the noise power of the measurements collected from the prototype (blue). The measured noise power shown in the blue traces of Fig. 11 was computed for the measurements collected in both receiver channels and phase shifts. The data shown in the plots indicate that the noise power in the measurement is not effected by changes in the phase shift applied to the input signals.

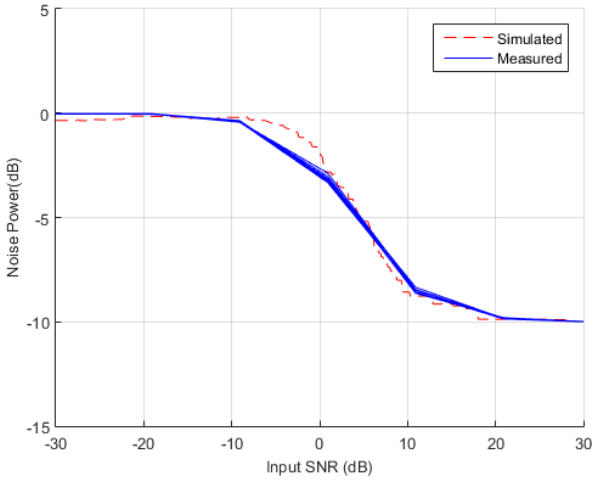

FIGURE 11. Measured and simulated monobit receiver noise power.

C. CHANNEL PHASE MEASUREMENTS

The phase of the peak signal located in bin 120 was calculated using (4) with the complex values extracted from the data set for each channel, input SNR and input phase shift. The analysis of the phase measurement considers only the desired signal in bin 120. Fig. 12 shows the mean phase measured in channel 1 (solid) and channel 2 (dashed) for each of the phase shifts and SNR inputs. The data shows that an input SNR level of −10 dB is necessary to obtain a constant measurement for

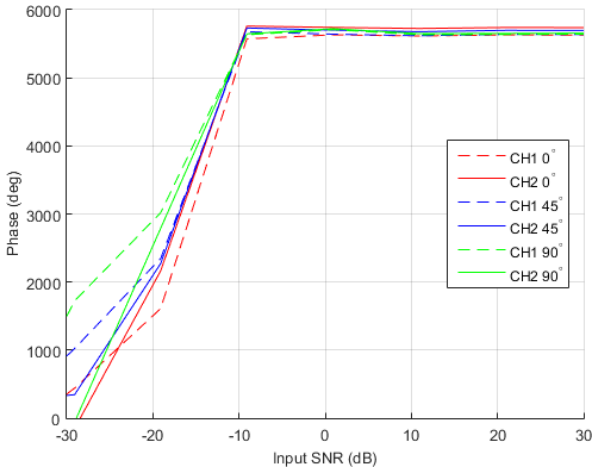

FIGURE 12. Measured monobit receiver channel 1 and channel 2 phase measurements for 0°, 45° and 90° input phase shifts.

increasing input SNR. The data for the fundamental signal in bin 120 in Fig. 10, shows that −10 dB input SNR is where the signal in bin 120 begins to become one of the dominant peaks in the FFT.

D. DIFFERENTIAL PHASE MEASUREMENTS

The differential phase is computed using expression (5) with the phase data from each channel used to generate the plots in Fig. 12. The resulting differential phase is plotted in Fig. 11. The figure contains the differential phase measurement as a function of input SNR from 0 dB to +30 dB. The measurements of the input signal phase shifts of 0°, 45° and 90° are shown in the blue, red and yellow traces of Fig. 13.

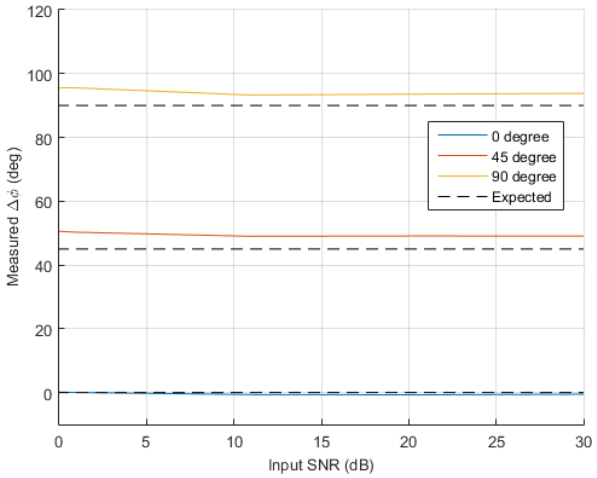

FIGURE 13. Measured monobit receiver differential phase vs input SNR for input phase shifts of 0°, 45° and 90°.

The measured differential phase for the 45° and 90° inputs contain a fixed bias of approximately 5°. The 0° degree measurement does not contain the bias. Characterization of the test setup has shown that this bias is associated with a mechanical phase shifter used to apply the phase shift into channel 2.

TABLE 3. Differential Phase Measurement Statistics.

	Max	Min	Mean	Sigma	Sigma^2
0°	1.07	-0.76	-0.32	0.58	0.33
45°	53.49	48.97	49.75	1.46	2.12
90°	95.54	93.30	94.12	0.80	0.64

Table 3 contains the maximum, minimum, mean, sigma (standard deviation) and sigma^2 (variance) of the data shown in Fig. 13. These metrics were computed in order to assess how well the differential phase behaves across the range of input SNR. The sigma values in column four of Table 3 shows the measurement accuracy of the prototype monobit receiver is worst at an input phase shift of 45°, which is the behavior predicted by the simulation and plotted in Fig. 6.

The absolute delta phase measurement error is plotted in Fig. 14. The absolute error was calculated by taking the absolute value of the desired delta phase (0°, 45°, 90° respectively) minus the mean delta phase shown in Fig. 13. The resulting plot in Fig. 14 shows the error between the desired differential phase and the measured differential phase. The 45° and 90° degree phase shifts appear to have a constant bias with respect to the input SNR. The 0° differential phase measurements have a slight improvement with increasing input signal-to-noise.

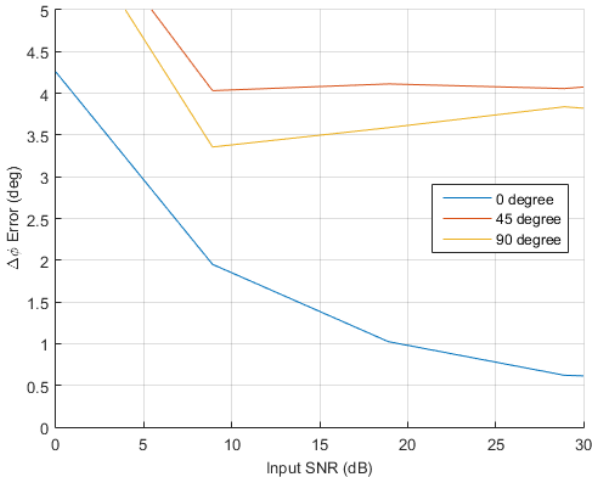

FIGURE 14. Measured monobit receiver Absolute Differential Phase Measurement Error vs input SNR for input phase shifts of 0°, 45° and 90°.

The behavior of the differential measurements at each input SNR is also considered. The standard deviation of the differential phase measurements used to generate the data points shown in Fig. 13 is plotted in Fig. 15.

The plot shown in Fig. 15 contains the sigma calculated for the 0°, 45° and 90° (blue, red and yellow traces, respectively) differential phase shifts as a function of input SNR. Along with the measured prototype monobit receiver data, the theoretical CRLB given by (8) is plotted as a red dashed line.

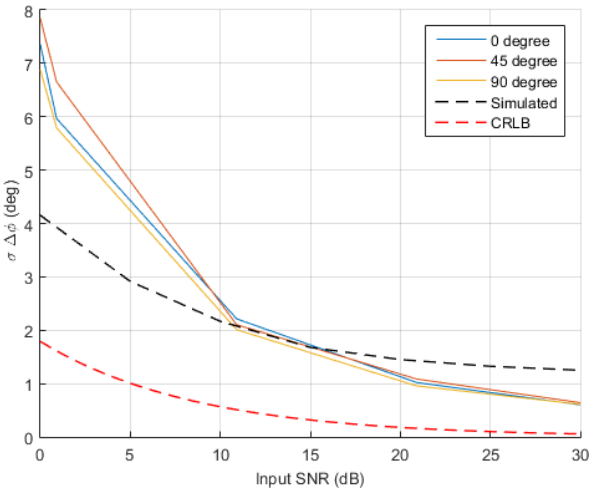

FIGURE 15. Measured monobit receiver differential phase sigma vs input SNR for input phase shifts of 0°, 45° and 90°.

The sigma calculated using the simulation of the monobit receiver is also shown as the black dashed line in Fig. 15.

The plot of the measurement accuracy of the measured data in Fig. 15 has a similar shape to the measurement accuracy curves of the CRLB and the monobit receiver simulation. In general the performance of measurements are expected to approach but may not realize the actual performance predicted by the theoretical CRLB due to error effects. In this case, there are additional noise error effects and nonlinearities introduced by the monobit sampling process that are not accounted for in the CRLB for the long baseline interferometer that result in performance degradation. The degradation of performance is translated into the shift up of the theoretical measurement accuracy performance predicted by the CRLB and observed in the plot of Fig. 15.

The accuracy of the measured data is better than predicted by the simulations for input SNR greater than 10 dB. The simulated measurement accuracy takes into account all of the frequency bins of the FFT. The measurement data collected from the prototype hardware a single FFT bin (frequency) was used. As a result, the simulated measurement accuracy can likely be considered a worst case measurement accuracy for the monobit receiver. The CRLB represents a theoretical best case bound on the performance of the differential phase measurement accuracy.

An explanation for the behavior of the prototype receiver at low input SNR may be the test setup itself. The signal generator has degraded performance at low input SNR level that leads to more input noise than desired, resulting in the behavior observed in the plots of the measured differential phase accuracy shown in Fig. 15.

IV. CONCLUSIONS

In this paper the differential phase measurement accuracy results obtained from both simulated and prototype monobit receivers were presented. The results discussed in this paper are motivated by an interest in using a monobit receiver architecture for a power constrained and size limited application requiring differential phase and frequency measurements.

The effect of the input signal phase shift and input SNR on the differential phase measurement accuracy of a monobit receiver architecture was examined and compared to the theoretical Cramer-Rao Lower Bound. The results of the simulated and measured performance indicate that differential phase measurements are suitable for the intended application. The results obtained show that useable differential phase measurements can be made at moderate input SNR and for a wide range of input signal phase shifts. The prototype monobit receiver achieves a measurement accuracy of approximately 2° at 13 dB input SNR and 0.66° at an input SNR of 30 dB. The differential phase measurement accuracy achieved on the prototype hardware was found to fall within a lower bound provided by the CRLB and an upper bound provided by the simulated monobit receiver.

The differential phase measurement accuracy of the simulated receiver is obtained by combining data sets with input signals in each FFT bin. Combining these data sets to obtain sigma serves to lower the predicted differential phase measurement accuracy (or increase the measurement error). The accuracy of the measurement degrades due to variations in the excess noise floor influenced by the number and magnitude of the harmonic sampling products introduced by the 1-bit sampling process at individual input signal frequencies.

Future extensions of this work includes further characterization of the monobit receiver prototype differential phase measurement accuracy as a function of input frequency and an evaluating the differential phase measurement accuracy of modulated signals. The effect of oversampling and digital decimation to improve the performance of the monobit receiver is also an area of future study. As well as developing calibration techniques to correct any phase imbalances between receiver channels. The processing of multiple RF input signals from spatially separated sources has been examined. It is possible to make accurate differential phase measurements when the RF energy falls into distinguishable FFT bins. Additional analysis of multi-tone inputs is part of the ongoing study into the monobit receiver discussed here.

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