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Realization of a Power-Efficient Transmitter Based on Integrated Artificial Neural Network

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ABSTRACT In wireless devices, a transmitter normally consumes most of power due to its power amplifier (PA), especially in the applications such as radar, base station, and mobile phone. It is highly desirable to design a transmitter that can emit signals smartly, i.e., the power emission is exactly based on the emitting distance required and the target. Such a design can save huge amount of power as there are almost countless wireless devices in use currently. In this paper, an intelligent radio-frequency transmitter integrated with artificial neural network (ANN) is implemented. The intelligent transmitter consists of an ANN module, a frequency generation module, and a switch-mode PA. The integrated three-layered fully connected ANN can be offline trained to smartly classify input data according to the required power and assign the transmission channel. Furthermore, with the integrated ANN, the average power consumption of the PA is reduced to 34.3 mW, which is 46.5 % lower than PA without the ANN. With the intelligent transmitter, wireless devices can save a large amount of energy in their operations.

INDEX TERMS Radio transmitters, radiofrequency amplifiers, energy efficiency, power control, frequency control, classification algorithms, machine learning.

I. INTRODUCTION

There are countless wireless devices in use worldwide consuming around 61 trillion Watt per hour [1]. Transmitter containing power amplifier (PA) consumes most of power in wireless systems, responsible for modulating the input signal into a predefined carrier frequency and boosting the radio signal to a sufficient power level to transmit through the air interface between the transmitter and the receiver [2], [3]. Conventionally, as transmitters do not "know" emitting distance and target, full power is normally used by PA in order to assure that signals can be received [4], [5]. Hence power giants like radar and base station may consume tens of thousands Watt per second. On the other hand, since wearable devices usually have a limited battery capacity, RF components in the wireless transmission systems should be power efficient to reduce energy consumption, in order to increase the battery lifetime and avoid using cooling systems [6]–[8]. To save energy consumption, it is highly desirable to have an intelligent transmitter that emits an exact amount of energy according to the emitting distance required and target.

Recently artificial neural network (ANN) becomes an increasingly interesting research topic due to its various potential applications [9]–[12]. ANN, which is inspired by biological neural networks, is based on the integration of artificial neurons and synapses. ANN has been proved useful in realizing brain-like behavior such as image or voice recognition [13]–[15]. ANN has also been used in RF circuit design. Work [16]–[18] studied the effect of using ANN solve transmitter's nonliearity problems. Work [19] presented the effect of training a BFSK Neural Network demodulator with noisy data. And work [20] proposed an ANN to optimize RF passive component synthesis in high frequency RF designs. Among various ANNs, multi-layer perceptron (MLP) is one of useful models for its good generalization, pervasive approximation

and classification capability. A typical MLP network consists of an input layer, which is formed by a set of source nodes, one or more hidden layers of computation neurons, and an output layer of nodes [21]. Considering the MLP's advantages, we have integrated an MLP neural network into a CMOS chip to realize an intelligent transmitter that can smartly determine the power and channel required due to its self-learning capability. To the authors knowledge, this is the first integrated ANN in RF circuit design.

In this work, a feed-forward MLP neural network is introduced into the transmitter for smartly controlling the power emission. In addition, the MLP can also smartly assign data transmission into an appropriate channel to avoid interfering with other data transmissions. The intelligent transmitter was designed and fabricated with a standard 0.13 μ m CMOS process. It occupies 1.96 mm² including the bonding pads and ESD devices. Measurement results show that the transmitter has a peak output power of 14.9 dBm and a power consumption of 75.6 mW from a 1.5 V power supply. With the MLP network identifying the input data and automatically adjusting the transmit power as well as the transmission channel, the average power consumption of the PA is reduced to 34.3 mW that is about 46.5 % lower than PA without the ANN. Obviously, with such intelligent transmitters, much power can be saved for wireless devices.

II. DESIGN OF INTELLIGENT TRANSMITTER

A. THE INTELLIGENT TRANSMITTER

The power consumption of body area radio networks is constantly increasing due to the growing number of portable terminals and higher traffic demands. Shortcomings of the state-of-the-art lie in the fact that current transmitters for multi-user, such as base station, are designed to serve peak demands without considering energy efficient off-peak operation [22]. Many algorithms have been proposed in the area of adaptive transmit power control and channel allocation. Work [22] proposed a radio resource management algorithm to minimize the base station supply power consumption for multi-user multi-input multi-output (MIMO) orthogonal frequency division multiplexing (OFDM). Work [23] investigated joint subchannel and power allocation in bandwidthhungry services. It implies that resource allocation algorithms are inevitable in indoor multi-user radio networks. However, this work proposed a self-adaptive RF transmitter with an integrated ANN that offers better performance with lower power consumption than running algorithms on external computing units.

Fig. 1 (a) illustrates the working mechanism of the intelligent transmitter. As shown in Fig. 1 (a), the intelligent transmitter can transmit data to a receiver in a specified channel with an exact amount of power determined by the transmission distance. As shown in Fig. 1 (a), receivers locate with different distances and are in different channels. After training the ANN, the transmitter can adjust the emitting power that is exactly required for Receivers A and D but



FIGURE 1. (a) Schematic illustration of data transmission from the intelligent transmitter to a specified receiver through a specified channel; (b) photograph of a die of the intelligent transmitter; (c) architecture of the intelligent transmitter.

Receiver C receives nothing from the transmitter as it is out of range. Of course as Receiver B locates within the range of transmission, it can receive signal also. On the other hand, the intelligent transmitter can also assign the channel smartly. As shown in Fig. 1 (a), Receivers A, B and C are assigned to Channel 1, while Receiver D is assigned to Channel 2. Therefore, although Receivers A and D are located in the same distance, either of the receivers cannot receive signals from the other one as they are in different channels, thus avoiding the interference. The prototype chip is shown in Fig. 1 (b), an MLP network, a Voltage Controlled Oscillator (VCO) and a PA are integrated in the chip. The transmitter was designed and fabricated in a standard 130 nm CMOS process. Dies of the intelligent transmitter were cut from the wafer and packaged in standard 32-pin quad flat noleads packages (QFP32).Fig. 1 (c) shows the configuration of the intelligent transmitter. The MLP network is used to



FIGURE 2. Data flow chart of the intelligent transmitter.

identify the input data, to determine the energy required for the signal transmission, and to smartly assign the channel; the PA is used amplify to the signal; and the VCO is used to provide the reference frequency for a specific channel.

B. DATA FLOW OF THE INTELLIGENT TRANSMITTER

As shown in Fig. 2, a GPU is used to train MLP to obtain weight matrix with past data. The weight matrix is transferred to the field-programmable gate array (FPGA) that is used to send data to the transmitter. The intelligent transmitter uses serial peripheral interface (SPI) bus protocol to receive weight matrix and input data. A computing core calculates the required supply voltage and frequency with the registered weight matrix and the input data. A low dropout regulator (LDO) and a voltage-controlled oscillator (VCO) are used as voltage and frequency control of the switch mode power amplifier (PA), respectively.

C. TEST BOARD AND FPGA WAVEFORMS OF THE INTELLIGENT TRANSMITTER

The Fabricated transmitter chip and its test board are shown in Fig. 3. Dies of the intelligent transmitter were cut from the wafer and packaged in standard 32-pin quad flat no-leads



FIGURE 3. Photograph of the intelligent transmitter chip and the test PCB board.

package (QFP32). The Artificial Neural Network (ANN) based on Multilayer Perceptron (MLP) was realized in logic circuit. The test board was fabricated in printed circuit board (PCB), which consisted of a packaged intelligent transmitter chip, three LDO chips (two AMS1117 chips from AMS and one TPS74301 chip form Texas Instruments), and other passive devices (from Murata). A field-programmable gate array (FPGA) board was used to transfer data and analyze accuracy.

FPGA waveforms for the proposed MLP are shown in Fig. 4. The waveforms (from the bottom to top) correspond to the high 8-bit of input data, low 8-bit of input data, classification output, max done signal, and next data signal, respectively. A working cycle is fulfilled in 433 μ s. In the first 418.4 μ s, the input data is received by MLP. After MLP performs its max out calculation, a pulse is detected in "Max Done" and the MLP classification output is available in "Class Out". A pulse in "Next Data" comes after the pulse in "Max Done", which means that MLP is ready for next input.

III. DESIGN OF MLP NEURAL NETWORK

An MLP neural network is used to smartly adjust PA transmission power according to transmission distance required, as well as to assign transmission channel. MLP has an excellent identification accuracy [24], [25] and its integration in an integrated circuit is easy [26]. The MLP consists of threelayered fully-connected layers [27]. We use tanh as the activation function for both the input layer and the hidden layer. As e^x and e^{-x} can be calculated without multiplications, has a good compatibility with integrated circuit. Details of implementing function by circuit are presented in Supplementary Note 1. Results from the circuit-realized function and ideal function are consistent, as demonstrated in Supplementary Note 2. Maxout function is used to make the determination of classification as shown in Fig. 5. The details of implementing Maxout circuit are provided in Supplementary Note 3. Supplementary Note 4 presents the verification of the Maxout function. The booth's multiplication is used to realize matrix multiplication. The implementation details are provided in Supplementary Note 5.

The MLP was trained with samples from past data and then it can classify input data into categories according to the transmission distances. A GPU-equipped computer was used



FIGURE 4. FPGA waveforms of a working cycle for MLP.

for the training process. The cross entropy [28], [29] between the given targets and outputs is used to calculate the network performance. Since we use as the activation function with its output between -1 and 1, the cross entropy is given by

$$CE_{tanh} = (-1 - t) \cdot \log(1 + y) - (1 - t) \cdot \log(1 - y) \quad (1)$$

where t is the target value; and y is the output of the MLP. Equation (1) returns a numerical value approaching infinity, which heavily penalizes output when it approaches -1 or 1. Equation (1) gives a minimum value when y equals to t. Although minimizing CE_{tanh} leads to a good accuracy of classification, lavishly minimizing CEtanh may cause overfitting. We use early dropout method to prevent overfittings [30], [31]. The samples of past data are randomly divided into three sets: training (80 %), validation (10 %), and examination (10%). Scaled conjugate gradient method [32] is used when optimizing weight matrices and bias. The training process keeps updating the weight and bias until validation check continuously fails for five times. As shown in Fig. 5, when working, data are input into the transmitter with SPI protocol, and are identified by the MLP network in serial to reduce system latency. FPGA is used to send data including the weight matrices and signal data to the intelligent transmitter. After the weight matrices are stored in the registers of the MLP, the MLP network identifies the received data and adjusts the working power of the PA according to the training. After the work mode adjustment, the transmitter can transmits data at the necessary power in its assigned channel.



FIGURE 5. Overall workflow diagram of the MLP integrated circuit.

The integrated MLP, in the chip as shown in Fig. 1 (b). It occupies 1 mm^2 area and dissipates 10 mW power. The MLP shares the SPI bus with the RF transmitter to send and accept data from the FPGA. The MLP, as well as its interface bus, can operate at the highest clock frequency of 10 Mb/s.

IV. DESIGN OF PA AND VCO

Co-design of digital signal processing (DSP) algorithms and PA circuits can lead to improved efficiency in multiple conditions [33]. A digitally assisted PA and VCO is one of the potential solutions to realize a better power efficiency and multiband transmitter. PAs with a reconfigurable amount of RF unit-cells are representative in digitally controlled PAs. The output power is controlled by changing the number of active unit-cells (AUC) [33], [34]. Another method to configure the output power of a PA is to dynamically controlled power supply (DPS) [33], [35]. The dynamically controlled power supply of PA can be realized by a programmable low dropout regulator (LDO) or a digitally driven buck converter. PAs in work [34] and [36] show second gate bias voltage control (SGBVC) and power combiners can also improve the average power efficiency.

As shown in Fig. 6 (a), the integrated PA consists of two stages, a pre-amplification stage and a power amplifier stage. The pre-amplification part amplifies the input voltage into full swing on-off switching voltage signal with a peak-to-peak voltage of 2.5 V, and amplifies the current to an enough level to drive the gate capacitor of the power amplifier



FIGURE 6. (a) Circuit schematic of the power amplifier in the intelligent transmitter; (b) PA output power; (c) PA power added efficiency (PAE); (d) power consumption of PA.

transistor in the second stage. And the power amplifier stage converts the DC power of the power amplifier transistor into an RF signal for information transmission. As shown in Fig. 6 (b) and (c), the output power of the implemented PA is 14.9 dBm and the power added efficiency (PAE) is 40.6 %. Fig. 6 (d) indicates that at the supply voltage of 1.5 V, the power consumption of the PA is around 60 mW. A 5th order Chebyshev low pass filter (LPF) is integrated between the load pull and the antenna to filter out the higher harmonics of PA. With the LPF, a higher harmonic suppression ratio of 37 dBc is achieved.



FIGURE 7. (a) Circuit schematic of the programmable ring oscillator; (b) schematic of the TSPC divider; (c) spectrum of the frequency generation module; (d) phase noise of the output signal from the frequency generation module.

A frequency generator is integrated between MLP network and PA to supply RF reference frequency for data transmission. The frequency generator consists of a programmable ring oscillator (Fig. 7 (a)) and a frequency divider (Fig. 7 (b)) based on true single-phase clock (TSPC) flip-flop. The ring oscillator is used instead of a resonant LC oscillator for its low

TABLE 1. Perfo	ormance comp	parison of	recent	transmitters.
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	RF	Peak	PAE (%)	CMOS	RF Power		
	Frequency	$\mathbf{P}_{\mathrm{out}}$		Technology	Control		
	(GHz)	(dBm)		(nm)			
2016	0.75-2.0	29	11.5-22	150 bulk	AUC &		
TMTT [33]					DPS		
2014	0.6-0.95	24.5	21.5-43	65 bulk	AUC &		
TMTT [34]					SGBVC		
2013	0.7-1.8	30	23-27	150 bulk	DPS		
JMWT [35]							
2016	0.6	21	47 ^a	180	Power		
TCAS-II [36]					Combinier		
2014	0.9	22	-	65	Dual-		
TCAS-I [37]					bandwith		
This Work	0.4-0.5	15	36.3-40.5	130	DPS &		
					ANN		
^a Peak PAE.							

power consumption and small chip area. The programmable current source in Fig. 7 (a) is used to adjust the transmitter transmission channel. And the frequency divider is used to avoid interference from higher harmonics of the ring oscillator. The ring oscillator consumes 45uA from a supply voltage of 2.5V. The spectrum of the generated frequency signal is shown in Fig. 7 (c). The output frequency can be varied in the range between 433 MHz and 438 MHz by adjusting the supply current of the ring oscillator. The phase noise of the generated signal is -96.0 dBc/Hz at a carrier frequency of 433 MHz as shown in Fig. 7 (d).

Table 1 summarizes the performance of the state-of-the-art transmitters and the presented transmitter. Concluded from the comparison, with the ANN, this transmitter has a higher PAE range.

V. MEASUREMENT RESULTS OF THE INTELLIGENT TRANSMITTER

A. DESIGN TOOLS AND MEASUREMENT

The MLP was trained with samples of past data, which contains about 40,000 bits of transmitted data, transmit power and transmission channel assignment in a wireless communication system. A spectrum analyzer (R&S[®] FSW67) was used to measure the power and frequency of the transmitted signal. The ANN was trained and evaluated with a computer equipped with an Intel 5930 CPU and 2 Nvidia 1080 GPUs. The training process and identification accuracy were defined and calculated with Python scripts.

The RF transmitter was designed with the IC design software Cadence Version 6.1.6 (passive and active components co-simulation) and ADS Version 2015.01 (passive components simulation). The Verilog code of ANN was converted into low-level circuit descriptions (netlists) with Synopsys Design Compiler (Version 2016.12). And the netlist of the ANN was converted into layout with Cadence Innovus (Version 15.20.000). The layout was compared with the schematic and corrected with IC verification tool Mentor Calibre (Version 2016). The transmitter and ANN were cosimulated with Verilog-AMS.



FIGURE 8. (a) Continuous validation check of epochs in training; (b) training gradient of epochs.

The intelligent transmitter was packed before measurement. Dies of the intelligent transmitter were cut from the wafer and packaged in standard 32-pin quad flat no-leads packages (QFP32). The test board was fabricated in printed circuit board (PCB), which is composed of a packaged intelligent transmitter chip, three LDO chips (two AMS1117 chips from AMS and one TPS74301 chip form Texas Instruments), and other passive devices (from Murata). An FPGA board was used to transfer data and analyze classification accuracy. And a spectrum analyzer (R&S[®] FSW67) was used to measure the power and frequency of the output signal.

B. RESULTS

Fig. 8 (a) shows the continuous validation check of each epoch. In Fig. 8 (a), the training process stops at Epoch 16 for a pre-termination setting as discussed above when validation check keeps failing for five times. The Gradient keeps decreasing till to Epoch 16 as shown in Fig. 8 (b). Based on the failure check result in Fig. 8 (a), the weight and bias in Epoch 11 are saved. The measured time-domain input data, output data and transmitted data are presented in Fig. 9 (a). Fig. 9 (a) certifies that the send-out data and the received data are consistent, showing that the transmitter works well. The calculated classification accuracy (Fig. 9 (b)) show that the classifier of the transmitter works as expected. The weighted average classification accuracy of the intelligent transmitter is higher than 95.1 %. That means the MLP neural network can assign transmission tasks into correct categories and the transmission power can be adjusted smartly. The measured output power and output frequency of the classified four categories is shown in Fig. 9 (c). The average power consumption of the



FIGURE 9. (a) time-domain waveforms of data in the intelligent transmitter; (b) measured classification accuracy of the intelligent transmitter; (c) measured output power and output frequency of the classified four categories.

transmitter is reduced from 64.1 mW to 34.3 mW, which is 46.5 % lower.

VI. CONCLUSION

An intelligent radio frequency (RF) transmitter integrated with artificial neural network (ANN) is implemented. The reconfigurable ANN in the transmitter makes the radio network possible to work without an extra power and channel allocation algorithm, which can reduce the complexity and computing resource of the radio network. The transmitter is designed to be used in indoor medical radio communications device in medical implant communication service (MICS) band. The intelligent transmitter was designed and fabricated with a standard 0.13 μ m CMOS process. It occupies 1.96 mm² including the bonding pads and ESD devices. Measurement results show that the transmitter has a peak output power of 14.9 dBm with a power consumption of 75.6 mW from a 1.5 V power supply. With the MLP network identifying the input data and automatically adjusting the transmit power as well as the transmission channel, the average power consumption of the PA is reduced to 34.3 mW that is about 46.5 % lower than PA without the ANN. The measured identification accuracy of the MLP is 95.1 %. The intelligent transmitter provides a promising method to significantly reduce the energy required by RF devices. With these smart RF devices, wireless communications in daily life can be more power-efficient and save a huge amount of energy.

REFERENCES

- M. Kennedy, A. Ksentini, Y. Hadjadj-Aoul, and G. Muntean, "Adaptive energy optimization in multimedia-centric wireless devices: A survey," *IEEE Commun. Surveys Tuts.*, vol. 15, no. 2, pp. 768–786, 2nd Quart., 2013.
- [2] X. Lu, P. Wang, D. Niyato, D. I. Kim, and Z. Han, "Wireless networks with RF energy harvesting: A contemporary survey," *IEEE Commun. Surveys Tuts.*, vol. 17, no. 2, pp. 757–789, 2nd Quart., 2015.
- [3] J. Joung, C. K. Ho, K. Adachi, and S. Sun, "A survey on power-amplifiercentric techniques for spectrum- and energy-efficient wireless communications," *IEEE Commun. Surveys Tuts.*, vol. 17, no. 1, pp. 315–333, 1st Quart., 2015.
- [4] H. Jin, D. Kim, and B. Kim, "Efficient digital quadrature transmitter based on IQ cell sharing," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1345–1357, May 2017.
- [5] L. Xia, J. Cheng, N. E. Glover, and P. Chiang, "0.56 V,-20 dBm RF-powered, multi-node wireless body area network system-on-a-chip with harvesting-efficiency tracking loop," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1345–1355, Jun. 2014.
- [6] Y. Song, R. Zhu, and Y. E. Wang, "An X-band pulsed load modulation transmitter with multilevel envelope delta-sigma modulations," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 11, pp. 3643–3653, Nov. 2016.
- [7] A. Paidimarri, N. Ickes, and A. P. Chandrakasan, "A +10 dBm BLE transmitter with sub-400 pW leakage for ultra-low duty cycles," *IEEE J. Solid-State Circuits*, vol. 51, no. 6, pp. 1331–1346, Jun. 2016.
- [8] H. Hwang, C. Lee, J. Park, and C. Park, "A current-shared cascade structure with an auxiliary power regulator for switching mode RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 11, pp. 2711–2722, Nov. 2014.
- [9] Z. Ghahramani, "Probabilistic machine learning and artificial intelligence," *Nature*, vol. 521, no. 7553, pp. 452–459, 2015.
- [10] M. W. Libbrecht and W. S. Noble, "Machine learning applications in genetics and genomics," *Nature Rev. Genet.*, vol. 16, no. 6, pp. 321–332, 2015.
- [11] M. Kabra, A. A. Robie, M. Rivera-Alba, S. Branson, and K. Branson, "JAABA: Interactive machine learning for automatic annotation of animal behavior," *Nature Methods*, vol. 10, no. 1, pp. 64–67, 2013.
- [12] G. Pilania, C. Wang, X. Jiang, S. Rajasekaran, and R. Ramprasad, "Accelerating materials property predictions using machine learning," *Sci. Rep.*, vol. 3, Sep. 2013, Art. no. 2810.
- [13] K. Bong, S. Choi, C. Kim, D. Han, and H. Yoo, "A low-power convolutional neural network face recognition processor and a CIS integrated with always-on face detector," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 115–123, Jan. 2018.
- [14] M. Price, J. Glass, and A. P. Chandrakasan, "A low-power speech recognizer and voice activity detector using deep neural networks," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 66–75, Jan. 2018.
- [15] P. Yao et al., "Face classification using electronic synapses," Nature Commun., vol. 8, p. 15199, May 2017.
- [16] M. Rawat and F. M. Ghannouchi, "Distributed spatiotemporal neural network for nonlinear dynamic transmitter modeling and adaptive digital predistortion," *IEEE Trans. Instrum. Meas.*, vol. 61, no. 3, pp. 595–608, Mar. 2012.
- [17] R. Zayani, R. Bouallegue, and D. Roviras, "Crossover neural network predistorter for the compensation of crosstalk and nonlinearity in MIMO OFDM systems," in *Proc. IEEE 21st Annu. Int. Symp. Pers., Indoor Mobile Radio Commun. (PIMRC)*, Instanbul, Turkey, Sep. 2010, pp. 966–970.
- [18] F. Mkadem and S. Boumaiza, "Physically inspired neural network model for RF power amplifier behavioral modeling and digital predistortion," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 4, pp. 913–923, Apr. 2011.
- [19] M. R. Amini and E. Balarastaghi, "Improving ANN BFSK demodulator performance with training data sequence sent by transmitter," in *Proc. 2nd Int. Conf. Mach. Learn. Comput. (ICMLC)*, Bengaluru, India, Feb. 2010, pp. 276–281.
- [20] B. Liu, D. Zhao, P. Reynaert, and G. Gielen, "Synthesis of integrated passive components for high-frequency RF ICs based on evolutionary computation and machine learning techniques," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 30, no. 10, pp. 1458–1468, Oct. 2010.

- [21] K. Hornik, M. Stinchcombe, and H. White, "Multilayer feedforward networks are universal approximators," *Neural Netw.*, vol. 2, no. 5, pp. 359–366, 1989.
- [22] H. Holtkamp, G. Auer, S. Bazzi, and H. Haas, "Minimizing base station power consumption," *IEEE J. Sel. Areas Commun.*, vol. 32, no. 2, pp. 297–306, Feb. 2014.
- [23] H. Zhang, C. Jiang, N. C. Beaulieu, X. Chu, X. Wen, and M. Tao, "Resource allocation in spectrum-sharing OFDMA femtocells with heterogeneous services," *IEEE Trans. Commun.*, vol. 62, no. 7, pp. 2366–2377, Jul. 2014.
- [24] I. Heazlewood, J. Walsh, M. Climstein, J. Kettunen, K. Adams, and M. DeBeliso, "A comparison of classification accuracy for gender using neural networks multilayer perceptron (MLP), radial basis function (RBF) procedures compared to discriminant function analysis and logistic regression based on nine sports psychological constructs to measure motivations to participate in masters sports competing at the 2009 world masters games," in *Proc. ISCS*, Loughborough, U.K., 2016, pp. 93–101.
- [25] B. Zhang, "Reliable classification of vehicle types based on cascade classifier ensembles," *IEEE Trans. Intell. Transp. Syst.*, vol. 14, no. 1, pp. 322–332, Mar. 2013.
- [26] I. Hubara, M. Courbariaux, D. Soudry, R. El-Yaniv, and Y. Bengio, "Quantized neural networks: Training neural networks with low precision weights and activations," *J. Mach. Learn. Res.*, vol. 18, no. 1, pp. 6869–6898, 2017.
- [27] M. Lin, Q. Chen, and S. Yan. (2013). "Network in network." [Online]. Available: https://arxiv.org/abs/1312.4400
- [28] E. P. L. van Nieuwenburg, Y.-H. Liu, and S. D. Huber, "Learning phase transitions by confusion," *Nature Phys.*, vol. 13, no. 5, pp. 435–439, 2017.
- [29] E. P. L. van Nieuwenburg, L. Ye-Hua, and D. H. Sebastian, "Learning phase transitions by confusion," *Nature Phys.*, vol. 13, no. 5, pp. 435–439, 2017.
- [30] N. Srivastava, G. Hinton, A. Krizhevsky, I. Sutskever, and R. Salakhutdinov, "Dropout: A simple way to prevent neural networks from overfitting," *J. Mach. Learn. Res.*, vol. 15, no. 1, pp. 1929–1958, 2014.
- [31] M. E. Charlson, P. Pompei, K. L. Ales, and C. R. MacKenzie, "A new method of classifying prognostic comorbidity in longitudinal studies: Development and validation," *J. Chronic Diseases*, vol. 40, no. 5, pp. 373–383, 1987.
- [32] P. de Chazal and M. D. McDonnell, "Regularized training of the extreme learning machine using the conjugate gradient method," in *Proc. IJCNN*, Anchorage, AK, USA, May 2017, pp. 1802–1808.
- [33] T. Nakatani, D. F. Kimball, and P. M. Asbeck, "Techniques for power dynamic range and back-off efficiency improvement in CMOS digitally controlled polar transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 550–561, Feb. 2016.
- [34] H. Choi, Y. Lee, and S. Hong, "A digital polar CMOS power amplifier with a 102-dB power dynamic range using a digitally controlled bias generator," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 3, pp. 579–589, Mar. 2014.
- [35] T. Nakatani, D. F. Kimball, L. E. Larson, and P. M. Asbeck, "0.7–1.8 GHz multiband digital polar transmitter using watt-class currentmode class-D CMOS power amplifier and digital envelope modulation technique for reduced spurious emissions," *Int. J. Microw. Wireless Technol.*, vol. 5, no. 3, pp. 271–284, 2013.
- [36] Y. Yin, B. Chi, Y. Gao, X. Liu, and Z. Wang, "A 0.1–5.0 GHz reconfigurable transmitter with dual-mode power amplifier and digitally-assisted self-calibration for private network communications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 11, pp. 3266–3277, Nov. 2014.
- [37] J. Hur et al., "A multilevel class-D CMOS power amplifier for an outphasing transmitter with a nonisolated power combiner," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 7, pp. 618–622, Jul. 2016.



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