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A Reconfigurable Voltage Converter With Split-Capacitor Charging and Energy Recycling for Ultra-Low-Power Applications

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ABSTRACT This paper presents a reconfigurable on-chip switched capacitor (SC) voltage converter aimed at ultra-low- power applications. The proposed voltage converter provides an additive advantage of energy saving during both sleep-to-active and active-to-sleep transitions. This is done by incorporating two techniques, so called, split-capacitor charging (step-wise charging), and energy recycling. Split-capacitor charging is proved to reduce the energy loss during the sleep-to-active transition by 66%. An existing symmetric energy recycling technique recovers 75% of the energy from the capacitor bank at the expense of a large-output voltage ripple. In this paper, an improved method called asymmetric energy recycling reconfiguration (s) is introduced. The asymmetric energy recycling reduces the output voltage ripple by 50% compared with the symmetric recycling technique, without sacrificing the recycling efficiency. It can salvage 75.42% of the capacitor energy in active-to-sleep transition that would have been wasted through leakages during a long sleep period. Circuit simulations of the proposed SC voltage converter demonstrate up to 23.13% improvement in energy efficiency compared with conventional SC converters for a short active period.

INDEX TERMS Switched capacitor, DC-DC converter, ultra-low power converter, step-wise charging, energy recycling.

I. INTRODUCTION

Advancements in process technology and evolution of ultra-low-power (ULP) circuits have initiated a trend towards multiple power domains on chip. It is often required to have a separate voltage converter for each power domain to individually provide dynamic voltage scaling (DVS) and enhance the power efficiency of ULP applications [1]. Inductor-based DC-DC voltage converters are usually preferred for higher power efficiency and flexible conversion ratios. On-chip integration of large inductors, however, is not feasible with current silicon technologies. On the other hand, switched capacitor (SC) converters can provide both efficiency and on-chip integration, and thus can be configured to supply multiple power domains without requiring external capacitors [2]–[4].

Various reconfigurable SC converters have been proposed to provide multiple voltage conversion ratios to supply individual power domains with high energy efficiency [5]–[8]. Chang *et al.* [9] used a high-density deep trench capacitor to overcome the power loss induced by the bottom plate parasitic capacitance and thus enhancing the efficiency to 90%. On-chip ferroelectric capacitors (Fe-Caps) were used to further enhance the efficiency to 93% by utilizing extremely low bottom plate parasitic capacitance of Fe-Caps [10]. Most of these SC converters are designed and optimized for regular operations with long active period [6], [11], [12].

Recently, an increasing number of ULP applications such as wearable computing, biomedical and implantable devices are event-driven [13]–[15]. Such applications often perform a periodic task for a very short active interval, and, stay

in the sleep mode for an extended period. In these applications, therefore, the power loss due to the transitions (sleep-to-active and active-to-sleep) is increasing more significantly. Thus, the conventional SC converters that are not specifically designed for efficient transitions tend to suffer from poor average power consumption [16]. To improve the power efficiency, it is crucial that one minimizes the energy losses associated with these transitions [17]–[19]. Some inductor-based step-wise charging methods have been proposed to minimize the losses associated with sleep-to-active transitions [20], [21]. Such methods are not a feasible solution, since it is not possible to integrate multiple inductors of large size on-chip.

A separate capacitor bank has been proposed to efficiently drive a capacitive load from sleep-to-active transition [22], [23]. The separate capacitor bank itself, however, wastes half of the source energy during its charging process after a long sleep period, and thus its efficiency can be substantially degraded. In [17], we presented a split-capacitor charging method, and achieved an energy saving of 66% during sleep-to-active transitions without the need of an additional capacitor bank or inductors. The method in [17] splits the charging process into multiple steps and performs step-wise charging by successively reconfiguring the internal capacitor bank. However, [17] does not address the other losses during the active-to-sleep transition. While [17] offers favorable savings for boost conversion cases, its performance drastically drops for buck conversion cases.

Also, we introduced a notion of energy recycling and reported an energy saving of 85.86% during active-to-sleep transitions [18]. During its recycling process, the recycled energy is continuously provided to the load, which would otherwise be wasted through leakage during a long sleep period. However, it has a drawback of larger output voltage ripple, which is unavoidable side effect of its symmetric recycling configurations. Furthermore, considering the output switch losses, the actual energy saving was reduced to 75%. The voltage converter of [18] was evaluated only for boost conversion cases and did not address the sleep-to-active transition.

Reference [19] targets both the transitions i.e. sleep-to-active and active-to-sleep for a ULP application, where active period is much shorter than the sleep period. It showed a power saving of 64% in both the transitions. For sleep-to-active transitions, the capacitors are charged progressively. As the size of these capacitors is not uniform, it is challenging to generate accurate target voltages. In addition, since it returns the recycled energy back to the battery during active-to-sleep transition, it would not be applicable to the circuits that are not directly connected to a battery.

In this paper, an enhanced SC converter is presented, which supports both split-capacitor charging (SCC) [17] and energy recycling (ER) [18] sharing one capacitor bank to improve the overall power saving. To ensure the stability and constant voltage of capacitors, the capacitor bank is step-wise charged in symmetric structure. For recycling its energy,

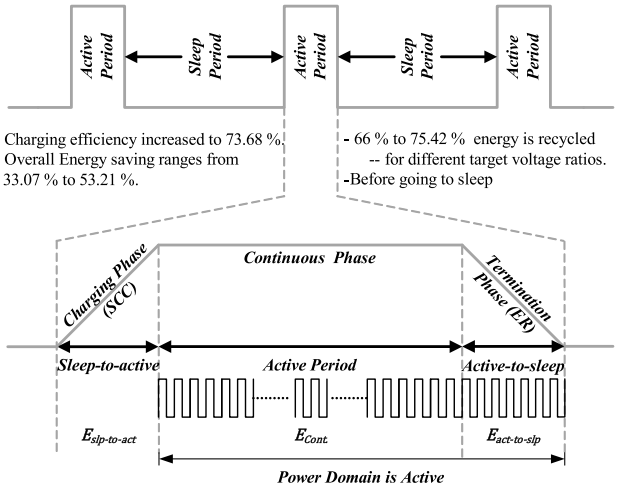

FIGURE 1. Three-phase operation of the proposed ULP SC converter.

we are introducing asymmetric configurations to achieve maximum energy saving while minimizing the output voltage ripple. These features make the proposed SC converter well suited for the ULP applications where multiple on-chip voltage converters are required for driving loads with short active period. It can also reduce the overall capacitor size and digital controller overhead compared with the work of [19].

Section II explains a typical ULP voltage converter operation targeting a very short active period. Section III presents the proposed architecture of the SC converter, and describes its SCC and ER operations. Section IV covers analytical model for the proposed architecture. In Section V, the schematic implementation and simulation results of the proposed converter are presented, followed by the conclusion in section VI.

II. ULP VOLTAGE CONVERTER OPERATION

For a ULP application, the operation of a typical SC voltage converter can be divided into three phases: (1) Charging phase, (2) Continuous phase, (3) Termination phase, as shown in Fig. 1. Firstly, in the Charging phase (corresponding to sleep-to-active transition), the internal capacitors are charged to a certain voltage. Secondly, in the Continuous (corresponding to the active in conventional SC converter) phase, the energy is delivered to the load, while the load executes its tasks, and the capacitor bank is discharged and recharged again. Finally, in the Termination phase (corresponding to active-to-sleep transition), the converter transitions to a long sleep period, and any energy remaining in the capacitors is wasted through leakage current during the long sleep period.

In Continuous phase, the capacitor bank of an SC converter toggles between two steps: (1) delivering power to the load circuit and (2) recharging the capacitor bank from the source. These steps, called continuous-delivery and continuous-recharging steps, decide the voltage conversion ratio provided by the converter. For example, Fig. 2(a) shows an example of

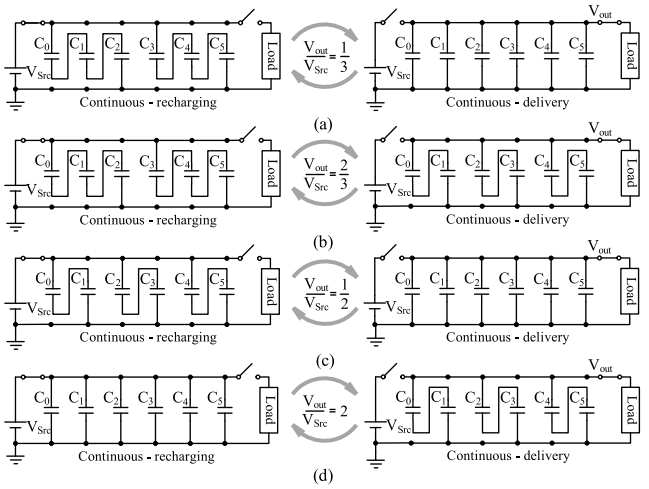

FIGURE 2. **Continuous phase of the proposed SC converter, which corresponds to the active mode in conventional converters.**

the Continuous phase for a voltage conversion ratio of 1/3. Similarly, Fig. 2(b), Fig. 2(c) and Fig. 2(d) represent Continuous phases for voltage conversion ratios of 2/3, 1/2, and 2, respectively.

Capacitor and switches are sized based on load wattage requirements, output ripple voltage, and operating frequency. Ideally, the converter spends equal time among recharging and delivery steps. Thus, the switches and the capacitors must be capable of handling twice the amount of power needed by the load. Large switches allow more current to flow and charge/discharge capacitors quickly. Large capacitors offer small change in voltage against the change in amount of charge stored/delivered.

Assuming a load current of 100uA at 0.8 V, the average power consumption turns out to be 80 uW. For a frequency of 20MHz, with 50 ns period, load would consume 4 pJ per clock cycle. Ideally, during one clock period twice of 4 pJ (i.e. $\Delta E = 8$ pJ of energy) will be transferred, either from source to capacitors or from capacitors to the load. Thus, the capacitors must be large enough to offer small voltage change (less than 5%) against 8 pJ change in stored energy. The change in energy corresponding to the change in voltage can be derived as:

$$\Delta E = E_1 - E_2 = \frac{1}{2}CV_1^2 - \frac{1}{2}CV_2^2 \tag{1}$$

$$\Delta E = \frac{1}{2}C\left(V_1^2 - V_2^2\right) \tag{2}$$

Here, V_1 and V_2 are the initial and final voltages on the capacitor. Assuming V_2 is $0.95V_1$ (corresponding to 5% change in voltage), equation (2) becomes:

$$\Delta E = \frac{1}{2}C\left(V_1^2 - 0.9025 \cdot V_1^2\right) \tag{3}$$

$$\Delta E = \frac{1}{2}CV_1^2\left(9.75 \times 10^{-2}\right) \tag{4}$$

The energy lost by the capacitors is restored by an input voltage source (V_{Src}), thus $V_1 = V_{Src}$. So, the equivalent capacitance C_{eq}, as seen by the source, during charging becomes:

$$C_{eq} = \frac{2 \times \Delta E}{\left(9.75 \times 10^{-2}\right) \times V_{Src}^2} \tag{5}$$

Equation (5) can be used to calculate total capacitance for required ΔE and less than 5% voltage change. Depending upon the capacitor bank structure during continuous-recharging step, the equivalent capacitance can be used to determine size of unit capacitor as well as size of the whole capacitor bank. The resistance offered by the switches (and capacitive ESR) should be small enough to allow high enough current to flow. The current flow through switches must be sufficient to deliver 8 pJ in one clock cycle, this 8 pJ of energy will be supplied from the source to charge the capacitors.

Conventionally, the Charging phase starts from continuous-recharging step when the converter transitions from sleep-to-active. Also, the conventional converters usually terminate the operation on continuous-delivery step, when the converter transitions from active-to-sleep. Energy consumption associated with these different phases can significantly affect the overall performance of the SC converter. During the Charging phase, let $E_{slp-to-act}$ be the required energy to charge the capacitors in the converter up to the target voltage level. During the Continuous phase, let $E_{Cont.}$ be the total energy consumed by the load circuit including the energy needed to recharge the consumed energy of the capacitors. In Termination phase, on the other hand, let $E_{act-to-slp}$ be the energy wasted through leakage current during long sleep periods.

It is well known problem that charging a capacitor from 0 to V_{Src} requires energy $E_{slp-to-act}$ that can be expressed by equation (6).

$$E_{slp-to-act} = C_{eq} \cdot V_{Src}^2 \tag{6}$$

On the other hand, the energy stored in the capacitor E_{cap} is given by equation (7).

$$E_{cap} = 0.5 \cdot C_{eq} \cdot V_{Src}^2 \tag{7}$$

This indicates that at least the half of energy drawn from the external power source is wasted during the conventional (one-step) charging process.

Most of the ULP voltage converters are designed to optimize the performance by minimizing the energy $E_{\text{Cont.}}$ associated with the Continuous phase [24], [25]. In ULP applications of our concern, the continuous period is very short, compared to the sleep period. In these applications, therefore, the energy $E_{slp-to-act}$ and $E_{act-to-slp}$ during the transitions tends to become more prominent. In [19], $E_{act-to-slp}$ and $E_{slp-to-act}$ account for 41% $\sim$ 50% of the overall energy consumption of the Phoenix processor. The detailed analysis of these two transitions (sleep-to-active transition and active-to-sleep transition) is discussed in Section III.

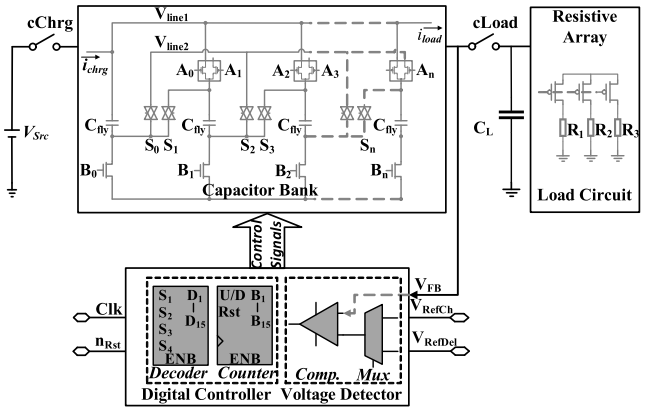

FIGURE 3. Overall architecture of the proposed voltage converter comprising of capacitor bank, digital controller, load circuit and voltage detector (feedback).

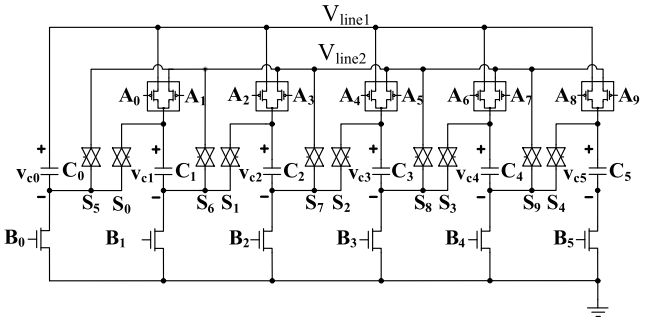

FIGURE 4. Proposed capacitor bank with $N = 6$ capacitors and corresponding switches.

III. PROPOSED VOLTAGE CONVERTER ARCHITECTURE

The proposed architecture aims at minimizing the wasted energy during the Charging and Termination phases without sacrificing the energy efficiency of Continuous phase. This is accomplished by incorporating SCC and ER techniques into a single capacitor bank of the proposed converter.

A. OVERALL OPERATIONS

During the Continuous phase, the proposed converter behaves as a regular series-parallel SC converter by switching between two steps which are continuous-recharging and continuous-delivery, repeatedly. The transition between the recharging and the delivery step is initiated with the use of voltage references for charging and delivery, V_{RefCh} and V_{RefDel}, respectively. Whenever the output voltage falls below V_{RefDel} during the delivery step, the converter switches to the recharging step. During the recharging step, the capacitors are charged up to V_{RefCh} before moving to the delivery step again.

In the Charging phase of the proposed architecture, the capacitors are charged to V_{RefCh} in a progressive manner using SCC which we previously reported in [17]. One-step charging wastes 50% of the energy (equation (6) and equation (7)) and SCC can mitigate this wastage energy. On the other hand, during Termination phase of the proposed converter, the remaining energy in the capacitors (which would have been wasted through leakages) is recycled and provided to the load circuit using the ER technique. Thus, in the proposed SC converter, the definition of active period can be extended to include both Continuous and Termination phases (shown in Fig. 1). In the proposed SC converter, the Charging and Termination phases are also referred to as SCC and ER phases, respectively.

Fig. 3 illustrates the proposed architecture, which consists of a capacitor bank of N capacitors, a digital controller, and a voltage detector. The digital controller governs Charging (SCC), Continuous, and Termination (ER) phases. The voltage detector compares the equivalent voltage of the capacitor bank with the reference voltages in each phase. Using the multiplexer in the voltage detector, one of the two reference voltages (V_{RefCh} and V_{RefDel}) is selected for comparison. An example capacitor bank is depicted by Fig. 4 in detail, which is composed of six capacitors, line voltages (V_{line1} and V_{line2}) and their switches. These switches are controlled by the digital controller to arrange the capacitor bank in various configurations, as required by each of the three phases. Here, V_{line1} is the target voltage that is provided to the load circuit through output switch. On the other hand, V_{line2} is internally used for flexible arrangement of the capacitors in the capacitor bank.

B. INCORPORATING SPLIT-CAPACITOR CHARGING (SCC)

As mentioned earlier, the proposed converter has the capability of integrating both SCC and ER techniques into a single capacitor bank. The integrated SCC-ER converter, thus, can further improve the energy efficiency without incurring area overhead compared to converters using either only SCC [17] or only ER [18]. In the Charging phase of the proposed converter, the SCC technique is used. The goal of SCC is to significantly reduce the energy losses by splitting the capacitor charging process in multiple steps. In order to get high energy efficiency from SCC, the voltage difference among the capacitors is kept as small as possible between the current and the next step. The multi-step arrangement of the capacitors for SCC is maintained in symmetric structures to keep equal voltages on all the capacitors and to ensure no losses due to charge sharing.

During SCC phase, an external voltage source V_{Src} provides energy to the capacitor bank, while the load is disconnected. For example, Fig. 5 shows an SCC procedure for a capacitor bank with six flying capacitors ($N = 6$). It aims to charge all the capacitors to V_{Src}, so it can supply V_{Src} to the load after SCC completes. The following describes four possible charging steps for this example. The first step of SCC phase arranges all the flying capacitors in series (one branch only) as shown in Fig. 5 (a), and each capacitor gets charged from $0V$ to $(1/6)V_{Src}$. In the second step, the capacitor bank is rearranged in two branches, each having three series capacitors to charge each capacitor from $(1/6)V_{Src}$ to $(1/3)V_{Src}$, as shown in Fig. 5 (b). In the third step, the capacitors are rearranged in three parallel branches with two series capacitors in each branch, and each capacitor gets

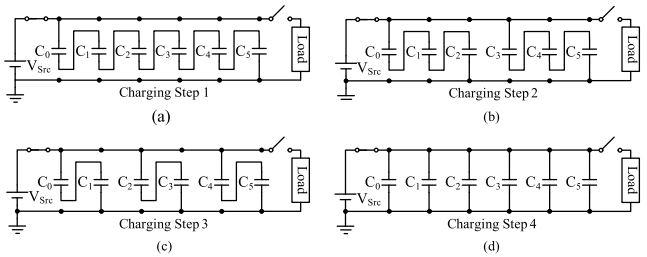

FIGURE 5. Example configuration steps for SCC with $N = 6$ capacitors.

TABLE 1. Maximum number of charging steps for various number of capacitors.

Sr.	Maximum number of SCC Steps.	Number of Capacitors (N)
1	2	2
2	3	4
3	4	6
4	6	12
5	8	24

charged from $(1/3)V_{Src}$ to $(1/2)V_{Src}$, as shown in Fig. 5 (c). Finally, in the fourth charging step, all the capacitors are rearranged in parallel to charge each capacitor from $(1/2)V_{Src}$ to V_{Src}, as shown in Fig. 5 (d). In this way, it is reported in [17] that the charging energy efficiency is as high as 75%, which is significant improvement over conventional one-step charging efficiency of up to 50%.

In order to detect the completion of each SCC step, V_{line1} is compared against a voltage reference, V_{RefCh}. Upon reaching the condition of $V_{line1} = V_{RefCh}$, the current SCC step is concluded, and the next step is triggered by the digital controller. Here, V_{RefCh} is kept slightly lower than V_{Src} to ensure that it takes a finite amount of time for each SCC step.

While the above example shows four possible SCC steps – the maximum number of steps with $N = 6$, it can be reduced to a smaller number depending on the continuous-recharging step. This is because the final step of the Charging phase must be same as the initial step of the Continuous phase, for smooth transition between the two phases.

For example, the SCC steps are reduced to two for Continuous phases of Fig. 2(a)∼2(b), and three for Continuous phase of Fig. 2(c). However, the SCC steps are not reduced for Continuous phase shown in Fig. 2(d). Hence, we can infer that the number of possible SCC steps vary with voltage conversion ratios. The reduction in SCC steps and its impact is discussed later in Section IV.

The maximum number of SCC steps for a given number of capacitors (N) in a capacitor bank can be determined by an algorithm described by the process shown in Fig. 6. The algorithm (given in Appendix I) calculates the maximum number of charging steps for a capacitor bank of N capacitors, by finding all common divisors of N. Here, N is incrementally chosen from a specified range of 1 to N_{max}. Table 1 shows the maximum number of SCC steps calculated

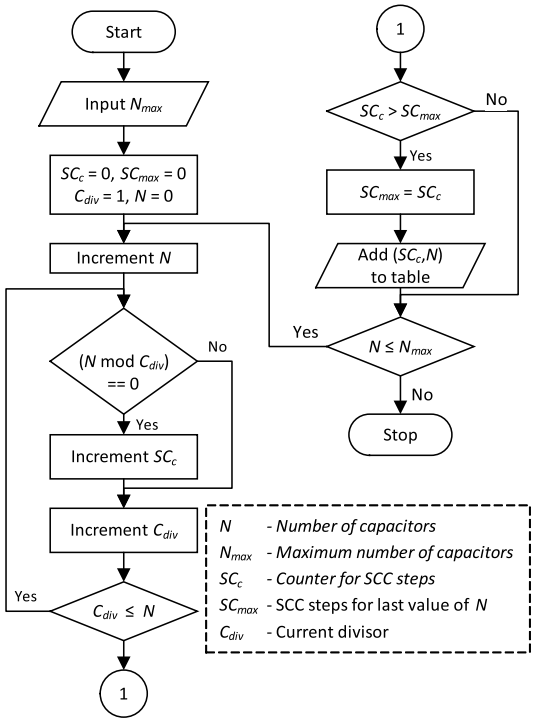

FIGURE 6. Calculating the maximum number of SCC steps for a range $N = 1$ to N_{max} (number of capacitors in the capacitor bank).

by the algorithm for five example capacitor banks of 2∼24 capacitors. Table 1 lists only the optimal number of capacitors to achieve the maximum number of SCC steps. For example, a capacitor bank of $N = 6$, 8, and 10 can provide up to four SCC steps, although Table 1 shows only the result for $N = 6$, which indicates the optimal capacitor bank.

C. ENERGY RECYCLING (ER)

In the ER phase, the capacitor bank goes through a series of configurations to retrieve the remaining energy from the capacitors and provide the recovered energy to the load circuit. Thus, the power source is disconnected during the entire ER phase. In the Symmetric ER which we previously reported in [18], the energy recycling steps are the same as the steps in the SCC phase in the reverse order, for a given capacitor bank of N capacitors. For the example of Fig. 4, the symmetric ER steps are the same steps as Fig. 5 repeated in reverse order. Unlike SCC, however, the voltage source is disconnected while the load is connected during the ER phase. The Symmetric ER, however, has a drawback. Its limited number of recycling steps result in large voltage ripple at the output, due to the abrupt change of voltage in each step. For example, the transition from Fig. 5(b) to Fig. 5(a) would double the output voltage.

The proposed Asymmetric ER can significantly reduce the voltage ripple by reducing the voltage difference between any two consecutive steps. This is attributed to the increased number of recycling steps in the proposed Asymmetric ER compared to the Symmetric ER. In order to achieve

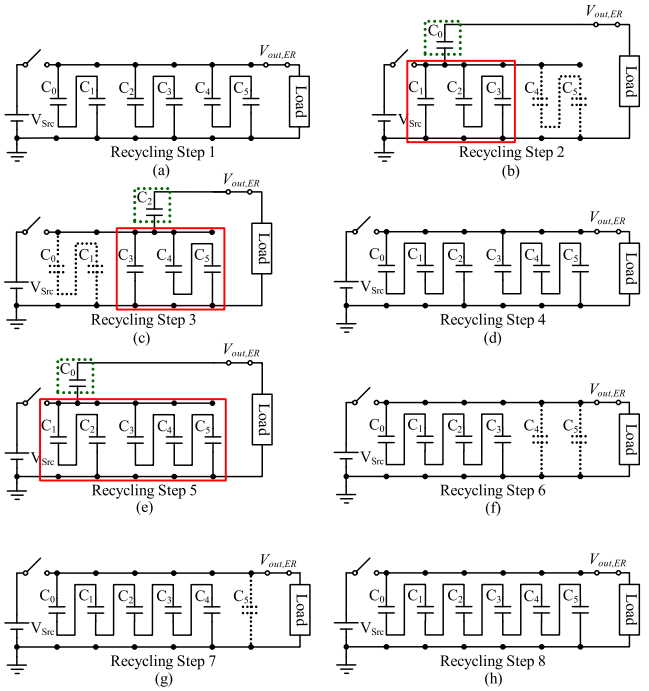

FIGURE 7. Asymmetric ER steps starting from a continuous-delivery step that has three branches with two series capacitors in each branch.

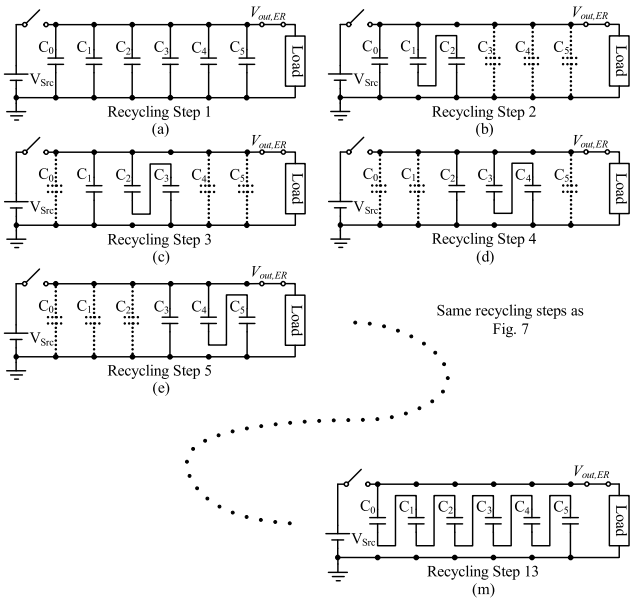

FIGURE 8. Asymmetric ER steps for a continuous-delivery step having six branches each having one series capacitor.

smaller voltage steps, charge sharing is utilized among the capacitors. Asymmetric ER steps are shown in Fig. 7 for the capacitor bank of six capacitors. Since ER phase follows Continuous phase, ER phase must start from the configuration where the Continuous phase ended. For this reason, the proposed architecture configures the first step of the ER phase as the same as the last step of Continuous phase (i.e. continuous-delivery step). For $N = 6$, the asymmetric recycling steps shown in Fig. 7 are only applicable to the continuous-delivery step that has three branches with two series capacitors in each branch as shown in Fig. 2(b) and 2(d).

For the above scenario, if the previous symmetric ER steps are used, it would have produced only three recycling steps. These three steps correspond to Fig. 7(a), (d) and (h), where all the branches are symmetric in each step. In contrast, if the proposed Asymmetric ER is employed, we can add five additional asymmetric steps (Fig. 7(b), (c), (e), (f), and (g)) producing a total of eight steps. In these asymmetric ER steps, during the first iteration, the output voltage is given by $V_{Out,ER} = 2V_C$ (Fig. 7(a)), with each capacitor having the same voltage.

The key idea behind the Asymmetric ER is to introduce additional fractional steps, instead of jumping from $2V_C$ (Fig. 7(a)) to $3V_C$ (Fig. 7(d)) directly. The incremental step taken from $2Vc$ to $2.5V_C$ is shown in Fig. 7(b), where this fractional increment is accomplished by charge sharing. The capacitors conducting this charge sharing are indicated by the red box in Fig. 7(b). This charge sharing process reduces the voltage steps to smaller values. The asymmetric configurations of the proposed converter are constructed by selecting two parallel branches, moving a capacitor from the first branch to the top of the capacitor bank, as shown in the dotted box in Fig. 7(b). After moving the capacitor to the top, the residual capacitors in the two branches would perform charge sharing. The rest of the capacitor bank for the asymmetric configuration can remain reserved for the next steps. For the next recycling step, the top capacitor (C_0) and the capacitor in the first branch (C_1) of the asymmetric structure are disconnected, while remaining capacitors $C_2 \sim C_5$ are used as shown in Fig. 7(c). In this fashion, we can obtain the maximal number of the charge sharing reconfigurations, and consequently achieve the maximal utilization of the remaining energy in the capacitors.

During the ER phase, the controller transitions to the next recycling step, when the output voltage falls below a specified threshold i.e. $V_{Out,ER} < V_{RefDel}$. For the ER steps, we can predict the achievable output voltage using the analytical model introduced in Section IV.

Once all the capacitors in the capacitor bank have been reconfigured for generating $V_{Out,ER} = 2.5V_C$, the next symmetric configuration step (Fig. 7(d)) is selected, which produces $V_{Out,ER} = 3V_C$. In this way, the above process is repeated to produce $V_{Out,ER} = 3.5\ V_C, 4V_C, 5V_C$, and $6V_C$.

Now consider another configuration example for the same capacitor bank of Fig. 4 with $N = 6$. Suppose that the continuous-delivery step has six branches, each having one series capacitor as shown in Fig. 2(a). If the Symmetric ER method is used, we can obtain only four steps illustrated by Fig. 5(d), (c), (b), and (a), respectively. Here, this ordering indicates the sequence of the ER steps. In these recycling steps, the output voltage gets doubled in the second step, boosted by three times in the third step, and pushed up by six times in the fourth step. If we employ the Asymmetric ER method in contrast, the number of recycling steps can

be increased to thirteen steps, as opposed to only four steps of the Symmetric ER case as illustrated by Fig. 8. Consequently, the Asymmetric ER can substantially reduce the output voltage ripple by reducing the voltage boost levels in each ER step. An algorithm to generate asymmetric ER steps, for any given number of flying capacitors and continuous-delivery step, is given in Appendix I. The algorithm divides ER steps in to two different categories i.e. non-charge sharing and charge sharing. Non-charge sharing steps are those where $V_{Out,ER}$ is an integer multiple of V_C. The algorithm terminates with the ER step where all the flying capacitors are arranged in series.

D. DESIGN PROCEDURE OF PROPOSED VOLTAGE CONVERTER

Since both Charging (SCC) and Termination (ER) phases are constrained by the Continuous phase, we can define a design procedure that offers smooth adoption of the proposed architecture for any voltage conversion ratio. The proposed design procedure is as follows:

1. Determine the required voltage conversion ratio.
2. Choose the number of flying capacitors (N), from the list given in Table 1.
3. Select the recharging and delivery steps of the Continuous phase, based on the voltage conversion ratio V_{Out}/V_{Src} (Examples are provided in Fig. 2).
4. Determine SCC steps, using algorithm in Appendix I.
   a. The continuous-recharging step limits the number of useable SCC steps.
   b. If more SCC steps are needed for higher energy efficiency, go back to step 2 and choose a larger capacitor bank.
5. Determine ER steps, using algorithm in Appendix I.
   a. The continuous-delivery step constraints the initial configuration of the ER.
   b. If more ER steps are needed for smaller output ripple voltage, go back to step 2 and choose a larger capacitor bank.

IV. ANALYTICAL MODEL OF THE PROPOSED ARCHITECTURE

This section presents the mathematical analysis of the SCC and ER phases, respectively, of the proposed SC converter.

A. EFFICIENCY OF SCC

First, we analyze the energy efficiency η of SCC when the number of SCC steps is k, the efficiency η can be expressed by

$$\eta = \frac{\sum_{i=1}^{k} (\eta_i E_{si})}{E_s} \tag{8}$$

Here, η_i indicates the energy efficiency of i^{th} step, while E_{si} denotes the energy taken from the source for that step. E_s represents total energy taken from the source, for all the steps combined. The energy efficiency η_i of the i^{th} step can be expressed by equation (9), which had been reported in our previous work [17].

$$\eta_i = \frac{1}{2}\left(1 + \frac{V_{c(i-1)}}{V_{ci}}\right) \tag{9}$$

Here, $V_{c(i-1)}$ indicates the initial voltage of the capacitor in the beginning of i^{th} step, while V_{ci} denotes the final voltage of the capacitor at the end of i^{th} step. From equation (9) it can be observed that the resistance of the switches and the capacitive ESR has no effect on efficiency during SCC.

TABLE 2. SCC steps and their efficiencies for various target voltage ratios ($N = 6$).

Case	Target Voltage Ratio	Step-wise SCC Configurations* & Efficiencies (η_i)				Overall Charging Efficiency (η)	Improvement
		1	2	3	4		
1	1/3, 2/3	1,6 50%	2,3 75%			50(1/3) + 75(2/3) = 66.6%	33.20%
2	1/2, 1, 3/2	1,6 50%	2,3 75%	3,2 83.3%		50(1/6) + 75(1/3) + 83.33(1/2) = 75 %	50%
3	2, 3, 6	1,6 50%	2,3 75%	3,2 83.3%	6,1 75%	50(1/24) + 75(1/12) + 83.33(1/8) + 75(3/4) = 75 %	50%

**In Table 2, capacitor bank configuration is represented as: {Number of branches, Series capacitors in each branch}*

For $N = 6$, Table 2 summarizes the charging efficiencies η_i of each step as well as the overall efficiencies η for various lengths of SCC steps, calculated using equation (8) and equation (9). The reduction in SCC steps was discussed in Section III-A and its impact can be observed by Table 2. Case 3 in Table 2 shows an unrestricted four-step SCC, which charges the capacitor bank up to V_{Src}, and results in an overall efficiency of 75%. Case 2 shows an SCC limited to three-steps, which charges the capacitor bank up to $(1/2)V_{Src}$, and also results in an overall efficiency of 75%. Thus, limiting SCC to three steps does not affect the overall efficiency. On the other hand, Case 1 limits SCC to two steps, charges capacitor bank to $(1/3)V_{Src}$, and reduces the overall efficiency to 66.6%. From this example, we can conclude that significant reduction in SCC steps can reduce energy efficiency. In such cases, choosing a capacitor bank of a larger N can compensate the degraded charging efficiency.

B. EFFICIENCY OF ASYMMETRIC ER

Now we analyze the energy efficiency of the proposed ER phase i.e. Asymmetric ER. To evaluate ER phase and limitation on ER steps, consider the Continuous phases shown in Fig. 2(b) and 2(d), for target voltage ratios of 2/3 and 2, respectively. In these two cases, the continuous-delivery step has three branches with two series capacitors in each branch. The ER phase following such cases starts from the array configuration illustrated by Fig. 7(a), which is in fact the same structure as the continuous-delivery step. The remaining steps follow the sequence illustrated by Fig. 7(b)∼(h).

The output voltage at the start of each recycling step can be calculated as follows. The first recycling-step shown

in Fig. 7(a), has a symmetric structure in this example. The output voltage $V_{Out,ER1}$ of this step is represented by equation (10).

$$V_{Out,ER1}=\left(\begin{array}{l}\left(\frac{2}{6}\right)\times(V_{C0}+V_{C1})+\left(\frac{2}{6}\right)\times(V_{C2}+V_{C3})\\+\left(\frac{2}{6}\right)\times(V_{C4}+V_{C5})\end{array}\right) \tag{10}$$

Here, V_{ci} denotes the instant voltage provided by the i^{th} capacitor C_i at the start of the current step *ER1*.

During the ER phase, as the load circuits draw current from the capacitor bank while conducting their tasks, the output voltage decreases. When the output voltage drops to a predefined threshold voltage V_{RefDel}, the controller reconfigures the capacitor bank to the next ER step. The second recycling-step is shown in Fig. 7(b), whose array structure is chosen as an asymmetric one in this example. The output voltage $V_{Out,ER2}$ of the second step can be calculated by equation (11).

$$V_{Out,ER2}=\left(V_{C0}+\left(\frac{2}{3}\right)\times(V_{C1})+\left(\frac{1}{3}\right)\times(V_{C2}+V_{C3})\right) \tag{11}$$

Here, the factors, (2/3) and (1/3), represent the asymmetric contribution of each capacitor branch to the output voltage produced by the charge sharing effect, respectively.

Similarly, the third recycling step is shown in Fig. 7(c) using an asymmetric structure. The output voltage $V_{Out,ER3}$ of this step can be calculated by equation (12).

$$V_{Out,ER3}=\left(V_{C2}+\left(\frac{2}{3}\right)\times(V_{C3})+\left(\frac{1}{3}\right)\times(V_{C4}+V_{C5})\right) \tag{12}$$

As discussed earlier, these recycling steps can be categorized in two kinds of arrangements. i.e. symmetric and asymmetric arrangement of capacitors. A generalized expression of the output voltage for symmetric arrangement of the capacitors (Fig. 7(a), 7(d), and (h)) in the capacitor bank is given by equation (13).

$$V_{Out,Sym.}=\sum_{k=0}^{p-1}\frac{q}{N}\left[\sum_{j=q.k}^{q.k+q-1}V_{Cj}\right] \tag{13}$$

In equation (13), N indicates the number of capacitors in the capacitor bank, while p represents the number of branches in the array, and q is the number of series capacitors in each branch of symmetric structure. V_{cj} represents the individual capacitor voltage of C_j, which ranges from C_0 *to* C_{N-1}.

For asymmetric recycling steps, we restrict the array configurations by allowing only one capacitor at the top of array. For the above example with $N = 6$, Fig. 7(b), (c), and (e) show all the asymmetric steps. From this example, it can be observed that:

- At most one capacitor can be placed at the top of the array represented by C_i.
- Up to two branches can be placed at the bottom, where m and n represent the number of capacitors in each branch, respectively.

TABLE 3. Comparison of the output voltages of ER steps (analytical model vs. circuit simulation).

Energy Recycling (ER) Steps	Type	Target Voltage (500 mV)	
		Analytical Model	Simulated Results
1	Symmetric	500	500
2	Asymmetric	542	543
3	Asymmetric	443	460
4	Symmetric	573	569
5	Asymmetric	545	543
6	Asymmetric*	596	592
7	Asymmetric*	630	620
8	Symmetric	637	625

** In Table 3, no charge sharing is performed.*

A generalized expression of the output voltage for asymmetric arrangement of capacitors is given by equation (14).

$$V_{Out,Asym.}=\left[V_{ci}+\left(\frac{n}{m+n}\right)\left(\sum_{j=i+1}^{m}V_{cj}\right)+\left(\frac{m}{m+n}\right)\left(\sum_{k=m+1}^{m+n}V_{ck}\right)\right] \tag{14}$$

Here, V_{ci} represents the voltage of the top capacitor, while V_{cj} represents the voltage of each capacitor in the bottom left branch, and V_{ck} represents the voltage of each capacitor in the bottom right branch. In equation (14), m indicates the number of capacitors in bottom left branch, while n represents the number of capacitors in bottom right branch of the asymmetric structure.

There is an exception in asymmetric configurations where charge sharing is not performed, as shown in Fig. 7(f) and 7(g). This is due to the fact that the number of capacitors in the capacitor bank is insufficient to perform charge sharing and there is only one branch in such asymmetric configurations. The output voltage of such exceptional configurations can be represented by a simplified equation defined by equation (15).

$$V_{Out,Asym.(no\ charge\ sharing)}=\sum_{j=0}^{n}V_{cj} \tag{15}$$

Here, n represents the number of series capacitor in the only branch, and V_{cj} represents the voltage of each capacitor.

Table 3 demonstrates the output voltages calculated by the above analytical model for the example of Fig. 7 with eight ER steps. Here, each capacitor was initially charged up to 250 mV, at the start of the ER. To evaluate the accuracy of the analytical model presented in this section, we implemented the proposed SC converter circuit with $N = 6$ capacitors and measured the simulation results using Cadence circuit simulator. Table 3 compares the output voltages obtained from analytical model and the circuit simulations. We can observe that the two results match well with discrepancies less than 3.7%. This indicates that the presented

TABLE 4. Specifications for evalution of the proposed SC converter.

Sr.	Description	Values
1	Input source voltage V_{Src}	750 mV (Nominal)
2	Target output voltage V_{target}	375 mV, 500 mV, and 1.4 V
3	Capacitor bank size C	48 pF
	Unit Capacitor C_{fly}	8 pF
4	Load Resistance R_L	70 kΩ, 125 kΩ, and 130 kΩ
5	Load Capacitance C_L	4 pF
6	Reference for charging V_{RefCh}	$0.98 \times V_{Src} = 735$ mV
7	Reference for Load V_{RefDel}	375 mV, 500 mV, and 1.4 V

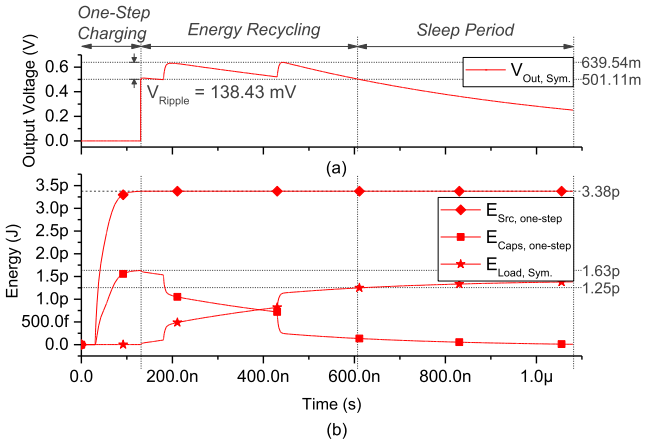

FIGURE 9. Simulation results of SC converter ($N = 6$) with one-step charging and symmetric ER for a target voltage $(2/3)\,V_{Src} = 500$ mV: (a) Output voltage $V_{Out,Sym.}$ (b) Input energy $E_{Src,one-step}$, stored energy in the capacitor bank $E_{Caps,one-step}$, and output energy $E_{Load,Sym.}$.

analytical model can serve as a fast and accurate design tool to determine the output voltage for various capacitor bank configurations during ER.

V. SIMULATION RESULTS

We have implemented an SC converter consisting of six capacitors and a controller based on the proposed architecture, which is illustrated by Fig. 3. It was implemented using a 0.13um CMOS process, and its simulations were carried out using the Spectre simulator of Cadence Design Suite. For the sake of simplicity, we assume that the digital controller is powered separately and that the overhead for the digital controller is negligible. In fact, for the SC converter with small capacitors, the power consumption of the digital controller was less than 10% of the overall power consumption in this simple example. This factor rapidly decreases as the capacitor bank of SC converter becomes larger.

To evaluate the performance of the above SC converter, we configured it with the following specifications shown in Table 4.

The performance analysis is conducted in two parts. The first part is focused on the two transitions i.e. sleep-to-active and active-to-sleep only, and, assesses the performance of one-step charging, SCC, Symmetric ER and Asymmetric ER only. The second part analyzes the SC converter operated in the Continuous phase of various lengths along with the

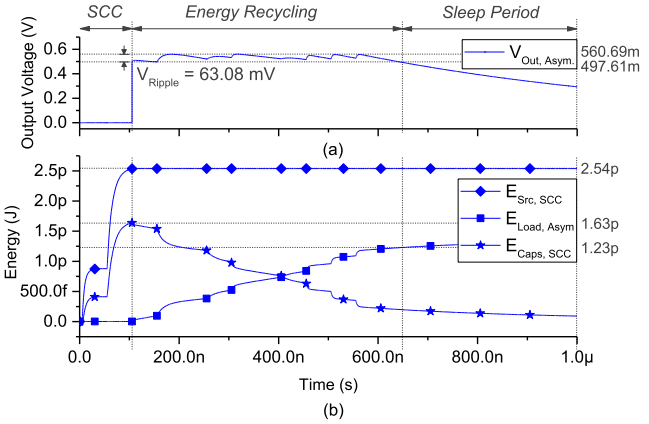

FIGURE 10. Simulation results of SC converter ($N = 6$) with SCC and Asymmetric ER for a target voltage $(2/3)\,V_{Src} = 500$ mV: (a) Output voltage $V_{Out,Asym.}$ (b) Input energy $E_{Src,SCC}$, stored energy in the capacitor bank $E_{Caps,SCC}$, and output energy $E_{Load,Asym.}$.

SCC and Asymmetric ER and compares the efficiency with conventional SC converters.

A. PART I – ENERGY EFFICIENCY AND VOLTAGE RIPPLE FOR VERY SHORT ACTIVE PHASE

In the first part, we have conducted three experiments to highlight the benefits of SCC over one-step charging, and, Asymmetric ER over Symmetric ER. The three experiments target the following voltage conversion ratios:

1) $V_{target}/V_{Src} = 2/3$ and $V_{target} = 500$ mV.
2) $V_{target}/V_{Src} = 1/2$ and $V_{target} = 375$ mV.
3) $V_{target}/V_{Src} = 2$ and $V_{target} = 1.4$ V.

For the first experiment, we configured the voltage ratio as 2/3 with $R_L = 125$ kΩ. Fig. 9 shows the simulation results of the SC converter configured for one-step charging and Symmetric ER, while Fig. 10 shows the simulation results of the converter configured for SCC and Asymmetric ER. Here, E_{Src} represents the energy taken from the energy source, E_{Caps} is the energy stored in the capacitors, and E_{Load} is the energy delivered to the load. The one-step charging of Fig. 9 directly charges all the six capacitors. In contrast, the SCC of Fig. 10 charges the six capacitors in two steps as shown in Fig. 5(a) and (b). Thus, each capacitor is charged to (1/3) V_{Src} which is 250 mV.This comparison demonstrates that the SCC of two steps improved the charging efficiency by 33.07% (from (1.63pJ/3.38 pJ) 48.22% shown in Fig. 9(b) to (1.63 pJ/2.54 pJ)64.17% shown in Fig. 10(b)) compared to one-step charging.

In the ER phase when SC converter is configured to perform Symmetric ER, Fig. 9(b) illustrates that 76.68% of the stored energy is recycled and delivered to the load circuit. For Asymmetric ER, 75.46% of the stored energy is delivered to the load circuit as shown in Fig. 10(b). With only slight degradation in the recycled energy, the Asymmetric ER shown in Fig. 10(a) obtains a ripple voltage that is 75.35 mV smaller than the Symmetric ER shown in Fig. 9(a) (64.08 mV compared with 138.43 mV). This demonstrates that the enhancement of ER with asymmetric configurations

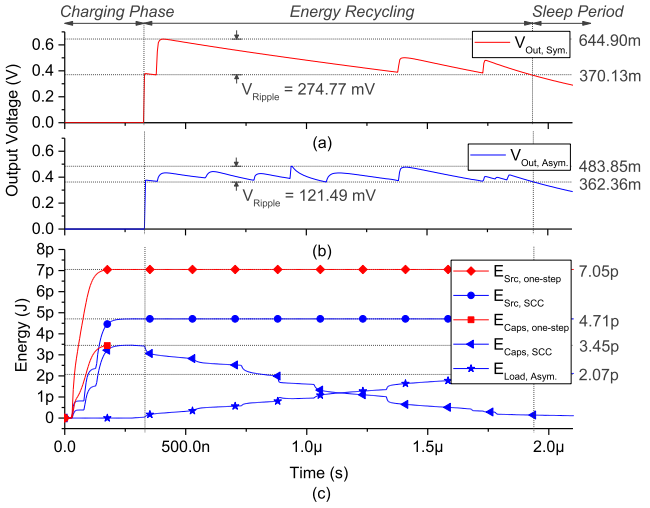

FIGURE 11. Simulation results of SC converter ($N = 6$) for a target voltage (1/2) $V_{Src} = 375$mV : (a) Output voltage $V_{Out,Sym.}$, (b) Output voltage $V_{Out,Asym.}$, (c) Input energy E_{Src}, stored energy E_{Caps}, and output energy E_{Load}.

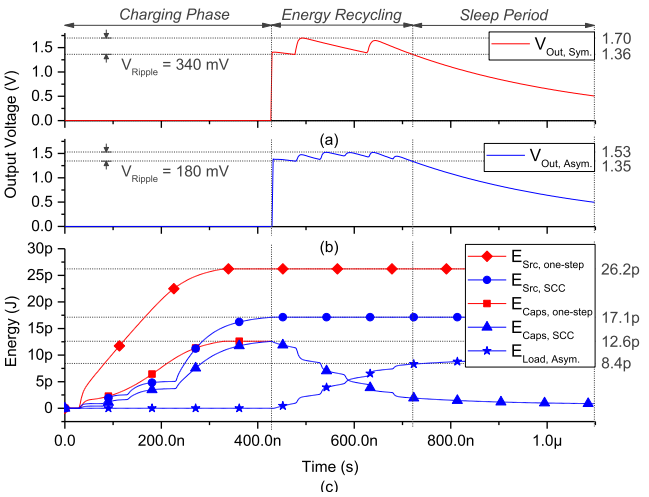

FIGURE 12. Simulation results of SC converter ($N = 6$) for a target voltage (2) $V_{Src} = 1.4$V : (a) Output voltage $V_{Out,Sym.}$ (b) Output voltage $V_{Out,Asym.}$ (c) Input energy E_{Src}, stored energy E_{Caps}, and output energy E_{Load}.

significantly reduces the ripple voltage. The reduction in ripple voltage is achieved at little cost in the energy efficiency, compared with our previous Symmetric ER.

For the second experiment, we configured the SC converter with a voltage ratio of 1/2 with $R_L = 130\text{k}\Omega$. Fig. 11 compares the SC converter configured for one-step charging with Symmetric ER (red curves in Fig. 11), against the SC converter configured for SCC with Asymmetric ER (blue curves in Fig. 11).

During Charging phase, the capacitors are charged in three steps as shown in Fig. 5(a)∼5(c) for the SCC case, while the capacitors are charged in one step for the one-step charging case. For both SCC and one-step charging, all the capacitors are charged to $(1/2)\,V_{Src}$ which is 375 mV. The charging efficiency obtained was 73.24% for the SCC case, whereas it was only 48.93% for the one-step charging case – a notable improvement of 49.68%.

In the ER phase of the SC converter configured with Symmetric ER, Fig. 11(a) illustrates that the ripple voltage is as high as 274.77 mV, whereas the ripple voltage becomes as low as 121.49 mV for the Asymmetric ER shown in Fig. 11(b). In addition, Fig. 11(c) illustrates that Asymmetric ER recycled about 60% of the stored energy and delivered this energy to the load circuit.

For the third experiment, the voltage conversion ratio of 2 with $R_L = 70\text{k}\Omega$ is selected. Fig. 12 compares the SC converter configured with one-step charging and Symmetric ER (red curves in Fig. 12), against the SC converter configured with SCC and Asymmetric ER (blue curves in Fig. 12). In the Charging phase of the SC converter with SCC, the capacitors are charged to the input source voltage V_{Src}(750 mV) in four steps as shown in Fig. 5(a)∼5(d), On the other hand, in case of one-step charging, the capacitors are charged in one step to the desired V_{Src}(750 mV). With SCC, the charging efficiency obtained was 73.68%, while it was only 48.09% with the one-step charging – an improvement of 53.21%.

In the ER phase, Fig. 12(a) reveals that the Symmetric ER produced a ripple voltage of 340 mV. In contrast, Fig. 12(b) illustrates that the Asymmetric ER produced a ripple voltage of 180 mV – nearly half the Symmetric case. In addition, Fig. 12(c) illustrates that 66.66% of the stored energy is recycled by the SC converter with Asymmetric ER.

Therefore, for applications with a very short active period the SC converter with SCC and the Asymmetric ER can substantially reduce the energy losses. It provides a charging efficiency as high as 73.68% during sleep-to-active transition. Also, it can recycle up to 75.42%of the capacitors' remaining energy during active-to-sleep transition before switching to a long sleep period.

In comparison with Symmetric ER, Asymmetric ER recycles 5 ∼ 10% less capacitor energy due to charge sharing. However, large ripple voltage of Symmetric ER needs a linear regulator such as a low dropout regulator (LDO). Such linear regulators would significantly lower the energy efficiency and diminish the gain in energy efficiency offered by the Symmetric ER based SC converters. Therefore, the Asymmetric ER introduced in this paper, when integrated with the SCC, can be an efficient solution for low power circuits with a long sleep period and a short active period. Since asymmetric ER adds more steps and control signals due to additional switches, the complexity of the controller would be increased. However, this complexity is still less than integrating an LDO, at the output to reduce the ripple voltage, in case of symmetric ER.

B. PART II – ENERGY EFFICIENCY FOR LONGER ACTIVE PHASE

This section presents simulation results with Continuous

phase included. In order to measure the improvements provided by SCC and Asymmetric ER, in general applications including the Continuous phase, longer simulations have

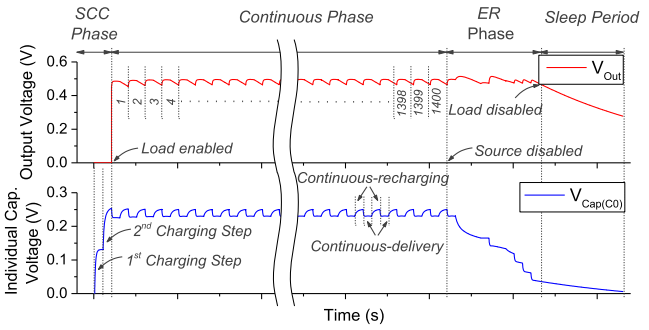

FIGURE 13. Simulation results of the proposed SC converter including all the three phases (Charging, Continuous, and Termination) showing output voltage as well as individual capacitor voltage of the capacitor bank.

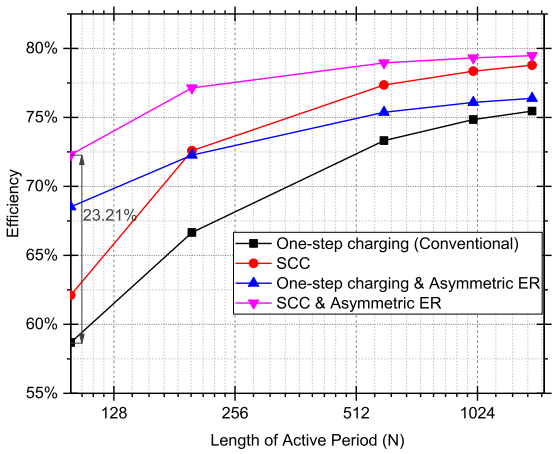

FIGURE 14. Simulation results of SC converter as a Buck converter with a conversion ratio of 500mV/750mV for the four different cases.

been carried out. The simulations were conducted with up to 1400 active cycles during Continuous phase with various buck and boost conversion ratios. For example, Fig. 13 shows an example simulation of the proposed SC converter for buck conversion case with $V_{Src} = 750$ mV and $V_{Out} = 500$ mV. Here, the SC converter starts with the Charging phase, in which SCC technique is used to charge the capacitors in two steps, before proceeding to Continuous phase. In the Continuous phase, continuous-recharging and continuous-delivery steps are repeated 1400 times. The converter, then, shifts to the Termination phase, where the remaining energy in the capacitors bank is recycled and provided to the load circuit. The following simulation experiments are based on similar three phase operations with variable length of the Continuous phase. We first demonstrate the energy efficiency of a buck converter experiment followed by a boost converter experiment.

We conducted extensive simulations with a buck conversion ratio of 500 mV/750 mV with the following four different cases:

1. One-step charging without ER (Conventional)
2. SCC without ER
3. One-step charging followed by Asymmetric ER
4. SCC followed by Asymmetric ER

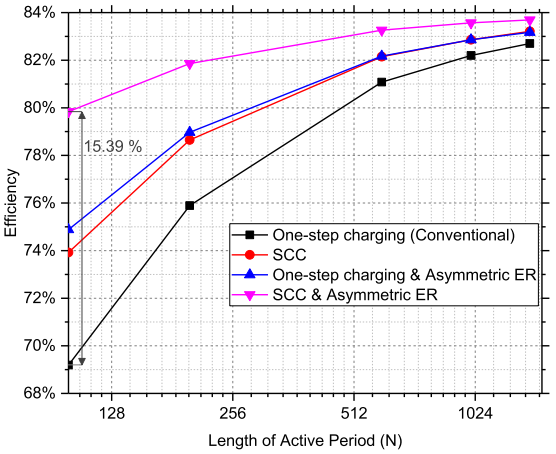

FIGURE 15. Simulation results of SC converter as a Boost converter with a conversion ratio of 1.4V/750mV for the four different cases.

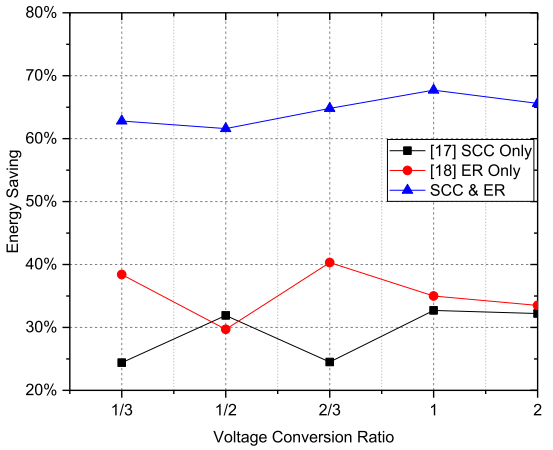

FIGURE 16. Relative gain of SCC and ER compared to conventional SC DC-DC converters.

Fig. 14 compares the energy efficiency of the SC converter among the four different cases, for various lengths of Continuous phase. In Case-4 the improvement in energy efficiency is prominent (23.21% higher than Case-1), when the Continuous phase is relatively short (around 100 cycles). Although the difference in energy efficiency decreases as the active period grows, Case-4 still provides 5% higher energy efficiency than Case-1 even for a long Continuous phase of 1024 cycles.

Similarly, the above set (four cases) of simulations is repeated for a boost conversion ratio of 1.4 V/750 mV and the results are shown in Fig. 15. Like in the buck conversion scenario of Fig. 14, Case-4 provides substantially higher energy efficiency in the boost conversion as well. Here, Case-4 achieves 15.39 % higher efficiency than Case-1 for relatively short Continuous phase of around 100 cycles. As the length of the active period increases the improvement offered by SCC and ER decreases, due to the fact that the energy saved during SCC and ER becomes smaller compared

to $E_{Cont.}$. Here, $E_{Cont.}$ represents total energy during Continuous phase as defined in Section II.

Fig. 16 reveals an important observation that the energy savings provided by SCC and ER vary with different voltage conversion ratios. For certain voltage conversion ratios, SCC offers more savings than ER and vice versa. Therefore, in order to obtain the maximum energy savings, we can conclude that the proposed architecture that integrates both SCC and Asymmetric ER in a single capacitor bank is an efficient choice, since it offers much higher energy savings, the sum of both savings, with no extra hardware overhead.

VI. CONCLUSION

In this paper an on-chip reconfigurable switched capacitor voltage converter has been proposed, which targets ultra-low power applications with short active and long sleep period. Energy losses associated with sleep-to-active and active-to-sleep transitions have been minimized by the proposed converter. The additional energy saving has been provided during the transitions without sacrificing the energy efficiency during Continuous (active in conventional) phase. For sleep-to-active transition, the split-capacitor charging technique has been used to achieve a charging efficiency of 73.68%. Furthermore, in active-to-sleep transition before going to a long sleep period, asymmetric energy recycling technique has been employed to retrieve up to 75.42% of the capacitor's energy. An extensive range of simulations were carried out to show energy efficiency improvements, offered by the converter employing split-capacitor charging and energy recycling, over conventional switched capacitor voltage converter. The simulations have revealed 23.21% and 15.39% improvements in buck and boost conversion cases, respectively, for relatively short active periods.

APPENDIX I

This algorithm generates a list of SCC steps for capacitor sizes ranging from $N = 1$ to N_{max}, by sequentially going through all the entries ($N = 1$ to N_{max}).

```
Procedure SCC_Steps_Calculator (parameter N_max)
{ for N = 1 to N_max //N_max - maximum number of Capacitors.
  {
    SC_C = 0// Counter for SCC steps (Valid divisors).
    SC_max,previous = 0// SCC steps for last value of N.
    for C_Div = 1 to N //Current Divisor.
    {//Calculate SCC steps (valid divisors) for this
        entry
      if ((N mod C_Div) == 0) //If this is a valid divisor
        Increment SC_C //Increment SCC steps count
    }
    if SC_C > SC_max,previous
    {//If this is the largest value SC_C obtained
    so far.
      SC_max,previous = SC_C
      //Create new entry in the table.
      Table[index] = [SC_C, N]
      Increment index
    }
    else
    //Skip this entry
  }
}
```

The following algorithm generates all the asymmetric ER steps for a given size of capacitor bank (Total_Caps) and number of series capacitors in continuous-delivery step (NO_Series_Caps). A MATLAB code, verifying this algorithm, is available at:

- https://github.com/syedasmat/Asymmetric-ER

```
Procedure Get_Asym_ER_Steps (parameter Total_Caps,
                             NO_Series_Caps)
{
ER_Step = 1
While (NO_Series_Caps <= Total_Caps)
{
  // Repeat as long as next ER configuration is possible
  // when number of req. Series caps > Total_Caps,
  // the next ER config. is not possible
  If (IsInteger(NO_Series_Caps))
  {
    // No charge sharing is needed, because
    // NO_Series_Caps is an integer
    // Either make a symmetric structure or,
    // make single branch of NO_Series_Caps
    NO_Leftover_Caps = Total_Caps
    While (NO_Series_Caps < NO_Leftover_Caps)
    {
      Make_a_branch(NO_Series_Caps)
      NO_Leftover_Caps = NO_Leftover_Caps - NO_Series_Caps
    }
    Increment ER_Step
  } //End of If (IsInteger (NO_Series_Caps))
  Else //of If (IsInteger (NO_Series_Caps))
  {
    // Charge sharing is needed, because
    // NO_Series_Caps is a fractional value
    If (NO_Series_Caps >= 2.5)
      NO_T_Caps = 1
    else
      NO_T_Caps = 0
    // Num. of Bottom Left caps
    NO_BL_Caps = floor (NO_Series_Caps) - NO_T_Caps
    // Num. of Bottom Righ Caps = NO_BL_Caps + 1
    // Minimum Num. of Required Capacitors
    Min_NO_Req_Caps = NO_T_Caps +2 × NO_BL_Caps + 1
    // Num. of Leftover capacitors for use
      NO_LO_Caps = Total_Caps
      First_Cap_Id = 0
  While (Min_NO_Req_Caps <= NO_Leftover_Caps)
  {
    //Charge Sharing Asymmetric config. is possible
    Make_CS_Struc(First_Cap_Id, NO_T_Caps, NO_BL_Caps)
    First_Cap_Id = First_Cap_Id + NO_T_Caps +NO_BL_Caps
    NO_LO_Caps = NO_LO_Caps - NO_T_Caps -NO_BL_Caps
    Increment ER_Step
      }
    } //End of else of If (Is Integer (NO_Series_Caps))
    No_Series_Caps = No_Series_Caps + 0.5
  } //End of While (NO_Series_Caps <= Total_Caps)
}
```

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