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Electrostatically-Doped Hetero-Barrier Tunnel Field Effect Transistor: Design and Investigation

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ABSTRACT In this paper, an electrostatically-doped hetero-barrier tunnel-field-effect-transistor (ED-Het-TFET) based on stepped broken-gap (type-III) is simulated, investigated, and compared with the conventionally-doped stepped broken-gap hetero-barrier TFET (Het-TFET). ED-Het-TFET employs GaSb source region, $In_{0.85}Ga_{0.15}As$-based channel-drain regions, and $In_{0.2}Ga_{0.8}As$ as tunnel barrier, with a uniform p-type doping, done initially throughout the device layer. Two metal gates (c-gate and n-gate) with proper workfunctions are used to invert the doping in $In_{0.85}Ga_{0.15}As$ layer to realize n-type channel-drain regions. A 2-D calibrated simulations have shown improvement in the OFF-state current and the I_{ON}/I_{OFF} ratio. OFF-state current in the ED-Het-TFET has improved by more than an order of magnitude. Furthermore, transient analysis reveals that ED-Het-TFET performs on par with its conventional counterpart in terms of rise propagation delay during circuit level implementation. A high I_{ON}/I_{OFF} ratio of $\sim 10^8$ (average subthreshold slope of ~11 mV/decade) is obtained at 20-nm gate length for a very low operating voltage of 0.1 V, enabling it to be a device for future ultra-low power applications.

INDEX TERMS Broken-gap, electrostatically-doped (ED), hetero-barrier-tunnel-field-transistor (Het-TFET), III-V semiconductor.

I. INTRODUCTION

The biggest challenge in the continuous scaling of metal-oxide-semiconductor-field-effect-transistor (MOSFET) device dimensions is the increase in leakage power [1]. The device scaling demands that the supply voltage (V_{DD}) and the threshold voltage (V_T) to be scaled proportionally to keep the overdrive (V_{DD}-V_T) high enough for performance enhancement. However, this results in a significant increase in leakage/static power dissipation in nanoscaled devices [1], [2]. A potential approach to reduce leakage is to scale the sub-threshold slope (S) of a MOSFET. However, S in the conventional MOSFET is limited by Fermi-Dirac distribution of charge carriers and is subjected to the 60 mV/dec subthreshold slope limit [1]–[3]. Steep S devices, like Tunnel-FET, possess reduced leakage current and enables further V_{DD} and device scaling without performance degradation, due to band-to-band tunneling (BTBT) as its current injection mechanism. However, the requirement of ultra-sharp doping profile, both in the MOSFET as well as in the TFET, demands complex and challenging fabrication process. These issues have recently been addressed with the use of electrostatic-doping (ED) as a doping method in junctionless-field-effect-transistor (JLFET) [4] and junctionless-tunnel-field-effect-transistor (JL-TFET) [5]. The basic principle is to modify the background doping i.e., (N^+-N^+-N^+)/(P^+-P^+-P^+) to (P^+-I-N^+)/(N^+-I-P^+) using ED for realizing source/channel/drain regions in n-/p- TFETs. The absence of chemically-doped junctions offer easy fabrication, less variability and enables further scaling [4]–[6].

ED using proper metal workfunctions have also been the working principle of another class of TFETs known as Charge-Plasma based TFETs (CP-TFETs) [7], [8], wherein, the device layer (majorly silicon) remains intrinsic, unlike JL-TFETs. Silicon-based CP-TFETs have received acute attention from the device research community due to its improved analog/radio frequency (RF) parameters [7], [9], [10]. In addition to this, TFETs must also overcome the issue of ambipolar conduction to fit in for the complementary digital logic applications [7], [11], [12]. During ambipolar conduction, TFET allows the drain current to flow at negative gate bias ($V_{GS} \leq 0$), due to BTBT at the channel/drain interface [7], [11]. This lateral-BTBT is similar to what we call the parasitic leakage in case of JLFET [13] and should be

suppressed for effective circuit level implementation. To mitigate the ambipolar issue, various TFET architectures have been examined extensively in literature [7]–[11]. Very recently, we have used the ED concept to realize the dopant segregation layers (DSLs) in Schottky-barrier MOSFETs [14], [15]; source doping in vertically Gaussian-doped TFET on SOI (VG-SOI-TFET) [11]; buried-metal-layer in SOI-based junctionless-FET (BM-SOI-LJLT) [13]—to improve upon the device transfer characteristics and analog/RF performances.

The above-stated devices exhibit good OFF-state characteristics, however, low ON-current is still an issue in silicon-based TFETs characterized by indirect and large bandgap (E_g), and therefore, obtaining high I_{ON}/I_{OFF} ratio at low V_{DD} is a big challenge. With III-V materials having the potential to overcome this low I_{ON}, TFETs based on the staggered-gap (type-II) [16] and broken-gap (type-III) hetero-interfaces [17]–[21] have been explored extensively. Due to high mobility materials and broken band structure, these devices are promising candidate for ultra-low power applications and can result in large I_{ON}/I_{OFF} ratio at scaled V_{DD}. Recent designs include staggered-type GeSn/SiGeSn TFETs in which Sn composition can be finely tuned and correspondingly GeSn transition from indirect to direct bandgap can be achieved [16], [22]. Hence, direct bandgap with small E_g enhances BTBT rate at source/channel tunneling junction in hetero-junction GeSn/SiGeSn TFETs. Along these lines, fabrication of many hetero-structures have been accomplished such as GeSn quantum-well p-type TFET [23]; and InAsSb/GaSb nanowire; and InAs/GaSb nanowire with thin GaInAs inserts using metal-organic vapor phase epitaxy (MOVPE) [24]–[27].

Herein, a two-dimensional (2-D) calibrated simulation study of an ED device based on stepped broken-gap (type-III) structure is performed (namely, ED-Het-TFET). Conventional Het-TFET structure is same as simulated in [19] and [20], and used here as baseline for discussion. Significant improvements in I_{ON}/I_{OFF} ratio and OFF-state leakage have been achieved compared with the conventionally-doped Het-TFET. ED-Het-TFET has the advantage of ED and can achieve high I_{ON}/I_{OFF} ratio with threshold being defined by the onset of band overlap across the barrier [19], [20]. Admitting the fact that ED-Het-TFET fabrication would require advancement in III-V technology, however, its abrupt switching mechanism at low operating V_{DD} is a compelling reason to investigate the device thoroughly.

ED-Het-TFET is a complex structure, however, Register *et al.* [19], Asthana *et al.* [21], and Daley *et al.* [28] have proposed that their device can be fabricated as a vertical hetero-structure stack grown via epitaxy. On similar lines, ED-Het-TFET structure can be fabricated by following the steps given in a US patent granted to Daley *et al.* of IBM [28], as a single layer stack comprising of layers of hetero-materials that have a vertical structural arrangement. Our proposed device uses similar material system as used in [19] and [20], however, Daley *et al.* [28] in their patent has mentioned many suitable binary and ternary compound of III-V material system that can be used to realize a stepped broken-gap structure like ED-Het-TFET.

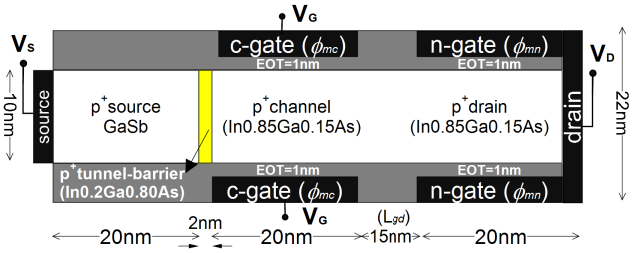


FIGURE 1. Schematic diagram of the ED-Het-TFET with all the dimensions. L_{gd} = 15nm, ϕ_{mc} = 4.8 eV, ϕ_{mn} = 3.1 eV and EOT = 1nm.

This paper is divided into four sections. Section II describes the device structure and operation. Section III discusses various results. Section IV concludes the paper.

II. DEVICE STRUCTURE AND OPERATION

The schematic diagram of the ED-Het-TFET with all the relevant dimensions is shown in Fig. 1. The device layer consists of a 20nm GaSb as source, a 2-nm $In_{0.2}Ga_{0.8}As$ as tunnel-barrier and 55nm extension of $In_{0.85}Ga_{0.15}As$ acting as a channel/drain region, all uniformly p-type doped initially, with a concentration of $1\times10^{18}cm^{-3}$. ED-Het-TFET is a double-gated arrangement, employing two gates on the top (c-gate and n-gate) and two at the bottom. The c-gate (ϕ_{mc}) and n-gate (ϕ_{mn}) have workfunctions of 4.8 eV and 3.1 eV respectively, chosen to induce channel and drain regions doping electrically (ED). The c-gate controls the band modulation over the channel region and is equivalent of a "gate" electrode whereas n-gate induces the drain region electrostatically and is equivalent of a "drain" electrode (as shown in Fig. 1. and Fig. 3(a)). The isolation gap between the c-gate and n-gate electrode (L_{gd}) is 15nm as in [8] and the effective gate oxide thickness (EOT) of 1nm is chosen in all cases [19], [20]. The value of bandgaps chosen for GaSb, $In_{0.2}Ga_{0.8}As$ and $In_{0.85}Ga_{0.15}As$ are 0.726 eV, 1.12 eV and 0.445 eV, respectively [19], [20]. All simulations were performed using Synopsys Sentaurus, version J-2014.09 [20], [29] at room temperature. Fig. 2(a) shows the calibration performed to match the data reported in [19] and [20], by tuning the model parameters. An interface specific non-local BTBT model is used instead of the dynamic non-local BTBT model, owing to the presence of thin barrier along with the added backward compatibility to the BTBT model used in [19] and [20]. Other than the need of non-local mesh, this model is consistent with the dynamic non-local BTBT model. The material specific effective masses for electrons and holes are: 0.041 and 0.4 for source; 0.055 and 0.49 for tunnel-barrier; and 0.029 and 0.43 for channel-drain regions, all in agreement with [19] and [20]. No band gap narrowing model (BGN) is used in the channel because of the absence of mole-fraction

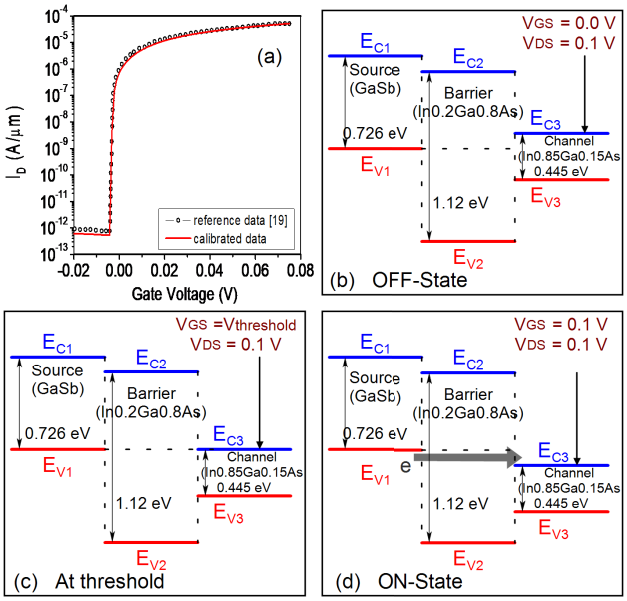


FIGURE 2. (a) Calibration of I_D-V_G characteristic performed using the results reported in [19] and [20] for the 2-nm tunnel barrier. (b) Schematic illustration of a band alignment in a three material-system used in ED-Het-TFET. (a) OFF-state (V_{GS} = 0 V, V_{DS} = 0.1 V), (c) At threshold, and (d) ON-state (V_{GS} = 0.1 V, V_{DS} = 0.1 V).

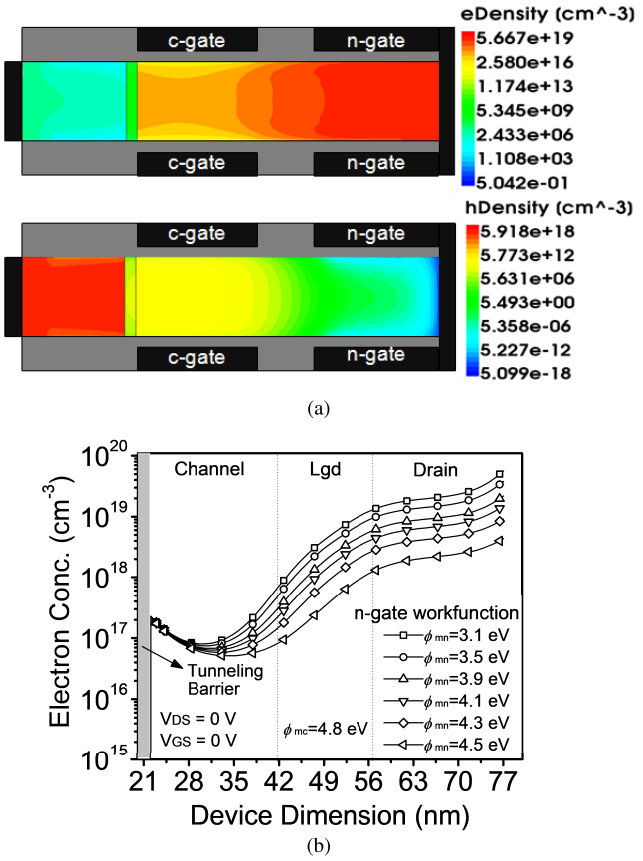


FIGURE 3. (a) 2-D electron and hole concentration profile of the ED-Het-TFET at equilibrium (V_{GS} = 0 V, V_{DS} = 0 V). (b) Electron density on the drain side with varying n-gate workfunction, ϕ_{mn} at equilibrium (V_{GS} = 0 V, V_{DS} = 0 V). L_{gd} = 15nm and ϕ_{mc} = 4.8 eV.

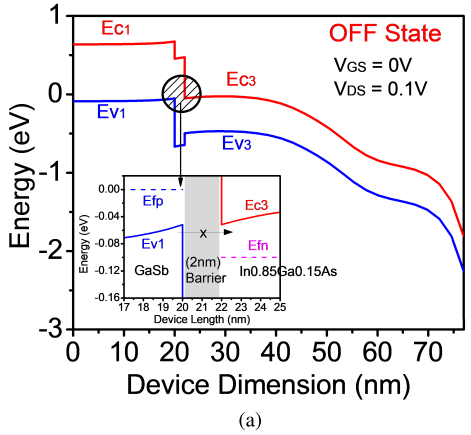
dependent BGN model for $In_{1-x}Ga_xAs$. To include the quantum confinement effects, modified local density approximation (MLDA) model is activated. Thermionic emission current model for hetero-junction interface along with Drift-Diffusion transport model and Shockley-Read-Hall (SRH) recombination model is used.

III. RESULTS AND DISCUSSION

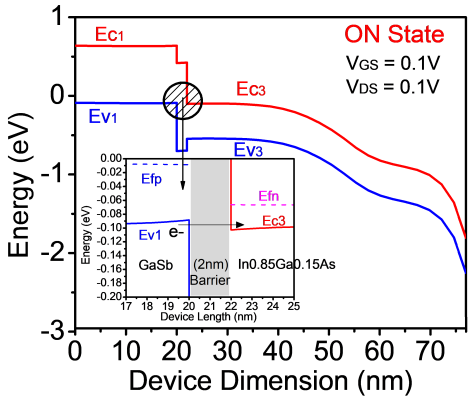
The working principle of the ED-Het-TFET can be explained by observing the schematic of a band alignment in a three material system, as shown in Fig. 2(b), (c) and (d). Herein, the interface formed between the source and the barrier, and the barrier and the channel is of staggered-gap type while the effective interface formed between the source and the channel is of broken-gap type [19], [20]. In OFF-state (V_{GS} = 0 V, V_{DS} = 0.1 V), when zero V_{GS} is applied, the source-VB edge and the channel-CB edge do not overlap ($E_{V\text{-source}} < E_{C\text{-channel}}$) (see Fig. 2(b)), and therefore no tunneling of electrons occurs. As soon as V_{GS} greater than the threshold is applied (see Fig. 2(c)), the tunnel window opens, due to the source-VB edge and channel-CB edge overlap ($E_{V\text{-source}} > E_{C\text{-channel}}$) and the device reaches the ON-state (V_{GS} = 0.1 V, V_{DS} = 0.1 V). Electrons as a tunneling current can now flow across the barrier from source to the channel region as shown in Fig. 2(d).

A. BAND DIAGRAM AND CARRIER CONCENTRATION

Fig. 3(a) shows the electron and hole concentration profile for the ED-Het-TFET at equilibrium. The electron density induced electrically remains close to $\sim 10^{17} cm^{-3}$ and $\sim 5 \times 10^{19} cm^{-3}$ in the channel and drain region respectively while the hole density in the source region is of the order of $10^{18} cm^{-3}$ determined by initial p-type doping. With proper carrier distribution due to the difference in metal electrodes work function, a p^+-barrier-n-n^+ structure is created at equilibrium. Also, to have sufficiently inverted drain region, different n-gate metal work function is used to obtain high electron density, as depicted in Fig. 3(b). It shows that an order of magnitude variation in induced electron density can be obtained ranging from $\sim 10^{18} cm^{-3}$ (at 4.5 eV) to $\sim 10^{19} cm^{-3}$ (at 3.1 eV) when proper n-gate metals are used. Fig. 4(a) and 4(b) shows the band alignment of the proposed device in the OFF-state (V_{GS} = 0 V, V_{DS} = 0.1 V) and ON-state (V_{GS} = 0.1 V, V_{DS} = 0.1 V), respectively. As can be seen in the inset, the instance valence-band on the source side (E_{V1}) and the conduction-band on channel side (E_{C3}) overlaps, across the thin barrier, band-to-band tunneling (BTBT) current starts, resulting in steep turn-on of the device. To be specific, here the turn-on voltage (V_{BtBt}) is taken to be the V_{GS} at which the BTBT starts. A steep rise in drain current (over 7-orders of magnitude) is observed for a 2-nm tunnel-barrier within the critical sub-threshold region. However, the average S of the ED-Het-TFET, when calculated as the



(a)



(b)

FIGURE 4. (a) Energy band profile of the device in the OFF-state ($V_{GS} = 0$ V, $V_{DS} = 0.1$ V). (b) ON-state ($V_{GS} = 0.1$ V, $V_{DS} = 0.1$ V). BTBT starts as soon as the band overlaps across the thin barrier. $L_{gd} = 15$nm, $\phi_{mc} = 4.8$ eV and $\phi_{mn} = 3.1$ eV.

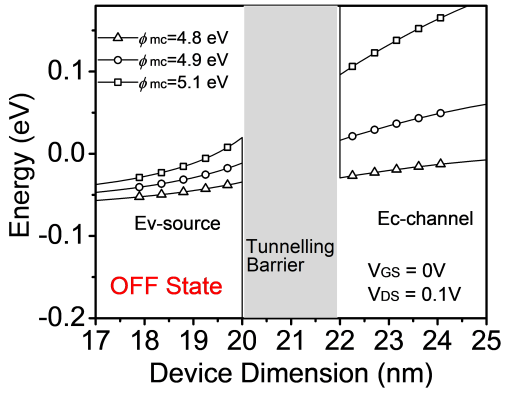
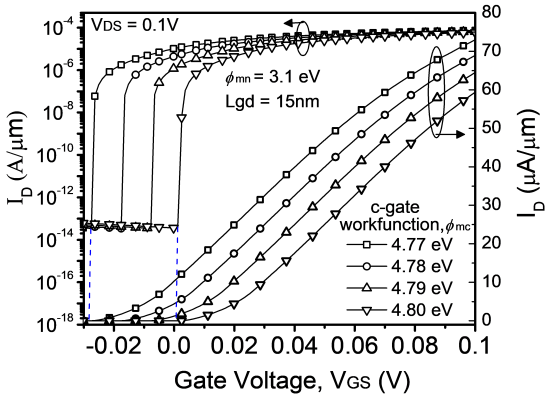
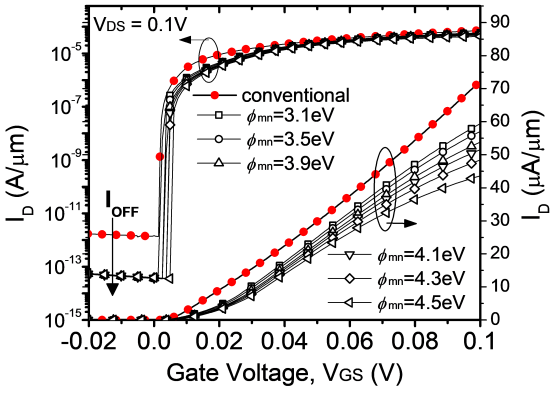


FIGURE 5. Band alignment across the 2-nm tunneling barrier is shown for different values of ϕ_{mc} in the OFF-state. $L_{gd} = 15$nm and $\phi_{mn} = 3.1$ eV.

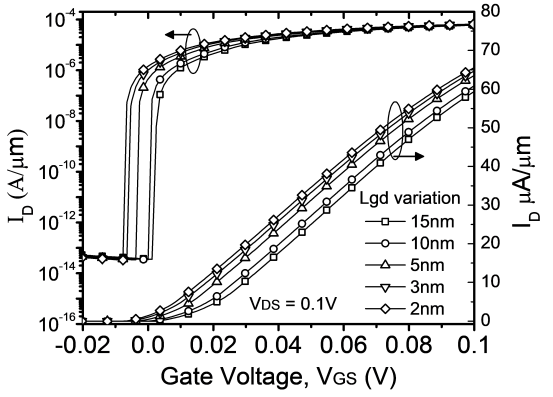
change in the order of the drain current upon the difference of gate voltages at $V_{GS} = V_{BtBt}$ and $V_{GS} = 0.1$V, comes out to be around $\sim 10-11\ mV/dec$ in all cases. Note that there is no need to completely deplete the channel (carriers) in the OFF-state since the current is controlled through thin tunneling barrier, which in this case, depends on the band alignment. The band-alignment across the barrier is a sensitive function



(a)



(b)



(c)

FIGURE 6. (a) I_D-V_G characteristic corresponding to the different values of ϕ_{mc} at $L_{gd} = 15$nm and $\phi_{mn} = 3.1$ eV. (b) I_D-V_G characteristic for different values of ϕ_{mn} at $L_{gd} = 15$nm and $\phi_{mc} = 4.8$ eV. (c) I_D-V_G for various L_{gd} at $\phi_{mc} = 4.8$ eV and $\phi_{mn} = 3.1$ eV.

of ϕ_{mc}, as evident from Fig. 5 (shown here for OFF-state). The relative gap between the valence band on source side (E_{V1}) and conduction band on channel side (E_{C3}), across the barrier, increases with increase in ϕ_{mc}. This, in turn, would affect the voltage at which the device switches from OFF- to ON- state i.e., the V_{BtBt} voltage.

B. TRANSFER AND OUTPUT CHARACTERISTICS

Fig. 6. shows the transfer characteristics of the ED-Het-TFET for different c-gate (ϕ_{mc}), n-gate (ϕ_{mn}) and isolation gap

TABLE 1. On-current variation with key parameters: n-gate work-function (ϕ_{mn}), gate-to-drain separation (L_{gd}) and c-gate work-function (ϕ_{mc}).

ϕ_{mn} (eV)	I_{ON} ($\mu A/\mu m$)	L_{gd} (nm)	I_{ON} ($\mu A/\mu m$)	ϕ_{mc} (eV)	I_{ON} ($\mu A/\mu m$)
3.1	60	15	60	4.77	72.7
3.5	57	10	61	4.78	68.7
3.9	53.8	5	63.5	4.79	64.4
4.1	51.5	3	64.7	4.8	60
4.3	48.4	2	65.6		
4.5	43.6				

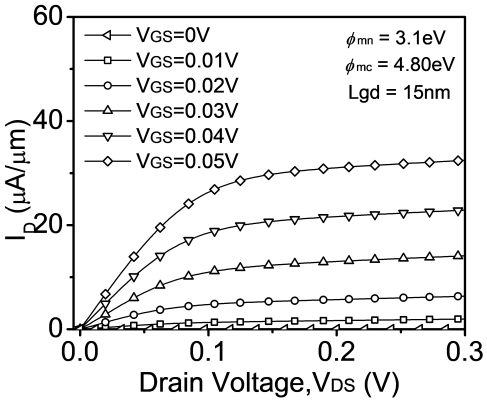


FIGURE 7. Output characteristics of the ED-Het-TFET for $\phi_{mc} = 4.8$ eV, $L_{gd} = 15$nm and $\phi_{mn} = 3.1$ eV.

(L_{gd}) values. It is observed in Fig. 6(a) that smaller ϕ_{mc} results in early turn-on of the device with high ON-current (maximum I_{ON} of $\sim 60\mu A/\mu m$ at 4.8 eV). The increase in I_{ON} for smaller ϕ_{mc} can be attributed to maximum band overlap across the barrier after threshold, resulting in maximum BTBT (can be seen in Fig. 5). Further, a 0.03 eV shift in flat-band due to the change in c-gate workfunction from 4.77 eV to 4.8 eV has resulted in a exact shift of 0.03 eV in the turn-on voltage, V_{BtBt}, as can be seen in Fig. 6(a). The effect of variation in n-gate workfunction (ϕ_{mn}) on the performance of the ED-Het-TFET is shown in Fig. 6(b). The workfunction, ϕ_{mn} has a prominent impact on the electron density (refer to Fig. 3(b)) in the drain region rather than the band alignment across the barrier. This high electron density creates a high-conductive path close to the channel-drain region primarily affecting the device ON-state current instead of the turn-on voltage, V_{BtBt}. To have a fair I_{ON} and I_{OFF} comparison, same V_{BtBt} is used for both the conventional and the proposed structures. The conventional Het-TFET offers better I_{ON} of $\sim 72.5\mu A/\mu m$ while its ED counterpart achieves more than an order of magnitude reduction in the OFF-state current (see Fig. 6(b)). Further, the impact of L_{gd} on I_D-V_G characteristics is plotted in Fig. 6(c). With decreasing L_{gd}, the effective resistance offered by the channel/drain conducting layer decreases, thereby, increasing I_{ON} to a maximum of $\sim 65.6\mu A/\mu m$ at $L_{gd} = 2$nm. The ON-current values obtained for various ϕ_{mn}, ϕ_{mc} and L_{gd} values are listed in table 1. The output characteristic of the ED-Het-TFET reaches good saturation for varying V_{DS}, as shown in Fig. 7.

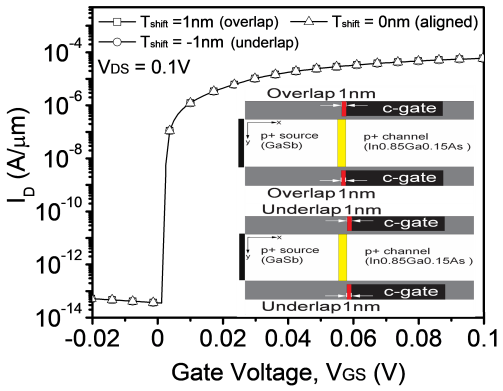


FIGURE 8. Impact of gate metal misalignment on I_D-V_G characteristics of three different structure is plotted: aligned ($T_{shift} = 0$nm), underlap ($T_{shift} = -1$nm) and overlap ($T_{shift} = 1$nm). Corresponding underlap and overlap structure is shown as inset.

C. GATE MISALIGNMENT (T_{shift})

Since c-gate workfunction is an important factor in determining the turn-on voltage (V_{BtBt}) of the device, it is worth exploring the impact of gate misalignment on the device dc characteristics. To study this effect, a shift of 1nm of c-gate metal (both top-gate and bottom-gate) is taken on each side of the tunnel-barrier/channel interface. It is observed that the misalignment has no effect on the V_{BtBt} of the device and the I_D-V_G curves remain identical for all three cases of $T_{shift} = 1$nm (overlap), 0nm (aligned), and -1nm (underlap). ON-state current remains same for all three cases, as evident from Fig. 8.

D. TUNNELING BARRIER WIDTH (T_b)

Fig. 9(a) shows the impact of T_b width variation on the dc characteristics of the ED-Het-TFET. For $T_b = 1.5$nm, the device turns on at negative V_{GS} with I_{ON} reaching up to $\sim 93\mu A/\mu m$. At $T_b = 2$nm, I_{ON} of $\sim 60\mu A/\mu m$ is observed whereas for $T_b > 2$nm (thick-barriers), the tunneling deteriorates, resulting in low ON-current ($\leq 30\mu A/\mu m$) at much higher turn-on voltage. The change in I_{ON} and V_{BtBt} can be explained with the energy band diagrams for various T_b's in the OFF-state, as depicted in Fig. 9(b). It is observed that the BTBT occurs even in the OFF-state at smaller T_b's owing to the rise in the band overlap across the barrier. Hence, for a broken-gap structure with $T_b < 2$nm (at fixed c-gate and n-gate workfunctions), sufficient band-overlap is observed even at $V_{GS} \leq 0$ resulting in the BTBT current. We observe that the band overlap in OFF-state decreases with increase in T_b. For $T_b = 2$nm, there is no band overlap and therefore, the device turns off properly.

E. IMPACT ON PARASITIC CAPACITANCE (CGD)

It is important to analyze the parasitic capacitive distribution as device switching speed depends both on I_{ON} and the capacitances. For silicon-TFETs, gate capacitance (C_{gg}) is completely mirrored by the gate-drain capacitance (C_{gd}), for all regions of operation [30]. Fig. 10(a) plots the C_{gd}

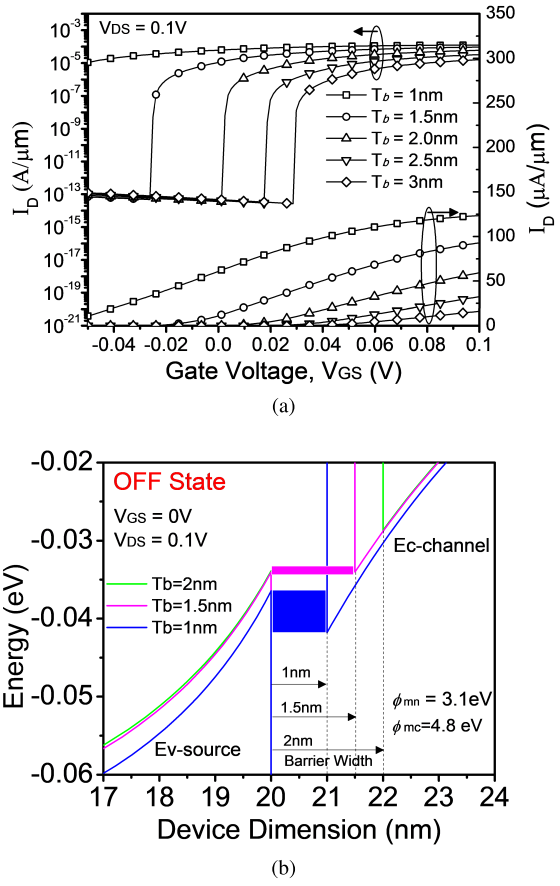


FIGURE 9. (a) Impact of tunnel width variation on the I_D-V_G characteristics. (b) Energy band profile of the ED-Het-TFET in the OFF-state for various T_b's. I_{ON} increases with decrease in tunneling barrier, T_b. For $T_b \leq 1$nm, the device does not turn off, owing to the rise in BTBT due to the increased band overlap between the source-E_V and the channel-E_C. Overlap across the barrier is shown by rectangles (blue–$T_b = 1$nm, magenta–$T_b = 1.5$nm). No overlap is seen for $T_b = 2$nm–green.

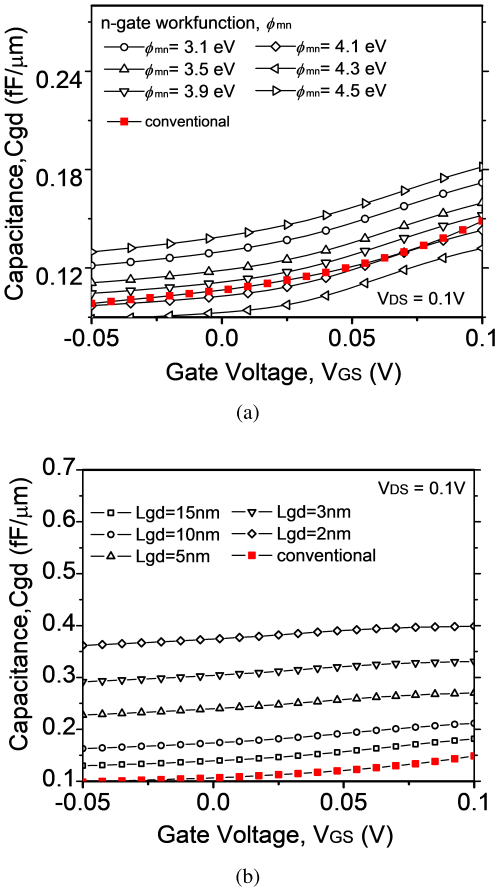


FIGURE 10. (a) Gate-drain capacitance, C_{gd} varying with n-gate workfunctions, ϕ_{mn} for $L_{gd} = 15$nm, $V_{DS} = 0.1$ V and $\phi_{mc} = 4.8$ eV. (b) C_{gd} variation with different L_{gd} for $\phi_{mc} = 4.8$ eV, $V_{DS} = 0.1$ V and $\phi_{mn} = 3.1$ eV.

variation for both the conventional and the ED-Het-TFET with different ϕ_{mn} values as a function of V_{GS}. A small increment in C_{gd} is observed for the V_{GS} swing of 0.1V, irrespective of the ϕ_{mn} chosen. It is observed that the C_{gd} variation of the conventional structure is comparable to that of the ED-HetTFET, for all values of gate bias. The impact on C_{gd} as a function of L_{gd} is plotted in Fig. 10(b), with the conventional one shown for reference. The reduction in L_{gd} increases the coupling between the c-gate and n-gate leading to a significant rise in parasitic, C_{gd}. The maximum value resonates above ∼0.4 fF/μm for the worst possible case of $L_{gd} = 2$nm. The above observations establish the fact that C_{gd} is more sensitive function of L_{gd} compared to the ϕ_{mn}.

F. CIRCUIT ANALYSIS

The circuit analysis of the ED-Het-TFET and the conventional Het-TFET has been performed by designing inverters, as shown in Fig. 11(a). A ramp input of 0.1 V peak-voltage with 10-ps rise/fall time is applied to an inverter designed with the resistive load of $R_d = 20$ kΩ. The switching characteristics of the inverter circuit can be measured in terms of rise/fall propagation delay (τ_{PLH}, τ_{PHL}) and overshoot/undershoot voltage. The absence of fall propagation delay and zero overshoot/undershoot is a big advantage compared to the Si-based inverters [14], [30]. Fig. 11(b) shows the plot of the transient response against the parameter, L_{gd}. In terms of fall in τ_{PLH}, ED-Het-TFET is on par with the conventional Het-TFET, at $L_{gd} = 15$nm. During the input transition from 0-1, ED-Het-TFET with steep rise in drain current (high turn-on trans-conductance, g_m) allows the drop across the resistor to rise, in turn, allowing the output (V_{out}) to fall sharply without any delay. But before switching occurs from 1-0, a comparatively higher C_{gd} results in substantial rise in the rise-propagation delay, τ_{PLH}. Also, as L_{gd} varies from 2nm to 15nm, τ_{PLH} decreases due to smaller C_{gd} offered as shown in Fig. 10(b). Apart from this, another point to notice is the limited output voltage swing with decreasing L_{gd}. This can be understood from Fig. 6(c), which shows considerable drain current flowing at negative V_{GS} for L_{gd} values varying from 2nm to 10nm. This allows a fraction of V_{DD} to drop across the resistor even before the 0-1 input transition occurs. Thus, the device is conducting even in the logic '0' state.

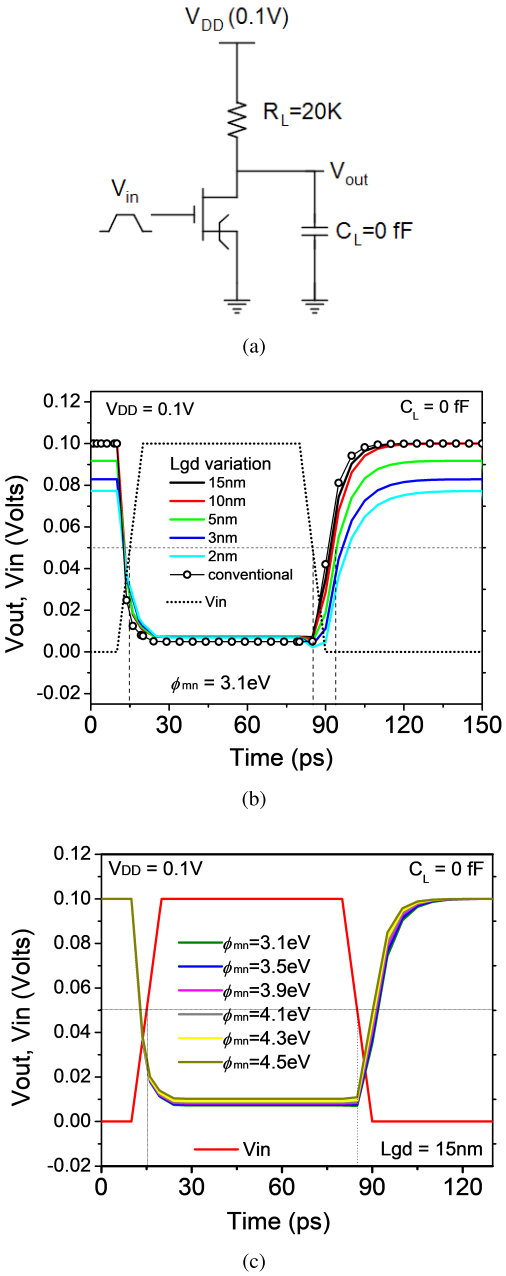


FIGURE 11. **(a) Inverter designed using ED-Het-TFET with resistive load $R_d = 20$ kΩ. (b) Shows inverter characteristic with varying L_{gd}, $C_L = 0$ fF. (c) Shows inverter characteristic for various n-gate workfunctions, ϕ_{mn}, $C_L = 0$ fF.**

Further, Fig. 11(c) shows there is a negligible effect of ϕ_{mn} variation on the inverter characteristics.

IV. CONCLUSION

In this work, we proposed and simulated an electrostatically-doped (ED) device employing stepped broken-gap (type-III) band structure (ED-Het-TFET) and compared it with the conventionally-doped Het-TFET. ED-Het-TFET exhibits the advantage of both ED-based devices and III-V stepped-broken hetero-barrier TFET. We showed that the ED-Het-TFET has improved OFF-state leakage and I_{ON}/I_{OFF} ratio. OFF-state current in ED-Het-TFET is reduced by more than an order of magnitude. We also observed that the parameter L_{gd} turns out to be deciding factor as it affects both the I_{ON} and C_{gd}, critical for deciding the dynamic switching performance. In addition to this, at $L_{gd} = 15$nm, the transient analysis of ED-Het-TFET performs on par with the conventional device.

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