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Thermal-Aware Synthesis of 5G Base Station Antenna Arrays: An Overview and a Sparsity-Based Approach

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ABSTRACT Heat removal capabilities and radiation performances of several sparse antenna array topologies are studied for cooling enhancement in 5G millimeter-wave base station antennas. Both electromagnetic (EM) and thermal aspects are jointly considered for the first time in array layout optimization, and a novel connection between layout sparsity and thermal management is presented. Two types of active electronically scanned arrays (AESAs), based on the traditional and planar approaches, are examined. Thermal management in AESAs is discussed, with a focus on cooling challenges at millimeter waves. Being relatively low cost and low profile while supporting flexible beamforming, passively cooled planar AESAs with fanless CPU coolers are proposed, for the first time, to be used in 5G base stations. Additional cooling for such arrays is achieved by increasing the inter-element distances in the layout. Linear irregular arrays, spiral arrays, thinned arrays, circular ring arrays, and heat sink antenna arrays are revisited with a critical discussion on their EM and thermal performance. The results are compared with regular and square layouts that are used as benchmarks throughout this paper.

INDEX TERMS Antenna synthesis, base station antennas, fifth generation (5G), millimeter-wave communications, passive cooling, sparse arrays.

I. INTRODUCTION

The demanding throughput metrics of 5G [1], [2] can only be achieved with a broad operational spectrum on the order of hundreds of MHz to a few GHz which is extremely difficult to obtain below 24 GHz [3]. However, transmissions in mm-wave have significantly less favorable RF link budgets because of low power amplifier efficiency (less than 20%) [4], [5], reduced receiving effective aperture and decreased diffraction and dispersion effects [6].

To mitigate these drawbacks, large scale antenna arrays with hundreds of elements are expected to be deployed in 5G systems. Using a transceiver behind every antenna element leads to unacceptable amounts of heat dissipation and is associated with high manufacturing costs at this moment. This currently makes hybrid beamforming approaches more attractive compared to digital beamforming [7], [8]. In a nearest future, however, transition to fully digital beamforming is expected in order to handle multiple data streams and simultaneously generate multiple beams from a single array, which increases the capacity of a mobile communication system significantly via Beam-Division Multiple Access [9]. Therefore, in the longer term, with the rapid development of powerful ICs for advanced digital signal processing, it is highly probable that fully-digital beamforming and active electronically scanned arrays (AESA's) will prevail due to their superior performance and beamforming flexibility [10], as it already does now for some military radar applications [11], satellite communications [12], radio astronomy [13], personnel imaging [14], and so on.

Using fully-digital beam forming in antenna array means that each antenna element needs 2 DACs and 2 ADCs (for I and Q channels), 1 PLL, 1 LNA, 1 PA, 1 Tx/Rx switch,

some amplifiers and filters, which should ideally be placed on a single chip. Due to the power dissipated by all these components (mostly by the inefficient PAs), these chips act as volume heat sources. The excess heat originating from these chips should be transferred and removed from the antenna system in order to maintain a safe, long-lasting and reliable operation at the base station. However, as a result of having a separate transceiver chip for each antenna element, high packaging densities of front-end circuitry at mm-waves make integration of a cooling system a challenging task. Moreover, the strict cost and heat removal requirements of high volume 5G base station market favor the use of low-cost, passive cooling strategies via the use of heat sinks, heat spreaders, heat pipes or thermal interface materials (TIM) instead of fans or forced liquids that require the use of electricity [15].

For the antenna synthesis community, the passive cooling strategies in digital beamforming mainly include decreasing the number of the antenna elements (and thus the heat sources) or re-arranging the element (or chip) locations, assuming that the chip positions correspond to the antenna positions in a two-dimensional array. In terms of the array layout, the most straightforward and link-budget efficient way to enhance cooling is to create sparsity by increasing the physical distance between the elements. This is because the dissipated heat from one element causes a temperature rise at all the neighboring elements whose strength decreases with increasing distance. At the same time, no negative impact is seen on the link budget (or EIRP) since the number of elements is kept the same. Since this kind of sparsity may lead to grating lobes or high side lobes of the antenna array, it goes against the low-interference requirement of multi-user communication systems. However, clearly, while synthesizing the array, the radiation requirements (in terms of the array gain, side lobes, beam width, etc.) have to be satisfied as well, which can be addressed by introducing irregularity in the sparse array layouts [16], [17]. Hence, antenna (or chip) layout designs providing passive cooling at base stations must approach the problem from both heat removal capacity and electromagnetic radiation capability aspects.

From the electronic cooling perspective, heat source layout optimization has been recently studied to decrease the maximum temperature and temperature non-uniformity in the domain as much as possible. Initial studies were focused on optimizing locations of a few heat sources or sinks (up to five) using combinatorial algorithms such as Genetic Algorithm and Artificial Neural Network [18], [19] and Particle Swarm Optimization [20]. In recent studies, up to several tens of heat sources were optimally located via Bionic Optimization [21], [22], Simulated Annealing [23] and Convex Optimization [24], which provided certain levels of reduction in the temperature of the domain, depending on the applied boundary conditions (isothermal, convective or adiabatic).

Regarding the antenna arrays' radiation patterns, a large variety of aperiodic (thinned or sparse) array synthesis methods have been introduced recently. Nature-based layouts [25], [26], deterministic or analytical techniques [27]–[29], global or evolutionary optimization algorithms (such as Genetic Algorithms [30], Simulated Annealing [31] and Ant Colony Optimization [32]), Compressive Sampling [33]–[35], Matrix Pencil Methods [36], Constraint Relaxation [37] and Iterative Convex Optimization [38]–[41] are some of the widely used techniques in sparse and thinned array design approaches.

To the best of authors' knowledge, there is no prior work that jointly considers the radiation pattern requirements and heat removal capabilities of 5G antenna arrays. Although thermal-awareness was implied by Aslan *et al.* [38], [39] by pre-defining a guaranteed minimum inter-element spacing in the final layout [38], [39], quantitative thermal analysis has not been performed, which is necessary to understand to which extent the layout optimization method contributes to the array cooling.

In this paper, both electromagnetic radiation and thermal management aspects of 5G base station antennas are jointly studied for the first time by examining various array layouts and element position optimization techniques. The sparsity in the layout is formed by keeping the element number same and increasing the inter-element spacings. Several existing techniques are exploited to create irregularity in the layout with the aim of enhancing the cooling performance and, at the same time, to reduce the high side lobes or grating lobes. Thermal performance for different sparse array topologies are studied and compared. In this work, we use simple, conventional patch antennas that are connected to the chips at the same 2-D locations to avoid practical challenges on chips integration with the antennas. By using smartly designed antenna elements and irregularly clustered sub-arrays instead of the patches, EM performance might be further improved.

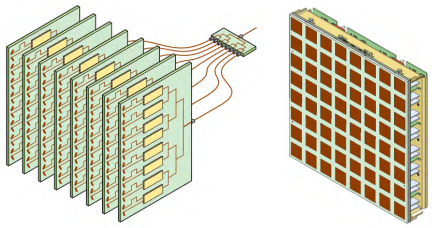
This paper is organized as follows. Thermal management in active electronically scanned arrays (AESA's) are discussed in Section II. The basics of the thermal model that is used in this paper is described in Section III. Thermal and electromagnetic (EM) simulation settings and results are given in Section IV. Section V concludes the paper.

II. THERMAL MANAGEMENT IN AESAs

In this section, firstly, two types of active electronically scanned arrays (AESA's) are presented; namely, traditional AESA's and planar AESA's, with a critical discussion on their advantages and disadvantages. Thermal management in these two types of arrays are then reviewed by providing some examples. Later, the challenges with excessive heat dissipation at mm-waves is shown via several array cooling strategies proposed in the literature. Lastly, a few examples on heat sink antennas are revisited, which may help enhance the cooling in array antennas.

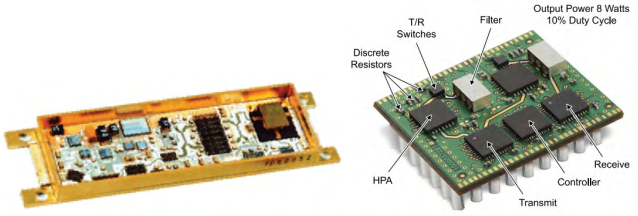
A. TRADITIONAL VS PLANAR AESAs

The development and use of AESA's roots back to more than 50 years of valuable research and implementation, exclusively in space and defense applications [42], [43]. An example of traditional structure of AESA's is given in Fig. 1(a).



(a) (b)

FIGURE 1. Illustration of AESA construction (taken from [42]), (a) traditional approach, (b) planar approach.



(a) (b)

FIGURE 2. Sample AESA T/R modules (taken from [42]) for, (a) a traditional AESA, (b) a planar AESA.

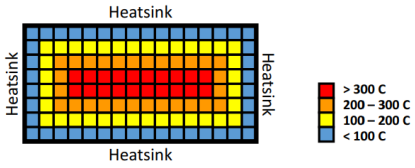


FIGURE 3. Temperature distribution across a traditional 8x16 AESA (taken from [44]).

In such constructions, a number of circuit cards are placed orthogonal to the antenna array. Each card feeds a row of antenna elements with individual transmit/receive (T/R) modules mounted on them. The advantage of this approach can be stated as providing a large surface area for the T/R modules and for the thermal load. A major disadvantage is the need for a large number of RF boards and cabling for signal routing. Moreover, in the case of having large size T/R modules, it could be difficult to make a compact design.

Fig. 1(b) visualizes an alternative approach that, in this paper, is referred to as planar AESA. In this approach, a single multi-layer RF board is used to integrate the antenna elements and RF beamformers. The radiating elements are placed on one side of the board while all the beamforming electronics are mounted directly onto the back of the board. Compared to the traditional approach, this alternative has the advantage of reducing the area of RF boards and the number of connectors and cables. Therefore, planar AESA's can provide low-cost and low-profile apertures, which makes handling and mounting of the arrays more flexible. Due to these advantages, planar AESA's are good candidates for the high-throughput, but low-cost antennas in the first phase of digital 5G systems.

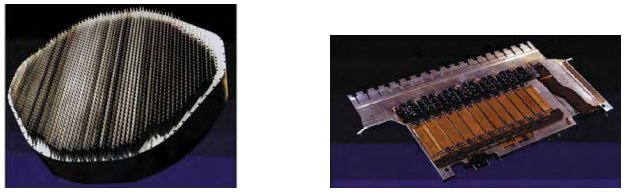
Despite their superiority in compactness, planar AESA's have limited space to fit all the beamforming electronics. With increased frequency, since the spacing between the radiating elements becomes even smaller, the problem of excessive heat dissipation gets more problematic. A possible solution might be adding more functionality into a single IC, which is quite challenging. A more straightforward option is to create a sparsity in the radiating elements and thus to increase the spacing between the T/R modules for passive heat removal, which is the main focus of this paper.

For better understanding and visualization of the described concepts, an active X-band T/R module in a traditional AESA developed by Raytheon for missile defense applications [42] and a low-profile planar AESA T/R module developed for a multi-function phased array radar [42] are shown in Fig. 2.

B. COOLING IN TRADITIONAL AESA's

In [44], the thermal problem in traditional AESA's was discussed by investigating the effect of PA efficiency on the operating temperature of the PAs. The severity of the problem was shown using the PA in [45] as the baseline for LTE signals, which provides around 9% PA efficiency. An 16x8 array was assumed around which an ideal heat sink with 30 degree constant temperature is maintained. The resulting temperature distribution is given here in Fig. 3 which clearly shows that the heat gets trapped in the center of the array, resulting in an unacceptable temperature rise.

Although serious challenges with thermal management occurred recently in the wireless communication area with the introduction of 5G and its intended performance requirements, which has created more interest in thermal management [44], [47], [48], excessive heat dissipation has always been a critical issue for phased array antenna design in such systems as military electronics [49], [50] and space applications [51]. As an example, an X-band airborne phased array antenna [46] is given here in Fig. 4 which shows many microwave modules having transmit and receive circuitry with GaAs power amplifiers that are attached to liquid cooled slats.



(a) (b)

FIGURE 4. An airborne phased array radar antenna (taken from [46]), (a) array aperture, (b) a row of microwave modules on a slat.

C. COOLING IN PLANAR AESA's

It was seen that the heat generated from a traditional AESA gets trapped in the middle region of the array since the cooling is done at the array edges where the heat sink is placed (as shown previously in Fig. 3). Therefore, for such arrays, it is

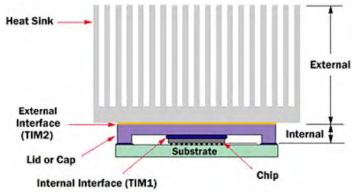


FIGURE 5. Chip package attached to a heat sink (taken from [52]).

necessary to transfer the generated heat towards the edges via cold plates or fluid channels. Thermal management in planar AESA's is different than the traditional counterparts due to the placement of the beamforming and amplification chips. Since the chips are now located at the opposite site of the substrate compared to the radiating elements, external heat sinks can be attached to the chips, without affecting the radiation performance. As seen in Fig. 5, thermal interface materials (TIMs) or some flat plates with large thermal conductivities are used to enhance the thermal conduction and heat spreading from the chip to the lid and heat sink [52].

A sample design with a package mounted on evaluation board with heat sink is shown here in Fig. 6 which presents a low-cost 60 GHz antenna-in-package (AiP) phased array [48].

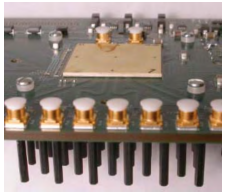


FIGURE 6. Package mounted on evaluation board with heat sink (taken from [48]).

D. ARRAY COOLING AT MM-WAVES

This section is allocated to the existing cooling strategies for mm-wave antennas which are mainly active cooling methods exploiting either forced air or liquid cooling. However, due to the reliability, maintenance and cost issues, such active cooling methods are not suitable for high-volume 5G base station markets. Therefore, having a potential for reliable and low-cost passive array cooling in 5G antennas, CPU coolers are also revisited at the end of the section.

In [53], cooling systems for a Ka-band (operating at 30 GHz) transmit aircraft antenna were designed. TriQuint's GaAs MMIC power amplifier [54] was used to feed each antenna, for which the power dissipation could reach up to 3.8 W in the worst case. Two active cooling strategies were employed; forced air cooling (which is easier to set up than liquid cooling) and forced liquid cooling. The designs were demonstrated for 4x4 arrays. In Fig. 7(a) the forced air cooling design is shown where the heat is spread through the copper cold plate and fans are used to blow air towards the heat sinks. In Fig. 7(b), the liquid is pumped through the

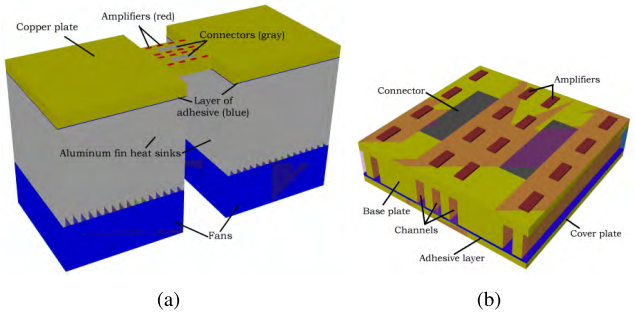


FIGURE 7. Cooling systems for a 4x4 Ka-band transmit antenna array (taken from [53]), (a) forced air cooling, (b) forced liquid cooling.

channels of the cold plate in order to transfer the heat towards the outside of the array where it is then dissipated via heat exchange to a different liquid or air.

Another liquid cooling design was made for a 3x16 element digital beamforming transmitter array at 30 GHz for mobile satellite communication application at Ka-band [55], which is shown here in Fig. 8. Together with the designs given in Fig. 7, this example highlights the challenge of thermal management in mm-wave antennas.

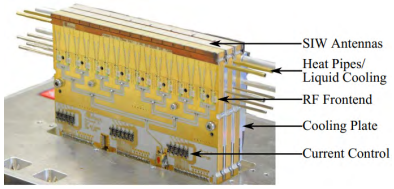


FIGURE 8. Cooling of a 3x16 element digital beamforming transmitter array at 30 GHz (taken from [55]).

Despite being effective in removing the heat, active cooling systems with fans or pumps require the use of electricity and make the system more complex and hard to maintain. On the other hand, passive thermal management is a relatively cheaper and more energy-efficient solution. However, since the heat is removed only passively via natural convection by utilizing only heat spreaders or heat sinks, it is not easy to achieve thermal performance similar to that of the active counterparts unless there is sufficient surface area that is in contact with outside.

To achieve fully-passive cooling in 5G base station arrays, CPU coolers (without fans) can potentially be used in planar AESA's, for which the heat sink can be attached to the chips at the opposite side of the radiating elements. Although they are bulky and heavy, the heat sink modules for CPU coolers are able to provide competitive results in heat removal when compared to the active systems [59].

A sample CPU cooler is illustrated in Fig. 9 which is the CPU processor package of Fujitsu Primepower2500 [56]. Fig. 10 shows how the heat can be absorbed from the chips by the heat pipes (which are totally passive with low thermal resistance and efficient heat transfer) and transported to the fin stack which is cooled via natural convection, and a sample CPU cooler fin stack from FSP Windale [58].

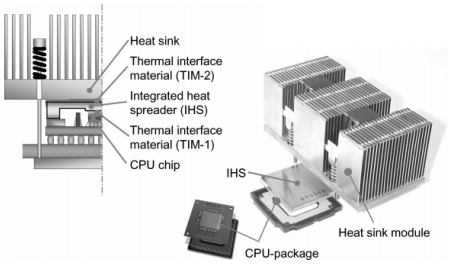


FIGURE 9. CPU processor package of Fujitsu Primepower2500 (taken from [56]).

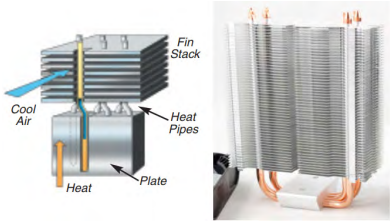


FIGURE 10. CPU cooling via heat pipes and a remote fin stack (taken from [57] and [58]).

E. COOLING ENHANCEMENT AT ANTENNA ELEMENT LEVEL

There are also a few techniques that focus on cooling on the antenna element level instead of the array (or system) level. These techniques are briefly covered in this section and their suitability for AESA's are discussed.

An active heat sink patch antenna was proposed in [60]. The idea was to create a heat spreader connecting the transistor to the radiating patch, as seen in Fig. 11. It was found that such an antenna is able to provide a desirable radiation and thermal performance at the same time. Therefore, it could be a good alternative to exploit heat spreaders between the chips, ground plane and the radiating elements in planar AESA's for cooling enhancement.

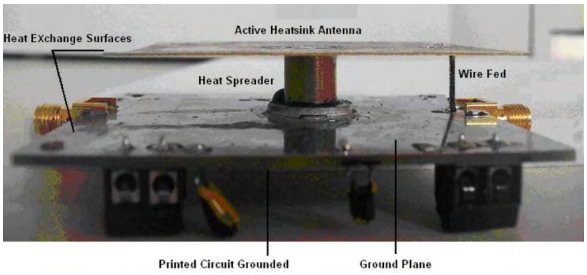


FIGURE 11. RF transmitter with the heat-sink patch antenna using a heat spreader (taken from [60]).

Other techniques concentrate more on the finned or fractal element structures for dual (electromagnetic and thermal) functionality [61], [62]. Examples of such antennas are provided in Fig. 12. Although their structure can be optimized for a certain desired radiation pattern, they are not suitable for flexible beam forming as required by AESA's.

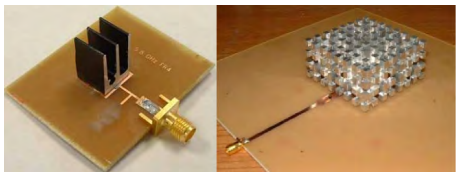


FIGURE 12. Finned and fractal heat-sink antennas (taken from [61] and [62]).

III. THERMAL MODEL

The thermal model that is used in this paper is a basic two-resistor compact thermal model whose guidelines are standardized by JEDEC in [63] using junction-to-case and junction-to-board thermal metrics. Although other (and more accurate) complex approaches do exist (such as the DELPHI model [64]), the two-resistor model is chosen here because of its simplicity and intuitiveness. The basics of this model are shortly covered in this section for a smooth transition to the simulation environment.

The two-resistor model of JEDEC consists of three nodes, as seen in Fig. 13. The thermal problem is re-formulated using a thermal resistance network which is similar to electrical circuit modeling. The junction node represents the junction of the IC where the heating power, P_h, is applied. The case node represents the top of the package. The equivalent thermal resistance between the junction and the top of the case is given by θ_{JCtop}. The board node represents the contact of the package with the PCB. θ_{JB} is the equivalent thermal resistance between the junction and the board. It is worthy of note that, in this model, it is assumed that the heat flows through the case node and the board node. Therefore, the heat flow through the sides of the package is not taken into account.

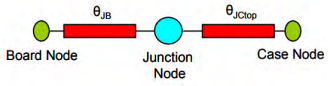


FIGURE 13. Two-resistor thermal model of JEDEC (taken from [63]).

The top of the package is in contact with a thermal interface material and a heat sink in passively cooled planar AESA's, which is equivalent to a case-to-ambient resistance. The PCB has several layers including the ground plane and the radiating elements are on the opposite side. The overall topology of PCB and the radiating elements can be included in an equivalent board-to-ambient resistance. Fig. 14 presents the complete network of such a thermal model.

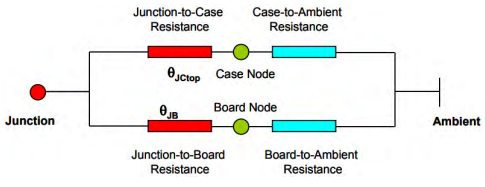


FIGURE 14. Complete equivalent thermal resistance representation of the two-resistor model (taken from [63]).

For co-thermal-EM array simulation, it is needed to represent the two-resistor model in 3D. Fig. 15 explains how this is achieved. The junction node is represented by a block formed by a high conductivity material (such as aluminum), while the equivalent thermal resistances are replaced with surface resistances on the top and bottom of the block for θ_{JCtop} and θ_{JB}, respectively. The sides of the block are insulated to prevent the heat flow through the sides.

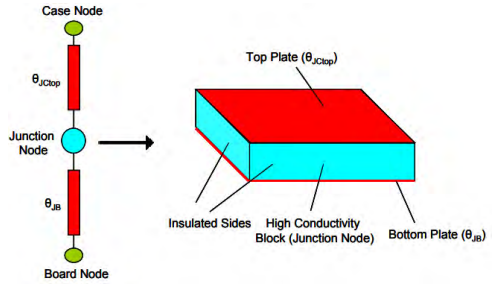


FIGURE 15. Representation of two-resistor model in a simulation environment via a block-and-surface resistance approach (taken from [63]).

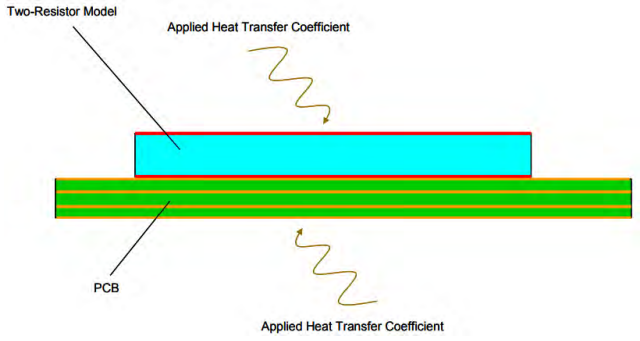


FIGURE 16. Application of two-resistor model in conduction-based simulation tools (taken from [63]).

From a broad point of view, it can be said that the 3D thermal modeling tools are divided into two main categories; conduction-based tools and computational fluid dynamics (CFD) tools. In this paper, CST Microwave Studio and CST MPhysics Studio are used for the EM and thermal simulations, respectively. The thermal solver in CST is a conduction-focused tool for which the solid portions in the design are handled with the governing equations for conduction heat transfer, but the airflow effects are not solved directly. Instead, they are represented by equivalent heat transfer coefficients (h.t.c.'s) at the solid-air interfaces, as shown in Fig. 16.

In planar AESA's, the applied h.t.c. at the upper part of the junction, which is equivalent to the case-to-ambient resistance shown in Fig. 14, indicates how much heat is removed via the heat sink. Although the exact value of h.t.c. depends on the ambient temperature, the exact surface area of the case and the average temperature of the case surface, for mm-wave packages around 30 GHz, it is on the order of thousand Watts per meter-square Kelvin (1000 W/m^{2}K) under the passive CPU cooler conditions [59]. On the other hand, the PCB surfaces that are in contact with air are cooled only via natural convection, for which the approximate heat transfer coefficient is on the order of ten Watts per meter-square Kelvin (10 W/m^{2}K) [63].

IV. SIMULATION SETTINGS AND RESULTS

This section presents the thermal and EM simulation results of several antenna (or chip) layouts in planar AESA's. The analyses are made via parametric studies considering different heating power, P_h (which is the power dissipated per RF channel), and h.t.c's that represent the heat removal capability of a heat sink that is attached to the chips. Simple patch antennas are used in the simulations. At this point, it is worth noting that using optimized antenna element structures or clustered sub-array arrangements [65], [66] instead of the conventional patch antennas could potentially improve the EM performance of the array.

First, the simulation settings in CST and realization of the 3D model are described. Second, the thermal and EM performance of a single element in a unit cell is studied. The section is continued with the analyses and discussions on several array topologies that are based on arrays of regular and irregular linear arrays, spiral arrays, sparse circular arrays, thinned arrays and heat sink antenna arrays.

A. SIMULATION SETTINGS IN CST DESIGN STUDIO

The design of a unit cell structure is visualized in Fig. 17. Fig. 17(a) shows the back side of the unit cell in which the conducting aluminum block representing the IC junction is visible. The sides of the block are isolated with vacuum. Resistive sheets are used at the top and bottom of the block. The substrates for the chip and the patch antenna are also shown together with the ground plane. Fig. Fig. 17(b) presents the front side of the cell for which the radiating patch (with tuned dimensions to obtain the center frequency, f_c, at 28.5 GHz for the arrays) is seen. Locations of the feeding probe that is used for EM simulations and the heat spreader

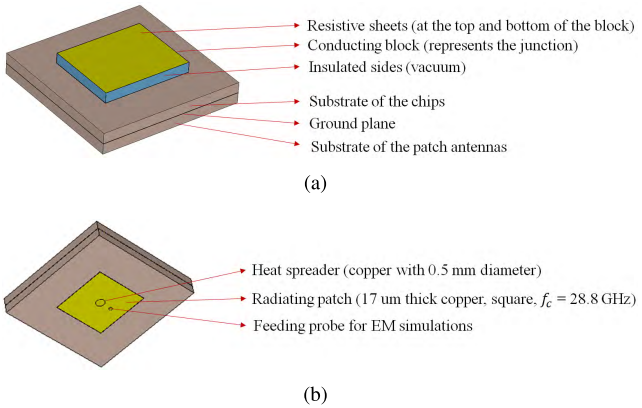


FIGURE 17. Design of a unit cell in CST, (a) back side with a chip, (b) front side with a patch.

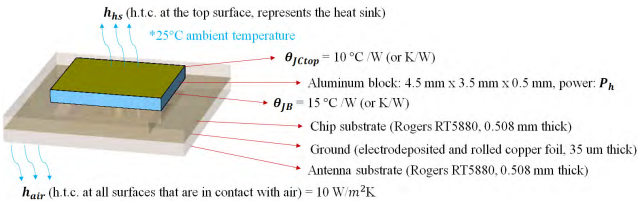


FIGURE 18. Realization of the two-resistor model in CST and selected parameters.

(used only in Section IV-B and Section IV-H) are also visible. The diameter of the heat spreader is taken as 0.5 mm in all the cases analyzed in Section IV and the matching of the antenna is achieved for this selection in the EM simulations.

Realization of the two-resistor model and several parameter values that are common to all simulations presented in this paper are provided in Fig. 18. Apart from the fixed patch dimensions (given in Section IV-B), it is assumed that the chip size is 4.5 x 3.5 x 0.5 mm^3, θ_{JCtop} is equal to 10 K/W and θ_{JB} is taken as 15 K/W. Note that these values are taken as a reference which should be modified depending on the particular chip to be used. In addition, both for the antenna and chip, Rogers RT5880 substrate (with 0.508 mm thickness) is used, considering its low cost and sturdiness. The ambient temperature is taken as 25 degree Celsius. Heat transfer coefficient (h.t.c) for all the surfaces that are in contact with air (h_{air}) and cooled via natural convection is assumed to be equal to 10 W/m^{2}K. The emissivity coefficient at all the surfaces is assumed to be equal to 0.9 (emissivity represents the energy emitted via thermal radiation, whose effect is negligible compared to the convective cooling). The heating power generated by each chip (P_h) and the equivalent h.t.c. representing the heat sink (h_{hs}) are varied for several cases that are used in the parametric studies throughout the paper.

B. SINGLE ELEMENT IN A UNIT CELL

In this section, simulation results for a single antenna element and a chip in a unit cell with dimensions 7 x 7 mm^2 are given. P_h = 3 W is assumed. Fig. 19 presents the thermal simulation results for such a structure with varying h_{hs}. A case with no heat sink is defined in Fig. 19(a) with h_{hs} = 10 W/m^{2}K. Fig. 19(b) shows an ideal active cooling scenario for which $h_{hs} = 10^5$ W/m^{2}K, which is not realizable in practice for low-cost 5G products. A sample passive CPU cooling with h_{hs} = 3000 W/m^{2}K is presented in Fig. 19(c). For the same CPU cooling case, a heat spreader is added in the middle of the radiating patch in Fig. 19(d). The operational frequency band is centered at 28.8 GHz for the unit cell considering the slight shift in the array antennas which gives a center frequency of 28.5 GHz. This results in the patch dimensions 3.13 mm x 3.13 mm without the heat spreader and 3.20 mm x 3.20 mm with the heat spreader.

In Fig. 19, it is seen that when there is no heat sink, the junction temperature can reach up to 750°C, which is unbearable. This clearly shows the necessity in attaching heat

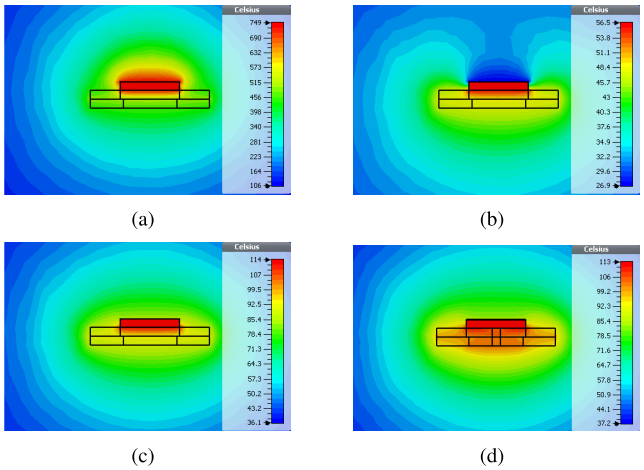


FIGURE 19. Temperature distributions for a single element along the vertical cut at the center of a 7 mm x 7 mm unit cell with P_h = 3 W, (a) no heat sink (h_{hs} = 10 W/m^{2}K), (b) ideal active cooling ($h_{hs} = 10^5$ W/m^{2}K), (c) sample CPU cooling (h_{hs} = 3000 W/m^{2}K), (d) CPU cooling with a heat spreader (h_{hs} = 3000 W/m^{2}K).

sinks to the IC packages in planar AESA's. For an ideal cooling, the maximum temperature becomes 56.5°C, which is quite good when compared to the ambient temperature of 25°C. However, such an ideal system cannot be realized in practice. A more suitable and passive cooling via a CPU cooler results in 114°C maximum temperature. Using a heat spreader helps distribute the heat through the ground plane and the patch, as seen in Fig. 19(d). For the given settings, the spreader provides only 1°C additional cooling, without affecting the radiation pattern and the matching of the antenna (see Fig. 20 and Fig. 21). The improvement could get better for different parameter settings, especially when the heat flow through the substrate is larger or the patch dimensions are increased. Besides, the improvement in the case of antenna arrays is still to be seen. Therefore, the effect of exploiting heat spreaders in arrays is discussed later in Section IV-H.

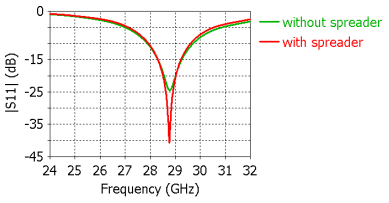
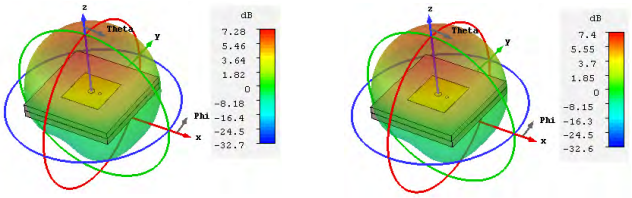


FIGURE 20. Reflection coefficient of a single element in a unit cell with and without the heat spreader.

Although simulations with a single element give some hints about the thermal control on the level of each chip, the maximum temperature values computed here will increase once antenna arrays are considered, which is due to the contribution of all the neighboring elements on the total temperature field. Therefore, next, thermal and EM simulation results are given for several array topologies that can be used in 5G.



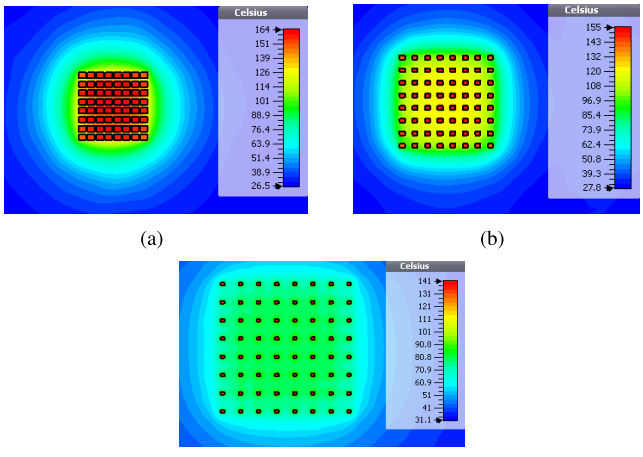
(a) (b)

FIGURE 21. Realized gain of a single element at the center frequency of 28.8 GHz, (a) without the heat spreader (copper filling is replaced by RT 5880 in the simulation), (b) with the heat spreader.

TABLE 1. A parametric study on $T_{\max}$ with the 8x8 regular square array layout by varying P_h, h_{hs} and d_e.

Case #	*P_h (W)	h_{hs} (W/m^{2}K)	d_e (λ)	$T_{\max}$ (°C)
C-1	2	1000	0.5	164
C-2	2	1000	1	155
C-3	2	1000	2	141
C-4	2	3000	0.5	86
C-5	2	3000	1	84
C-6	2	3000	2	81
C-7	3	1000	0.5	232
C-8	3	1000	1	218
C-9	3	1000	2	197
C-10	3	3000	0.5	117
C-11	3	3000	1	114
C-12	3	3000	2	109

* The dissipated heat per channel depends heavily on the EIRP requirements of the system. The values used here are set to relatively higher values than those of a typical small-cell base station serving one user at a time, with the objective of providing sufficient EIRP to more concurrent users per array and/or larger cells, for which the cooling problem becomes significant.



(a) (b)

(c)

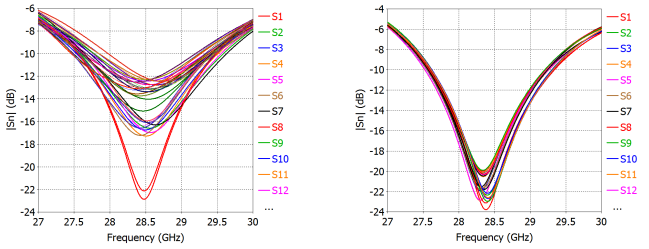
FIGURE 22. Sample temperature distributions with passive CPU cooling for the 8x8 regular square array along the horizontal cut in the middle of the conducting blocks representing the junctions, (a) Case C-1, (b) Case C-2, (c) Case C-3.

The results of the parametric study with the 8x8 regular array layouts are given in Table 1. Fig. 22 provides sample temperature distributions at the IC junctions for Cases C-1, C-2 and C-3 for better visualization of the results.

C. REGULAR ARRAY LAYOUTS

As a start, a parametric study for 8x8 regular square array layouts has been performed by changing the heat dissipated at each RF channel (P_h), equivalent h.t.c of the passive CPU cooler (h_{hs}) and the spacing between the elements (d_e). Center frequency of 28.5 GHz has been used in calculation of λ, and thus, the physical locations of the chips. At the output, the maximum junction temperature for the whole array ($T_{\max}$) has been computed which is given by the highest temperature at the aluminum blocks. Note that, although it has been experimentally seen that the effect of increased substrate dimension on $T_{\max}$ is very small (less than 1°C), the substrate and ground plane dimensions are equal to 18λx18λ in each case for fairer thermal comparison among all the cases with different aperture sizes.

EM simulations have also been performed for the same 8x8 regular patch arrays with $d_e = 0.5\lambda$, $d_e = 1\lambda$ and $d_e = 2\lambda$. As for matching, the active reflection coefficients have been computed to see the center frequency and operational bandwidth. The results for the two cases with the smallest and largest inter-element spacings are given in Fig. 23 for the broadside beam, which confirms that the arrays are nicely matched at the center frequency of 28.5 GHz with a bandwidth of more than 1 GHz.



(a) (b)

FIGURE 23. Active reflection coefficients at each port of the 8x8 regular square array for the broadside beam, (a) $d_e = 0.5\lambda$, (b) $d_e = 2\lambda$.

Lastly, the realized gains for such arrays are provided in Fig. 24 for broadside beams. The formation of grating lobes is clearly seen in Fig. 24(b) and Fig. 24(c) for which $d_e = 1\lambda$ and $d_e = 2\lambda$, respectively. On the other hand, Table 1 shows that increasing the inter-element spacing helps increase the cooling performance, whose extent depends very much on the selected parameters such as the heating power of the chip and the capability of the attached heat sinks. This trade-off between the EM and cooling performance is the motivation to search for alternative array layouts that are capable of yielding satisfying outcomes in both EM and thermal aspects. Examples of such layouts are given next employing several techniques that were previously addressed in the literature.

D. ARRAY OF LINEAR IRREGULAR ARRAYS

From Fig. Fig. 24(b) and Fig. 24(c), it was seen that increasing the inter-element spacing for cooling enhancement leads to grating lobes in the radiation pattern. In the case of having users sharing the same time-frequency resource and located in the directions of grating lobes, the interference towards those users is going to be very high. Zero-forcing or orthogonal beam forming are commonly used digital beamforming algo-

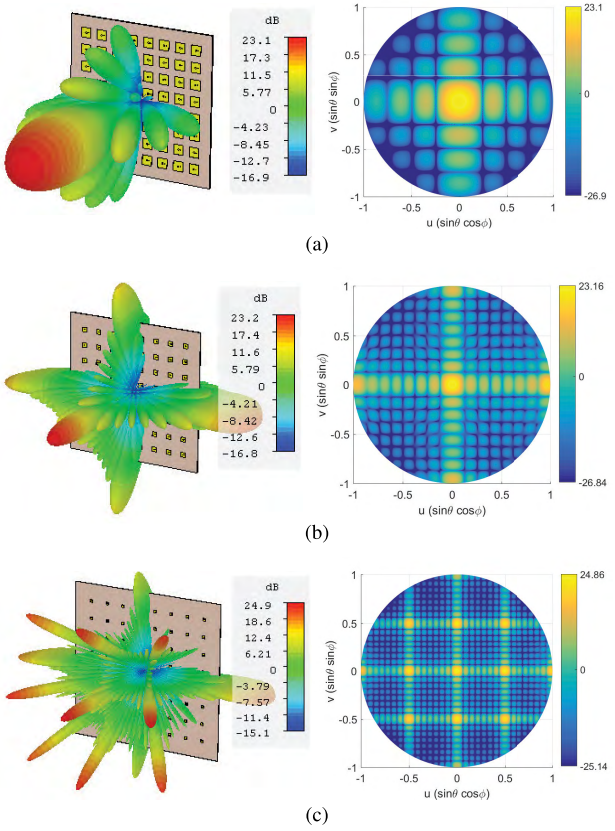


FIGURE 24. Realized gains of 8x8 regular square array layouts for broadside beams at 28.5 GHz, (a) $d_e = 0.5\lambda$, (b) $d_e = 1\lambda$, (c) $d_e = 2\lambda$.

rithms at the base stations which allows killing the inter-user interference in a multi-user network completely by placing nulls in the directions of the interferers [67]–[69]. However, when two (or more) users are positioned close to the grating lobes (which may occur frequently for randomly distributed users), zero-forcing fails and a null is placed in the direction of each user. In order to prevent this, irregular array layouts can be used which help reduce the level of grating lobes and ensure good performance with zero-forcing [16], [17].

For the layout given in this section, the convex optimization method proposed in [38] has been used to synthesize an 8-element linear array with a guaranteed minimum inter-element spacing, $d_{\min}$, of 2λ for the aim of minimizing the maximum side lobe level in the visible region for the broadside beam. Using the optimized linear array, an 8x8 irregular planar array has been created for performance comparison with the 8x8 regular array with 2λ inter-element spacing.

Fig. 25 shows the optimized locations of the elements for the synthesized irregular array. The radiation pattern of the array in broadside with the new element locations is given in Fig. 26. Compared to the radiation from the regular array given in Fig. 24(c), around 5 dB grating lobe suppression is obtained with the new topology. At the same time, since 2λ minimum inter-element spacing is guaranteed, much better cooling performance is obtained as compared to the regular counterparts with $d_e = 0.5\lambda$ (see Table 2).

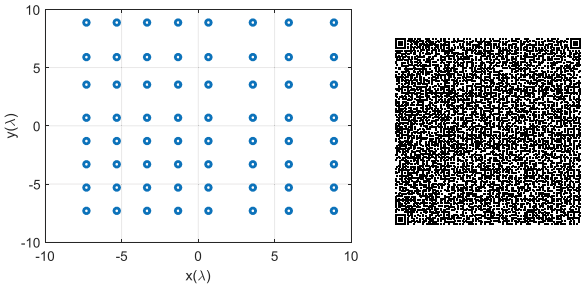


FIGURE 25. Element locations in the 8x8 optimized irregular array layout with $d_{\min} = 2\lambda$ with a QR code including the positions (in λ).

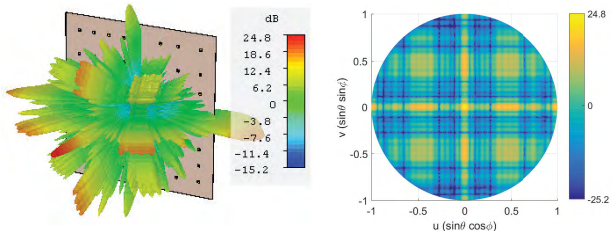


FIGURE 26. Realized gain of the 8x8 optimized irregular array layout with $d_{\min} = 2\lambda$ for the broadside beam at 28.5 GHz.

TABLE 2. Comparison of maximum temperature values in several cases for 8x8 regular array layout with $d_e = 0.5\lambda$ and irregular optimized array layout with $d_{\min} = 2\lambda$.

Case #	$T_{\max}$ (°C) regular array (from Table 1)	$T_{\max}$ (°C) irregular array
C-1	164	140
C-4	86	81
C-7	232	196
C-10	117	109

For the multi-user scenario, two simultaneous co-frequency users located at 100 meter distance from the base station with angular positions $\theta_1 = 0$, $\phi_1 = 0$ and $\theta_2 = 30$ degrees, $\phi_2 = 0$ have been considered. Note that both users are located at the grating lobes shown in Fig. 24(c). Zero forcing is performed for these users by inverting the channel matrix that is formed by assuming a LoS-only propagation path. The formulation of this technique have already been widely studied [16], [67]–[69]. Therefore, only the resulting excitation coefficients at each element in the 8 antenna columns (including 8 elements arranged vertically) are given here with a discussion on the outcome.

Table 3 and Table 4 provide the related excitation coefficients for the regular and optimized irregular array layouts, respectively. The realized gains (at the $\phi = 0$ cut) in this case are given in Fig. 27. As mentioned before, due to the grating lobes, zero forcing does not work for the regular array layout (see Fig. 27(a)). However, the irregular layout and resulting grating lobe suppression make formation of maxima and nulls possible at the corresponding user locations as seen in Fig. 27(b).

TABLE 3. Zero-forcing excitations at each column of the 8x8 regular square array with $d_e = 2\lambda$ for user-1 ($\theta_1 = 0$, $\phi_1 = 0$) and user-2 ($\theta_2 = 30$ degrees, $\phi_2 = 0$) located at 100 meter distance from the base station.

Column #	User-1		User-2	
	Amplitude	Phase (in degrees)	Amplitude	Phase (in degrees)
1	0.5410	-158.1766	0.5410	-158.2201
2	0.0978	171.9686	0.0975	172.1213
3	0.2314	39.3215	0.2313	39.0852
4	0.3812	31.9362	0.3811	31.7519
5	0.3812	28.2898	0.3812	28.1056
6	0.2315	21.2354	0.2316	20.9992
7	0.0969	-111.0076	0.0973	-110.8543
8	0.5391	-140.0903	0.5392	-140.1336

TABLE 4. Zero-forcing excitations at each column of the 8x8 optimized irregular array with $d_{\min} = 2\lambda$ for user-1 ($\theta_1 = 0$, $\phi_1 = 0$) and user-2 ($\theta_2 = 30$ degrees, $\phi_2 = 0$) located at 100 meter distance from the base station.

Column #	User-1		User-2	
	Amplitude	Phase (in degrees)	Amplitude	Phase (in degrees)
1	0.1994	118.2254	0.1992	2.1942
2	0.1995	117.6059	0.1993	1.9589
3	0.1995	117.1821	0.1993	1.7976
4	0.1995	116.9539	0.1994	1.7105
5	0.1994	116.9214	0.1995	1.6977
6	0.6185	127.6195	0.6185	-169.7093
7	0.5950	107.3294	0.5951	150.0215
8	0.2541	147.1600	0.2543	-59.1379

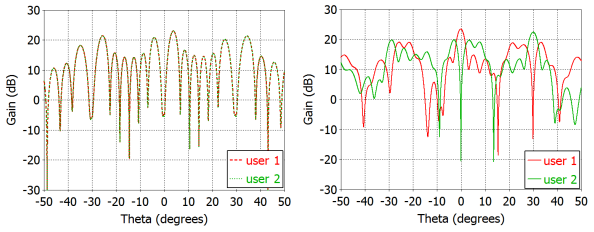


FIGURE 27. Zero forcing results (in terms of realized gains) for 8x8 arrays with two users sharing the same time-frequency resource and located at 100 meter distance from the base station at two grating lobe positions of the regular layout ($\theta_1 = 0$, $\phi_1 = 0$, $\theta_2 = 30$ degrees, $\phi_2 = 0$), (a) regular array with $d_e = 2\lambda$, (b) optimized irregular array with $d_{\min} = 2\lambda$.

E. SPIRAL ARRAYS

Spiral arrays have been shown to provide low side lobe levels and grating lobe free scanning capabilities with large inter-element spacings [25]. Ring arrays have been used for space applications since the 80's and spiral arrays for space use were revisited in the last decade [25], [26].

In polar coordinates, the elements in a spiral can be arranged according to the following equations [25],

$$\rho_n = \alpha\sqrt{\frac{n}{\pi}} \tag{1}$$

$$\Psi_n = 2\pi n\beta \tag{2}$$

where ρ_n is the radial distance of the n^{th} element, the parameter α relates to the mean distance between the neighboring elements and Ψ_n is the angular displacement of each element which depends on the parameter β.

A special case occurs when β is equal to the golden angle ($\beta = \frac{\sqrt{5}+1}{2}$), which resembles to the distribution of sunflower seeds. Being an irrational number, this particular selection of β prevents any rotational periodicity and shadowing of radiators.

Due to these appealing features and its impact on side lobe level suppression even for relatively large inter-element spacings, a uniform sunflower array topology is proposed in this section for passively cooled 5G base stations. Note that density tapering can also be applied on such arrays by optimizing the element positions to further reduce the side lobe levels [26] while keeping the optimum power efficiency without amplitude tapering, which is not addressed here.

In this paper, $\alpha = 2.213\lambda$ is used to have $d_{\min} = 2\lambda$. The element locations for this sunflower array antenna topology for an 64-element array is given in Fig. 28. The resulting radiation pattern for the broadside beam is given in Fig. 29(a). In order to scan the beam, appropriate phase shifts can also be applied at each element using the following relation

$$\Phi_{n,s} = e^{-jk(\sin\theta_s\cos\phi_s x_n + \sin\theta_s\sin\phi_s y_n)} \tag{3}$$

where $\Phi_{n,s}$ is the excitation coefficient at the n^{th} element for the scan angle (θ_s, ϕ_s). For $\theta_s = 30$ degrees and $\phi_s = 225$ degrees, the realized gain in Fig. 29(b) is obtained. In both cases, no grating lobes appear and the maximum side lobe level becomes around -13 dB when compared to the broadside gain. Besides this advantage on the EM performance, the sunflower layout with $d_{\min} = 2\lambda$ is able to achieve much better cooling when compared to regular square layout with $d_e = 0.5\lambda$ (see Table 5).

TABLE 5. Comparison of maximum temperature values in several cases for 8x8 regular array layout with $d_e = 0.5\lambda$ and 64-element sunflower array layout with $d_{\min} = 2\lambda$.

Case #	$T_{\max}$ (°C) regular array (from Table 1)	$T_{\max}$ (°C) sunflower array
C-1	164	138
C-4	86	81
C-7	232	194
C-10	117	108

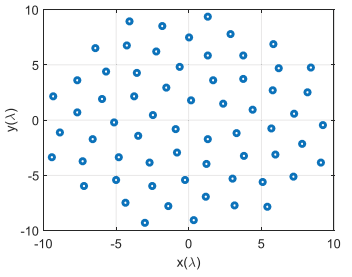


FIGURE 28. Element locations in the 64-element spiral array layout with $d_{\min} = 2\lambda$ with a QR code including the positions (in λ).

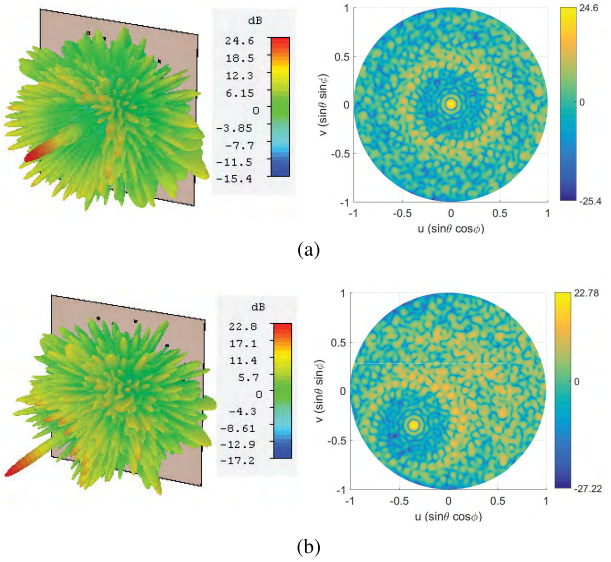


FIGURE 29. Realized gain of the 64-element sunflower array with $d_{\min} = 2\lambda$ at 28.5 GHz, (a) broadside beam, (b) scanned beam ($\theta_s = 30$ degrees and $\phi_s = 225$ degrees).

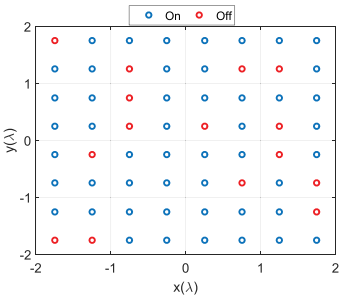


FIGURE 30. Element locations in a 49-element array obtained via random thinning of an 8x8 regular square array layout.

F. THINNED ARRAYS

In this section, the aim is to investigate the effect of array thinning on the EM and thermal performance of the arrays. The 8x8 regular square grid with $d_e = 0.5\lambda$ has been used as the reference and 15 elements have been randomly selected to be switched off. Here, the cooling performance of the thinned array is compared both with the 8x8 regular array (which has 15 extra heat sources) and 7x7 regular array (which has the same number of sources, but densely populated with $d_e = 0.5\lambda$). EM performance of the thinned array layout is also compared with the regular counterparts.

A realization of random array thinning is given in Fig. 30, which is used for the results given in this section. Table 6 provides the comparison of $T_{\max}$ between the 8x8 regular array layout with $d_e = 0.5\lambda$, 7x7 regular array layout with $d_e = 0.5\lambda$ and the 49-element randomly thinned array whose layout is shown in Fig. 30.

In the thermal analysis given in Table 6, it is seen that due to the same inter-spacing of the heat sources, the maximum temperature values are the same in each case analyzed in this section for the 49-element arrays as compared to the 64-element arrays with regular layouts. However, due to the sparsity of the thinned array, enhancement in cooling can be obtained, especially in the cases with relatively low h_{hs} (Case C-1 and C-7). This improvement comes at the expense of reduced EM performance, which is explained next.

TABLE 6. Comparison of the maximum temperature values in several cases between the 8x8 regular array layout with $d_e = 0.5\lambda$, 7x7 regular array layout with $d_e = 0.5\lambda$ and the 49-element randomly thinned array.

Case #	$T_{\max}$ (°C) 8x8 regular array (from Table 1)	$T_{\max}$ (°C) 7x7 regular array	$T_{\max}$ (°C) 49-element thinned array
C-1	164	164	158
C-4	86	86	85
C-7	232	232	224
C-10	117	117	115

As for the EM performance, compared to the 64-element array, the realized gain is reduced by 1.2 dB for the 49-element thinned array and the maximum side lobe level is approximately 3 dB larger compared to the regular square layout (see Fig. 31). Besides, since the number of transceiver modules is lower for the thinned arrays, both the transmit power and the gain and consequently, the EIRP at the users are lower than for the fully-populated arrays. Moreover, unless complex signal processing algorithms exploiting the channel matrix information (such as zero forcing or MMSE [67]) are used, the high level of side lobes in Fig. 31 could result in high interference levels at the other co-frequency users that are served simultaneously. Therefore, an alternative sparse array topology is introduced next, which helps reduce the level of side lobes while keeping a comparable cooling performance.

G. SPARSE CIRCULAR RING ARRAYS

In sparse circular ring array layout, the sparsity is achieved along the radial direction, which helps for the cooling, and circular arrays are exploited to enhance the EM performance by reducing the level of high side lobes that occur in the case of the randomly thinned arrays. Here, the compressive-sensing method proposed in [70] has been used to synthesize a low side lobe 49-element circular isophoric (i.e. uniform amplitude) sparse array.

Fig. 32 shows the optimized element locations for which the inter-element spacings are larger than 0.525λ

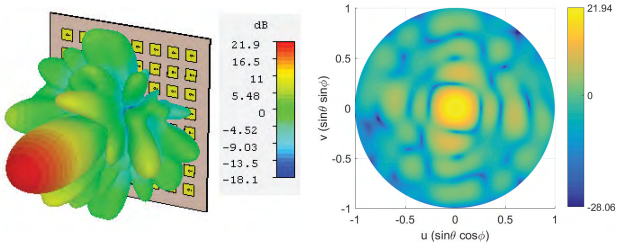


FIGURE 31. Realized gain of the 49-element randomly thinned array (whose layout is given in Fig. 30) for the broadside beam at 28.5 GHz.

(i.e. $d_{\min} = 0.525\lambda$). Comparison of the maximum temperature values between the 49-element regular array with $d_e = 0.5\lambda$ and the designed sparse circular ring array is provided in Table 7. It is seen that enough sparsity is achieved with the circular ring array to have almost the same cooling performance as with the randomly thinned array in each study case (C-1, C-4, C-7 and C-10).

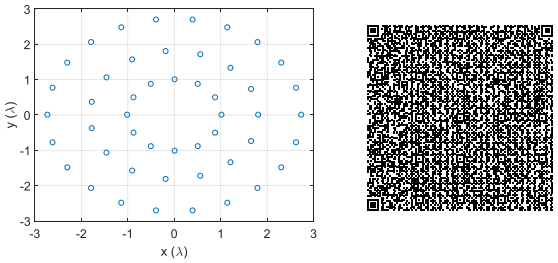


FIGURE 32. Element locations in the 49-element optimized sparse circular ring array with $d_{\min} = 0.525\lambda$ with a QR code including the positions (in λ).

TABLE 7. Comparison of the maximum temperature values in several cases for the 7x7 regular array layout with $d_e = 0.5\lambda$ and 49-element sparse circular ring array layout with $d_{\min} = 0.525\lambda$.

Case #	$T_{\max}$ (°C) thinned array (from Table 6)	$T_{\max}$ (°C) sparse circular ring array
C-1	164	159
C-4	86	85
C-7	232	225
C-10	117	115

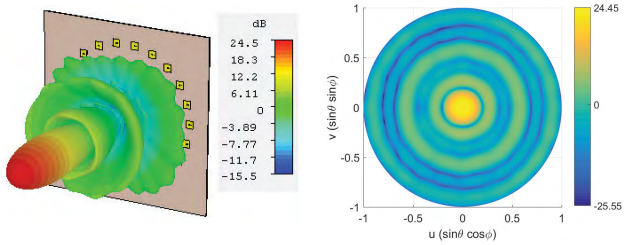


FIGURE 33. Realized gain of the 49-element sparse circular ring array for the broadside beam at 28.5 GHz.

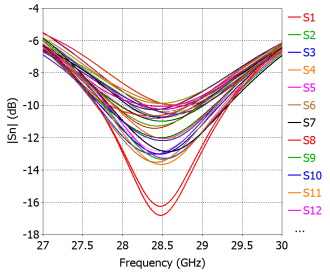
In terms of the EM performance, the realized gain of the circular ring array (given in Fig. 33) shows that the maximum side lobe level is reduced by nearly 7 dB when compared to the thinned array, which results in around -17 dB maximum side lobe level with respect to the broadside gain. Note that, since the layout is optimized only for the broadside beam, wide-angle scanning could yield higher side lobes in the visible region. This issue might be handled using the recently introduced multiple beam optimization techniques [16], [38] or additional amplitude tapering at the expense of decreased power efficiency.

H. HEAT SINK ANTENNA ARRAYS

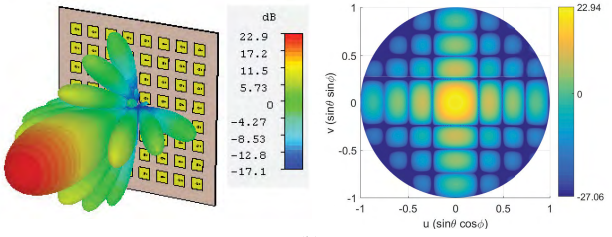
Heat sink antenna arrays can be designed by placing a copper heat spreader pin in the middle of each patch, connecting

TABLE 8. A parametric study on $T_{\max}$ with the 8x8 regular square array layout by exploiting heat spreaders and varying P_h, h_{hs} and d_e.

Case #	$T_{\max}$ (°C) without spreader (from Table 1)	$T_{\max}$ (°C) with spreader
C-1	164	164
C-2	155	153
C-3	141	134
C-4	86	86
C-5	84	84
C-6	81	80
C-7	232	232
C-8	218	214
C-9	197	187
C-10	117	117
C-11	114	113
C-12	109	107



(a)



(b)

FIGURE 34. EM simulation results of the 8x8 regular square array layout with $d_e = 0.5\lambda$ for the broadside beam including the heat spreaders, (a) active reflection coefficients, (b) realized gain at 28.5 GHz.

the radiating patch to the chip and the ground plane (revisit Fig. 17(b) for visualization). The details of such a design and related design parameters were previously explained for a single element in a unit cell in Section IV-A and in Section IV-B.

Here, the effect of exploiting heat spreaders in antenna arrays is studied by using the 8x8 square array layout as the reference. The thermal simulations for the cases used in Table 1 with no spreaders have been repeated including the heat spreaders. The comparison of $T_{\max}$ with and without the spreaders for the 8x8 regular square layouts is provided in Table 8.

It is seen that the improvement in heat removal via the heat spreaders is most significant when the heat dissipation per chip is relatively large (equal to 3 W among the cases studied in the paper), h.t.c. of the heat sink is relatively low (equal to 1000 W/m^{2}K among the cases studied in the paper) and the inter-element spacing is relatively large (equal to 2λ in this paper).

Fig. 34 presents the EM simulation results (active reflection coefficients and the realized gain) for the 8x8 regular square array layout with $d_e = 0.5\lambda$, including the heat spreaders. When compared to the results in Fig. 23(a) and Fig. 24(a) with no spreaders, it can be inferred that the effect of heat spreaders on the EM performance is not significant since they are located in the middle of the radiating patches, which prevents the parasitic radiation. Thus, heat spreaders between the chips and the patches can be integrated for cooling enhancement in all the layouts studied throughout the paper.

V. CONCLUSION

Thermal management problem in 5G base station antenna arrays at mm-waves has been addressed. Using passively cooled planar AESA's with fanless CPU coolers has been proposed, for the first time, as an energy-efficient and relatively low-cost solution with a large beamforming flexibility, which makes them suitable candidates for the first phase of digital 5G systems.

A novel relation between thermal management and layout sparsity has been found. In order to enhance the cooling performance, sparsity has been introduced in the antenna layouts by increasing the inter-element spacings. Several sparse array topologies have been proposed and evaluated in terms of their thermal and electromagnetic performances.

From the simulation results, the following main observations have been made.

1) Fanless CPU coolers with relatively large h.t.c.'s can provide sufficient cooling at the base station antennas, especially when the power dissipated per chip is relatively low.
2) In the case of having highly inefficient transceiver ICs and a heat sink with lower heat transfer capability, layout sparsity could provide significant reduction in the maximum junction temperature of the array.
3) Although capable to achieve additional cooling, increasing the inter-element distance in regular square layouts to create sparsity leads to the formation of grating lobes, which might result in very high interference among the simultaneous co-frequency users.
4) Alternative sparse array layouts that are based on linear or planar irregular arrays, spiral arrays, thinned arrays or circular ring arrays can be used to obtain better electromagnetic performance (compared to the regular square arrays) while keeping the cooling capacity.
5) It was found that for different sparse topologies investigated, the major factor to reduce the temperature was the average distance between the elements. The sunflower topology has been found to be the best one from this point of view since the inter-element spacing in this topology can be the largest among all investigated ones while keeping low side lobe levels.

Furthermore, creating a conduction path between the chips, ground plane and the radiators by exploiting heat spreaders located in the middle of the patches provides additional cooling without affecting the radiation performance. Cooling with spreaders increases with increasing power dissipation per chip and decreasing h.t.c. of the heat sink attached to the chips.

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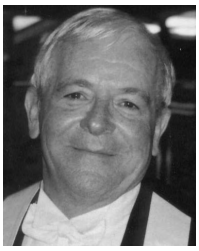

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