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Transformerless Common-Mode Current-Source Inverter Grid-Connected for PV Applications

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ABSTRACT The use of a transformer in grid-connected photovoltaic (PV) generation systems provides isolation between the grid and the PV array, this increases the cost, weight, and the size of the system. However, the transformer elimination increases the efficiency and the security issues, these should be taken into account, but also to remove the isolation leads the apparition of a leakage current due to the PV parasitic capacitance to the ground. This paper presents a five-switch common-mode current-source inverter for grid-connected applications and a control scheme based on finite control set, where an additional force section is considered, in order to regulate the current injected to the grid. The proposed topology can reduce the leakage current in photovoltaic systems due to the common mode connection. The operation modes, consideration design, control technique, and the simulation results are presented.

INDEX TERMS Photovoltaic, grid-connected, transformerless, common-mode, parasitic, capacitance, leakage current.

I. INTRODUCTION

PV grid-connected inverters should have galvanic isolation for safety reasons [1], [2]. It may be on the grid side, but this uses a low-frequency transformer that is big and heavy. When galvanic isolation is at the direct current (DC) side, the transformer can operate at high-frequency which permits to reduce the weight and cost; however, this solution makes a more complex system. For this reason, the PV systems are connected to the grid without transformer, which improves their efficiency, reduces the weight and size [3], [4]. However, transformer elimination produces a common mode (CM) resonant circuit due to the coupling among the inverter, AC output filter, the grid impedance, and the PV parasitic capacitance [5]. For security reason, both the neutral grid line and the PV panel chassis must be grounded. The CM voltage produces a leakage current ($i_{leakage}$), that circulates through the parasitic capacitance C_{p1} and C_{p2} in the PV panel to the ground, as it is shown in Fig. 1. Different conditions as the value of CM voltage, the modulation strategy and the value of the parasitic capacitance can affect the value of the leakage current [6]. The parasitic capacitance value depends on many factors such as [7]:

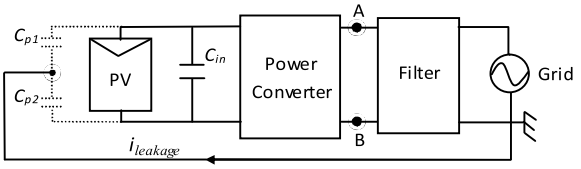

FIGURE 1. Diagram of leakage current in transformerless PV grid-connected PV converter.

1) PV panel and frame structure.
2) The surface of the cells.
3) The distance between cells.
4) Weather conditions.
5) Type of electromagnetic compatibility filter.

Some researchers have proposed methods to reduce the leakage current significantly because it is responsible for higher current harmonics, higher losses, and electromagnetic interferences issues [8], [9]. Some solutions are as follow [7]:

1) Disconnect the AC side and the PV during freewheeling times.
2) Connect the midpoint of the DC-link capacitors to the neutral line of the utility grid.

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3) Connect the PV negative terminal to the neutral line of the utility grid directly, referred here as CM converters.

II. TRANSFORMERLESS INVERTER TOPOLOGIES FOR PV GRID-CONNECTED

A. HALF- AND FULL- BRIDGE VOLTAGE AND CURRENT SOURCE TOPOLOGIES

The half bridge inverter consists of two input capacitors and the output filter, this topology is simple and connects the neutral grid cable to a negative terminal from PV panel, its disadvantage is that the input voltage must be more than two times than grid voltage in order to be able to inject current. This problem is solved by means of a full bridge inverter. However, it is still higher than the grid voltage, this topology has four switches, one input capacitor, and the output filter [10]. In [11] is proposed a buck-boost converter that still needs an input voltage higher than grid voltage, but it has the advantage of having a reduced low-frequency input current ripple and a low leakage current. A single phase current source H5 (CH5) inverter is proposed in [12]. It reduces the leakage current by mean a novel space vector modulation and its uses IGBT as switch, the same concept of the reduction of the leakage current by a new space vector modulation is applied in [13] but for a current source three-phase CH7 inverter.

A H6-type single-phase inverter topology is proposed in [14] where the PV is disconnected to the grid in some operation modes in order to reduce the leakage currents, is similar way this is realized by other inverter with six switches proposed in [15] that has the same propose of reduce the leakage current but in this topology obtain a higher efficiency due to the lower switching frequency.

Another topology with eight switches called H8 is proposed in [16] this topology is a three-phase inverter for PV applications and has a reduction in the leakage currents due to the disconnection of the PV array in some switching times.

In order to the inverter topology contributes to power quality of the residential and smart grids the inverter must be capable to inject reactive power, that is the case in [17] where two single-phase topologies H5 and HERIC inverter are controlled by mean a special modulation for add the reactive power injection characteristic, the same characteristic is given to a single-phase full-bridge with DC bypass topology in [18].

B. MULTILEVEL TOPOLOGIES

In the multilevel neutral point clamped (NPC) inverter, the midpoint of the capacitive voltage divider should be connected to the neutral line of the grid [19]. However, the input voltage must be higher than twice the grid that is the main drawback.

An advantage of the multilevel topologies with more than 3 levels is the low harmonic distortion, and it is used in PV applications, but the number of switches increases in comparison with the half or full bridge topology, this increases the complexity of the system [20].

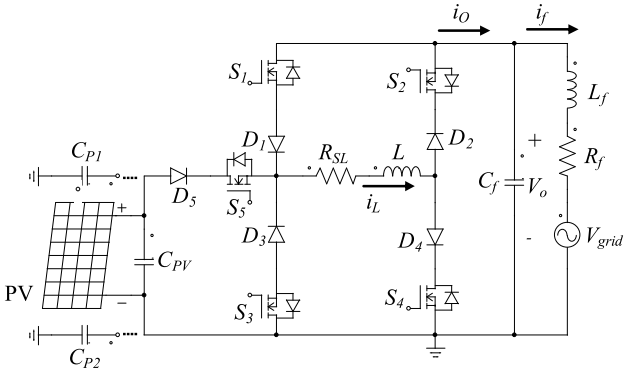

FIGURE 2. Five switch common mode inverter topology proposed.

C. COMMON MODE TOPOLOGIES

The Karschny inverter is a common mode current source topology which the negative terminal to the PV array is connected directly to the neutral terminal of the grid. It has a flying inductor which provides the current to the output in the positive and negative direction, this topology need more diodes than the full bridge and it has three devices conducting at the same time, which reduce the efficiency [21], but a low-frequency input-current is demanded from the panel. In [22] the negative terminal of the PV panel is connected in a similar way to the Karschny inverter, but this topology has a flying capacitor which is connected to the output filter in the positive and negative cycle. This topology demands a low-frequency input-current ripple from the panel.

Another CM topology is proposed in [23]. It has a flying capacitor and a boost stage, an important characteristic of this topology is that just two of six power switches are switching at high frequency.

Other CM inverters have been proposed in [24] and [25] that are based on the half-bridge inverter, but they require more elements than the typical configuration.

III. PROPOSED TOPOLOGY

Fig. 2 shows the CM proposed topology. It consists of five unidirectional switches composed by MOSFET with its respective series diode, the current source is provided by the inductor L operating in continuous conduction mode (CCM). The power source is a PV array with a capacitive filter, at the output of the topology a second order filter is employed as it can see the parasitic capacitor C_{P2} is short circuit due that is connected to the same electrical point.

A. OPERATION MODES

The proposed topology has six operation modes, Fig. 3 exhibits the circulating operation mode generated by means of the activation of switches S_1 and S_2, this mode maintains constant the current through the inductor, and the output filter provides the current to the grid.

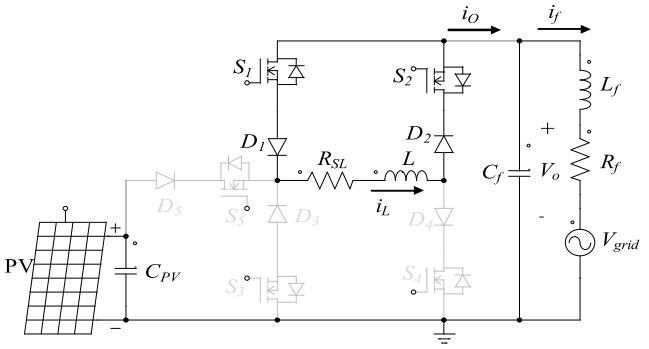

FIGURE 3. Circulating operation mode, a) activating the switches S_1 and S_2.

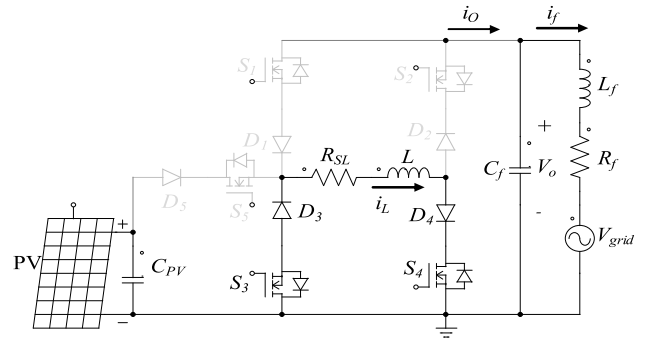

FIGURE 4. Circulating operation mode activating the switches S_3 and S_4.

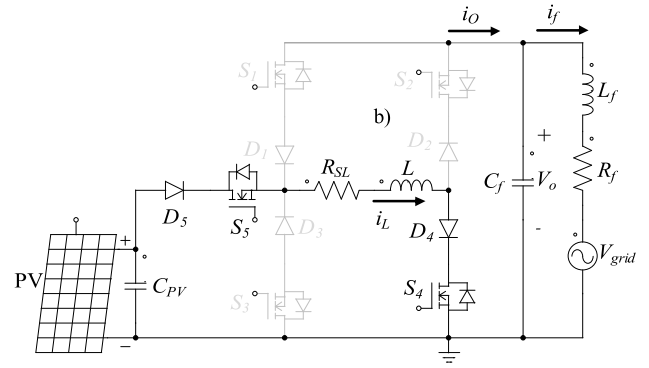

FIGURE 5. Charge of inductor operation mode, activating switches S_5 and S_4.

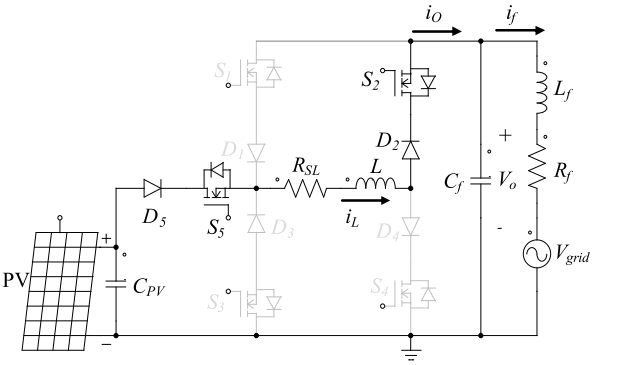

FIGURE 6. Operation mode where is adding the PV and inductor voltages, activating the switches S_2 y S_5.

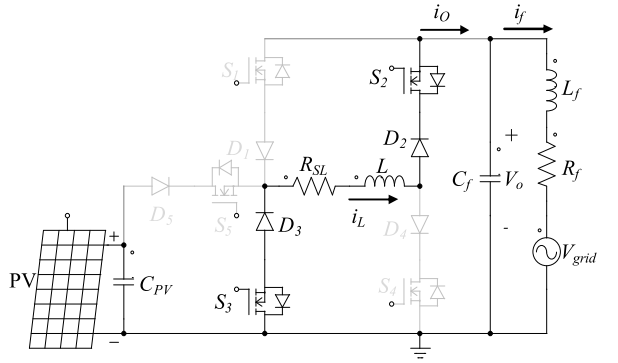

FIGURE 7. Download current inductor operation mode, activating switches S_2 and S_3.

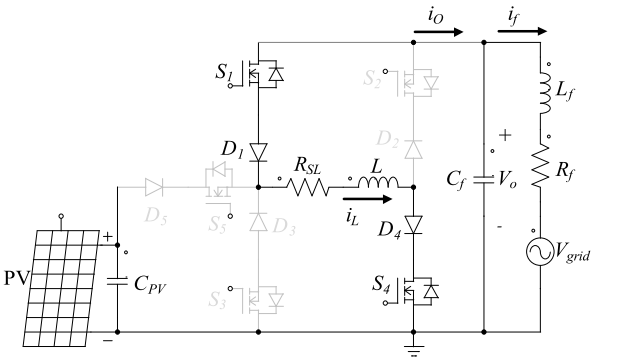

FIGURE 8. Discharge current inductor in the negative cycle, activating the switches S_1 and S_4.

The same effect can be produced in the Fig. 4 but with the activation of switches S_3 and S_4.

Fig. 5 shows the operating mode when the inductor is being charged and is generated by the activation of switches S_5 and S_4, in this operation mode the inductor is connected in parallel with the PV power source hence the current i_L increases. Also, the output filter is connected to the grid.

Fig. 6 shows the operating mode when the PV power source and the inductor voltage are added, this is generated by the activation of switches S_2 and S_5, and the inductor L provides the current to the filter and then to the grid.

The operating mode generated by the activation of switches S_3 and S_2 is shown in Fig. 7, in this mode, the inductor L provides the current to the filter and to the grid in the positive direction hence the inductor is discharged, whereas the PV panel is disconnected from the power converter. In Fig. 8 is produced a similar effect in the current inductor activating switches S_1 and S_4, but the current to the capacitor is injected in a negative path.

Table 1 exhibits the summary of the five operating modes, the effect in the inductor current, current level in the output current i_O, and switching states. Only one circulating operating mode was considered.

A possible selection of the operation modes considering the phase shift between currents i_o and i_f is shown

TABLE 1. Operation modes of topology proposed.

Operation mode	S_1	S_2	S_3	S_4	S_5	i_L	Level i_o
1	1	1	0	0	0	Circulating	0
2	0	0	0	1	1	Charge	0
3	0	1	0	0	1	Charge	$+i_L$
4	0	1	1	0	0	Discharge	$+i_L$
5	1	0	0	1	0	Discharge	$-i_L$

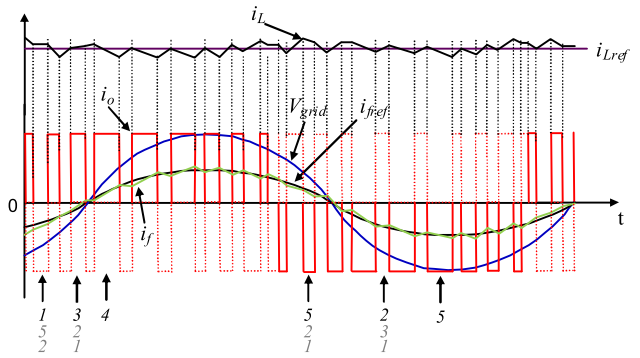

FIGURE 9. Selection of operation modes considering the phase shift between i_o and i_f.

in figure 9 where the current i_f is in phase whit grid voltage (V_{grid}), the operation mode selected can change in order to maintain the tracking of i_{Lref} and i_{fref}, for example for maintain the current i_L in circulating mode and reduce de error for i_f, the operation mode 1 is used, but also can be used the operation modes 5 and 2 depending of the values of i_{Lref}, i_L, i_f, i_{fref} and V_{grid}.

IV. MODULATION STRATEGY

In order to obtain the control signals for the switches to produce a low Total Harmonic Distortion (THD) in the output waveform i_f, a control strategy based on the finite control set is applied. It consists in the evaluation of the feasibility of the five operating modes and then the selection of the best condition to force the good operation.

The scheme of the controller is shown in Fig. 11, it is based on the solution of the dynamical equations of the current i_L and i_f as it is shown in Table 2 where "C" is a constant. It consists of the five sections for the finite control mode: convergence to i_f, convergence to i_L, the add of both convergences, determination to the maximum value, and a logic table. The operating mode for the forced conditions are chosen by means of the selection section, In order to limit the switching frequency, a limitation section is used too.

The convergence section of the current i_f generates as output a value of logic '1' when the i_f converge to the desired value and logic '0' when i_f doesn't converge.

The Fig. 10 shows the operation of the convergence section, according to Table 2, the actual value can converge to three different final values as is an exhibit in the Table 3.

TABLE 2. State stable equations considered.

Mode OMn	Value i_L when $t\uparrow$	Value i_f when $t\uparrow$	
1	$i_L = i_L - C$	if $V_O > V_{grid}$ then $i_f \rightarrow i_L$ if $V_O > V_{grid}$ then $i_f \rightarrow -i_L$	(1)
2	$i_L = \frac{V_{pv}}{R_{SL}}$	if $V_O > V_{grid}$ then $i_f \rightarrow i_L$ if $V_O > V_{grid}$ then $i_f \rightarrow -i_L$	(2)
3	$i_L = \frac{V_{pv} - V_O}{R_{SL}}$	$i_f \rightarrow i_L$	(3)
4	$i_L = \frac{0 - V_O}{R_{SL}}$	$i_f \rightarrow i_L$	(4)
5	$i_L = \frac{V_O}{R_{SL}}$	$i_f \rightarrow -i_L$	(5)

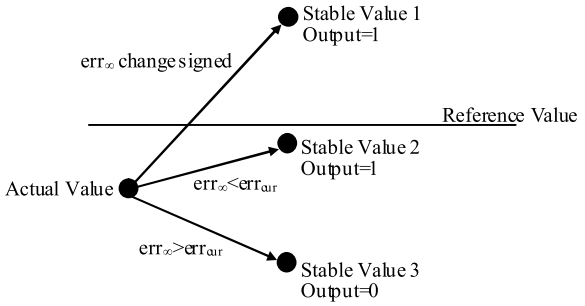

FIGURE 10. Convergence from the actual value to the reference.

TABLE 3. Output value from the convergence section.

Error convergence	*Output value*
err_∞ change signed	1
$err_\infty < err_{cur}$	1
$err_\infty > err_{cur}$	0

Where err_∞ is the error value when $t \rightarrow \infty$ and err_{cur} is the actual value of the error. The output value from convergence section is logic '1' when the error value changes its signed or when it is reduced and logic '0' in the other case.

In order to obtain the convergence data only with a combinational logic, Table 4 shows the inputs and the output for this section. Where C_1 is the comparison between the sensed value and its reference, C_2 is the comparison

between the reference value and the stable state value from Table 2 and C_3 is the comparison between the actual value and the stable state value from Table 2.

$$X = \overline{C_1 C_3} + C_2 C_3 + C_1 \overline{C_2} \tag{6}$$

Equation (6) determines the outputs of section 1 and section 2. By adding both convergence sections, the

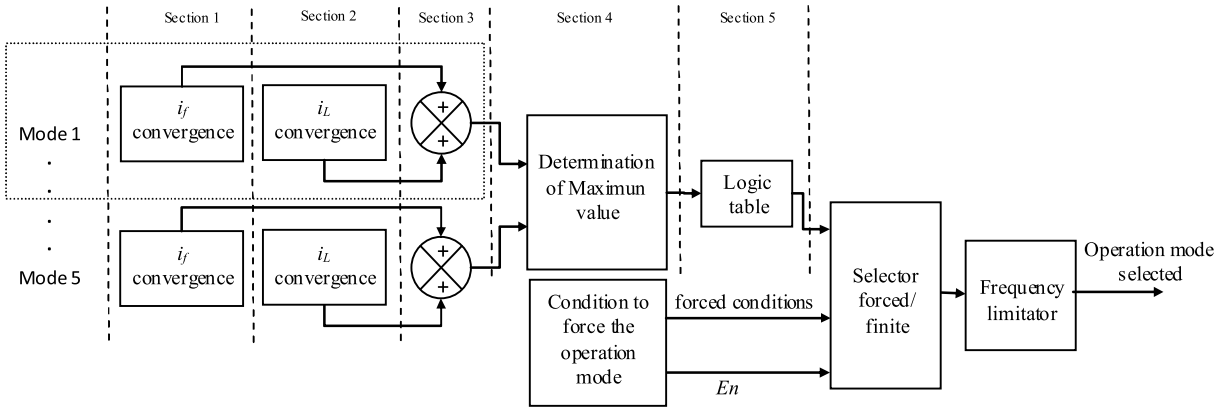

FIGURE 11. Control scheme proposal.

TABLE 4. Combinations for the convergence section.

C_1	C_2	C_3	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

maximum value can be 2 and the minimum 0. This maximum value is used in order to select the best operation mode (OM), but certainly, more than one option may be obtained, five operating modes as input imply 32 combinations as it is shown in Table 5, five combinations are used when only one maximum exists. In the other cases is selected the operation mode which charges the inductor only.

Table 6 is used to make a forced commutation that permits to reduce the current error e_f. As Fig. 12 shows, "FC_4" is the comparison between the absolute value e_f with its reference value H_{yst}, "FC_3" is the sign of the error of the current i_L, "FC_2" is the comparison between current i_L with the peak value of the output current reference $i_{pk\_f\_ref}$, and "FC_1" is the sign of the error of the output current i_f, "*En*" is the signal to select the forced operating state or the normal operating state. The combinations are selected to force the faster dynamic generating the corresponding operation mode.

V. CONSIDERATION DESIGNS

A. OUTPUT FILTER

Considering the current i_O as the input to the output filter, and the current i_f as the output, the transfer function is determined by the equation 7.

$$\frac{I_0(S)}{I_f(S)} = \frac{\frac{1}{L_f C_f}}{S^2 + \frac{R_f}{L_f}S + \frac{1}{L_f C_f}} \tag{7}$$

TABLE 5. Logic table for selection to the operation modes.

OM5	OM4	OM3	OM2	OM1	S_5	S_4	S_3	S_2	S_1
0	0	0	0	0	0	0	0	1	1
0	0	0	0	1	1	1	0	0	0
0	0	0	1	0	1	0	0	1	0
0	0	0	1	1	1	1	0	0	0
0	0	1	0	0	0	0	0	1	1
0	0	1	0	1	1	1	0	0	0
0	0	1	1	0	1	0	0	1	0
0	0	1	1	1	1	1	0	0	0
0	1	0	0	0	0	0	1	1	0
0	1	0	0	1	1	1	0	0	0
0	1	0	1	0	1	0	0	1	0
0	1	0	1	1	1	1	0	0	0
0	1	1	0	0	0	0	1	1	0
0	1	1	0	1	1	1	0	0	0
0	1	1	1	0	1	0	0	1	0
0	1	1	1	1	1	1	0	0	0
1	0	0	0	0	0	1	0	0	1
1	0	0	0	1	1	1	0	0	0
1	0	0	1	0	1	0	0	1	0
1	0	0	1	1	1	1	0	0	0
1	0	1	0	0	0	1	0	0	1
1	0	1	0	1	1	1	0	0	0
1	0	1	1	0	1	0	0	1	0
1	0	1	1	1	1	1	0	0	0
1	1	0	0	0	0	1	0	0	1
1	1	0	0	1	1	1	0	0	0
1	1	0	1	0	0	1	0	0	1
1	1	0	1	1	1	1	0	0	0
1	1	1	0	0	0	1	0	0	1
1	1	1	0	1	1	1	0	0	0
1	1	1	1	0	1	0	0	1	0
1	1	1	1	1	1	1	0	0	0

The value of the inductor is given for the next equation (8), where f_n is the frequency in Hertz of the resonant peak to the output filter. The series resistance of the inductor L_f is neglected because its value is small. The resonant frequency

TABLE 6. Combinations to force section.

FC_4	FC_3	FC_2	FC_1	En	S_5	S_4	S_3	S_2	S_1
0	0	0	0	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	0	0	1	1
0	0	1	1	0	0	0	0	1	1
0	1	0	0	0	0	0	0	1	1
0	1	0	1	0	0	0	0	1	1
0	1	1	0	0	0	0	0	1	1
0	1	1	1	0	0	0	0	1	1
1	0	0	0	0	0	0	0	1	1
1	0	0	1	0	0	0	0	1	1
1	0	1	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1	0
1	1	0	0	0	0	0	0	1	1
1	1	0	1	0	0	0	0	1	1
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1	1	1	1	1	0	0	1	1	0

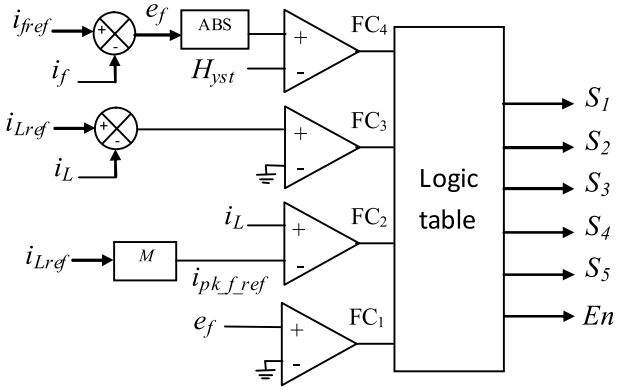

FIGURE 12. Scheme to the forced state section.

of the simulation results is selected to 270Hz and the capacitor is 22μF.

$$L_f = \frac{1}{2\pi f_n C_f} \tag{8}$$

B. CAPACITOR AND INDUCTOR INPUT

The input capacitor is selected according to [28] and is given by the next equation (9). Where f is the frequency of the grid voltage: ΔV_{PV} is the amplitude of the voltage ripple across the decoupling capacitor connected across the PV array, for an use of 99% of the power from PV array, the ripple voltage must be ΔV_{PV}=$0.05* V_{PV\_mpp\_max}$, hence for the peak value from the grid of 170V and 60Hz, and $I_{PV\_mpp\_max}$=7A, the capacitor must be C_{PV}=1000μF, but it can be reduced without affecting the tracking to the output reference.

$$C_{PV} = \frac{I_{PV\_mpp\_max}}{4\pi \Delta V_{PV}} \tag{9}$$

The inductor L is selected according to the constant time given by the equation (10). In order to have a total discharge

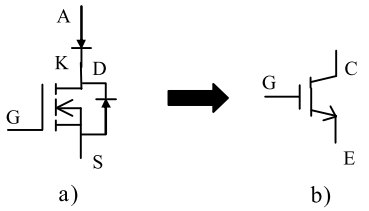

FIGURE 13. Switch a) composed by MOSFET with an antiparallel diode and a series diode b) IGBT without antiparallel diode.

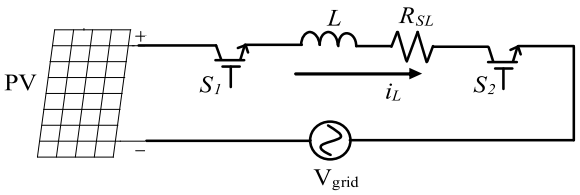

FIGURE 14. Series circuit for loses analyses.

time of 0.02s and a maximum series resistance R_{SL}=1Ω, the value of the inductor L=20mH, with a maximum value of the current of the double of $I_{PV\_mpp\_max}$.

$$\tau = \frac{L}{R_{SL}} \tag{10}$$

C. PARASITIC ELEMENTS

According to [2] the Std. DIN VDE 0126 the ground leakage current must be limited lower than 300mA if there is no leakage current suppression method applied to the system. The parasitic capacitance C_{p1} is up to 100nF/kWp with the traditional silicon technology [2].

D. LOSES ANALYSES

Switch used in the proposed topology is composed by a MOSFET with its antiparallel diode, with a series diode for break the reverse current, but can be used a IGBT without the antiparallel diode and without series diode as it can see in Fig. 13.

Due to all the operation mode has only two switches activated, loses analyses can be obtained by means Fig. 14.

Total power dissipation due all the elements is given by the equation (11) in the case of a switch with a MOSFET or the equation 12 due an IGBT. Where $R_{DS(on)}$, V_{DS}, f_{con}, t_r, t_f, V_{CEsat}, are on series resistance of MOSFET, drain-source voltage of MOSFET, commutation frequency, rise time, fall time, and saturation collector-emitter voltage of IGBT.

$$P_L = i_L R_{SL} i_L + 2[V_D + R_{DS(on)} i_L + f_{con}(t_r + t_f)]\} \tag{11}$$

$$P_L = i_L R_{SL} i_L + 2[V_{CEsat} + f_{con} V_{CEsat}(t_r + t_f)]\} \tag{12}$$

The efficiency is given by the equation 13.

$$\%efficiency = \frac{i_f V_{grid}}{i_f V_{grid} + P_L}(100\%) \tag{13}$$

According with the equation 13 Fig. 15 shows the behavior of the efficiency of the converter with different values of the

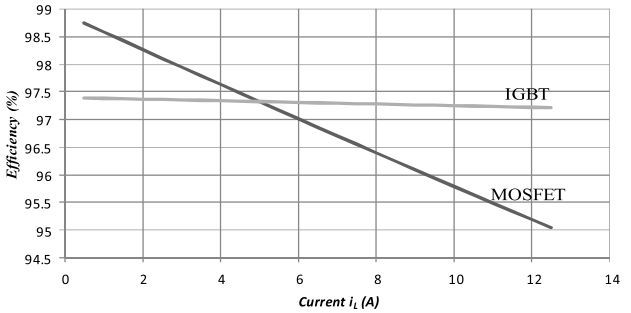

FIGURE 15. Efficiency behavior with different inductor current.

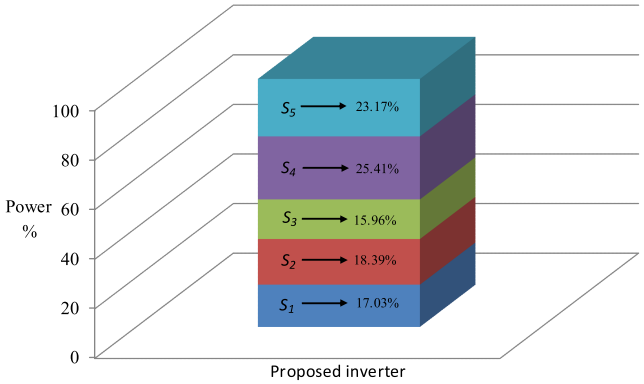

FIGURE 16. Power losses distribution for the inverter proposed.

current i_L for switches shown in Fig. 14 as it can see, the efficiency is reduced by the current of the inductor, it can be improved by means the modulation index or even by mean the use of semiconductor with the silicon carbide manufacture.

The maximum drain-source voltage for switches S_1 and S_5 is given by equation 14 and the maximum drain-source voltage for switches S_2, S_3 and S_4 is given by equation 15, the maximum current for each switch is given by the current in the inductor L as is shown in equations 16 as it can see the voltage stress is higher for switches S_1 and S_5 due to the voltage of the grid and the PV.

$$V_{DS1max} = V_{DS5max} = V_{PV} + V_{gridpk} + 2\pi f L_f I_{gridpk} \quad (14)$$

$$V_{DS2max} = V_{DS3max} = V_{DS4max} = 2\pi f L_f I_{gridpk} \quad (15)$$

$$i_{DS1max} = i_{DS2max} = i_{DS3max} = i_{DS4max} = i_{DS5max} = I_L \quad (16)$$

Fig. 16 shows the distribution of losses in the switches, as it can see the main losses are in switch S_4 due to this switch is used in two cases when the inductor is connected in series with the PV or with the grid.

VI. SIMULATION RESULTS

The simulation results are presented and were obtained with the simulator PSIM 9.1 with the values of Table 6. The current in the inductor L can be changed in order to modify the power demanded to the PV panel, and the parasitic capacitance C_{p1} was selected according to [2].

TABLE 7. Simulation parameters.

Description	Symbol	Value
Series resistance link inductor	R_{SL}	0.1Ω
Current link inductor-	L	20mH
Filter Capacitance	C_f	22μF
Filter inductor	L_f	15.79mH
Voltage grid	V_{grid}	170Vpk
Voltage output circuit of the PV	V_{OC}	250V
Short circuit current of the PV	I_{SC}	10A
Voltage in the maximum power point	V_m	150V
Current in the maximum power point	I_m	7A
DC-link capacitance	C_{PV}	470 μF - 1000μF
Limit switching frequency	f_{lim}	150kHz
Hysteresis to the output error	H_{yst}	0.01Amp
Parasitic capacitance to the PV	C_{p1}	100nF
Modulation index	M	0.5

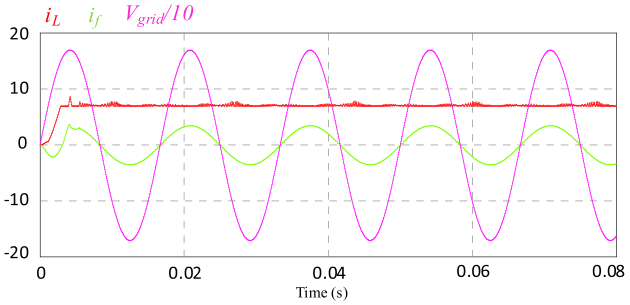

FIGURE 17. Startup and state stable operation.

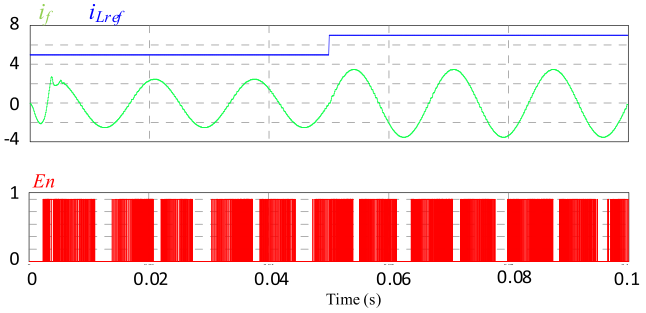

FIGURE 18. Change of reference from 3A to 7A and the "*En*" signal.

Fig. 17 shows the grid voltage attenuated 10 times, i_L current and the current injected to the grid since t=0, as it can be observed the injected current at steady state is in phase with the grid voltage and the current i_L is regulated to 7A, as the modulation index M=0.5, the peak value of i_f is 3.5A. The power factor PF=0.9997 and the THD=0.019 with a fundamental frequency of 60Hz.

The forced operation occurs when the signal "*En*" is logic '1'. Fig. 18 this signal is exhibited and a change of

TABLE 8. Comparison of the proposed converter.

Converter	Semiconductors			Passive elements		Other characteristics				
	Voltage stress	Switches	Diodes	Capacitors	Inductors	Low Freq. ripple	Gain	Output waveform	Leakage current	Efficiency
Half Bridge Converter	$>2V_{pk}$	2	0	2 bulky 1 small	2	High	< 1	Bipolar	<2.5mA	98%
NPC Converter	$>2V_{pk}$	4	2	2 bulky 1 small	2	High	< 1	Unipolar or Bipolar	<2mA	97%
Virtual DC bus Ref. [23]	$>V_{pk}$	5	0	2 bulky 1 small	2	High	< 1	Unipolar or Bipolar	≈0A*	98%
Common mode Ref. [22]	$>V_{pk}$	7	2	2 bulky 2 small	2	Low	> 1	Unipolar or Bipolar	<10mA	96%
Common mode Ref. [21]	$>2V_{pk}$	2	0	2 bulky 1 small	3	High	< 1	Bipolar	<5mA	96%
Common mode Ref. [24]	$>2V_{pk}$	3	5	4 bulky 3 small	3, but one with 3 windings	Medium	> 1	Bipolar	<1mA	96%
Common mode Ref. [25]	$>2V_{pk}$	4	0	2 bulky 1 small	3	High	< 1	Bipolar	≈0A*	96%
Common mode Ref. [26]	$>2V_{pk}$	3	0	3 bulky 1 small	5	High	> 1	Bipolar	≈0A*	90%
Common mode Ref. [27]	$>2V_{pk}$	4	2	3 bulky 1 small	2	Medium	< 1	Unipolar or Bipolar	≈0A*	97%
Common mode Ref. [7]	$>V_{pk}$	5	1	1 bulky 2 small	3	Low	> 1	Unipolar or Bipolar	<2mA	96%
Current source Ref. [12]	$>V_{pk}$	5	5	1 bulky	2	Low	> 1	Unipolar	<200mA	--*
Proposed (simulation)	$>V_{pk}$	5	5	1 bulky 1 small	2	Medium	> 1	Bipolar	<2mA	>92%

*V_{pk} is the voltage peak of the ac mains. * No measurement available.*

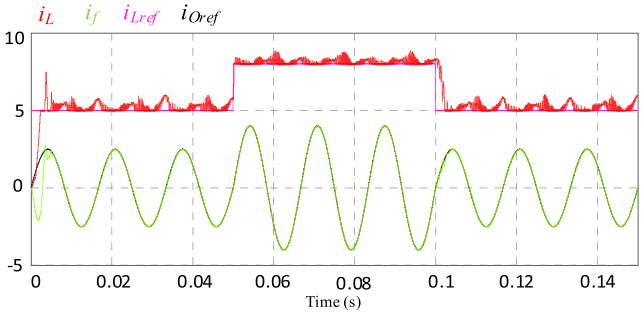

FIGURE 19. Dynamic response with a change of i_{Lref}.

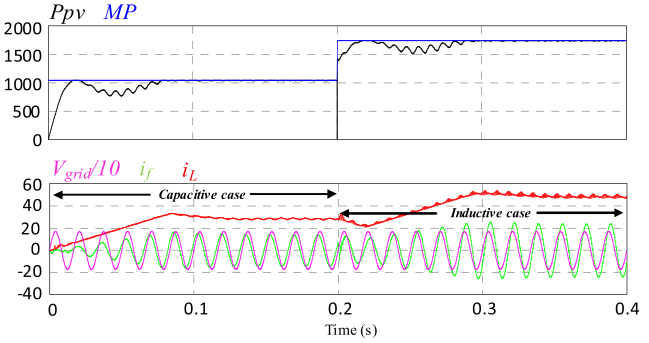

FIGURE 20. MPPT and reactive power injected.

reference is made from 3A to 7A, as it can be observed the forced operation signal, this mainly occurs near to zero crossing, but it depends on the conditions in the circuit.

A change of the inductor current reference from 3A to 7A and vice-versa was made in Fig. 19, as it can be seen; the current i_L and i_f are tracking its references.

At the top of Fig 20 is shows the power demanded (P_{PV}) and the maximum power from PV panel (*MP*), when the maximum power point tracking (MPPT) algorithm perturb and observe (P&O) is applied, a change in the power condition is made at 0.2s from 1050W to 1750W algorithm change the reference of the inductor current i_{Lref}.

The proposed controller has a variable switching frequency, no matters if active or reactive power is injected, but it is limited by f_{lim}. The reactive power injection is possible in this topology due to the operation modes 4 and 5 are capable to obtain energy from the grid depending on condition of the system, at bottom of figure 20 is show the current of the inductor i_L, the current i_f, and the grid voltage V_{grid} attenuated ten times, the current has an initial phase of 10 degrees in

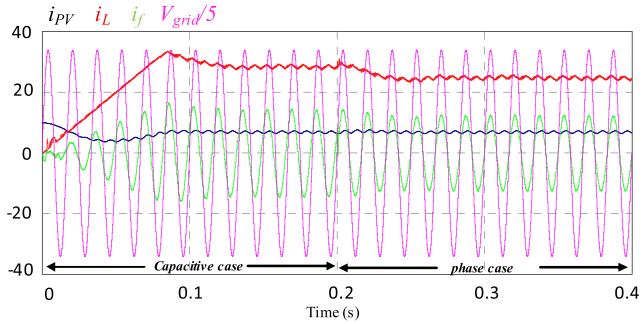

FIGURE 21. Current i_{PV} for shift phase of i_f.

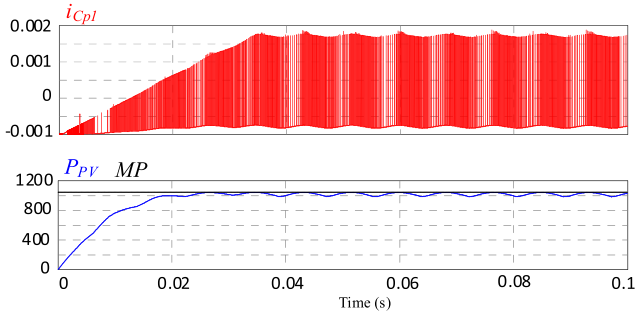

FIGURE 22. Leakage current to the parasitic capacitor C_{P1} under change of current reference with C_{PV}=1000μF.

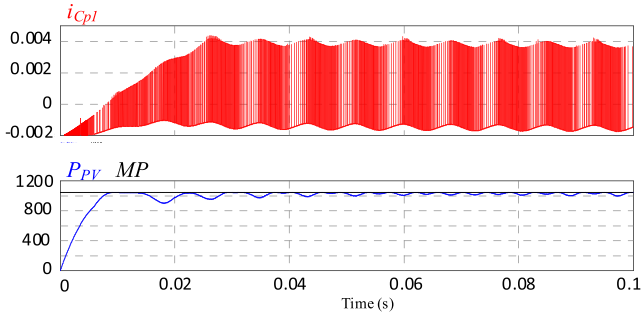

FIGURE 23. Leakage current to the parasitic capacitor C_{P1} under change of current reference with C_{PV}=470μF.

the inductive case and at 0.2s a change in the phase reference is made to 10 degrees in the capacitive case.

Fig. 21 show the current from the PV panel i_{PV}, the inductor current i_L, the injected current i_f and the grid voltage V_{grid} attenuated 5 times as it can see the current from panel is close to the maximum current to the PV panel from table 7 that is I_m=7A due to MPPT algorithm.

The parasitic capacitance current i_{Cp1}, and the theoretical maximum power point (*MP*) is exhibited in Fig. 22 since the start-up. Where it is illustrated that the leakage current is around 4mA and the power demanded from the PV panel is close to the theoretical maximum power point that is 1050 Watts, this results was obtained with a capacitor C_{PV}=1000μF. Fig. 23 shows the same data but with a capacitor C_{PV}=470μF.

Table 8 shows a comparison of different characteristic between topologies with the same application, some efficiency values are given in the paper and in other cases the value is estimated by means of the information from papers.

VII. CONCLUSION

In this paper, a single-phase transformerless current-source inverter topology has been presented for grid-connected PV applications. A common mode converter was used in order to reduce the ground leakage current without adding additional active components to the circuit; the control applied is based on the finite control strategy. The sinusoidal reference waveform is tracking, but also it is in phase with the grid voltage. The value of the output current can be changed by means of the control of the current in the flying inductor. This reference may be obtained from a maximum power point tracking algorithm to make a more effective system.

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