IEEE Access
Multidisciplinary : Rapid Review : Open Access Journal

Received September 3, 2018, accepted September 19, 2018, date of publication October 1, 2018, date of current version November 9, 2018.

Digital Object Identifier 10.1109/ACCESS.2018.2873081

RBER Aware Multi-Sensing for Improving Read Performance of 3D MLC NAND Flash Memory

MENG ZHANG[1], FEI WU[1], (Member, IEEE), XUBIN CHEN[2], YAJUAN DU[3], WEIHUA LIU[1], YAHUI ZHAO[1], JIGUANG WAN[1], AND CHANGSHENG XIE[1], (Member, IEEE)

[1]Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, Wuhan 430074, China
[2]Electrical, Computer and Systems Engineering Department, Rensselaer Polytechnic Institute, NY 12180, USA
[3]School of Computer Science and Technology, Wuhan University of Technology, Wuhan 430070, China

Corresponding author: Fei Wu (wufei@hust.edu.cn)

This work was supported in part by the National Natural Science Foundation of China under Grant 61872413, Grant U1709220, Grant 61821003, and Grant 61876019, in part by the Wuhan Science and Technology Project, China, under Grant 2017010201010108, in part by the Fundamental Research Funds for the Central Universities, China, under Grant 2016YXMS019, in part by the 111 Project, China, under Grant B07038, and in part by the Key Laboratory of Data Storage System, Ministry of Education.

ABSTRACT 3D-multi-level cell (MLC) NAND flash memory adopts 3D stack technology and stores two bits per cell, leading to improved storage capacities, but sacrificing data reliability. Low-density parity-check (LDPC) codes showing strong error correction capability benefit from their soft decision decoding, which is widely exploited to guarantee data reliability. Nevertheless, adopting LDPC codes can introduce a concern about read performance, because their iterative soft-decision decoding requires Log-Likelihood Ratio (LLR) information, called soft decision information, by applying multi-sensing voltages. This process of obtaining LLR information leads to high sensing and transferring latencies, lowering down 3D-MLC read performance. In particular, when raw bit error rates (RBER) are much higher due to the long retention periods and program/erase (P/E) cycles, this problem becomes more serious. In this paper, we propose a RBER-aware multi-sensing scheme for reducing sensing and transferring latencies, and thus improving read performance. This proposed scheme exploits the variations of RBER in flash pages with the increase of retention time and P/E cycles to dynamically apply sensing voltages. Simulation results show that this scheme significantly decreases the number of required sensing voltages while maintaining LDPC error correction capability, enhancing 3D-MLC read performance.

INDEX TERMS 3D MLC NAND flash memory, LDPC codes, multi-sensing, decoding latency, read performance.

I. INTRODUCTION

NAND flash memory, current a popular nonvolatile memory, has high storage capacity benefiting from multi-bit stored in per cell and three-dimensional stack structure [1], [2]. However, data reliability becomes a problem due to high raw bit error rates (RBER) from retention (RT) errors and program/erase (P/E) cycles [3]. As P/E cycles and retention time increase, the oxide layer of storage cells is gradually worn out so that electrons are much easier to leak, leading to overlapping on threshold voltage distributions with high percentages. Therefore, bit errors become much higher when data is read from the cells. To reduce bit errors and, hence, ensuring data reliability, error correction codes (ECC), one of the most effective means, are extensively adopted in NAND flash-based storage systems [4]–[6]. ECCs with strong error capability are well received in 3D NAND flash memories. Low-density parity-check (LDPC) codes [7]–[9] become more prevalent because their soft decision decoding introduces remarkable error correction performance. Nevertheless, using LDPC codes leads to a concern about read performance [10], [11]. LDPC soft decision decoding is launched by inputting the initial soft decision information (i.e., the log-likelihood ratio (LLR) information) when RBER is much higher. In terms of NAND flash-based storage systems, one needs to apply multi-sensing voltages in the overlapping region of two adjacent threshold voltage distributions to obtain more accurate LLR information. High precision LLR information can improve decoding performance and reduce decoding latency. However, more accurate LLR information requires to apply more sensing voltages, resulting in

2169-3536 © 2018 IEEE. Translations and content mining are permitted for academic research only.
Personal use is also permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

higher sensing and transferring latencies [12], [13]. The read performance of flash is directly affected by the numbers of applying sensing voltages. Especially, when retention and P/E cycles-induced RBER is much higher, applied sensing voltages increase, causing higher read latency and therefore significantly cutting down 3D-MLC read performance.

It has been found [14], [15] that various error patterns exist in 3D floating gate (FG) MLC NAND flash memory, including value dependency of program disturb errors, value dependency of retention errors, and changes of RBER related with retention periods and P/E cycles different from planar flash. In this paper, based on these error patterns, we develop a scheme, called RBER aware multi-sensing, to reduce sensing and transferring latencies when implementing LDPC soft decision decoding operations. This proposed scheme exploits the effects of program disturb errors, retention errors, and P/E cycles on RBER of lower and upper pages to dynamically apply the sensing voltages for minimizing the number of using voltages, while retaining LDPC error correction capability. Simulation results show that 3D-MLC read performance is significantly improved due to decreased sensing and transferring latencies.

The main contributions of this paper are as follows.

- We show that upper and lower pages require to apply different numbers of sensing voltages for correcting decoding due to different margins of storage state distributions-induced unbalanced RBER when 3D-MLC suffers from program disturb, retention, and P/E cycles.
- By leveraging error patterns of 3D FG MLC NAND flash memory, we propose the RBER aware multi-sensing scheme for enhancing sensing and transferring-effected read performance. During decoding, this proposed scheme considers the effects of program disturb, retention, and P/E cycles-induced RBER on sensing voltages.
- To assess 3D-MLC read performance, we first do a numerical analysis based on the constructed read latency model, then exploit real workloads to evaluate the effects of the scheme on the system performance. Simulation results show that 3D-MLC read performance is significantly improved, verifying the effectiveness of the scheme.

The remainder of this paper is arranged as follows: Related backgrounds about 3D-MLC NAND flash and LDPC codes are introduced in Section II. The 3D-MLC read latency model is established in Section III. The proposed scheme is presented in Section IV. Section V gives the simulation methodology and analyzes results. Section VI introduces the related work and Section VII draws conclusions.

II. BACKGROUND

In this section, we introduce some related background about 3D-MLC NAND flash memory, including basic block structure, noise-induced bit errors. We also describe LDPC basic operations to clearly understand its working principle, involving how to gain initial LLR and min-sum decoding.

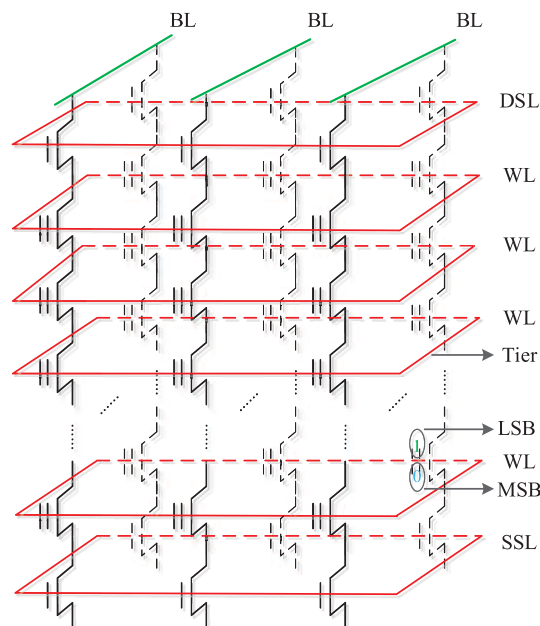

FIGURE 1. Block structure of 3D MLC NAND flash memory.

A. BASIC BLOCK STRUCTURE OF 3D-MLC NAND FLASH

3D-MLC NAND flash memory blocks are a three-dimensional stack structure, which include several storage tiers, as shown in Fig. 1. Each tier contains a certain number of word lines (WL) that consist of a large number of storage cells. There are two types of pages in each WL, lower and upper pages. Lower pages (LP) are constituted by collecting all left bits called least significant bits (LSB) from two bits in each cell. Similarly, upper pages (UP) are formed by collecting all right bits called most significant bits (MSB) [3]. The bit string in the same tier consists of the bit lines (BL). Source selective lines (SSL) and drain selective lines (DSL) control basic operations of 3D-MLC by applying voltages, such as read, program, and erase.

B. NOISE-INDUCED BIT ERRORS

Although the 3D-MLC NAND flash with high storage capacity benefits from adopting tier architecture and storing multi-bit per cell, data reliability and lifetime are significantly affected. The reason is that bit errors in 3D-MLC cells are induced by various noises, such as program disturb between storage tiers, program disturb of inner storage tiers, retention, and P/E cycles. 3D-MLC NAND flash memory stores two bits per cell with four storage states, as shown in Fig. 2. Here, 11 represents erased states without injected electrons. 10, 00, and 01 denote programmed states. The number of electrons in these states is increasing from low to high. The margins between adjacent states are different in 3D FG MLC NAND flash memory. The larger margin about 1v is between state 11 and state 10 and between state 00 and state 01. Conversely, the smaller margin about 0.6v is between state 10 and state 00. Therefore, there are different percentages of state shifts when experiencing retention errors.

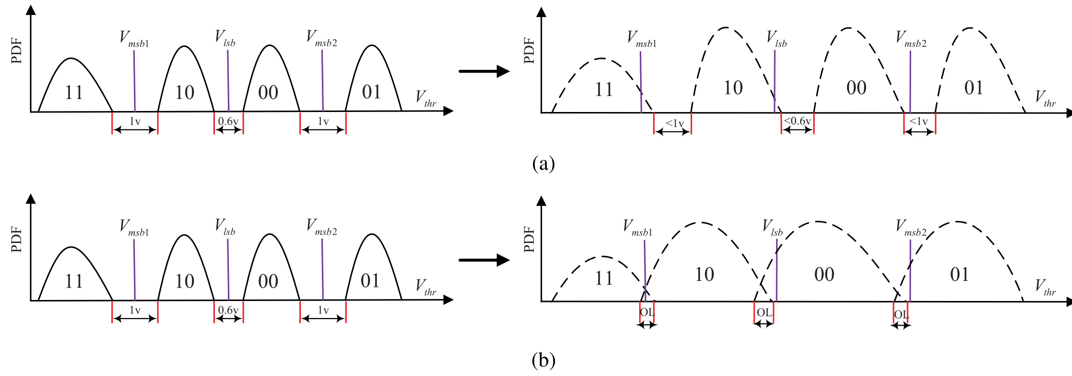

FIGURE 2. Threshold voltage distributions before and after undergoing program disturb and retention. Before 3D-MLC cells experience program disturb and retention, two bit values can be clearly distinguished by using reference voltages V_{lsb}, V_{msb1} and V_{msb2}. (a) left: before program disturb, right: after program disturb. (b) left: before retention, right: after retention, the window overlap (OL).

The percentage of state 00 shifting to state 10 is 53.4% due to the narrower margin between such two states, leading to higher bit errors in lower pages. The percentages of state 10 shifting to state 00 and state 10 shifting to state 11 are only 24.4% and 20.8%, respectively due to the larger margin between these two states [15]. The unbalanced state shift percentages lead to different bit errors in lower and upper pages when experiencing retention errors and P/E cycles. Moreover, program disturb happens between tiers and inner tiers, leading to threshold voltages shift to the right due to additional electrons into 3D-MLC cells under the effects of parasitic capacitance coupling.

C. LDPC CODES IN 3D-MLC NAND FLASH

In this section, we present how to use LDPC codes in 3D-MLC NAND flash memory, including calculating LLR information, decoding process with min-sum (MS) algorithms [5], [17].

1) LLR INFORMATION CALCULATION

LDPC codes show strong error correction capability benefiting from its soft decision decoding. Such decoding needs to gain the LLR information called soft decision information that represents the correct probability of bit 1 or 0. Obtaining the LLR information is an important step in using multi-sensing voltages. The LLR information is calculated through the following formulas [4].

$$LLR = \log \frac{P(bit = 1|V_{thr})}{P(bit = 0|V_{thr})} \tag{1}$$

where V_{thr} denotes the detected cell threshold voltage. P represents the probability density function (PDF). Specifically, for 3D-MLC NAND flash memory, the LLR information of LSB and MSB can be calculated by the formulas (2) and (3) [11].

$$LLR^{lsb} = \log \frac{\int_{v_{l1}}^{v_{l2}} P^{11}(v)dv + \int_{v_{l1}}^{v_{l2}} P^{10}(v)dv}{\int_{v_{l1}}^{v_{l2}} P^{00}(v)dv + \int_{v_{l1}}^{v_{l2}} P^{01}(v)dv} \tag{2}$$

$$LLR^{msb} = \log \frac{\int_{v_{m1}}^{v_{m2}} P^{11}(v)dv + \int_{v_{m1}}^{v_{m2}} P^{10}(v)dv}{\int_{v_{m1}}^{v_{m2}} P^{00}(v)dv + \int_{v_{m1}}^{v_{m2}} P^{01}(v)dv} \tag{3}$$

where v_{l1}, v_{l2}, v_{m1}, and v_{m2} represent the sensing voltages applied to the lower and upper pages.

2) MS DECODING

The min-sum decoding [17], [18], based on the belief propagation algorithm, is the soft decision decoding. This procedure is divided into three steps: check node updates, variable node updates, and soft-to-hard decoding decisions, to iteratively update the initial LLR information. After experiencing each update, the LLR information becomes more accurate to close the correct codeword information. For example, assuming that the calculated initial LLR information is $L_1, L_2, L_3, \ldots, L_9$, a group of real values to denote the probability of bit 1 or 0. By exploiting the following formulas [10], [11] to update this group LLR information, in the first step, check nodes connected by each variable node are updated via the formula (4).

$$C_{ij}^{l+1} = \prod_{k \in P(i)\backslash j} sgn(V_{ik}^{l}) \cdot \min \left\{ \left| V_{ik}^{l} \right| : k \in P(i)\backslash j \right\} \tag{4}$$

where l is the iteration number. $P(i)\backslash j$ is all check nodes connected by adjacent check nodes excluding the jth variable node. In the second step, variable nodes connected by each check node are updated via the formula (5).

$$V_{ij}^{l+1} = LLR_j + \sum_{m \in Q(j)\backslash i} C_{mj}^{l+1} \tag{5}$$

where LLR_j is the initial LLR information of the jth variable node. $Q(j)\backslash i$ is all variable nodes connected by adjacent check nodes excluding the ith check node. In the last step, the updated LLR information is decided via the formula (6) to change the soft information into the binary bits.

$$V_j^{l+1} = LLR_j + \sum_{i \in Q(j)} C_{ij}^{l+1} \tag{6}$$

where $Q(j)$ is all check nodes connected by the adjacent j^{th} variable node. The updated LLR information is assumed as $V_1, V_2, \ldots, V_8, V_9$. If $V_j \geq 0$, $bit_j = 1$, otherwise $bit_j = 0$. When one of two conditions is satisfied, $\vec{Bits} \cdot H^T = \vec{0}$ or l

with the maximum iteration, the decoding process is terminated. Otherwise, we continue implementing the decoding operations.

III. BIT ERRORS AND READ LATENCY MODELS OF 3D-MLC NAND FLASH

In this section, we study the bit error probability and asymmetric sensing voltages of upper and lower pages, and establish the read latency model to evaluate read performance of 3D-MLC NAND flash memory.

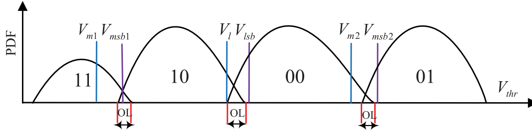

FIGURE 3. The threshold voltage distribution after 3D-MLC cells suffer from program disturb, retention, and P/E cycles.

A. BIT ERROR PROBABILITY

We study bit error probabilities between the upper and lower pages based on the threshold voltage distributions after experiencing program disturb, retention, and P/E cycles. As shown in Fig. 3, V_{msb1} and V_{msb2} are the hard sensing voltages applied to the upper pages. V_{lsb} and V_l are the hard and soft sensing voltages, respectively, applied to the lower pages. V_{m1} and V_{m2} are the soft sensing voltages applied to upper pages. One needs to apply two hard sensing voltages to read bit data of upper pages. Only one hard sensing voltage is required to read bit data of lower pages. When exploiting hard sensing voltages V_{msb1} and V_{msb2} to read bit data of upper pages, the bit error probability of $1 \rightarrow 0$ and $0 \rightarrow 1$ can be expressed through models (7) and (8). When using V_{lsb} to read data bit of lower pages, the bit error probability can be expressed through models (9) and (10), where $\mu_{11}, \sigma_{11}, \mu_{10}, \sigma_{10}, \mu_{00}, \sigma_{00}$, and μ_{01}, σ_{00} are the means and standard deviations of state 11, state 10, state 00, and state 01 distributions, respectively. V_{min} and V_{max} represent the minimum and maximum threshold voltages of the state 11 and 01 distributions. These models of bit error probability are constructed by using the methods of partition summation and approximation. Here n is equal to the number of partitioned voltage intervals. Δ is equal to the length of the divided voltage interval, $\Delta v_1 = \frac{V_{msb1}-V_{\min}}{n}$, $\Delta v_2 = \frac{V_{max}-V_{msb2}}{n}$, $\Delta v = \frac{V_{msb2}-V_{msb1}}{n}$, and $\Delta v_3 = \frac{V_{lsb}-V_{msb1}}{n}$. Similarly, when using soft sensing voltages to read bit data of upper and lower pages, the bit error probability models are also established and the initial LLR information is also approximately calculated.

$$
\begin{aligned}
&P_{msb}^{1\rightarrow 0} \\
&\approx \int_{V_{\min}}^{V_{msb1}} P^{10}(v)dv + \int_{V_{msb2}}^{V_{\max}} P^{00}(v)dv \\
&\approx \sum_{i=1}^{n} \int_{V_{\min}}^{V_{\min}+i\Delta v_1} P^{10}(v)dv + \sum_{i=1}^{n} \int_{V_{msb2}}^{V_{msb}+i\Delta v_2} P^{00}(v)dv \\
&\approx \Delta v_1 \cdot (pf_{\Delta v_1}^{10} - pf_{v_{\min}}^{10}) + \Delta v_2 \cdot (pf_{\Delta v_2}^{00} - pf_{v_{\max}}^{00}) \quad (7)
\end{aligned}
$$

$$
\begin{aligned}
&P_{msb}^{0\rightarrow 1} \\
&\approx \int_{V_{msb1}}^{V_{msb2}} P^{11}(v)dv + \int_{V_{msb1}}^{V_{msb2}} P^{01}(v)dv \\
&\approx \sum_{i=1}^{n} \int_{V_{msb1}}^{V_{msb1}+i\Delta v} P^{11}(v)dv + \sum_{i=1}^{n} \int_{V_{msb1}}^{V_{msb1}+i\Delta v} P^{01}(v)dv \\
&\approx \Delta v \cdot (pf_{\Delta v}^{11} - pf_{v_{msb}}^{11}) + \Delta v \cdot (pf_{\Delta v}^{01} - pf_{v_{msb}}^{01}) \quad (8)
\end{aligned}
$$

$$
\begin{aligned}
&P_{lsb}^{1\rightarrow 0} \\
&\approx \int_{V_{\min}}^{V_{msb1}} P^{00}(v)dv + \int_{V_{msb1}}^{V_{lsb}} P^{01}(v)dv \\
&\approx \sum_{i=1}^{n} \int_{V_{\min}}^{V_{\min}+i\Delta v_1} P^{00}(v)dv + \sum_{i=1}^{n} \int_{V_{msb1}}^{V_{msb1}+i\Delta v_3} P^{01}(v)dv \\
&\approx \Delta v_1 \cdot (pf_{\Delta v_1}^{00} - pf_{v_{minsb}}^{00}) + \Delta v_3 \cdot (pf_{\Delta v_3}^{01} - pf_{v_{minsb}}^{01}) \quad (9)
\end{aligned}
$$

$$
\begin{aligned}
&P_{lsb}^{0\rightarrow 1} \\
&\approx \int_{V_{\min}}^{V_{msb1}} P^{11}(v)dv + \int_{V_{msb1}}^{V_{lsb}} P^{10}(v)dv \\
&\approx \sum_{i=1}^{n} \int_{V_{\min}}^{V_{\min}+i\Delta v_1} P^{11}(v)dv + \sum_{i=1}^{n} \int_{V_{msb1}}^{V_{msb1}+i\Delta v_3} P^{10}(v)dv \\
&\approx \Delta v_1 \cdot (pf_{\Delta v_1}^{11} - pf_{v_{minsb}}^{11}) + \Delta v_3 \cdot (pf_{\Delta v_3}^{10} - pf_{v_{minsb}}^{10}) \quad (10)
\end{aligned}
$$

For the formulas (7), (8), (9), and (10),

$$P^{s_i}(v) = \frac{1}{\sqrt{2\pi}\sigma_{s_i}} \exp(-\frac{(v-\mu_{s_i})^2}{2\sigma_{s_i}^2})(s_i \in \{11, 10, 00, 01\})$$

For the formulas (7),

$$pf_{\Delta v_l}^{s_i'} = \sum_{i=0}^{n} \frac{1}{\sqrt{2\pi}\sigma_{s_i'}} \exp(-\frac{(v_{\min} + i\Delta v_l - \mu_{s_i'})^2}{2\sigma_{s_i'}^2}),$$

where $s_i' \in \{10, 00\}$ and $l \in \{1, 2\}$,

$$pf_{v_{\min}}^{10} = \alpha^{10}(\exp(-\frac{(v_{\min}-\mu_{10})^2}{2\sigma_{10}^2}) - \exp(-\frac{(v_{msb1}-\mu_{10})^2}{2\sigma_{10}^2}))$$

$$pf_{v_{\max}}^{00} = \alpha^{00}(\exp(-\frac{(v_{msb2}-\mu_{00})^2}{2\sigma_{00}^2}) - \exp(-\frac{(v_{\max}-\mu_{00})^2}{2\sigma_{00}^2}))$$

where $\alpha^{10} = \frac{1}{2\sqrt{2\pi}\sigma_{10}}$ and $\alpha^{00} = \frac{1}{2\sqrt{2\pi}\sigma_{00}}$.

For the formulas (8),

$$pf_{\Delta v}^{s_i''} = \sum_{i=0}^{n} \frac{1}{\sqrt{2\pi}\sigma_{s_i''}} \exp(-\frac{(v_{msb1} + i\Delta v - \mu_{s_i''})^2}{2\sigma_{s_i''}^2})$$

$$pf_{v_{msb}}^{s_i''} = \alpha^{s_i''}(\exp(-\frac{(v_{msb1}-\mu_{11})^2}{2\sigma_{s_i''}^2}) - \exp(-\frac{(v_{msb2}-\mu_{s_i''})^2}{2\sigma_{s_i''}^2}))$$

where $s_i'' \in \{11, 01\}$ and $\alpha^{s_i''} = \frac{1}{2\sqrt{2\pi}\sigma_{s_i''}}$.

For the formulas (9),

$$pf_{\Delta v_k}^{s_i'''} = \sum_{i=0}^{n} \frac{1}{\sqrt{2\pi}\sigma_{s_i'''}} \exp(-\frac{(v_{\min} + i\Delta v_k - \mu_{s_i'''})^2}{2\sigma_{s_i'''}^2}),$$

where $s_i'' \in \{00, 01\}$ and $k \in \{1, 3\}$

$$pf^{00}_{v_{minsb}} = \alpha^{00}(\exp(-\frac{(v_{\min}-\mu_{00})^2}{2\sigma^2_{00}})-\exp(-\frac{(v_{msb1}-\mu_{00})^2}{2\sigma^2_{00}}))$$

$$pf^{01}_{v_{minsb}} = \alpha^{01}(\exp(-\frac{(v_{msb1}-\mu_{01})^2}{2\sigma^2_{01}})-\exp(-\frac{(v_{\min}-\mu_{01})^2}{2\sigma^2_{01}}))$$

where $\alpha^{01} = \frac{1}{2\sqrt{2\pi}\sigma_{01}}$.

For the formulas (10),

$$pf^{s_i''''}_{\Delta v_k} = \sum_{i=0}^{n} \frac{1}{\sqrt{2\pi}\sigma_{s_i''''}} \exp(-\frac{(v_{\min} + i\Delta v_k - \mu_{s_i''''})^2}{2\sigma^2_{s_i''''}}),$$

where $s_i'''' \in \{11, 10\}$ and $k \in \{1, 3\}$

$$pf^{11}_{v_{minsb}} = \alpha^{11}(\exp(-\frac{(v_{\min}-\mu_{11})^2}{2\sigma^2_{11}})-\exp(-\frac{(v_{msb1}-\mu_{11})^2}{2\sigma^2_{11}}))$$

$$pf^{10}_{v_{minsb}} = \alpha^{10}(\exp(-\frac{(v_{msb1}-\mu_{10})^2}{2\sigma^2_{10}})-\exp(-\frac{(v_{\min}-\mu_{10})^2}{2\sigma^2_{10}}))$$

where $\alpha^{11} = \frac{1}{2\sqrt{2\pi}\sigma_{11}}$.

For the formula (7), when MSB is read, the hard sensing voltages V_{msb1} and V_{msb2} are applied between state 11 and 10 and between state 00 and 01. When V_{msb1} is applied, if the detected threshold voltage is less than V_{msb1}, the bit is read as 1 with high probability. However, the threshold voltage may fall into the range of the state 10 distribution. Once this happens, the bit 1 is misread as 0. This probability can be calculated as the first part of the formula (7). When V_{msb2} is applied, if the detected threshold voltage is greater than V_{msb2}, the bit is read as 1 with high probability. Nevertheless, the threshold voltage may fall into the range of the state 01 distribution. Once this happens, the bit 1 is also misread as 0. This probability can be calculated as the second part of the formula (7). Similarly, formulas (8), (9), and (10) can also be explained in the same way.

B. ASYMMETRIC SENSING VOLTAGES

Intuitively, there are different sensing voltages needed to detect the bit data of upper and lower pages because different numbers of threshold voltage window shifts result in different bit errors. For example, the threshold voltage window shifts happen between state 11 and state 10, state 00 and state 01, leading to bit errors in upper pages. The threshold voltage window shift appears between state 10 and state 00, resulting in bit errors in lower pages. There are more sensing voltages applied to upper pages to distinguish the bit value. However, as explained above, there are more prone to threshold voltage window shifts between state 10 and state 00 due to smaller margins when retention periods are long in 3D-MLC NAND flash memory. This can induce more bit errors in lower pages so that it may need more soft sensing voltages to obtain more accurate LLR information for fleetly correcting decoding.

C. ESTABLISHMENT OF READ LATENCY MODELS

In the process of flash read, the latency mainly includes three parts, i.e., flash sensing, data transferring, and LDPC decoding. In the flash sensing phase, data is read from flash medium to the page register. In the data transferring phase, data is transferred from the page register to the LDPC decoder. In the LDPC decoding phase, bit errors are corrected by the LDPC decoder. There are different sensing voltages to implement flash sensing operations. The more flash sensing operations are, the longer sensing and transferring latencies will be. Moreover, there are different iterations to implement the LDPC decoding operations. Based on this analysis, we establish a read latency model of 3D NAND flash memory, shown in (11) and (12), for better evaluating the read performance of upper and lower pages.

$$\begin{aligned} Lat^{up}_{read} &= Lat^{up}_{fs} + Lat^{up}_{trf} + Lat^{up}_{dec} \\ &= N^{up}_{fs} * (lat^{up}_{fs} + lat^{up}_{trf}) + N^{up}_{itr} * lat^{up}_{itr} \end{aligned} \quad (11)$$

$$\begin{aligned} Lat^{lp}_{read} &= Lat^{lp}_{fs} + Lat^{lp}_{trf} + Lat^{lp}_{dec} \\ &= N^{lp}_{fs} * (lat^{lp}_{fs} + lat^{lp}_{trf}) + N^{lp}_{itr} * lat^{lp}_{itr} \end{aligned} \quad (12)$$

Where Lat^{up}_{read} denotes the read latency of upper pages. Lat^{up}_{fs}, Lat^{up}_{trf}, and Lat^{up}_{dec} represent flash sensing latency, data transferring latency, and LDPC decoding latency of upper pages, respectively. N^{up}_{fs} denotes the number of sensing voltages used in upper pages. lat^{up}_{fs} denotes the latency taken by each flash sensing. lat^{up}_{trf} denotes the transferring latency taken by each sensing voltage. N^{up}_{it} represents the number of decoding iterations required to correct bit errors in upper pages. lat^{up}_{it} represents the latency cost by each decoding iteration. Other parameters have the same definition for lower pages. After using the proposed scheme, the reduced latency model can be expressed as (13) and (14).

$$\begin{aligned} \beta^{up} &= \frac{(N^{up}_{bfs} - N^{up}_{afs})(lat^{up}_{fs} + lat^{up}_{trf}) + (N^{up}_{bitr} - N^{up}_{aitr})lat^{up}_{itr}}{N^{up}_{bfs}(lat^{up}_{fs} + lat^{up}_{trf}) + N^{up}_{bitr}lat^{up}_{itr}} \\ \beta^{up} &= \frac{(N^{up}_{bfs} - N^{up}_{afs}) + (N^{up}_{bitr} - N^{up}_{aitr})\alpha^{up}}{N^{up}_{bfs} + N^{up}_{bitr}\alpha^{up}} \end{aligned} \quad (13)$$

$$\begin{aligned} \beta^{lp} &= \frac{(N^{lp}_{bfs} - N^{lp}_{afs})(lat^{lp}_{fs} + lat^{lp}_{trf}) + (N^{lp}_{bitr} - N^{lp}_{aitr})lat^{lp}_{itr}}{N^{lp}_{bfs}(lat^{lp}_{fs} + lat^{lp}_{trf}) + N^{lp}_{bitr}lat^{lp}_{itr}} \\ \beta^{lp} &= \frac{(N^{lp}_{bfs} - N^{lp}_{afs}) + (N^{lp}_{bitr} - N^{lp}_{aitr})\alpha^{lp}}{N^{lp}_{bfs} + N^{lp}_{bitr}\alpha^{lp}} \end{aligned} \quad (14)$$

Where $\alpha^{up} = \frac{lat^{up}_{itr}}{lat^{up}_{fs}+lat^{up}_{trf}}$ and $\alpha^{lp} = \frac{lat^{lp}_{itr}}{lat^{lp}_{fs}+lat^{lp}_{trf}}$. β^{up} and β^{lp} represent the decreased ratio of read performance of upper and lower pages. N^{up}_{aitr} and N^{up}_{bitr} represent the number of decoding iterations of upper pages after and before exploiting the proposed scheme, respectively. N^{up}_{afs} and N^{up}_{bfs} denote the numbers of sensing voltages used in upper pages after and before using the scheme. Similarly, the parameters of N^{lp}_{aitr}, N^{lp}_{bitr}, N^{lp}_{afs}, and N^{lp}_{bfs} can be defined for the lower pages.

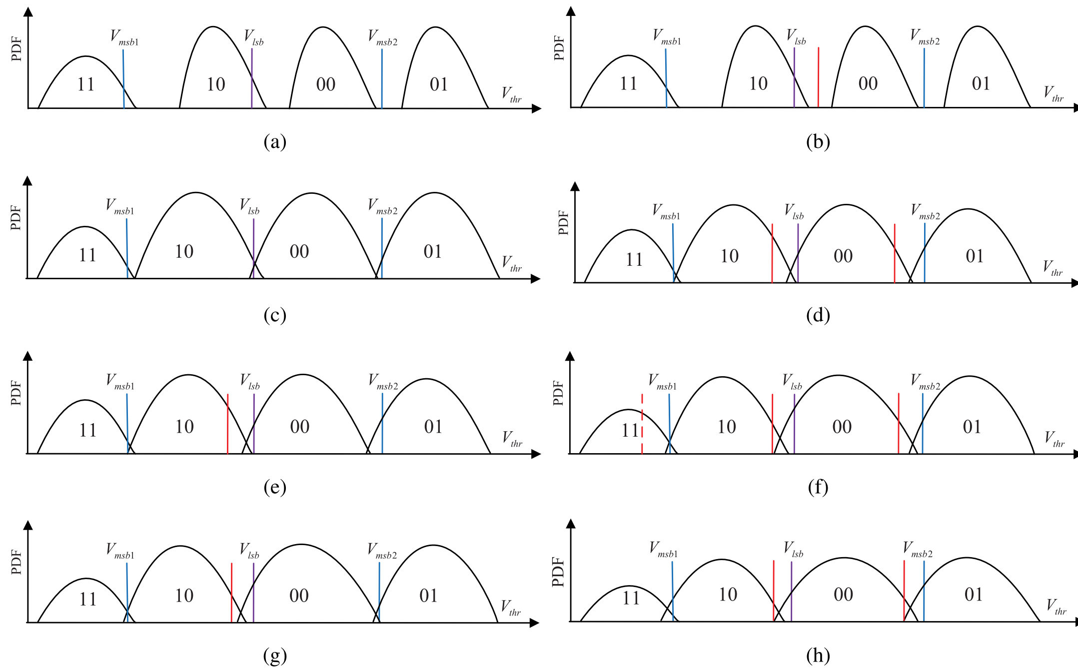

FIGURE 4. Schematic of the proposed scheme. (a) Lower pages: applying 1 sensing voltage for RT 1 day and P/E ≤ 2000. Upper pages: applying 2 sensing voltages for RT 1 day and P/E ≤ 4000 . (b) Lower pages: applying 2 sensing voltages for RT 1 day and 2000 < P/E ≤ 4000. Upper pages: applying 2 sensing voltages for RT 1 day and P/E ≤ 4000. (c) Lower pages: applying 1 sensing voltage for RT 1 week and P/E ≤ 500. Upper pages: applying 2 sensing voltages for RT 1 week and P/E ≤ 1500 . (d) Lower pages: applying 2 sensing voltages for RT 1 week and 500 <P/E≤ 4000. Upper pages: applying 3 sensing voltages for RT 1 week and 1500 <P/E≤ 4000 . (e) Lower pages: applying 2 sensing voltages for RT 1 month and P/E≤ 2500. Upper pages: applying 2 sensing voltages for RT 1 month and P/E≤ 1500. (f) Upper pages: applying 3 sensing voltages for RT 1 month and 1500 ≤ P/E ≤ 3000, and applying 4 sensing voltages for RT 1 month and 3000 <P/E≤ 4000 . (g) Lower pages: applying 2 sensing voltages for RT 1 year and P/E≤ 1500. Upper pages: applying 2 sensing voltages for RT 1 year and P/E≤ 500. (h) Lower pages: applying 2 sensing voltages for RT 5 years and P/E≤ 500. Upper pages: applying 3 sensing voltages for RT 5 years and P/E≤ 1000 .

IV. RBER-AWARE MULTI-SENSING

In this section, we present the proposed scheme, RBER-aware multi-sensing. We dynamically apply sensing voltages based on RBER induced by program disturb, retention, and P/E cycles for meeting the needs of reliability at different stages of 3D-MLC NAND flash memory. The scheme is capable of reducing the use of redundancy sensing voltages when implementing soft decision decoding to guarantee data reliability, leading to the number of decreased sensing voltages. The read performance is significantly improved by reducing read and transferring latencies. First, there are different margins between four state distributions of 3D MLC NAND flash, as given in reference [15]. Second, state 00 shifting to state 10 can lead to bit errors in lower pages. State 10 shifting to state 11 and state 01 shifting to state 00 can cause bit errors in upper pages. However, when experiencing the same P/E cycles and retention periods, the error percentages are much higher for the lower pages due to smaller margins (i.e., 0.6v). Conversely, the error percentages are much lower for the upper pages due to larger margins (i.e., 1v). The larger margins can generate stronger resistance to noise interference (i.e., it can tolerate more P/E cycles and longer retention periods). Therefore, for the same P/E cycles and retention periods, there are different RBERs in lower and upper pages. When implementing the LDPC decoding operations to correct bit errors in lower and upper pages, different numbers of sensing voltages with different intervals are needed. We dynamically apply the sensing voltages according to the threshold voltage shift characteristics, as shown in Figure 4. Although the variation of RBER with P/E cycles is quite different for different NAND flash chips, each sensing voltage can tolerate a determined RBER range. Once the RBER is beyond the range, the additional sensing voltage has to be used. In terms of different NAND flash chips, the RBER induced by retention and P/E cycles always changes from low to high. Different numbers of sensing voltages used can obtain different error correction capabilities for LDPC decoding.

Fig. 4 gives the scheme for different sensing voltages applied on lower and upper pages at different P/E cycles and retention time. Specifically, there are relatively low RBER at the early stage of P/E cycles in retention 1 day. The program disturb, making cell threshold voltages shift to the right, is considered as the main effect factor of causing RBER. Besides, as explained above, the RBER of lower and upper pages is different due to different margins of cell threshold voltages. There are different sensing voltages needed to implement hard and soft decision decoding. In this scheme, as shown in Fig. 4 (a), the hard decision decoding to correct errors in lower pages is triggered by using 1 sensing voltage

when P/E cycles are less than 2000. Once the P/E cycles are greater than 2000, the number of sensing voltages is increased to perform soft decision decoding according to the threshold voltage drift. Moreover, the sensing voltage interval is much larger due to a small amount of voltage drift in short retention time. It does not need more accurate LLR information to trigger soft decision decoding. As retention time increases, more charges leak from the cells, and this interval can be properly narrowed to adapt the variation and obtain more accurate LLR information for increasing error correction capability. For upper pages, the hard decision decoding with 2 sensing voltages can correct errors to ensure the reliability when P/E cycles are less than 4000 due to low RBER.

In retention 1 week, the RBER is relatively high so that the hard decision decoding for lower pages is used when P/E cycles are less than 500. The soft decision decoding is still exploited to guarantee the reliability. According to voltage drift to the right induced by retention, the extra sensing voltage is applied to the left of the first voltage and the interval is narrowed, compared with retention 1 day. For upper pages, the hard decision decoding only tolerates the P/E cycles to 1500. When P/E cycles are beyond 1500, utilizing 3 sensing voltages triggers the soft decision decoding. The extra sensing voltage is applied to the left of V_{lsb2}. Although there are the same margins between state 11 and state 10, state 00 and state 01, different voltage drift speeds lead to different drift ranges, i.e., larger drift range between state 00 and state 01. The applied sensing voltage range of upper pages is greater than that of lower pages. This is because larger margin can tolerate stronger noise disturb, leading to low bit errors. Thus, the soft decision decoding does not require more accurate LLR information.

In retention 1 month, the RBER is much higher than that of retention 1 day or 1 week. The hard decision decoding can not correct bit errors in lower pages. The soft decision decoding is needed to ensure data reliability. However, the soft decision decoding when using 2 sensing voltages only tolerates the P/E cycles to 2500. For upper pages, the hard decision decoding can maintain the P/E cycles to 1500. The soft decision decoding with 3 sensing voltages is leveraged, but fails to correct errors when P/E cycles are greater than 1500 and less than 3000. Therefore, using 4 sensing voltages triggers the soft decision decoding when P/E cycles are greater than 3000 and less than 4000. One extra sensing voltage is applied to the left of V_{lsb1} and the interval is relatively large due to much slower voltage drift speed of state 10 compared with state 01.

In retention 1 year and 5 years, due to much higher RBER, we only consider the P/E cycles with less than 1500, the soft decision decoding for lower and upper pages with 2 and 3 sensing voltages can keep the P/E cycles to 1500 in retention 1 year. The hard decision decoding for upper pages only retains the P/E cycles to 500. For retention 5 years, the soft decision decoding for lower and upper pages with 2 and 3 sensing voltages can maintain the P/E cycles to 500 and 1000, respectively. The scheme of RBER-aware multi-sensing that dynamically applies the sensing voltages to trigger hard and soft decision decoding is verified by performing computer simulations described in Section V. B. The applied methods of sensing voltages also come from the computer simulation results.

V. SIMULATION AND RESULTS

In this section, we first introduce the simulation methodology, including the simulation setup and parameters, and then give the results and analysis.

A. SIMULATION METHODOLOGY

In this simulation experiment, we first use the Matlab platform to perform a numerical analysis of the scheme. The parity-check matrix is constructed. Randomly generated bit sequences are encoded by LDPC codes to produce redundancy bits for correcting errors. The generated codewords are mapped into the gray code and sent to the AWGN channel with approximate flash memory channel [20]. The maximum decoding iterations are set as 50 [11]. The BF and NMS algorithms are considered as the hard and soft decoding algorithms, respectively. In the simulation process we consider the retention model [21], [22] that is given as follows:

$$\begin{aligned} \mu_t &= \alpha * K_{cons2} * PE^{0.5} \\ \sigma_t^2 &= \alpha * K_{cons3} * PE^{0.6} \end{aligned} \qquad (15)$$

where μ_t and σ_t^2 are the mean and variance. $\alpha = K_{cons1} * (V_{programmed} - V_{erased}) * ln(1 + t/t_0)$, $K_{cons1} = 0.333$, $K_{cons2} = 4 \times 10^{-4}$, $K_{cons3} = 2 \times 10^{-6}$, $V_{programmed}$ and V_{erased} represent the threshold voltages of program and erasure states, respectively. t and t_0 denote the retention and initial time, respectively. The means and standard deviations of states 11, 10, 00, and 01 are set as −1.2v, 0.28v, 0.85v, 0.1v, 2.15v, 0.1v, 3.85v, and 0.1v respectively. The maximum threshold voltage denoted as V_{max} is set as −0.5v, 1.2v, 2.5v, and 4.2v for distributions of state 11, 10, 00, and 01. Similarly, the minimum threshold voltage represented as V_{min} is set as −1.9v, 0.5v, 1.8v, and 3.5v. Sensing voltages of lower pages are set as 1.2v, 1.3v, 1.4v, 1.5v, and 1.7v. P/E cycles are changed from 500 to 4000. Retention periods are increased from 1 day, 1 week, 1 month, 1 year to 5 years for keeping consistency with the 3D-MLC characteristics introduced in [15]. Sensing voltages of upper pages are set as −0.5v, 0v, 2.3v, 2.5v, and 3.0v. Therefore, the margins between state 11 and 10, and also between state 10 and 00 are 1v and 0.6v, respectively. For assessing the read performance of 3D-MLC NAND flash memory, we set the latency cost by each decoding iteration as 0.5μs [9]. The sensing latency is set as 50μs. The transfer latency is set as 20μs [21], [23]. To further evaluate the system performance, we exploit the Disksim simulator [24] with the SSD module, which is widely used [9], [12], [13], [23] to evaluate NAND flash-based storage system performance, in order to conduct the simulation experiment by collecting real traces with different read ratios. In the system simulation, we configure the SSD

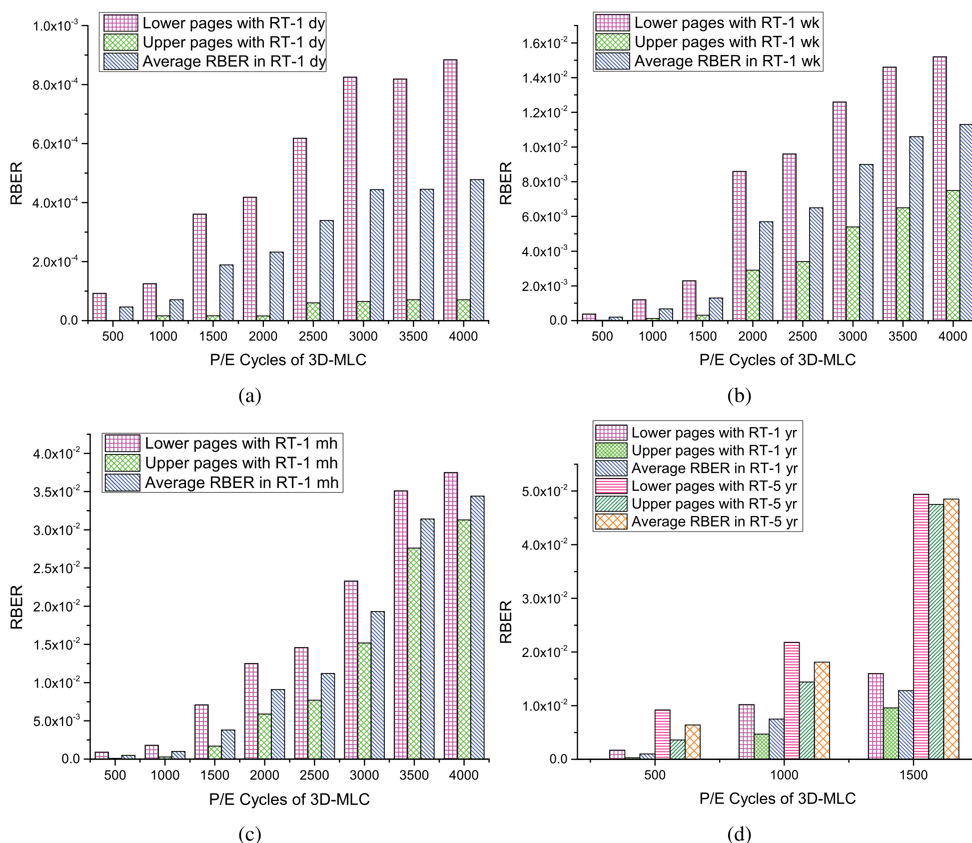

FIGURE 5. **The variation of RBER in Lower pages (LP) and upper pages (UP) under different retention periods and P/E cycles. (a) RBER of retention 1 day. (b) RBER of retention 1 week. (c) RBER of retention 1 month. (d) RBER of retention 1 year and 5 years.**

with eight channels. Each channel has eight planes. Each plane has 2048 blocks. Each block has 256 pages. Each page size is 4KB.

B. RESULTS AND ANALYSIS

In this section, we first simulate RBER of upper and lower pages under different P/E cycles and retention periods. Fig. 5(a) shows the increasing trend with P/E cycles when the retention period is 1 day. There is a greater RBER difference between lower and upper pages, a higher percentage in lower pages, but less than 1.0×10^{-3}. The variation of average RBER simulated in this experiment is close to the trend described in reference [15]. Fig. 5 (b) and 5 (c) show the RBER variations under retention 1 week and 1 month, respectively. Regardless of lower or upper pages, it rapidly increases with P/E cycles and retention periods as main effect factors. For the retention 1 year and 5 years, we only simulate the RBER of lower and upper pages when P/E cycles are changed from 500 to 1500. This is because it has become extremely high and even approximately reached 10^{-1} after 1500 P/E cycles. The difference becomes much narrower with the increases of P/E cycles and retention periods. Different margins between state distributions lead to different bit errors in lower and upper pages. There are more prone to bit errors in lower pages induced by the state shift from 10 to 00 since the smaller margin between such two state distributions has a weak resistance to noise interferences. Once the distribution boundary crosses the read reference voltage, it will happen to bit errors. Conversely, there are larger margins between state 11 and state 10, state 00 and state 01, resulting in a relatively strong resistance to noise interferences. However, such resistance also becomes weak with the increase of retention periods, narrowing the gap.

We will study the effects of the proposed scheme on LDPC decoding iterations for the lower and upper pages of 3D-MLC when retention periods and P/E cycles are changed. Fig. 6(a) shows the change trend of decoding iterations with P/E cycles in retention 1 day. For lower pages, when using 1 sensing voltage to implement hard decision decoding, iterations increase with P/E cycles such that bit errors cannot be corrected due to limited error correction capability of BF algorithms. For reducing bit errors and, hence, ensuring data reliability, soft decision decoding is leveraged by increasing the number of sensing voltages. Conventionally, the soft sensing voltages are applied at the left and right around the hard decision voltage, causing the use of unnecessary sensing voltages. We can rely on the bit error characteristics induced by retention and P/E cycles to apply the sensing voltage. As shown in Fig. 6(a),

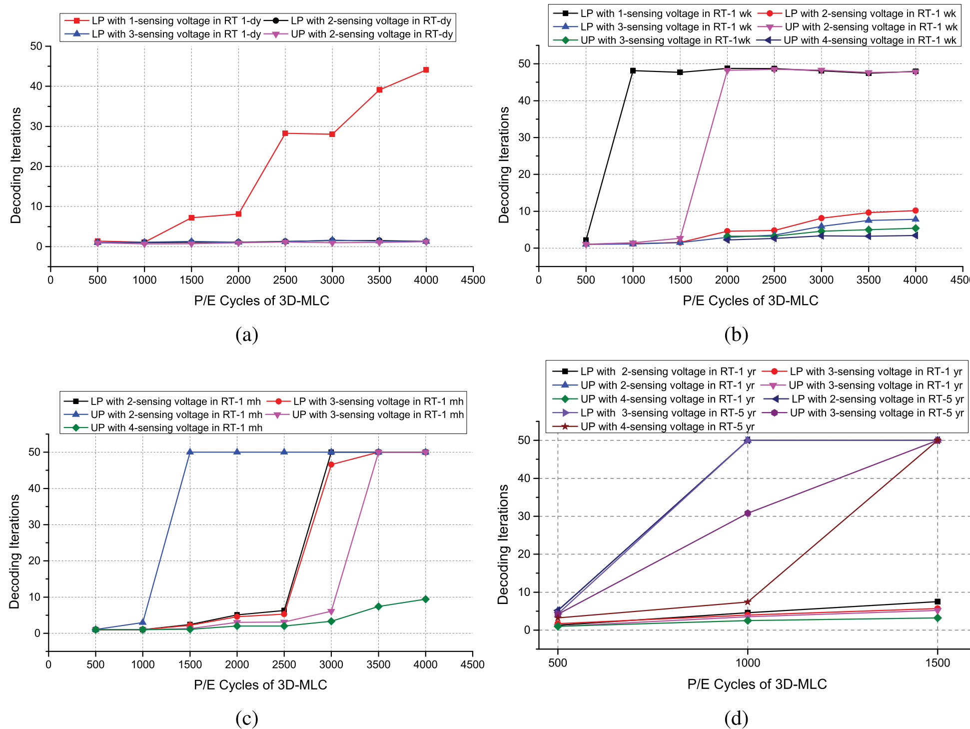

FIGURE 6. The variations of decoding iterations of lower and upper pages under different retention periods and P/E cycles. (a) Decoding iterations of retention 1 day. (b) Decoding iterations of retention 1 week. (c) Decoding iterations of retention 1 month. (d) Decoding iterations of retention 1 year and 5 years.

by using 2 sensing voltages, the decoding iterations of lower pages are low and very close to decoding iterations when applying 3 sensing voltages. For upper pages, only exploiting hard decision decoding via 2 sensing voltages can correct bit errors due to low RBER in the range of error correction capability, resulting in low iterations.

Moreover, we count decoding iterations in retention 1 week when using different sensing voltages. Simulation results in Fig. 6 (b) show that the iterations of hard decision decoding with 1 sensing voltage for lower pages are high when P/E cycles are greater than 1000. The decoding iterations with using 2 sensing voltages for lower pages are slightly higher than when using 3 sensing voltages. However, the number of sensing voltages is reduced. For upper pages, the iterations of hard decision decoding with 2 sensing voltages are high when P/E cycles are greater than 2000. The decoding iterations with 4 sensing voltages are lower, compared with the decoding iterations with 3 sensing voltages because more sensing voltages make the LLR information more accurate, leading to strong error correction capability. However, this situation also causes higher read and transferring latencies.

We also study the variation trend of decoding iterations with the increase of P/E cycles in retention 1 month when exploiting different sensing voltages, as shown in Fig. 6(c). For lower pages, when using 1 sensing voltage to perform hard decision decoding, the iterations approximately approach the set maximum value. Therefore, this figure only shows the soft decision decoding results of lower pages. The decoding iterations with 2 sensing voltages and 3 sensing voltages are close. When P/E cycles are greater than 2500, the decoding iterations are high and reach to the maximum value because the much higher RBER is beyond the current error correction capability of soft decision decoding. For upper pages, the decoding iterations are high and get to the set maximum value at the P/E cycles of 1500. The proposed scheme, using 3 sensing voltages, leads to similar decoding iterations with 4 sensing voltages when P/E cycles are less than 3000. Unfortunately, the scheme can not correct bit errors and has high decoding iterations due to high RBER. Nevertheless, the bit errors can still be corrected by using 4 sensing voltages, introducing low iterations.

Moreover, we further investigate the impacts of different sensing voltages on decoding iterations at the P/E cycles increased from 500 to 1500 when retention periods are extended to 1 year and 5 years. As shown in Fig. 6 (d), for lower pages with retention 1 year, the decoding iterations are less than 10 after applying 3 and 4 sensing voltages. By leveraging 3 and 4 sensing voltages, the decoding iterations are also less than 10 for upper pages. Yet, the reliability is only ensured at the P/E cycle of 500 through 2 sensing voltages to perform hard decision decoding. High decoding iterations appear at the P/E cycle of 1000. For lower pages with retention 5 years, the soft decision decoding with 2 and 3 sensing voltages can only keep the low iterations at the P/E cycle of 500. The decoding iterations sharply increase with the P/E cycles, approaching the maximum value of 50. High RBER

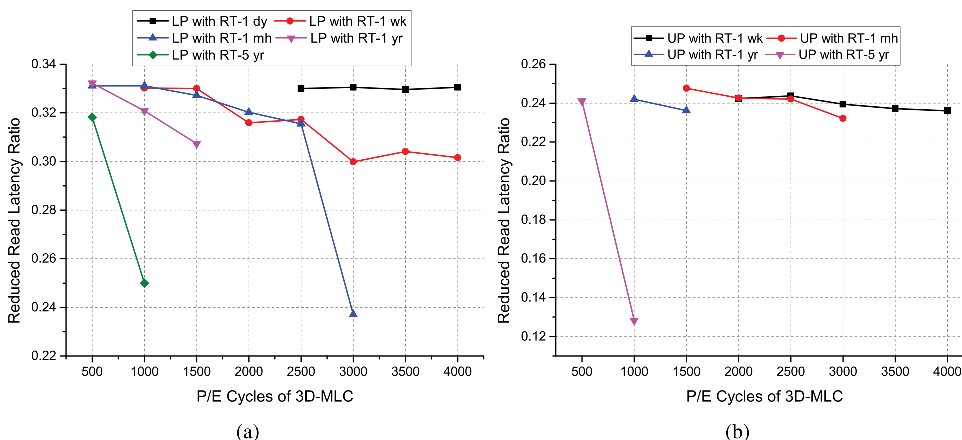

FIGURE 7. The reduced read latency ratio of lower and upper pages after using sensing voltages to implement soft decision decoding under different retention periods and P/E cycles. (a) Reduced read latency ratio of lower pages. (b) Reduced read latency ratio of upper pages.

induced by retention and P/E cycles causes high decoding iterations and reliability reduction as well as suboptimal read performance.

Finally, we evaluate the read performance by calculating the reduced read latency ratio based on models (13) and (14). Fig. 7 (a) and Fig. 7 (b) show the reduced read latency ratio of lower and upper pages with the increase of P/E cycles in different retention periods. In this evaluation, we consider the read latency decreased by exploiting soft decision decoding. For lower pages with retention 1 day, the soft decision decoding is leveraged at the P/E cycle of 2500 due to high decoding iterations caused by hard decision decoding. Therefore, the read latency ratio reduced to 33% is computed from the P/E cycle of 2500 to 4000, as shown in Fig. 7 (a). Similarly, in retention 1 week, the soft decision decoding is launched from the beginning of 500. The reduced read latency ratio shows a declining trend with P/E cycles, from 33% to 30%. This is because P/E cycles and retention-induced high RBER increases the decoding iterations when using 2 sensing voltages, compared with the decoding iterations when using 3 sensing voltages.

In retention 1 month, at the beginning of P/E cycles, the hard decision decoding fails to correct bit errors. The soft decision decoding with 2 sensing voltages is activated to reduce errors, but fails to correct errors at the P/E cycle of 3000, leading to the read latency ratio declining to 23.9%. Due to high RBER, in retention 1 year and 5 years, the proposed scheme can only maintain the reduced read latency ratio to 31% and 25%, respectively. Fig. 7 (b) shows the variation trend of reduced read latency ratio of upper pages with P/E cycles and retention periods. In retention 1 day, the hard decision decoding is capable to correct bit errors, and there is no need to leverage soft decision decoding. Therefore, this figure only shows the reduced read latency ratio in retention 1 week, 1 month, 1 year, and 5 years. The proposed scheme only leverages the soft decision decoding at the P/E cycle of 2000 in retention 1 week. The read latency is decreased to 24%. In retention 1 month, the soft decision decoding is activated at the P/E cycle of 1500 by using 3 sensing voltages, but fails to correct bit errors from the start of 3000. Therefore, the proposed scheme applies 4 sensing voltages to perform soft decision decoding. The read latency is reduced from approximately 25% to 23%. Similarly, in retention 1 year, the read latency ratio is decreased from 24% to 23.8%. In retention 5 years, the read latency ratio is reduced from 24% to 13%. Different P/E cycles and retention periods can result in different RBERs of lower and upper pages such that different sensing voltages are required to implement soft decision decoding for correcting more bit errors, further inducing different read latencies of 3D-MLC NAND flash memory.

Furthermore, to assess the effects of the scheme on the system performance, we conduct a real workload based simulation experiment. In this simulation, we select the retention period 1 week as an example to study the system response latency for different traces under different P/E cycles. We count the system response latency reduction ratios of lower and upper pages, as shown in Fig. 8 (a) and Fig. 8 (b), respectively. The selected traces have different read ratios, and the SYN represents the synthetic trace. The AVR denotes the average system response reduction ratio of six different traces. Simulation results show that there are different system response latency reduction ratios for workloads with different read ratios. For example, for SRC with 97.86% read ratio, the system response latency is reduced by up to 35.5% and 25.5% for lower pages and upper pages, respectively. For TS with 17.58% read ratio, the system response latency is approximately decreased by 15.0% and 10.5%, respectively. The average response latency is approximately reduced by 25.5% and 20.4%, respectively. For workloads with high read ratio, when high RBER is beyond the error correction capability of hard decision decoding, LDPC soft decision decoding is frequently invoked, introducing high sensing and transferring latencies. After exploiting the proposed scheme, the reduced system response latency is more

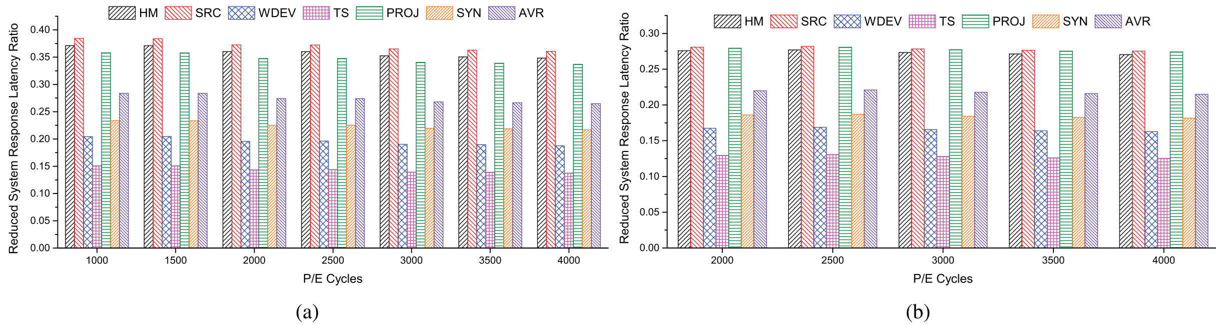

FIGURE 8. Reduced system response latency ratio under different real workloads when retention periods are set as 1 week. (a) System response latency reduction ratio of lower pages. (b) System response latency reduction ratio of upper pages.

obvious. As mentioned above, for the same P/E cycles and retention periods, there are higher RBER for the lower pages due to the narrower margins between threshold voltage distributions of state 10 and 00. The soft decision decoding is activated by using multi-sensing voltages when the P/E cycle is 1000 and retention time is 1 week. The reason is the bit errors exceed the error correction capability of hard decision decoding. Therefore, we count the system response latency when P/E cycles are increased from 1000 to 4000. Similarly, for the upper pages, there are lower RBER, the hard decision decoding can maintain the error correction capability when the P/E cycles are less than 2000. Once the P/E cycles are increased to 2000, the soft decision decoding is launched to reduce bit errors. Thus, we count the system response latency for upper pages from the beginning of 2000. The system response latency shows a steady change trend with the increase of P/E cycles since the applied numbers of sensing voltages can satisfy the reliability requirements in the variation range of P/E cycles. There are different system response latencies for lower and upper pages because different changes of RBER require different sensing voltages to obtain LLR information for implementing soft decision decoding.

C. DISCUSSION

In this paper, we focus on describing the proposed method and applying it to 3D FG MLC NAND flash. When performing LDPC soft decision decoding, different accuracy of soft decision information for lower and upper pages is obtained by applying multi-sensing voltages with different intervals according to different state shift percentages. Our proposed method can also be applied to 3D TLC and QLC for minimizing the use of sensing voltages, because their state transfer percentages are also different when experiencing retention and P/E cycles. Besides, the proposed method can also be used by combining other LDPC soft decision decoding algorithms, such as Layered Normalized Min-Sum [25] and Offset Min-Sum algorithms [26] among others. Since these algorithms are applied in NAND flash-based storage systems, they can also be used to obtain the LLR information for activating the soft decision process.

VI. RELATED WORK

There are many results proposed to study flash error characteristics and LDPC codes. Xiong *et al.* [14], [15] studied various error patterns of 3D-MLC NAND flash memory on a real FPGA platform, including the effects of program disturb, retention, and P/E cycles on RBER. Cai *et al.* [16] investigated various error characteristics of planar MLC NAND flash on a real FPGA hardware platform, such as retention, read interference, and program interference errors. By collecting large amounts of data from the Facebook data center, Meza *et al.* [27] conducted a large-scale study on flash failure characteristics. Tseng [28] *et al.* studied the flash error characteristics under the condition of power loss. Zhang *et al.* [29] tested the flash failure modes on an FPGA testing platform. Schroeder *et al.* [30] studied flash reliability characteristics by collecting the data from Google data centers. Cai *et al.* [52] investigated flash errors by collecting real experimental data, and developed corresponding recovery techniques to guarantee data reliability.

There are also some previous studies of the read performance of LDPC-based NAND flash memory. Zhao *et al.* [18] developed two schemes that are based on flash cell errors and can improve LDPC decoding throughput. Based on retention errors of MLC NAND flash, To improve read performance of solid state drives, Du *et al.* [21] developed a latency aware LDPC which is dependent on read level characteristics along with retention. Zhao *et al.* [23] proposed three effective schemes, relying on error characteristics of planar MLC flash, to improve read performance. Qiao *et al.* [31] developed a joint decoding scheme for improving LDPC decoding performance. Li *et al.* [32] proposed effective schemes to improve flash read performance by implementing different write and read strategies based on workload characteristics. Zhang [48] proposed a retention error-aware LDPC scheme to improve MLC read performance by reducing decoding latency. By exploiting channel characteristics of MLC flash memory, Ouyang *et al.* [51] proposed a non-uniform quantization method for the RBI-MSD algorithm of LDPC codes. Li *et al.* [12] proposed a smart soft sensing level placement scheme that is based on state shift characteristics of MLC cells. In [12, Fig. 3], the authors exploit the error

characteristics of planar MLC NAND flash, i.e., the error percentages of state S3 shift to S2 are much higher. Thus, more sensing voltages are applied between state S3 shift to S2, and without considering the effects of using sensing voltages with different intervals on LLR information precision. The sensing voltages with the same intervals are applied. Moreover, from the results of reference [14], [15], for the 3D MLC NAND flash, it is unnecessary to apply more sensing voltages between state 00 and state 01. This is because it decreases the error percentages induced by such two-state shifts. According to the RBER differences between the LSB and MSB pages, Zhang *et al.* [11] exploited the decoding results of the LSB pages with retention error characteristics for optimizing the soft decision information of decoding the MSB pages. The soft decision information of LSB pages does not change. The optimized soft decision information can improve error correction performance and, hence, reduce decoding latency. The work focuses on optimizing the LDPC soft decision error correction performance from the viewpoint of decoding algorithms. LDPC codes with excellent error correction performance are also used in emerging nonvolatile memory (NVM) technologies [50], communication systems [54], [55], and magnetic recording systems [53], [57]. In this paper, we focus on optimizing the method of obtaining the LLR information with different precision. Obtaining LLR information is the preprocessing of activating the LDPC soft decision decoding. Based on studying the error patterns of 3D-MLC [14], [15], we investigate the effects of RBER induced by program disturb, retention, and P/E cycles on LDPC codes. According to the variations of RBER in different retention periods and P/E cycles, we propose RBER-aware multi-sensing by dynamically adjusting the sensing voltage with different intervals to obtain LLR information with different precisions. This scheme can reduce the use of unnecessary sensing voltages when triggering the soft decision decoding at high RBER, while maintaining the LDPC error correction performance.

VII. CONCLUSION

P/E cycles and retention have a great effect on RBER of 3D-MLC NAND flash memory, leading to reduced data reliability and lifetime. LDPC codes with excellent error correction performance are widely used in order to improve reliability and lifetime. However, exploiting LDPC codes causes a problem about read performance because soft decision decoding requires LLR information by implementing multi-sensing operations, inducing high read and transferring latencies. In this paper, we propose a RBER-aware multi-sensing scheme to improve 3D-MLC NAND flash read performance while keeping the error correction capability. We dynamically adjust the sensing voltages based on the variations of RBER to satisfy requirements of different using stages and decrease read latency. Simulation results show the developed scheme significantly improves the read performance by lowering the use of unnecessary sensing voltages.

REFERENCES

[1] S. Ohshima and Y. Tanaka, "New 3D flash technologies offer both low cost and low power solutions," in *Proc. Flash Memory Summit*, Santa Clara, CA, USA, 2016.

[2] H. Kim, S.-J. Ahn, Y. G. Shin, K. Lee, and E. Jung, "Evolution of NAND flash memory: From 2D to 3D as a storage market leader," in *Proc. IMW*, Monterey, CA, USA, 2017, pp. 1–4.

[3] C. Zambelli *et al.*, "Characterization of TLC 3D-NAND flash endurance through machine learning for LDPC code rate optimization," in *Proc. IMW*, Monterey, CA, USA, May 2017, pp. 1–4.

[4] J. Wang, T. Courtade, H. Shankar, and R. D. Wesel, "Soft information for LDPC decoding in flash: Mutual-information optimized quantization," in *Proc. GLOBECOM*, Houston, TX, USA, Dec. 2011, pp. 1–6.

[5] H. Sun, W. Zhao, M. Lv, G. Dong, N. Zheng, and T. Zhang, "Exploiting intracell bit-error characteristics to improve min-sum LDPC decoding for MLC NAND flash-based storage in mobile device," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 24, no. 8, pp. 2654–2664, Aug. 2016.

[6] E. Yaakobi, L. Grupp, P. H. Siegel, S. Swanson, and J. K. Wolf, "Characterization and error-correcting codes for TLC flash memories," in *Proc. ICNC*, Maui, HI, USA, Jan./Feb. 2012, pp. 486–491.

[7] C. A. Aslam, Y. L. Guan, and K. Cai, "Retention-aware belief-propagation decoding for NAND flash memory," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 6, pp. 725–729, Jun. 2017.

[8] S. Tanakamaru, Y. Yanagihara, and K. Takeuchi, "Error-prediction LDPC and error-recovery schemes for highly reliable solid-state drives (SSDs)," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2920–2933, Nov. 2013.

[9] R.-S. Liu *et al.*, "EC-Cache: Exploiting error locality to optimize LDPC in NAND flash-based SSDs," in *Proc. DAC*, San Francisco, CA, USA, Jun. 2014, pp. 1–6.

[10] F. Wu *et al.*, "A program interference error aware LDPC scheme for improving NAND flash decoding performance," *ACM Trans. Embed. Comput. Syst.*, vol. 16, no. 5s, pp. 1–20, 2017.

[11] M. Zhang, F. Wu, Y. Du, C. Yang, C. Xie, and J. Wan, "CooECC: A cooperative error correction scheme to reduce LDPC decoding latency in NAND flash," in *Proc. ICCD*, Boston, MA, USA, Nov. 2017, pp. 657–664.

[12] Q. Li, L. Shi, C. J. Xue, Q. Zhuge, and E. H. M. Sha, "Improving LDPC performance via asymmetric sensing level placement on flash memory," in *Proc. ASP-DAC*, Chiba, Japan, Jan. 2017, pp. 560–565.

[13] Y. Du, Q. Li, L. Shi, D. Zou, H. Jin, and C. J. Xue, "Reducing LDPC soft sensing latency by lightweight data refresh for flash read performance improvement," in *Proc. DAC*, Austin, TX, USA, Jun. 2017, pp. 1–6.

[14] Q. Xiong *et al.*, "Characterizing 3D floating gate NAND flash," in *Proc. SIGMETRICS*, Urbana-Champaign, IL, USA, 2017, pp. 31–32.

[15] Q. Xiong *et al.*, "Characterizing 3D floating gate NAND flash: Observations, analyses, and implications," *ACM Trans. Storage*, vol. 14, no. 2, p. 16, 2018.

[16] Y. Cai, E. F. Haratsch, O. Mutlu, and K. Mai, "Error patterns in MLC NAND flash memory: Measurement, characterization, and analysis," in *Proc. DATE*, Dresden, Germany, Mar. 2012, pp. 521–526.

[17] J. Zhao, F. Zarkeshvari, and A. H. Banihashemi, "On implementation of min-sum algorithm and its modifications for decoding low-density parity-check (LDPC) codes," *IEEE Trans. Commun.*, vol. 53, no. 4, pp. 549–554, Apr. 2005.

[18] W. Zhao, H. Sun, M. Lv, G. Dong, N. Zheng, and T. Zhang, "Improving min-sum LDPC decoding throughput by exploiting intra-cell bit error characteristic in MLC NAND flash memory," in *Proc. MSST*, Santa Clara, CA, USA, Jun. 2014, pp. 1–6.

[19] J. Jung and I.-C. Park, "Multi-bit flipping decoding of LDPC codes for NAND storage systems," *IEEE Commun. Lett.*, vol. 21, no. 5, pp. 979–982, May 2017.

[20] Y. Cai, E. F. Haratsch, O. Mutlu, and K. Mai, "Threshold voltage distribution in MLC NAND flash memory: Characterization, analysis, and modeling," in *Proc. DATE*, Grenoble, France, Mar. 2013, pp. 1285–1290.

[21] Y. Du, D. Zou, Q. Li, L. Shi, H. Jin, and C. J. Xue, "LaLDPC: Latency-aware ldpc for read performance improvement of solid state drives," in *Proc. MSST*, Santa Clara, CA, USA, 2017, pp. 1–12.

[22] Y. Pan, G. Dong, Q. Wu, and T. Zhang, "Quasi-nonvolatile SSD: Trading flash memory nonvolatility to improve storage system performance for enterprise applications," in *Proc. HPCA*, New Orleans, LA, USA, Feb. 2012, pp. 1–10.

[23] K. Zhao, W. Zhao, H. Sun, T. Zhang, X. Zhang, and N. Zheng, "LDPC-in-SSD: Making advanced error correction codes work effectively in solid state drives," in *Proc. FAST*, San Jose, CA, USA, Feb. 2013, pp. 244–256.

[24] J. S. Bucy, "The DiskSim simulation environment version 4.0 reference manual," Dept. Comput. Sci., Carnegie Mellon Univ., Pittsburgh, PA, USA, Tech. Rep. CMU-PDL-08-101, 2008.
[25] D. E. Hocevar, "A reduced complexity decoder architecture via layered decoding of LDPC codes," in *Proc. SIPS*, Austin, TX, USA, Oct. 2004, pp. 107–112.
[26] L. Lugosch and W. J. Gross, "Neural offset min-sum decoding," in *Proc. ISIT*, Aachen, Germany, Jun. 2017, pp. 1361–1365.
[27] J. Meza, Q. Wu, S. Kumar, and O. Mutlu, "A large-scale study of flash memory failures in the field," in *Proc. SIGMETRICS*, Portland, OR, USA, 2015, pp. 177–190.
[28] H.-W. Tseng, L. Grupp, and S. Swanson, "Understanding the impact of power loss on flash memory," in *Proc. DAC*, San Diego, CA, USA, Jun. 2011, pp. 35–40.
[29] M. Zhang, F. Wu, H. Huang, Q. Xia, J. Zhou, and C. Xie, "FPGA-based failure mode testing and analysis for MLC NAND flash memory," in *Proc. DATE*, Lausanne, Switzerland, Mar. 2017, pp. 434–439.
[30] B. Schroeder, R. Lagisetty, and A. Merchant, "Flash reliability in production: The expected and the unexpected," in *Proc. FAST*, Santa Clara, CA, USA, Feb. 2016, pp. 67–80.
[31] L. Qiao, H. Wu, D. Wei, and S. Wang, "A joint decoding strategy of non-binary LDPC codes based on retention error characteristics for MLC NAND flash memories," in *Proc. IMCCC*, Harbin, China, Jul. 2016, pp. 183–188.
[32] Q. Li *et al.*, "Access characteristic guided read and write cost regulation for performance improvement on flash memory," in *Proc. FAST*, Santa Clara, CA, USA, Feb. 2016, pp. 125–132.
[33] G. Dong, N. Xie, and T. Zhang, "On the use of soft-decision error-correction codes in NAND flash memory," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 2, pp. 429–439, Feb. 2011.
[34] S.-L. Chen, B.-R. Ke, J.-N. Chen, and C.-T. Huang, "Reliability analysis and improvement for multi-level non-volatile memories with soft information," in *Proc. DAC*, San Diego, CA, USA, 2011, pp. 753–758.
[35] Z. Wang, Z. Cui, and J. Sha, "VLSI design for low-density parity-check code decoding," *IEEE Circuits Syst. Mag.*, vol. 11, no. 1, pp. 52–69, Feb. 2011.
[36] R. G. Gallager, "Low-density parity-check codes," *IRE Trans. Inf. Theory*, vol. 8, no. 1, pp. 21–28, Jan. 1962.
[37] D.-H. Lee and W. Sung, "Estimation of NAND flash memory threshold voltage distribution for optimum soft-decision error correction," *IEEE Trans. Signal Process.*, vol. 61, no. 2, pp. 440–449, Jan. 2013.
[38] G. Dong, N. Xie, and T. Zhang, "Techniques for embracing intra-cell unbalanced bit error characteristics in MLC NAND flash memory," in *Proc. Globecom Workshops*, Miami, FL, USA, Dec. 2010, pp. 1915–1920.
[39] Y. Cai, Y. Luo, E. F. Haratsch, K. Mai, and O. Mutlu, "Data retention in MLC NAND flash memory: Characterization, optimization, and recovery," in *Proc. HPCA*, Burlingame, CA, USA, Feb. 2015, pp. 551–563.
[40] J. Guo, W. Wen, J. Hu, D. Wang, H. Li, and Y. Chen, "FlexLevel: A novel NAND flash storage system design for LDPC latency reduction," in *Proc. DAC*, San Francisco, CA, USA, Jun. 2015, pp. 1–6.
[41] F. Chen, D. A. Koufaty, and X. Zhang, "Understanding intrinsic characteristics and system implications of flash memory based solid state drives," in *Proc. SIGMETRICS*, Seattle, WA, USA, 2009, pp. 181–192.
[42] L. Zuolo, C. Zambelli, A. Marelli, R. Micheloni, and P. Olivo, "LDPC soft decoding with improved performance in 1X-2X MLC and TLC NAND flash-based solid state drives," *IEEE Trans. Emerg. Topics Comput.*, to be published.
[43] L. Dolecek, "Making error correcting codes work for flash memory," in *Proc. Flash Summit*, Santa Clara, CA, USA, 2014, pp. 1–58.
[44] Y. Nakamura, T. Iwasaki, and K. Takeuchi, "Machine learning-based proactive data retention error screening in 1Xnm TLC NAND flash," in *Proc. IRPS*, Pasadena, CA, USA, Apr. 2016, pp. 1–3.
[45] T. Nakamura, Y. Deguchi, and K. Takeuchi, "AEP-LDPC ECC with error dispersion coding for burst error reduction of 2D and 3D NAND flash memories," in *Proc. IMW*, Monterey, CA, USA, May 2017, pp. 1–4.
[46] L. M. Grupp *et al.*, "Characterizing flash memory: Anomalies, observations, and applications," in *Proc. MICRO*, New York, NY, USA, Dec. 2009, pp. 24–33.
[47] D. Burshtein, "On the error correction of regular LDPC codes using the flipping algorithm," *IEEE Trans. Inf. Theory*, vol. 54, no. 2, pp. 517–530, Feb. 2008.
[48] M. Zhang, F. Wu, X. He, P. Huang, S. Wang, and C. Xie, "REAL: A retention error aware LDPC decoding scheme to improve NAND flash read performance," in *Proc. MSST*, Santa Clara, CA, USA, May 2016, pp. 1–13.
[49] N. Agrawal, V. Prabhakaran, T. Wobber, J. D. Davis, M. S. Manasse, and R. Panigrahy, "Design tradeoffs for SSD performance," in *Proc. ATC*, Boston, MA, USA, Jun. 2008, pp. 57–70.
[50] L. Dolecek and Y. Cassuto, "Channel coding for nonvolatile memory technologies: Theoretical advances and practical considerations," *Proc. IEEE*, vol. 105, no. 9, pp. 1705–1724, Sep. 2017.
[51] S. Ouyang, G. Han, Y. Fang, and W. Liu, "LLR-distribution-based nonuniform quantization for RBI-MSD algorithm in MLC flash memory," *IEEE Commun. Lett.*, vol. 22, no. 1, pp. 45–48, Jan. 2018.
[52] Y. Cai, S. Ghose, E. F. Haratsch, Y. Luo, and O. Mutlu, "Error characterization, mitigation, and recovery in flash-memory-based solid-state drives," *Proc. IEEE*, vol. 105, no. 9, pp. 1666–1704, Sep. 2017.
[53] A. Hareedy, C. Lanka, and L. Dolecek, "A general non-binary LDPC code optimization framework suitable for dense flash memory and magnetic storage," *IEEE J. Sel. Areas Commun.*, vol. 34, no. 9, pp. 2402–2415, Sep. 2016.
[54] Y. Fang, S. C. Liew, and T. Wang, "Design of distributed protograph LDPC codes for multi-relay coded-cooperative networks," *IEEE Trans. Wireless Commun.*, vol. 16, no. 11, pp. 7235–7251, Nov. 2017.
[55] Y. Fang, G. Bi, Y. L. Guan, and F. C. M. Lau, "A survey on protograph LDPC codes and their applications," *IEEE Commun. Surveys Tuts.*, vol. 17, no. 4, pp. 1989–2016, 4th Quart., 2015.
[56] K.-C. Ho, C.-L. Chen, and H.-C. Chang, "A 520k (18900, 17010) array dispersion LDPC decoder architectures for NAND flash memory," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 4, pp. 1293–1304, Apr. 2016.
[57] Y. Fang, G. Han, G. Cai, F. C. Lau, P. Chen, and Y. L. Guan, "Design guidelines of low-density parity-check codes for magnetic recording systems," *IEEE Commun. Surveys Tuts.*, vol. 20, no. 2, pp. 1574–1606, 2nd Quart., 2018.

MENG ZHANG is currently pursuing the Ph.D. degree with the Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, Wuhan, China. His current research interests include error correction codes (ECC), applications of ECC in non-volatile memory (NVM) technologies, flash memory reliability, and NVM storage systems.

FEI WU received the B.S. and M.S. degrees in electrical automation, control theory and control engineering from Wuhan Industrial University, Wuhan, China, in 1997 and 2000, respectively, and the Ph.D. degree in computer science from the Huazhong University of Science and Technology (HUST), China, in 2005. She is currently an Associate Professor with the Information Storage Lab, Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology. Her research interests include computer architecture, non-volatile storage, and green storage. She is a Senior Member of the China Computer Federation, and a member of the Information Storage of China Computer Society.

XUBIN CHEN received the B.E. degree from Wuhan University, Wuhan, China, in 2009, and the M.S. degree from Fudan University, Shanghai, China, in 2012. He is currently pursuing the Ph.D. degree with the Electrical, Computer and Systems Engineering (ECSE) Department, Rensselaer Polytechnic Institute, Troy, NY, USA. His current research interests include data storage and memory system design across software and hardware stacks.

YAJUAN DU received the Ph.D. degree from the City University of Hong Kong and the Huazhong University of Science and Technology. She is currently with the Wuhan University of Technology. Her research interests cover computer storage systems and coding algorithms, such as the low-density parity-check codes in NAND Flash memory.

WEIHUA LIU received the B.S. degree with the School of Computer and Information Engineering, Henan University. He is currently pursuing the Ph.D. degree with the Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology. His current research interests include intelligent storage, machine learning, system, and non-volatile memories.

YAHUI ZHAO received the B.S. degree from the School of Communication Engineering from the Changchun University of Science and Technology. She is currently pursuing the Ph.D. degree with the Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology. Her current research interests include ECC in SSDs, NVMs storage systems.

JIGUANG WAN received the B.S. degree in computer science from Zhengzhou University, China, in 1996, the M.S. and Ph.D. degrees in computer science from the Huazhong University of Science and Technology, China, in 2003 and 2007, respectively. His research interests include computer architecture, networked storage systems, file systems, parallel and distributed systems.

CHANGSHENG XIE received the B.S. and M.S. degrees in computer science and technology from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 1982 and 1988, respectively. He is currently a Professor with the Wuhan National Laboratory for Optoelectronics, HUST. His research interests include new storage technology and architecture, multimedia computing and network, computer storage, and network storage and security. He has served as the Deputy Director of the Wuhan National Laboratory for Optoelectronics, the Deputy Director of the Computer Peripheral Equipment Committee, China Computer Federation, the committee member of information storage of the China Computer Society, and the Vice Chairman of the China Expert Committee, International Network Storage Industry Association.