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Novel Microwave Rectifier Optimizing Method and Its Application in Rectenna Designs

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ABSTRACT In this paper, a fast converging and computationally efficient iterative method for rectifier optimization is proposed. The method is carried out in the advance design system. By taking into account the interaction between the received power and output performance, the impedance of the Schottky diode when operating optimally in the rectifier can be precisely obtained once the spice model, operating frequency, and the dc load value are given. The impedance can be used to design the matching to minimize the insertion loss. The time and effort needed for the method are smaller than the optimizing tools provided in ADS and other related works, and the reliability of simulation is enhanced. For demonstration, a compact rectifier operating at 5.81 GHz is optimized, fabricated, and measured. The measured power conversion efficiency exceeds 40% at input power level ranging from −5.5 to 12.5 dBm, and the optimum reaches 69.4% at 8.2 dBm. Good agreement can be found between simulated and measured data. Finally, the rectifier is integrated with a high-efficiency antenna to form a rectenna design; 69.2% optimal efficiency is obtained at 0.41 mW/cm^2 power density in the measurement.

INDEX TERMS Iterating method, rectifier, rectenna, Schottky diode modeling, wireless power transfer.

I. INTRODUCTION

With the development of low-power sensor networks, RF Energy Transfer/Harvesting have become a popular way to power the electrical devices wirelessly and prolong their life cycles [1]–[4]. In these applications, a passive device called rectenna receives RF energy and converts it into DC power efficiently [5]–[8].

The rectenna consists of an antenna element and a rectifier. For energy harvesting application, the rectenna is designed to receive energy from all directions in an ambient environment with low RF power density, thus requiring an omni-directional circularly-polarized antenna and a rectifier which operates efficiently at low input power [9], [10], [27]–[30]. However, as reported in [11], the average received ambient power does not exceed −30 dBm indoor and −35dBm outdoor at all frequencies utilized for RF energy harvesting. The available incident power level is too low for the Schottky diode in a rectifier to operate, hence setting a limit on practicability. In this condition, power transferring via a fixed source becomes necessary. In addition, the wireless sensor nodes utilized for the Internet of Things applications are often placed at certain locations. Hence, an antenna with high directional gain and a rectifier with high optimal power conversion efficiency are required to receive power from a fixed direction in wireless power transfer [16]–[19], [26]. However, the high optimal power conversion efficiencies were achieved at large incident power level in these reported designs (> 1 mW/cm^2), thus shortening the available transmitting distance according to the Friis Transmission Formula.

The optimal power conversion efficiency (PCE) of the rectifier and the related input power level determine the performance of a rectenna. The antenna element can be designed based on the application requirement. Acting as the key component of a rectifier, the Schottky diode operates in a highly nonlinear condition influenced by input power level, operating frequency, and DC load value. Therefore, accurate modeling of the diode as well as reliable rectifier optimization attract an increasing attention. There are three main approaches on diode modeling and rectifier optimization. The first one is to analyze the diode's behavior in a rectifier in time-domain by creating closed-form equations [12], [13], [37]. This approach provides an anticipation of a diode's optimal performance for diode selection but, at the same time, it introduces an error due to the

ideal assumptions. The second approach is to conduct a comprehensive measurement for a diode to get the V-I data at different input power levels, operating frequencies and load values. Then empirical formulas are formed by curve fitting to describe the nonlinear behavior of the diode [14], [15]. This approach provides precise model for a certain diode, but with a drawback of the time-consuming measurements required and not being universal for other diode models.

The third approach is to optimize the rectifier using the EM simulator and nonlinear diode model provided in a simulation environment like Advance Design System (ADS) [31]–[33]. In order to minimize the insertion losses of the microwave components connected to the diode, these components should be optimized to match the input impedance of the diode with its optimal operating condition. Since the input impedance of the diode and its received power interact with each other, larger time and computational resource costs and the risk of non-convergence appear when using the automatic optimizing tools provided in ADS. In [34], [35], a solution for this problem is reported. By fabricating the rectifier without matching and measuring its input impedance, this impedance can be utilized to design the matching component of the rectifier. However, the input impedance of the diode will again be changed after improving the matching, which leads to an error.

This paper proposes a fast converging, computationally efficient iterative method for rectifier optimization. The method is carried out in ADS. By considering the interaction between the input impedance and the received power, the optimal input impedance of the diode can be precisely obtained once the spice model, operating frequency and DC load are given. The impedance can be used to optimize the performance of the rectifier. For validation, the advantages of the proposed method when compared with the automatic optimizing tool in ADS and other related works are analyzed. A rectifier operating at 5.8 GHz is optimized based on the proposed method. Good agreement can be found between simulated and measured data. Finally, the rectifier is integrated with a high-efficiency antenna to form a rectenna. 69.2% optimal efficiency is obtained at 0.41 mW/cm^2 power density in the measurement.

II. RECTIFIER OPTIMIAZATION METHOD

This section describes the framework of the optimizing method and verifies its performance. First, the circuit topology and tools utilized for the optimization in ADS are introduced. Then, the iterative optimizing method are discussed in detail. At last, the advantages of this method when compared with ADS and the related works are analyzed, and a practical rectifier design based on the proposed method is implemented for verification.

A. SCHEMATIC OF THE OPTIMIZING METHOD AND THE BASIC SETTINGS

The classical single-shunt rectifier and the equivalent circuit of a Schottky diode are depicted in Fig. 1. The Schottky

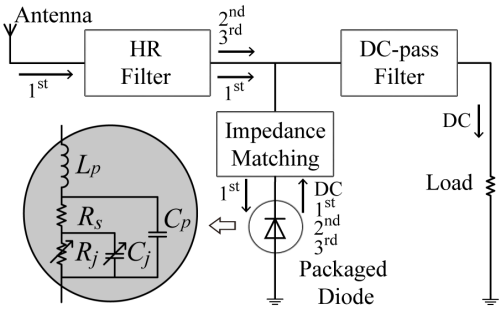

FIGURE 1. Topology and harmonic energy flowing of the conventional single-shunt rectifier.

TABLE 1. Key parameters of a Schottky diode.

Parameter	Description
I_S	Saturation current
B_v	Peak reverse breakdown voltage
I_{BV}	Maximum reverse leakage current
N	Ideal factor
C_{j0}	Zero-bias Junction capacitance
V_j	Threshold voltage
N_{bv}	Reverse breakdown ideality factor
X_{ti}	Saturation-current temperature exponent
E_g	Energy gap
M	Grading Coefficient

diode is reversely connected to the DC-pass filter in parallel. R_s denotes the series resistance of the diode and is provided by the manufacturer. R_j and C_j denote the nonlinearly varying junction resistance and capacitance of the diode. They are determined by the spice parameters provided in Table 1, the operating frequency, input power level and DC load [12], [13]. L_p and C_p denote the parasitic inductance and capacitance introduced by the diode package. For a certain package model, these two parameters are fixed and given.

The harmonic rejecting (HR) filter is a band-pass filter introduced next to the antenna element. Energy at fundamental frequency passes through the filter, while the higher order harmonic energy created by the operating Schottky diode will be reflected back to the diode for energy recollection, hence enhancing the PCE of the rectifier (Harmonic order higher than 3 is neglected). At the same time, a DC-pass filter is placed before the DC load to reflect the fundamental, 2nd and 3rd harmonic energy and pass the DC energy.

There are two reasons for selecting the single-shunt structure for the optimization. First, only one diode is utilized in the circuit, hence easing the difficulty on analyzing, and the circuit topologies with multi-diodes can be analyzed based on the single-diode case. Second, the DC-pass filter is replaced by an ideal inductance in the schematic. The DC load branch is considered open at RF frequencies, and the input impedance of the whole circuit is equal to that of the diode branch, thus making it easier to monitor the status of the diode.

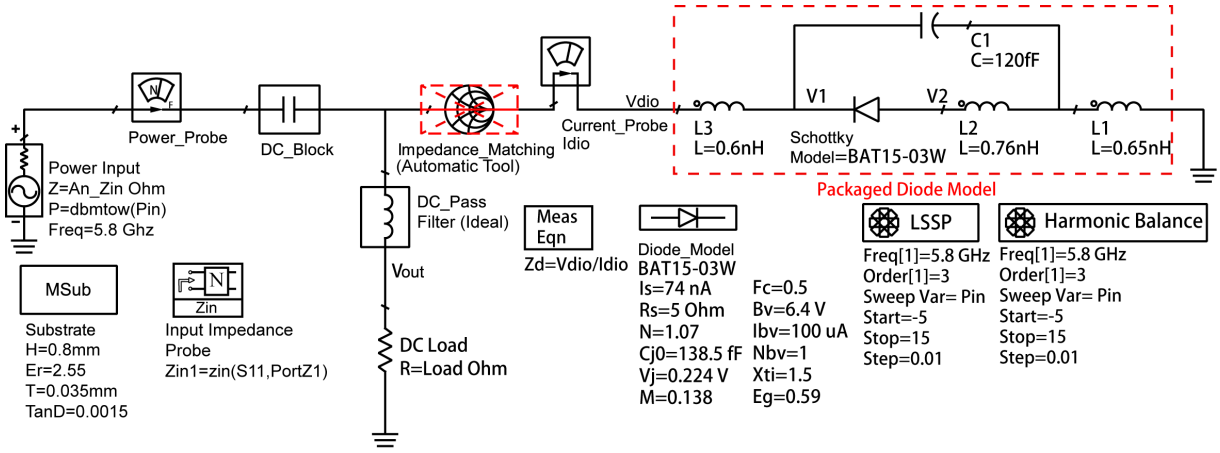

FIGURE 2. Schematic of the proposed optimizing method.

The ADS schematic is shown in Fig. 2. The antenna element is replaced by a RF power source with its internal impedance equal to the input impedance of the antenna *An_Zin* (in this demonstration, *An_Zin* = 50 Ohm). The HR filter is removed to eliminate its interference on matching and ease the monitoring of the diode impedance. The ideal impedance matching design tool is introduced to conveniently match the packaged diode. Rogers AD255C (ε_r = 2.55, h = 0.8 mm) is chosen as the substrate. Large Signal S-Parameter (LSSP) simulator is used to obtain the S_{11} and impedance of the circuit, while the Harmonic Balance (HB) simulator is introduced to monitor the voltage and current waveforms of each node. Diode model BAT15-03W (SOD323 package) is chosen for demonstration [36]. Since the input impedance and output voltage of the diode are influenced by the operating frequency, DC load, and the input power level, its optimal condition is determined by a particular set of these three parameters. Usually in an RF Energy Transfer application, the operating frequency of the system and the DC load carried by the rectifier can be predetermined. With the operating frequency to be set 5.8 GHz and the spice model of the BAT15-03W, the optimal load of the diode with highest PCE can be calculated through the method in [37] with a value of 1257 Ohm. For easier tuning, the DC load value is finally set 1300 Ohm.

B. THE ITERATIVE OPTIMIZING METHOD

The main goal of the proposed optimizing method is to obtain the input impedance of the Schottky diode with optimal PCE performance in the afore-mentioned conditions. To the best of our knowledge, the nonlinear diode model provided in ADS is conventionally used for PN junction diodes [38]. Hence, this schematic is verified first to prove its validity on simulating the optimal status of a Schottky diode.

By shorting the impedance matching tool and varying the input power level of the source, the relationship between peak reverse voltage of the diode and the output DC voltage versus input power is presented in Fig. 3(a). The input impedance of the diode when the input power varies is obtained by the input

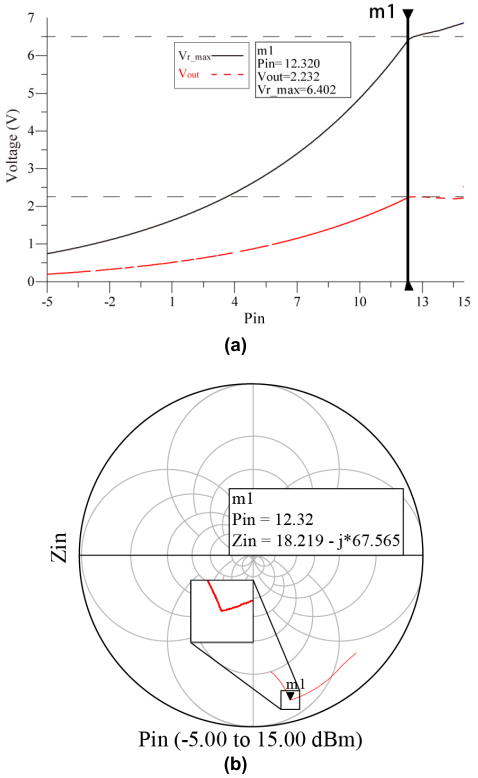

FIGURE 3. (a) Peak reverse voltage of the diode and V_{out} versus input power, (b) Input impedance of the diode versus input power.

impedance probe in ADS, as shown in Fig. 3(b). According to [12] and [13], the rectifier operates optimally when the diode's peak reverse voltage V_{r_max} reaches B_v. When V_{r_max} exceeds B_v, the inverse current rises quickly, and the PCE starts to decrease due to larger power consumption on series resistance R_s inside the diode. The B_v of diode model BAT15-03W is measured as 6.4 V with an inverse current of 100 μA. As can be observed in Fig. 3(a), V_{rmax} reaches 6.4 V when the input power P_{in} is equal to 12.32 dBm, and the output DC voltage V_{out} reaches a maximum of 2.23 V. At the same time, the input impedance of the diode Z_{d0} is in

the inflection point with a value of 18.219 − j*67.57 once P_{in} reaches 12.32 dBm. When P_{in} continues to increase, V_{out} stops rising. The PCE starts to decrease. Z_d varies according to another trend, which is similar to the phenomena reported in [25]. Hence, the results in Fig. 3 verify the validity of the schematic on simulating the optimal status of a Schottky diode. The initial optimal impedance Z_{d0} can be used to design the matching component.

Since Z_{d0} is obtained without any impedance matching to the source, a large amount of power is reflected back and the actual power received by the diode is much lower. After the introduction of matching component, the diode receives more power. The input impedance of the diode is again changed owing to the increased received power, which leads to a new mismatch. If this Z_{d0} is utilized to design the matching, a higher insertion loss will be produced, thus decreasing the optimal PCE. In ADS, the automatic optimization usually converges to a fixed goal. Hence, the varying of the diode impedance in each round of automatic optimization leads to a larger time and computational effort and to the risk of non-convergence.

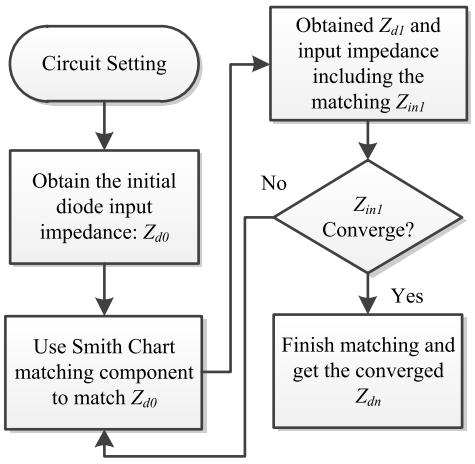

FIGURE 4. Flowchart of the proposed iteration theory.

To solve this problem, an iterative method with progresses shown in Fig. 4 is proposed in this work. The idea is to turn on the impedance matching design tool in Fig. 2 and optimize its performance by setting the matching goal to Z_{d0}. After improving the matching, the diode receives more power from the source and its input impedance shifts to a new value Z_{d1} (It should be noted that after turning on the matching component, the input impedance of the diode can no longer be monitored by the input impedance probe. Instead, it is calculated by the voltage and current values at node V_{dio} in Fig. 2.). This new Z_{d1} is then used to redesign the matching component. The "redesign-rematch-shift" progress forms an iteration. In each iteration step, the difference of power received by the diode becomes smaller and the impedance shifting of the diode mitigates. Finally, the input impedance of the circuit converges to a certain value, as shown in Fig. 5. Table 2 further provides data of Z_{dn} and the matched input impedance of the circuit Z_{in} at different iteration steps. As can

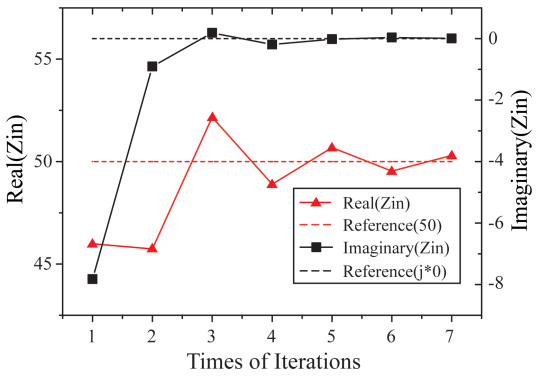

FIGURE 5. The input impedance of the circuit at different iteration steps.

TABLE 2. Diode performance at different iteration steps.

Iterating Times (n)	P_{in} (dBm)	Z_{dn}	Z_{inn}	S_{11} (dB)
0	12.32	18.219-67.665	18.219-67.665	-1.35
1	6.95	21.824-j68.068	45.991-j7.825	-20.79
2	6.75	22.402-j70.021	45.738-j0.905	-26.84
3	6.69	22.203-j69.072	52.164+j0.187	-33.45
4	6.65	22.338-j69.588	48.891-j0.193	-38.87
5	6.62	22.271-j69.297	50.687-j0.015	-43.32
6	6.60	22.305-j69.507	49.539+j0.036	-46.66
7	**6.60**	**22.284-j69.368**	**50.3+j0.003**	**-50.48**

be observed in Table 2, Z_{in1} is shifted from 50 Ohm after the first matching. The S_{11} of the circuit is only −20 dB. At larger iteration number, Z_d converges to a stable value while Z_{in} converges to 50 Ohm and S_{11} improves. By setting the threshold value of S_{11}, i.e. −50 dB, the iteration process is considered to be finished after certain steps of iterations, for example 7 in this demonstration.

C. VERIFICATION OF THE OPTIMIZING METHOD

The circuit in ADS can be automatically optimized both at schematic and layout levels [31]. The random and gradient approaches are available for automatic tuning in schematic optimization. S_{11} performance is set as the goal and the matching component is varied in the optimization. Since the impedance of the diode keeps changing after each variation, the error of the optimization can only be smaller when the restricted input power level for reaching the goal is set narrow (P_{in} range is finally set from 6 to 9 dBm in this experiment.). Without the optimization method, this restricted range of input power levels will have to be found after repeated trials, thus costing more effort and time.

The layout optimization considers the interconnecting effect of the components, thus increasing the simulation accuracy while costing more time and computational resources [39]. Since the momentum simulator can't process nonlinear components, the S-matrix of the distributed part of the circuit is simulated first, then the HB simulator in schematic uses this matrix and the packaged models of lumped elements to do the global simulation. To optimize the performance, the impedance of each distributed port of

the circuit should be set. Hence, the impedance of the diode in its optimal condition should be obtained in order to set the components connected to it. Although the automatic optimization can be carried out with default setting of the impedances (50 Ohm), it will again suffer the problem of the varying diode impedance when doing the global simulation.

To conclude, there are two advantages of the proposed method. First, it provides a design guidance for finding a precise input impedance of the diode with its optimal condition, thus improving the simulation accuracy. Second, this method offers a fast-converging tracking technique for defining the diode impedance with optimal performance, hence saving the time and computational resources.

TABLE 3. Simulated results of the method in different conditions.

Fixed: Load Value = 1300 Ohm, Diode Model: BAT15-03W Vary: Operating frequency (f_0)				
f_0 / GHz	Z_{dn} (Before)	Z_{dn} (After)	Iteration Rounds	S_{11} / dB
1.8	161.56-330.61j	84.06-282.08j	10	-55.5
2.4	93.10-254.38j	51.34-215.75j	9	-50.8
5.8	18.22-67.67j	22.28-69.37j	8	-50.5
Fixed: Operating frequency = 5.8 GHz, Diode Model: BAT15-03W Vary: Load Value / Ohm				
Load / Ohm	Z_{dn} (Before)	Z_{dn} (After)	Iteration Rounds	S_{11} / dB
500	29.73-52.39j	26.22-45.02j	4	-67.5
2000	13.80-71.36j	14.3-68.62j	8	-59.9
4000	8.148-72.90j	7.03-69.34	8	-52.2
Fixed: Operating frequency = 5.8 GHz, Load = 1300 Ohm Vary: Diode Model [31], [33], [35]				
Diode	Z_{dn} (Before)	Z_{dn} (After)	Iteration Rounds	S_{11} / dB
HSMS2860	24.31-88.86j	30.68-101.41j	5	-58.3
SMS7630	20.55-81.94	20.12-80.65j	3	-58.2
MA4E1317	13.14-93.81j	15.01-91.20j	12	-50.4

To validate the generality of the proposed modeling, three sets of simulations are carried out under different operating frequencies, load values and diode models. The simulated data are provided in Table 3. It can be observed that the S_{11} of the ideal circuits are all better than −50 dB within 12 rounds of iterations in different conditions. The impedances of the diodes converge to new values after iterations, and the deviation of the impedance before and after iterations become larger at lower frequency. The simulations also verify the advantages of the method on convergence rate and iteration rounds.

D. COMPACT RECTIFIER DESIGN

For further verification, a compact rectifier is designed and optimized. For low power input rectifier design, single-shunt structure is also preferable owing to single-diode consuming power and minimum components needed for the circuit [13]. As can be found in Fig. 1, both the HR and DC-pass filters need to block the 2nd and 3rd order harmonics, thus adding more microstrip components and increasing the total insertion loss. Such a schematic also makes it difficult to design the DC-pass filter with three stop-bands.

To solve this problem, the classical single-shunt structure is improved. As depicted in Fig. 6, the HR filter is kept but placed in front of the diode in the parallel branch. The 2nd and 3rd order harmonics are directly reflected back to the diode for second rectification. In this case, the DC-pass filter only needs to filter out the energy f_0, and the components for repeating filtering of the 2nd and 3rd order harmonics are eliminated. The design of the DC-pass filter is simplified and the total insertion loss is minimized, thus improving the PCE of the rectifier. However, these advantages come with a requirement that the HR filter should precisely match the input impedance of the optimally operating diode to lower the insertion loss of the filter at f_0.

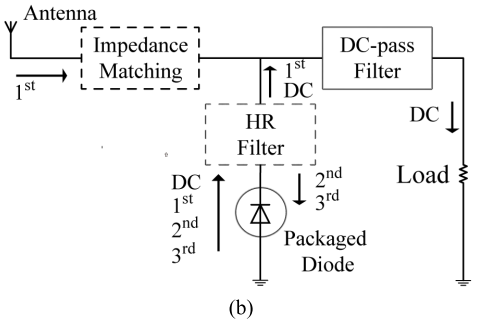

FIGURE 6. Topology and harmonic energy flowing of the proposed single shunt rectifier.

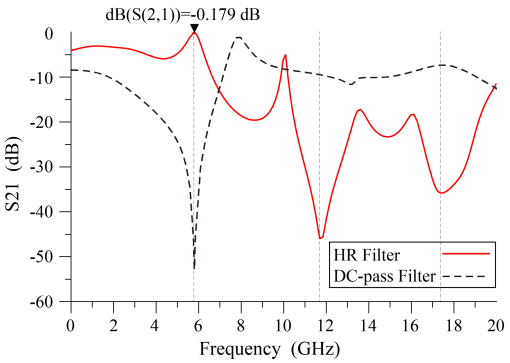

FIGURE 7. Simulated S-parameters of the optimized filters of the rectifier.

Diode model BAT15-03W is chosen as the operating diode and its optimal impedance at 5.8 GHz and 1300 Ohm load is 22.283 − j*69.368 according to Table 2. Rogers AD255C substrate is used in this design. Next, the HR filter consisting of two open ring stubs has been designed and optimized. The input port of the HR filter is set 50 Ohm and output port is set to the obtained optimal impedance of the diode. As shown in Fig. 7, the insertion loss of the optimized HR filter at fundamental frequency is 0.179 dB while providing better than 35 dB rejection at both 2nd and 3rd harmonic frequencies. Then the DC-pass filter is designed and optimized. The input port of the DC-pass filter is set 50 Ohm and output is set to the value of the DC load. The simulated S_{21} data of the optimized DC-pass filter is shown in Fig. 7. In the fundamental frequency, the filter provides better than 55 dB rejection (It should be noted that in the

global simulation, the DC-pass filter is considered shorted at DC). An impedance matching is utilized to match the non-ideal DC-pass branch and the antenna transition design. Global optimization has been utilized to create a more reliable design. The distributed components bring a sum of 0.4 dB insertion lost in the simulation. The layout of the optimized rectifier is shown in Fig. 8(a) indicating the main components.

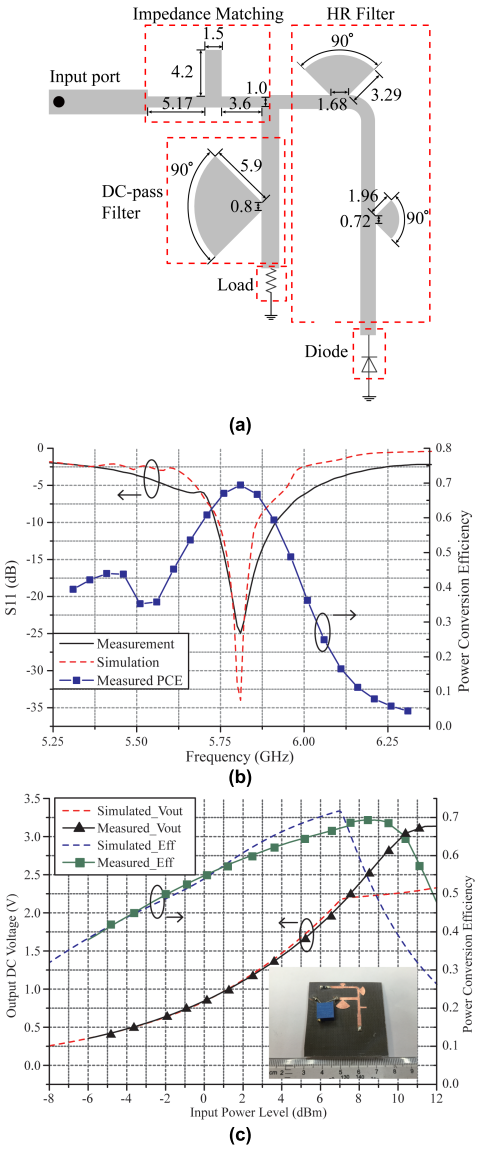

FIGURE 8. (a) Layout of the optimized rectifier; units: mm, (b) S_{11} comparison between the simulation and measurement and measured PCE versus frequencies with input power of 8.2 dBm, (c) V_{out} and PCE comparison between simulation and measurement.

The optimized design has been fabricated and measured. In the measurement, a SMA connector is soldered at the input port. The total size of the rectifier prototype does not exceed $0.77\lambda_0$*$0.77\lambda_0$. Keysight N5247A network analyzer is utilized for measuring the S_{11} performance and the E8257D RF source acts as the power input.

The PCE of the rectifier *Eff* is calculated as follow

$$Eff = V_{out}^2/(Load * P_{in}) \quad (1)$$

where Load denotes the optimal 1300 Ohm DC load also found in the measurement. The measured PCE (P_{in} = 8.2 dBm), simulated and measured S_{11} of the rectifier versus frequencies are plotted in Fig. 8(b). The fabricated rectifier operates optimally at 5.81 GHz with an input return loss of 25.1 dB. The PCE of the rectifier stays beyond 50% at 5.8 GHz ISM band. Good matching performance demonstrates the effectiveness of the optimizing method.

Fig. 8(c) shows the comparison between simulated and measured DC voltages V_{out} and PCE of the rectifier versus Pin at 5.81 GHz. The optimal PCE reaches 69.4 % at 8.2 dBm input power. PCE remains higher than 40% within an input power ranging from −5.5 to 12.5 dBm. The measured V_{out} and PCE curves fit well with the simulated ones further confirming the accuracy of the proposed method when input power level is lower than 7 dBm. When the input power level exceeds 7 dBm, the peak reverse diode voltage reaches B_v and the nonlinear diode model provided by ADS turns into a saturating state. The inverse current of the diode has a sudden increment and V_{out} stops rising, resulting in an inflection point for PCE curve in the ADS simulation. However, the optimal PCE is achieved when the inverse diode voltage reaches B_v in the measurement. V_{out} keeps on rising when the peak inverse diode voltage exceeds B_v, but with a smaller increasing rate, and the PCE starts to decrease due to larger power consumption in R_s instead of a sudden drop. Similar phenomena can be observed in the measured results reported in [12]. Compared with the verifying design in [37], the operating frequency of this prototype is further tuned to fit with the operating frequency of the antenna.

III. ANTENNA DESIGN FOR DEMONSTRATION

As discussed in Section I, the antenna element should be a directional one. For demonstration, a classical circular patch antenna is chosen. To enhance the radiation efficiency and the operating bandwidth, an air substrate is introduced between the patch and the ground plane [24]. The thickness of the patch substrate is thin when compared with the thickness of the air substrate and the size of the supporters are kept small. Hence, the loss in the conventional substrate is minimized.

Fig. 9 illustrates the main antenna design parameters. S_r is the radius of the patch, Ha is the thickness of the air substrate, L_s is the width of the cubic supporters, D_r is the shortest distance from the center of the patch to the edge of the ground plane, D_f defines the location of the feed, while L_g denotes the length of the ground plane. To minimize the insertion loss due to the discontinuity from the coaxial feed to the microstrip rectifier, a coax-to-MS line transition based on [23] is introduced. For flexible impedance tuning, an open stub with length of D_h is introduced at the left side of the feed.

EM simulation has been carried out in HFSS 15.0. Arlon DiClad 880 substrate (h = 0.25 mm, ε_r = 2.2) is chosen for the patch substrate. The characteristic impedance of the MS line is 50 Ohm and the length is set to $5\lambda/4$ at 5.8 GHz to prevent the input impedance from changing when replacing the line with the rectifier for forming the rectenna.

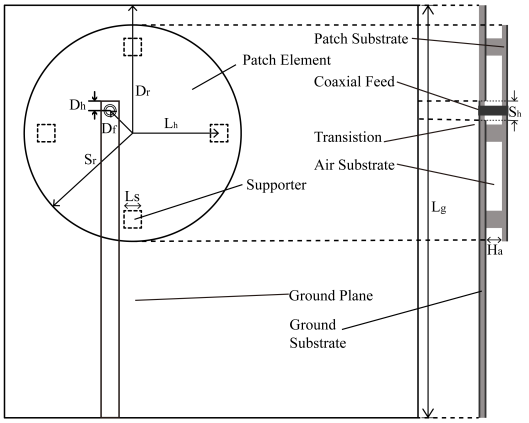

FIGURE 9. Geometry of the high-efficiency patch antenna.

TABLE 4. Optimized parameters of antenna element.

Parameter	Value (mm)	Parameter	Value (mm)
S_r	12.75	D_r	18
L_g	59	H_a	1.8
D_f	3.1	L_h	10
S_h	1.4	L_s	2
D_h	0.41		

It is not necessary to place the patch in the center of the ground plane. But to guarantee a high front-to-back ratio (at least 20 dB), the relationship between S_r and D_r should satisfy

$$D_r > 1.3S_r \tag{2}$$

The antenna is designed following these steps:

1) Set the initial H_a, calculate the effective dielectric constant and thickness of the combined substrate according to [21].

2) Calculate the initial S_r and D_f for the TM_{11} mode of the patch at the target frequency.

3) Replace the feed with the transition, retune S_r to the given frequency, and then tune D_f and D_h to optimize the matching.

The optimized values of the key parameters are provided in Table 4. The antenna design is fabricated and measured to confirm its performance. Satimo system and Keysight N5247A network analyzer have been utilized in the measurements. The antenna resonates at 5.81 GHz in measurement with $S_{11} = -26$ dB as presented is Fig. 10(a). Small discrepancy in resonance frequency between simulation and measurement is attributed to the fabrication error. S_{11} parameter remains below -10 dB from 5.68 GHz to 6.02 GHz covering the ISM band around 5.8 GHz. Thanks to the introduction of the air substrate, high total efficiency is achieved which exceeds 90% from 5.65 GHz to 5.92 GHz. The gain also remains higher than 8 dBi from 5.62 GHz to 5.95 GHz with a peak of 8.4 dBi at 5.81 GHz, as shown in Fig. 10(b). The simulated and measured radiation patterns at 5.81 GHz are depicted in Fig. 10(c). Discrepancy between measured and calculated patterns in 240 to 330 degree sector is due to

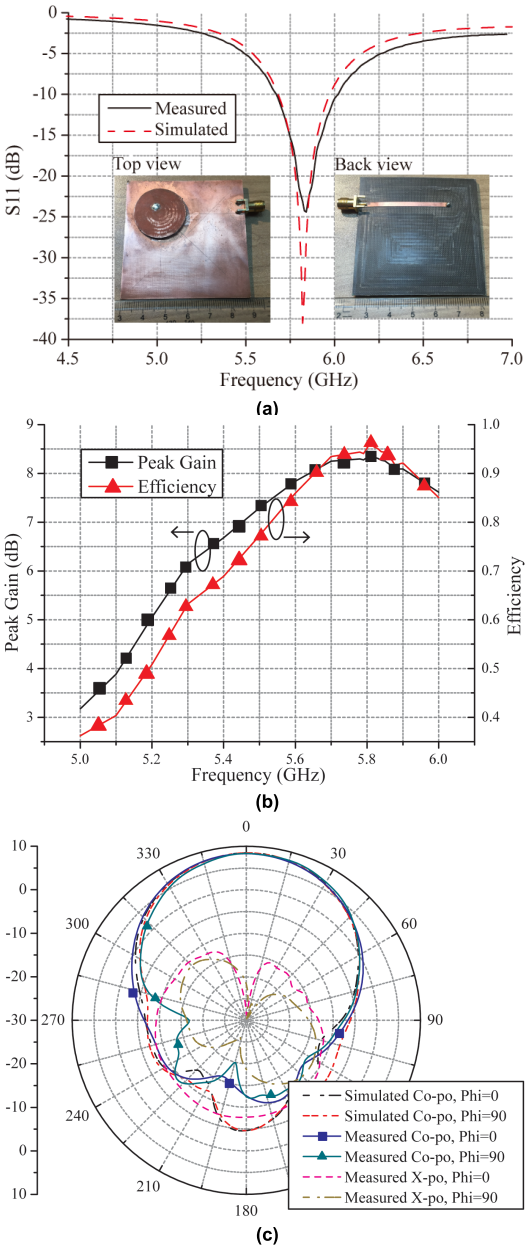

FIGURE 10. Antenna performance (a) S11 performance and view of the prototype, (b) measured peak gain and total efficiency, (c) measured and radiation patterns at 5.81 GHz.

the SMA connector being fixed at the edge of ground plane in measurements and also the cable effect.

IV. RECTENNA FABRICATION AND MEASUREMENT

With the optimized rectifier and antenna, the rectenna is readily formed. The feeding microstrip line of the antenna element in Section III is replaced by the rectifier. To minimize the impedance mismatch between the rectifier and the antenna, the input impedance of the antenna is measured and replaces the 50 Ohm source impedance *An_zin* in Fig. 2. The optimal impedance of the diode is again obtained and the matching component of the rectifier has been tuned to

optimize the performance. Finally, the rectenna prototype has been produced and measured.

Using the measuring method reported in [24] and [26], the proposed rectenna performance has been evaluated at 5.81 GHz in an anechoic chamber. The RF power is now generated by the Keysight E8257D power source. The signal is amplified and delivered to the power meter and to a standard horn antenna. The standard horn antenna with 11.6 dB directional gain at 5.81 GHz acts as a transmitting antenna and a power meter is utilized to monitor the output RF power level.

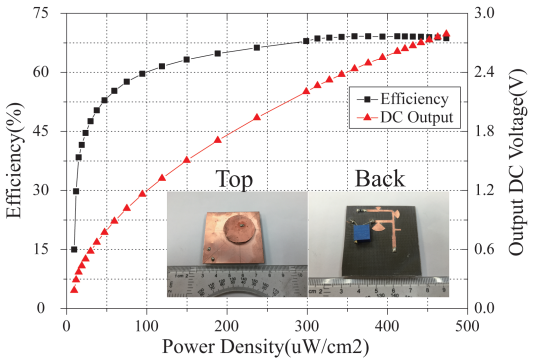

FIGURE 11. Total PCE and output DC voltage versus input power density and the fabricated prototype at 5.81 GHz.

The total size of the prototype does not exceed $0.91\lambda_0 * 0.96\lambda_0$. The measured PCE and output DC voltages versus the incident power density and the view of the prototype are shown in Fig. 11. The total efficiency of the rectenna reaches an optimal value of 69.2% with 412 μW/cm^2 incident power density. The total efficiency remains higher than 60% when incident power density P_d exceeds 95 μW/cm^2. The proposed design is able to operate efficiently at lower input power levels than the works in [19]–[26].

V. CONCLUSION

To precisely design the matching and filtering component in the rectifier, a novel rectifier optimization method is proposed in this paper. With given spice model of the diode, the operating frequency and DC load value, the proposed method accurately obtains the input impedance of the diode with its optimal operating condition. The convergence rate of the proposed method is higher and the needed iteration steps are lower than the automatic optimization tools provided in Advance Design System (ADS). To verify the effectiveness of this method, a compact single-shunt rectifier is designed. The filter rejecting 2nd and 3rd order harmonic energy is optimized to have minimized insertion loss at basic frequency with the diode impedance obtained by the method. The rectifier is fabricated and measured. The measured results fit reasonably well with the simulation. Next, a directional patch antenna with high radiation efficiency is designed. Finally, an integrated rectenna is fabricated and measured. The dimensions of the rectenna are relatively small taking into account its high efficiency at lower incident power density. Such a performance means that in the environment with limited power density, the transmitter can be placed at a longer distance in RF energy transfer application and power more wireless sensor nodes simultaneously.

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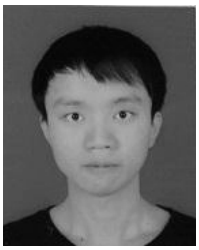

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