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A D-Band Amplifier in 65 nm Bulk CMOS for Short-Distance Data Center Communication

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ABSTRACT A novel pole-tuning technique with T-type network for interstage bandwidth extension is proposed in this paper. By exploiting the proposed technique in interstage of amplifiers, the transfer function of each stage exhibits two dominant poles, achieving a flat gain–frequency response over an ultrawide bandwidth. For verification, a four-stage amplifier based on the pole-tuning technique with T-type network has been designed and implemented in a 65-nm bulk CMOS technology. The fabricated prototype achieves a peak gain of 9.5 dB at 122 GHz with a 3-dB bandwidth of more than 26 GHz and a fractional bandwidth of larger than 21.3%, while consuming a dc power of 62 mW. At the operating frequency of 125 GHz, the saturation output power and the output $P_{1\,dB}$ are 8.6 and 4.6 dBm, respectively. The chip occupies a small silicon area of 0.27 mm^2 including all testing pads with a core size of only 0.105 mm^2. The proposed amplifier is suitable for short-distance data center communication as one of the key building blocks.

INDEX TERMS CMOS, millimeter-wave (mm-wave), broadband amplifiers, bandwidth extension, T-type network, pole-tuning.

I. INTRODUCTION

In recent years, various CMOS amplifiers operating in the frequency range exceeding 100 GHz [1]–[19], have been successfully demonstrated for extremely high data rate wireless communications, and the achieved data rate is around 10 to 20 Gbps for short distance data center applications [20]–[24]. Containing great spectrum resources from 110 to 170 GHz, D-band spectrum is ideally suitable for short-range and high-speed wireless systems at much lower atmospheric attenuation levels than those encountered in the currently popular 60-GHz band and W-band. In order to achieve data rate communications of tens of Gbps or higher, the high order modulation schemes such as quadrature amplitude modulation (QAM) [20] or quadrature phase-shift keying (QPSK) [21]–[23] are adopted for the advanced wireless systems. However, even though higher modulation scheme can be used, the availability of a wide system bandwidth is the key to obtain huge capacity and data rates. As one of the crucial building blocks of high speed wireless systems, the amplifier must provide an extremely wide bandwidth. Therefore, broadband amplifiers are tremendously desired in these systems.

However, it is very challenging to design the wide-bandwidth amplifier to operate at frequencies beyond 100 GHz using CMOS technology, due to the limitation of the cutoff frequency f_T of the transistors, the significant loss of silicon substrate, and the large parasitic effects, which seriously deteriorate the amplifier performance, especially gain and bandwidth. Various techniques are employed to mitigate these drawbacks. For example, capacitive cross-coupling neutralization technique [3], magnetic-coupled feedback embedded network [4], gain-boosting [5], inter-stage impedance network with T-type [8], and conjugate matching [11], are used for promoting the gain performance. In the literature, there are some bandwidth extension techniques demonstrated for CMOS amplifiers operating over 100 GHz. A D-band amplifier achieves a 3-dB bandwidth of 11 GHz with a peak gain of 13.8 dB

using the dual-frequency interstage matching technique [1]. A 110-180 GHz broadband amplifier with 10 dB small signal gain is developed by the impedance transformation technique [9], but existing a large gain ripple of 9 dB inside band. In [2], [7], [10], [13], [15], and [16], the interstage matching technique based on transmission line (TL) are employed to broaden the bandwidth. They achieve the 3-dB bandwidth of 17 GHz [2], 13 GHz [7], 27 GHz [10], 20.4 GHz [13], 13- GHz [15], and over 20 GHz [16] respectively; however, these amplifiers use a la rge number of TLs, which occupy large silicon area and lead to higher fabrication cost. Besides, transformer is extensively used for the design of wideband amplifiers [17]–[19]. However, the transformer will cause large insertion loss at operating frequencies above 100 GHz due to its inherent low-quality factor in CMOS process. Although the aforementioned bandwidth extension techniques can extend the bandwidth of CMOS amplifiers to some extent, new techniques that can expand extremely the bandwidth and maintain the available gain are still greatly desired.

In this paper, a pole-tuning technique with T-type network for interstage bandwidth extension is proposed and verified experimentally. Amplifiers operating above 100 GHz are typically employed multistage topology to achieve the available gain performance. The resulting multistage interstage match dominates the amplifier's overall gain and bandwidth performance. By exploiting the proposed technique in interstage of amplifiers, the transfer function of each stage exhibits two dominant poles. The 3-dB bandwidth of the amplifier is greatly extended without deteriorating the available gain by tuning the relative locus between two dominant poles. The proposed design technique is demonstrated in a D-band amplifier using 65-nm bulk CMOS technology. The paper is organized as follows. In Section II, The proposed bandwidth extension technique is described in detailed. Section III presents the circuit implementation of the D-band amplifier adopting the proposed technique. The measurement results that verify the design technique are discussed in Section IV. Finally, the paper is concluded in Section V.

II. THE POLE-TUNING TECHNIQUE WITH T-TYPE NETWORK

At low frequencies, a small-signal equivalent circuit model significantly reduces simulation time compared with the physical model which is simulated by the electromagnetic (EM) field simulator, employing analysis based a small-signal equivalent circuit can rapidly optimize the circuit performance including the gain-frequency response. However, at millimeter-wave (mm-wave) frequencies and above, parasitic effects have serious substantial influences on the frequency response; parasitic capacitances, inductances, and resistances must be taken into consideration. These parasitic components will introduce additional poles and zeros. The poles and zeros distributions dominate the amplifier's frequency response [25]. Fig. 1 shows the schematic and simplified small-signal equivalent circuit of a common

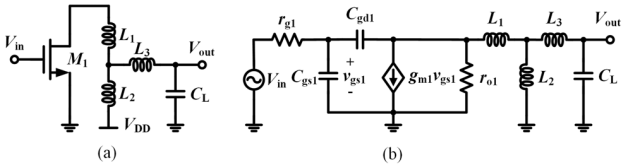

FIGURE 1. (a) Schematic of a CS amplifier with T-type network. (b) Simplified small-signal equivalent circuit of the CS amplifier.

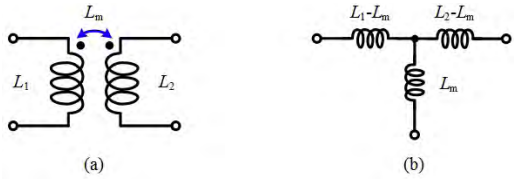

FIGURE 2. (a) Transformer. (b) Simplified equivalent T-type network for transformer.

source (CS) amplifier with T-type network. The T-type network that is composed of a shunt peaking inductor L_2 and the double-series peaking inductors L_1 & L_3, can serve as the function of a transformer, as shown in Fig. 2. Ignoring the gate resistor r_{g1} and the channel modulation resistor r_{o1}, the gain-frequency response of the CS amplifier can be calculated approximately as

$$A_V(s) = \frac{V_{out}(s)}{v_{in}(s)} = \frac{sL_2(g_m - sC_{gd1})}{s^5k_1 - s^4k_2 + s^3k_3 - s^2k_4 - 1} \quad (1)$$

Where

$$k_1 = C_{gd1}^2C_L(L_1L_2 + L_2L_3 + L_1L_3) \quad (2)$$
$$k_2 = C_{gd1}C_L(1 + g_m)(L_1L_2 + L_2L_3 + L_1L_3) \quad (3)$$
$$k_3 = C_{gd1}^2C_L(L_1L_2 + L_2L_3)/L_3 \quad (4)$$
$$k_4 = C_{gd1}(1 + g_m)(L_1L_2 + L_2L_3)/L_3 - C_L(L_2 + L_3) \quad (5)$$

Where g_{m1} and C_{gd1} are the transconductance and gate-to- drain parasitic capacitance of transistor M_1, respectively. According to (1), it can estimate that the CS amplifier may have five poles and two zeros; however, the main poles that dominate the gain-frequency response are very hard to be numerically solved because of the existence of complicated high-order polynomials in the equation. Therefore, the analytical method based-equation is too complicated to reveal the poles and zeros behavior in the frequency response. Instead, the pole-zero distribution plot of transfer function [25], [26] is employed to graphically analyze the effects on frequency response of the amplifier due to the changing of the pole positions.

The poles and zeros of the CS amplifier with T-type network are plotted in Fig. 3. Note that the poles and zeros far away from the imaginary axis are ignored because the frequency response is determined mainly by the poles close to the imaginary axis [25]. The effects of p_3 (p_4) and z_2 (z_3) on the CS amplifier's frequency response cancel out each other because their positions very close. Two pairs of complex conjugate poles p_1 & p_2 and p_5 & p_6 are introduced by the shunt

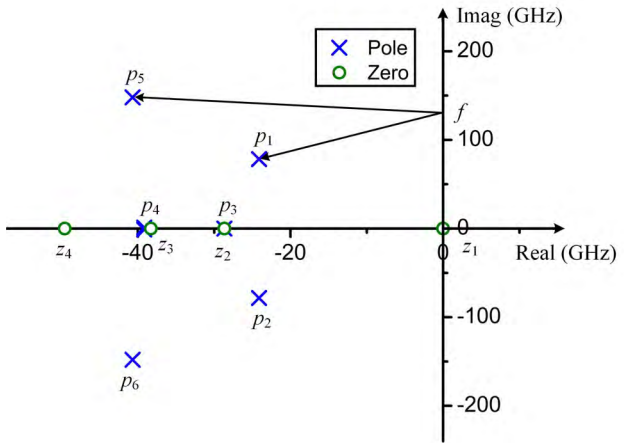

FIGURE 3. Pole-zero plot for the CS amplifier with T-type network.

inductor L_2 and double-series inductor L_1 & L_3. According to the geometric evaluation of the Fourier transform from the pole-zero plot [25], the effects of the poles p_1 and p_5 on the CS amplifier's frequency response are analyzed. For low frequencies, the length of the vector for the pole p_1 close to the imaginary axis is more sensitive to changes in frequency than that of the pole p_5 far from the imaginary axis. Hence, the frequency response is influenced mostly by the pole p_1. Specifically, the length of that pole vector has a minimum at the position of $f = \text{Im}[p_1]$, and a magnitude peak value (peak 1) of the frequency response can be estimated in the vicinity of that frequency [25]. As the frequency increases, the second magnitude peak value (peak 2) of the frequency response will appear at the position of $f = \text{Im}[p_5]$, where the pole vector of p_5 reaches its minimum [25]. In order to gain deeper physical insight into the influences on frequency response from the poles p_1 and p_5, the gain-frequency response of the amplifier is simulated with S-parameter simulation, as shown in Fig. 4. The location of the peak-gain point can be reflected by the ones of the pole. By tuning the relative positions between p_1 and p_5, the bandwidth of the CS amplifier with T-type network will be extended [25], [30]–[32]. Next, the effects on frequency responses from the T-type network including the inductors L_1, L_2, and L_3 are further investigated.

The shunt-peaking inductor L_2 delays the current flow to the inductor itself branch. The result leads to more initial charging current to the load capacitor C_L and reduces the rise time [27]–[29], which can extend the 3-dB bandwidth. Fig. 5 shows the locus of p_1 and p_5 as L_2 increases from 20 to 100 pH, while Fig. 6 demonstrates the gain-frequency response of the CS amplifier with T-type network under various L_2. As can be observed in Fig. 5 and Fig. 6, the pole p_1 (p_2) moves away from the imaginary axis and shifts to lower frequencies. As a result, the first dominant pole p_1 (p_2) of the frequency response shifts to the lower frequencies, and the magnitude of ones also declined since the minimum value of pole vector for p_1 (p_2) is increased. However, the pole p_5 (p_6) moves toward the imaginary axis and slowly shifts to lower frequencies. This results the minimum value of pole vector for p_5 (p_6) is decreased, which enhances the magnitude of the frequency response at the second dominant pole. By tuning the shunt-peaking inductor L_2, the first dominant

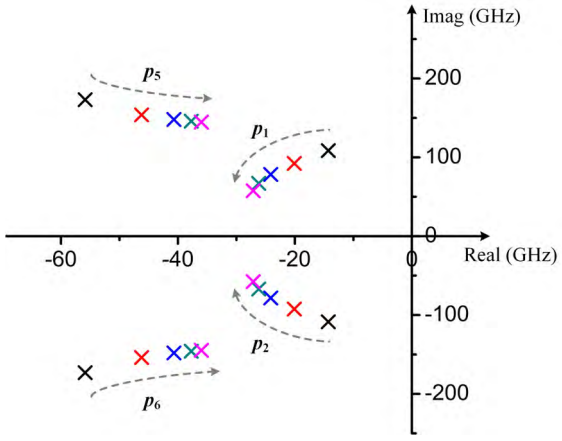

FIGURE 5. Locus of poles p_1 and p_5 when the inductance of inductor L_2 increases from 20 to 100 pH, dashed line with arrow indicates the moving direction as L_2 increases.

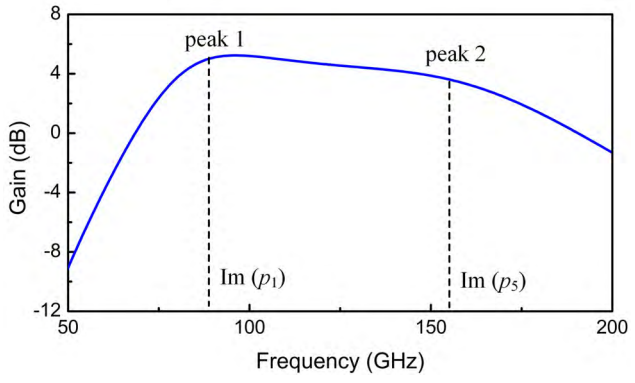

FIGURE 4. Gain-frequency response for the CS amplifier with T-type network.

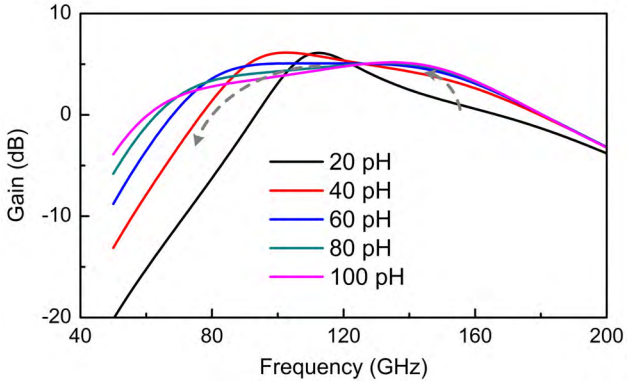

FIGURE 6. Gain-frequency response of the CS amplifier when the inductance of inductor L_2 increases from 20 to 100 pH, dashed line with arrow indicates the moving direction as L_2 increases.

pole, p_1, is suppressed, while the second dominant pole, p_5, is enhanced. Then, the CS amplifier can achieve a flat gain-frequency response over a broadband.

The series inductor L_1 is directly connected to the drain of the CS amplifier to isolate the load capacitor and the output capacitor of the CS amplifier. This resulting the initial current toward the rest of the network is delayed, so that the drain charge rise time is improved [27], [28]. Here, the increase in delay time is used to trade up to the increase in bandwidth. Fig. 7 shows the locus of p_1 and p_5 as L_1 increases from 20 to 100 pH, while Fig. 8 demonstrates the gain-frequency response of the CS amplifier with T-type network under various L_1. As L_1 increases, the second dominant pole p_5 (p_6) is more sensitive than the first ones, as indicated in Fig. 7. The pole p_5 (p_6) moves quickly closer to the imaginary axis and shifts to lower frequencies. The pole p_1 (p_2) also moves toward the imaginary axis, but shifts to lower frequencies slowly. This results two peak-gains are boosted because their vector lengths are reduced, as demonstrated in Fig. 8.

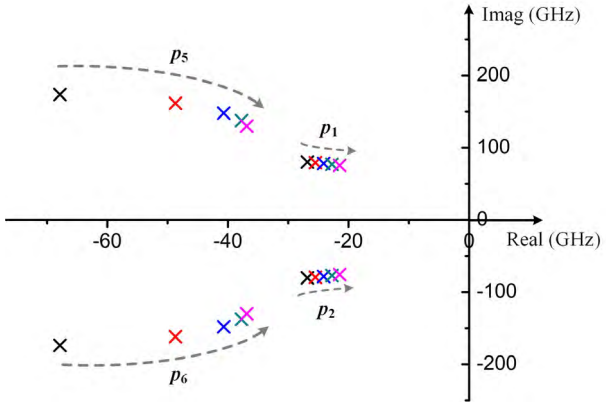

FIGURE 7. Locus of poles p_1 and p_5 when the inductance of inductor L_1 increases from 20 to 100 pH, dashed line with arrow indicates the moving direction as L_1 increases.

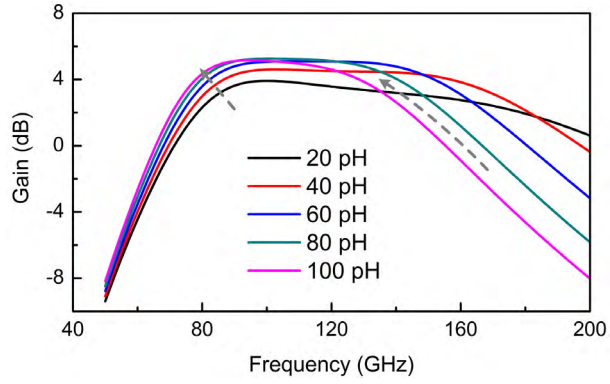

FIGURE 8. Gain-frequency response of the CS amplifier when the inductance of inductor L_1 increases from 20 to 100 pH, dashed line with arrow indicates the moving direction as L_1 increases.

The other series inductor L_3 is connected to the load capacitor of the CS amplifier to further isolate the load capacitor and the output capacitor of the CS amplifier. After the amplifier's drain voltage rises significantly for a period of time, the initial current begins to flow through L_3 to the load capacitor. Note that in order not to make the delay time too long and maintain a reasonable bandwidth extension at the same time, the inductance L_3 should not be too large. Fig. 9 shows the locus of p_1 and p_5 as L_3 increases from 10 to 50 pH, while Fig. 10 demonstrates the gain-frequency response of the CS amplifier under various L_3. As illustrated in Fig. 9, the locus of the second dominant pole p_5 (p_6) changes significantly as the inductance L_3 increases. The speed at which the pole p_5 (p_6) moves toward the imaginary axis is much larger than the speed at which the po le p_1 (p_2) moves away from the imaginary axis. As a result, the second peak-gain point is enhanced significantly while the first peak-gain point is restrained.

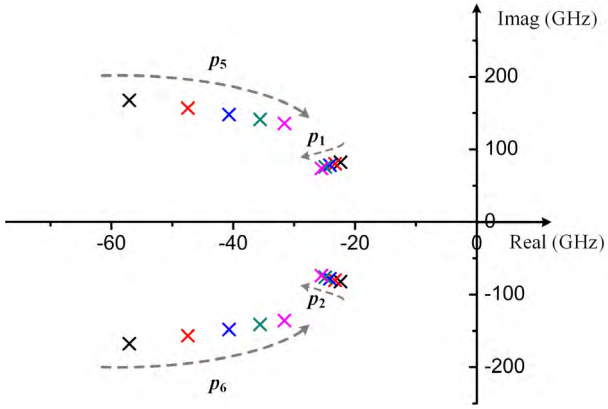

FIGURE 9. Locus of poles p_1 and p_5 when the inductance of inductor L_3 increases from 10 to 50 pH, dashed line with arrow indicates the moving direction as L_3 increases.

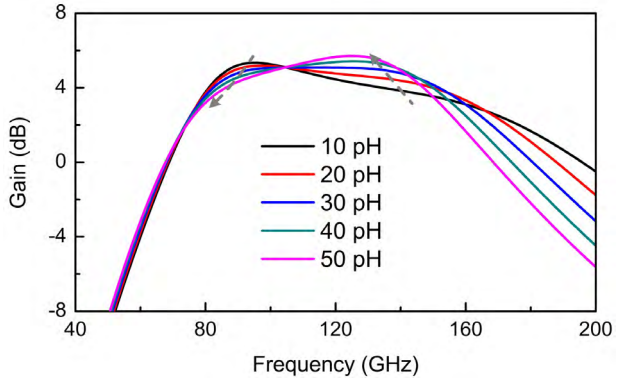

FIGURE 10. Gain-frequency response of the CS amplifier when the inductance of inductor L_3 increases from 10 to 50 pH, dashed line with arrow indicates the moving direction as L_3 increases.

In summary, the proposed T-type network has the following contributions to extend bandwidth of the amplifier. First, two dominant poles p_1 (p_2) & p_5 (p_6) are always on the left-half plane, which improves the stability of the amplifier. Second, the pole p_5 (p_6) always moves toward

the imaginary axis, and the minimum value of pole vector for p_5 (p_6) is reduced, which enhances the magnitude of the frequency response at the second dominant pole. Third, the direction of movement of p_1 (p_2) can be controlled, which gets an additional degree of freedom to tune the overall gain-frequency response of the amplifier. Therefore, by designing the on-chip T-type network properly at mm-wave frequencies, a flat gain-frequency response can be achieved over a wide-bandwidth.

III. WIDEBAND AMPLIFER IMPLEMENTATION

A four-stage wideband amplifier using pole-tuning technique with T-type network has been designed in a 65-nm bulk CMOS process, as shown in Fig. 11. In the design, the finger width of 1 μm and minimum gate length of 60 nm are chosen for all nMOS transistors to obtain the optimum tradeoff between the lowest ohmic-loss due to gate-resistance and the maximum attainable cut-off frequency f_T of nMOS transistor. The first stage uses cascode topology to achieve high reverse isolation, while the other stages use common source structure to provide available gain and output power. The input stage adopts L-type matching network to provide wideband input matching and the last stage with shunt-peaking inductor works as a wideband output buffer [33]. The parasitic capacitances of the RF testing pads are considered in the design of the matching network.

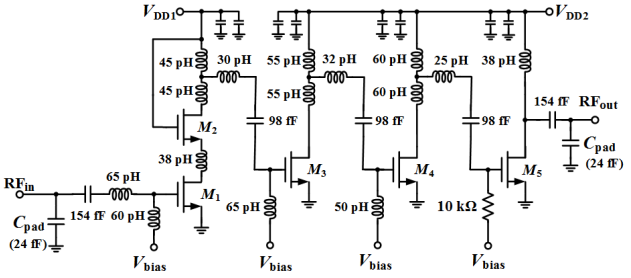

FIGURE 11. Schematic of the broadband amplifier with T-type network.

As can be seen in Fig. 11, the pole-tuning technique with T-type network for intrastage bandwidth extension are implemented in the first three stages. As aforementioned, the T-type network has the same equivalent circuit model as the transformer. The T-type network should also be implemented through transformer. Thus, the transformer can serve as the function of a T-type network, and provide good interstage DC isolation. However, the transformer will cause large insertion loss at mm-wave frequencies due to its low-quality factor in CMOS process. As a result, the gain of the amplifier is seriously deteriorated. Instead, the T-type network is implemented using arc-shaped TLs with defected ground structure for a high-quality factor and a compact footprint. As illustrated in Fig. 12, the main signal lines are realized by the sub top-metal M_8 with thickness of 3.3 μm while the ground plane is designed by the bottom metal M_1 with thickness

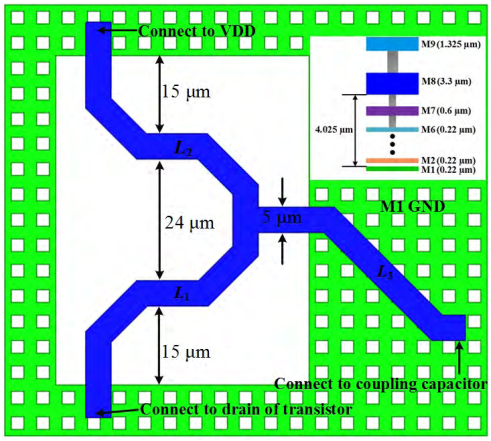

FIGURE 12. Layout of the implemented T-type network.

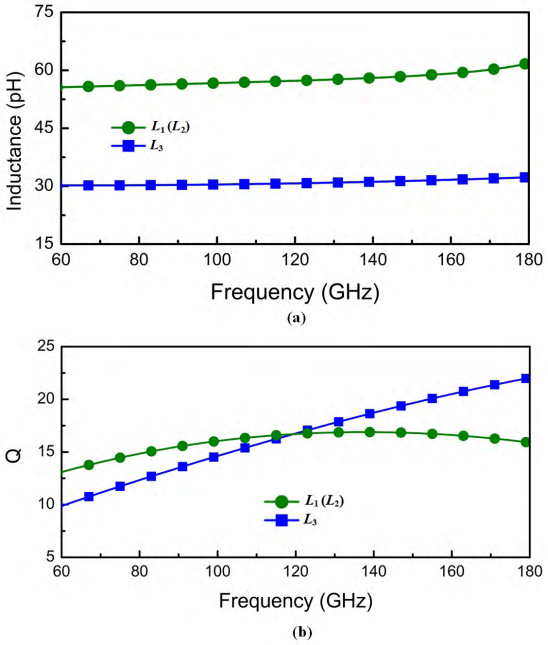

FIGURE 13. EM simulation results of the T-type network. (a) Inductance. (b) Quality factors.

of 0.22 μm. Fig. 13 shows the EM simulation results of the effective inductances and quality factors for the inductors L_1, L_2, and L_3. L_1 (L_2) and L_3 are 55 pH and 32 pH, respectively, and the quality factors are above 15 at the operating frequency of 120 GHz. Note that the other two T-type networks can be achieved through fine-tuning the size parameters of the aforementioned structure. In order to reduce mm-wave signals coupling to the silicon substrate so as to cause the extra energy loss, all inductors and interconnections are realized with the top thick metal layers. In this work, the design parameters including all T-type network, inductors, testing pads, interconnections, vias and so on, are optimized using 3-D EM simulator High-Frequency Structure Simulator and circuit co-simulations.

IV. EXPERIMENTAL RESULTS

The proposed wideband amplifier was fabricated using GLOBALFOUNDRIES 65-nm bulk CMOS technology. The nMOS transistor for low-power applications achieves a cutoff frequency f_T around 200 GHz and a maximum oscillation frequency f_{MAX} around 220 GHz, respectively. The thickness, dielectric constant and resistivity of the substrate are 737 μm, 11.9 and 1.5 $\Omega \cdot$ cm, respectively. Fig. 14 shows the die micrograph of the broadband CMOS amplifier. The whole chip occupies a silicon area of 0.27 mm^2 including all testing pads with a small core size of only 0.105 mm^2. At a gate bias condition of 0.9-V (V_{bias}), the CMOS amplifier draws a total DC current of 45 mA from both 2-V (V_{DD1}) and 1.2-V (V_{DD2}) supply voltages, which leads to a power consumption of 62 mW.

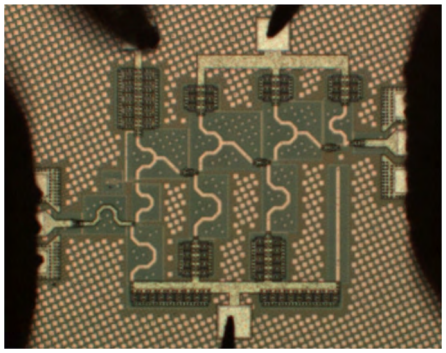

FIGURE 14. Die micrograph of the broadband amplifier.

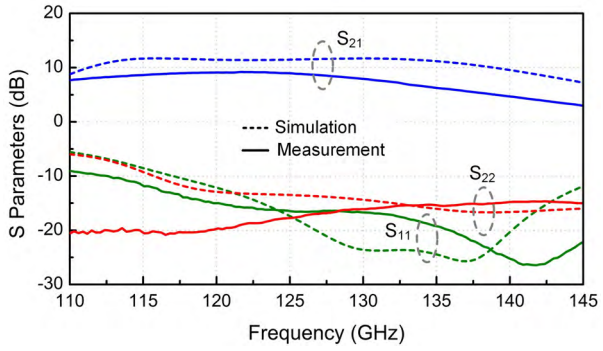

FIGURE 15. Simulated and Measured S-parameters for the amplifier.

On-wafer measurements of S-parameters were performed from 110 to 170 GHz using Cascade Microtech Elite 300 probe station with Cascade 50-μm pitch ground-signal-ground (G-S-G) waveguide probes, Agilent N5247A PNA-X Microwave Network Analyzer, and two 110-170 GHz VDI's frequency extension modules. The system is calibrated using a short-open-load-thru (SOLT) probe-tip calibration technique on a Cascade Impedance Standard Substrate.

The simulated and measured S-parameters of the proposed CMOS amplifier are plotted in Fig. 15. It can be seen that the amplifier exhibits a very flat gain response ($|S_{21}|$) with a peak value of 9.5 dB at 122 GHz. The measured 3-dB gain bandwidth is from 110 GHz to 136 GHz. Note that the measured result indicates that the low corner frequency of the 3-dB gain bandwidth is below 110 GHz, which cannot be captured by measurement because of the limitation of our available testing facilities. Therefore, the 3-dB gain bandwidth of the CMOS amplifier is larger than 26 GHz. Ultra-wideband input matching and output matching are achieved. The measured input return loss ($|S_{11}|$) is better than 10 dB from 111 GHz to beyond 145 GHz, while the measured output return loss ($|S_{22}|$) is higher than 10 dB from 110 GHz to beyond 145 GHz. As illustrated in Fig. 16 (a), the measured reverse isolation is better than 43 dB in the entire 3-dB bandwidth of the amplifier. Fig. 16 (b) presents the measured group delay, which is around 30 ps with a small variation of $\pm$5 ps over the measured frequency band. According to the followed formulas Eq. (6) and (7), the stability factor K and delta Δ calculated from the measured S-parameters are shown in Fig. 17 (a) and (b), respectively. From 110 GHz to 145 GHz, the minimum K of the proposed amplifier is more than 20, and the Δ is smaller than 1, which indicates that the CMOS amplifier is unconditional stable.

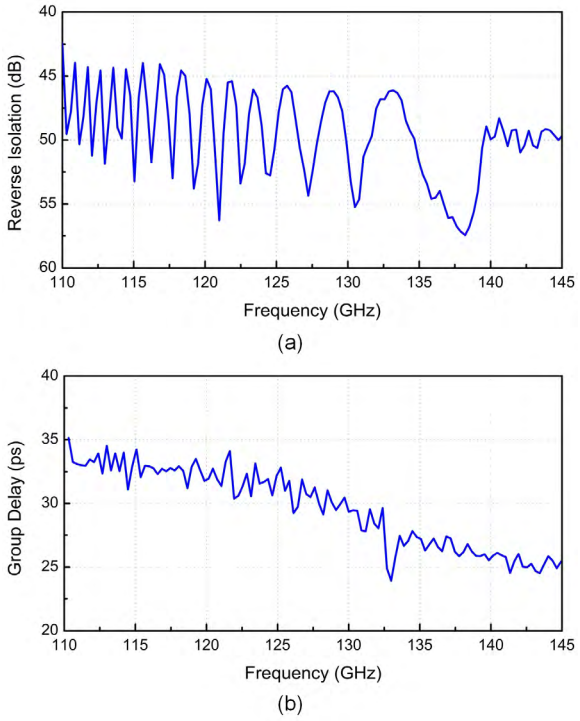

FIGURE 16. Measured reverse isolation and group delay.

$$K = \frac{1 - |S_{11}|^2|S_{22}|^2 + |\Delta|^2}{2|S_{12}| \cdot |S_{21}|} > 1 \quad (6)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (7)$$

Compared with simulated results, the measured 3-dB bandwidth shifts down by $\sim$6 GHz and the measured gain degrades by $\sim$ 3 dB. The discrepancies between measured results and simulated results are mainly due to the existence of

TABLE 1. Performance summary and comparison with recently reported mm-wave CMOS amplifiers.

References	Technology	Topology	f_p* (GHz)	Gain (dB)	BW (GHz)	FBW (%)	OP_{1dB} (dBm)	P_{sat} (dBm)	Peak PAE (%)	P_{DC} (mW)	Area (mm^2)
[1]	65 nm CMOS	6-stage CS	116	13.8	11	9.4	-14	-3	N.A.	40	0.605
[2]	65 nm CMOS	8-stage CS	126	14.4	17	13.4	N.A.	N.A.	N.A.	22.6	1.9
[3]	65 nm CMOS	4-stge CS	109	20.3	17	15.5	12.5	15.2	10.3	N.A.	0.34
[4]	65 nm CMOS	4-stage CS	142	18.5	3.4	2.3	N.A.	N.A.	N.A.	7.9	0.16
[5]	65 nm CMOS	3-stage cascode	190	16.3	4	2.1	N.A.	N.A.	N.A.	51.4	0.46
[7]	40 nm CMOS	9-stage CS	213.5	10.5	13	6.1	-7.2	-3.2	0.75	42.3	0.12
[8]	65 nm CMOS	4-stage cascade	147	7.1	10†	6.8	N.A.	N.A.	N.A.	104	0.35
[9]	65 nm CMOS	4-stage cascade +1-stage CS	170	19	70♀	48.2♀	N.A.	N.A.	N.A.	109	0.37
[10]	65 nm CMOS	3-stage CS	150	8.2	27	18	1.5	6.3	8.4	25.5	0.41
[11]	65 nm CMOS	3-stage cascade	144†	20.6	29♀	20.3♀	5	> 5.7	3.6	102	0.208
[12]	40 nm CMOS	3-stage CS	160	11.6	24	15	1.5	4.1	2.5	42	0.288
[13]	65 nm CMOS	2-stage Cascode + 3-stage CS	118.6	8.13	20.4	17.2	N.A.	N.A.	N.A.	19.8	N.A.
[14]	65 nm CMOS	3-stage CS + 3-stage CG	140	8	10	7.1	-12	-1.8	N.A.	63	N.A.
[15]	40 nm CMOS	6-stage CS	133	16.8	13	9.7	6.8	8.6	7.4	89.1	0.3
[16]	65 nm CMOS	4-stage CS	90	14.8	19†	20.7†	6	10	7.3	86	0.33
[17]	65 nm CMOS	2-stage cascade + 1-stage CS	108.5	10.3	17	15.6	10.1	11.8	10	N.A.	0.204
[18]	65 nm CMOS	3-stage CS	86.4	18.6	4.8	5.5	9.6	11.9	9	N.A.	0.37
[19]	65 nm CMOS	2-stage cascade + 1-stage CS	109	12.2	16	14.6	9.6	12.9	8.2	N.A.	0.32
[26]	65 nm CMOS	5-stage cascade	69	13.3	27.5	35.6	-2	0	N.A.	12	0.24
[29]	130 nm SiGe	3-stage CS	95†	20†	16†	16.8†	N.A.	16.3	14.1	N.A.	0.64
[33]	65 nm CMOS	3-stage cascade	104	16.7	21.5	21.6	N.A.	N.A.	N.A.	48.6	0.29
This Work	**65 nm CMOS**	**1-stage cascade + 3-stage CS**	**122**	**9.5**	**> 26**	**> 21.3**	**4.6#**	**8.6#**	**11.5#**	**62**	**0.27**

FBW=BW/f_c, where f_c is the center frequency of the 3-dB bandwidth;
†estimated value from figures;
*peak-gain frequency;
♀10-dB bandwidth;
#simulated.

the randomized dummy metallization, which is added to pass design rule check (DRC) by the foundry during fabrication. These dummy metallization introduced additional parasitic capacitance, which deteriorated the real value and Q factor of passive components, including the inductors, capacitors, transmission lines, and so on. In addition, the limited accuracy of the active device's model operating at D-band that foundry provided is also a probable reason.

The power-handling capability P_{1dB} is not measured at D-band due to power limitation of our available testing facilities. The large-signal characterization and P_{1dB} were simulated at 125 GHz for the CMOS amplifier, as illustrated in Fig. 18. The proposed amplifier achieves a saturation output power of 8.6 dBm with 11.5% PAE, while the output P_{1dB} is 4.6 dBm.

Table I summaries the performance of the proposed CMOS amplifier and comparison with recently reported amplifiers. The bandwidth of the proposed amplifier is significantly extended by the proposed pole-tuning technique with T-type network. Compared with the recently reported CMOS

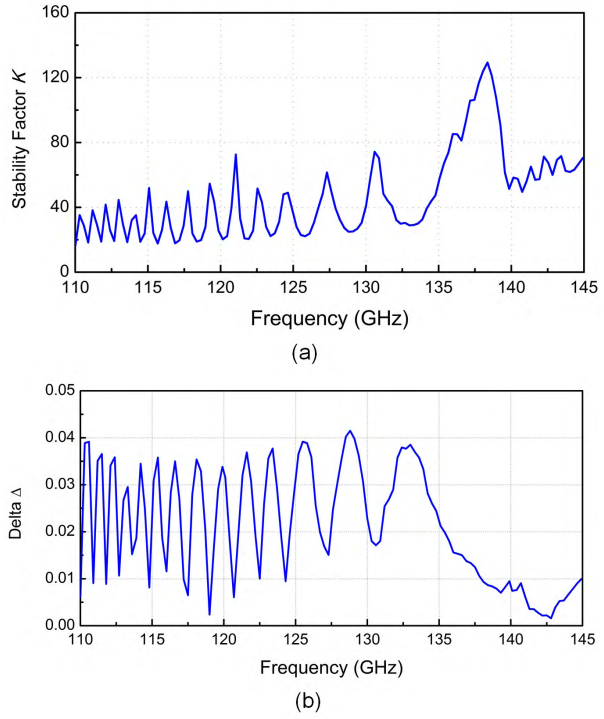

FIGURE 17. Measured stability factor K and delta Δ.

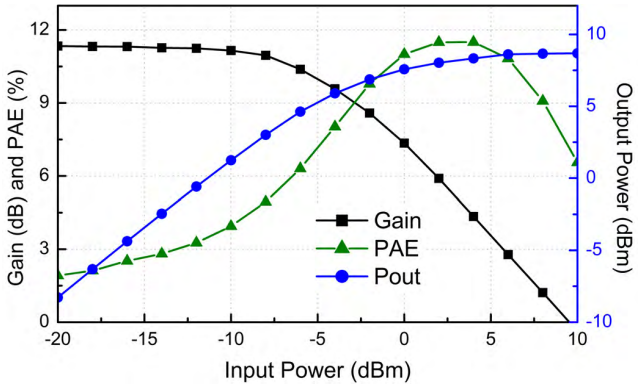

FIGURE 18. The simulated large-signal gain, P_{1dB}, and PAE of the CMOS amplifier.

amplifiers operating over 100 GHz, the proposed amplifier exhibits competitive performance of bandwidth and FBW, as well as PAE.

V. CONCLUSION

A pole-tuning technique with T-type Network has been proposed and successfully applied to the implementation of a D-band amplifier in 65-nm CMOS bulk technology. By exploiting the proposed technique in interstage of amplifiers, the transfer function of each stage exhibits two dominant poles, achieving a flat gain-frequency response over an ultrawide bandwidth. The amplifier exhibits a peak gain of 9.5 dB, and a 3-dB bandwidth of more than 26 GHz with low power consumption of 62 mW. At 125 GHz, the saturation output power is 8.6 dBm with peak PAE 11.5%, while the output P_{1dB} is 4.6 dBm. The proposed intrastage bandwidth extension technique is expected to be a useful method for wideband amplifier designs, particularly for operating frequency over 100 GHz.

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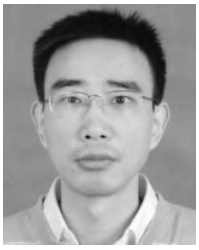

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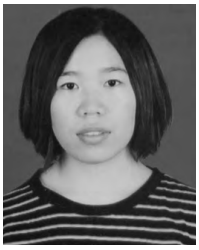

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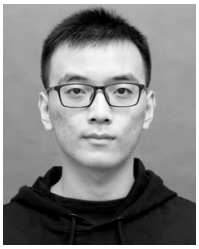

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