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Negative Capacitance Transistor to Address the Fundamental Limitations in Technology Scaling: Processor Performance

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ABSTRACT Negative capacitance field-effect transistor (NCFET) addresses one of the key fundamental limits in technology scaling, akin to the non-scalable Boltzmann factor, by offering a sub-threshold swing below 60 mV/decade. In this paper, we investigate how the NCFET technology can open the doors not only for the continuation of Moore's law, which is approaching its end, but also for reviving Dennard's scaling, which stopped more than a decade ago. We study NCFET for the 7-nm FinFET technology node, from physics to processors and demonstrate that prior trends in processor design with respect to voltage and frequency can be revived with the NCFET technology. Our work focuses on answering the following three questions towards drawing the impact of NCFET technology on computing efficiency: In how far NCFET technology will enable processors: 1) to operate at higher frequencies without increasing voltage; 2) to operate at higher frequencies without increasing power density, which is substantial, because maintaining on-chip power densities under tight constraints due to limited cooling capabilities is inevitable; and 3) to operate at lower voltages, while still fulfilling performance requirements, which is substantial for the emerging Internet of Things, in which available power budgets for such devices are typically very restricted.

INDEX TERMS Negative capacitance, emerging technology, sub-threshold swing, performance, power, Dennard's scaling.

I. INTRODUCTION

In the early 2000s, when the complementary metal-oxide semiconductor (CMOS) technology entered the so-called nano era, in which the feature sizes of transistors became below 90 nm, the prior trend of voltage scaling started to falter. Since then, the well-known Dennard's scaling [2], which states that both the dimensions of transistors and the operating voltage should be scaled by the same factor to maintain a constant electric field, had stopped. As a matter of fact, the operating voltage of processors (V_{DD}) remained almost constant in the last decade, whereas the transistor's dimensions steadily kept scaling down following Moore's law [3]. Consequently, unsustainable heat, that inevitably generated due to excessive on-chip power densities, became a crucial obstacle for technology scaling [4]. To overcome this challenge, the maximum frequency of processors stopped increasing with every new generation, in order to limit the speed of moving electrons inside the chip and, hence, restrict their ability to generate heat [5]. Since then, processor manufacturers have moved from a single-core design to multi-core design, to keep providing processors with better performance with every new generation, despite the enforced limit on the maximum operating frequency. Although this enabled the continuation of Moore's law in the last decade, the latter will unavoidably stop in the near feature as the transistor scaling is approaching its end. This is expected to happen when the dimensions of transistors reach 2-3 nm, where quantum effects become predominant [5]. Moving to 3D architectures, in which several layers are stacked on top of each other, may allow processors to keep moving along the Moore's performance curve, but removing the ever-increasing heat generated by chips is challenging, and this may limit their deployment

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to memory chips [5] as they involve less power densities than processing units. Fig. 1 demonstrates that around 2005, the frequency increase in processors was discontinued to avoid unsustainable power densities, despite the continuous increase in the number of transistors.

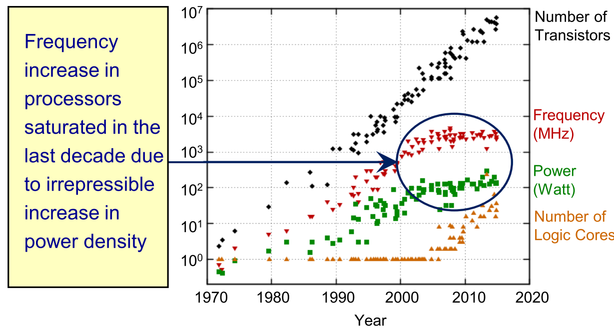

FIGURE 1. The trends in microprocessors based on gathered experimental data. The data and plotting script obtained from [1].

In summary, the prior trends of voltage and frequency scaling stopped since more than a decade in which neither the speed of processors nor the operating voltage has improved. In addition, the current trend of performance improvement in processors may also stop soon, as increasing performance through integrating more CPU cores with every new generation, becomes difficult, if not impossible, because the process scaling is approaching its end. Therefore, besides the discontinuation of Dennard's scaling, Moore's law may also die in the fear future [6].

A. THE FUNDAMENTAL LIMITATION BEHIND VOLTAGE SCALING

The speed of a processor is essentially governed by the drive current (ON current, I_{ON}) that its constituent transistors can provide. I_{ON} of a transistor is proportional to $(V_{DD} - V_T)$, where V_T denotes threshold voltage. To maintain the same level of I_{ON} with V_{DD} scaling, V_T also must be reduced by the same amount. Reducing V_T, however, exponentially increases the leakage current (OFF current, I_{OFF}) of transistor, which in turn raises the stand-by power consumption of a processor. This is primarily because of the non-scalable sub-threshold swing SS of transistor, which determines the change in gate voltage required to cause a decade change in the current as shown in Fig. 2. As a matter of fact, SS is fundamentally limited to 60 mV/decade at room temperature due to the Boltzmann distribution of charge carriers at the source of transistor – often termed as the "Boltzmann tyranny" [7], [8].

This fundamental limit restricts the minimum possible V_T to be 300 mV, because in a good design, the I_{ON}/I_{OFF} ratio should be at least 5 orders of magnitudes. To ensure a reliable operation, safety margins need to be included, so that at the end the V_{DD} reaches around 1.0 V or slightly below. Precisely, this is the main reason behind the discontinuation of V_{DD} scaling, which, in turn, had led to preventing the frequency of processors from increasing to avoid unsustainable power densities and heat as explained earlier.

B. NEGATIVE CAPACITANCE FET (NCFET)

NCFET is an emerging transistor technology, that can surmount the fundamental Boltzmann constraint of 60 mV/decade sub-threshold swing at room temperature, through integration of a ferroelectric layer within the gate stack. The concept of NCFET was first proposed by Salahuddin and Datta [9]. Gradually, it gained popularity due to its remarkable characteristics, such as steep switching, high ON current and excellent short channel immunity, i.e., reduced short channel effects because Drain-Induced Barrier Lowering (DIBL) effect is lower or even negative [9]–[13]. Both theories and experiments have consistently proved its potential at the device level as well as at the circuit level [14]–[19]. In practice, NCFET technology enables the transistor to reach the same ON current, without increasing the OFF current, but at a lower V_{DD}, due to steeper sub-threshold swing (i.e., $SS < 60$ mV/decade) as we demonstrate in Fig. 2. As it can be noticed, due to the steeper SS in NCFET technology, the same I_{ON}, as the conventional FETs at iso-I_{OFF}, can be achieved but at a lower operating voltage.

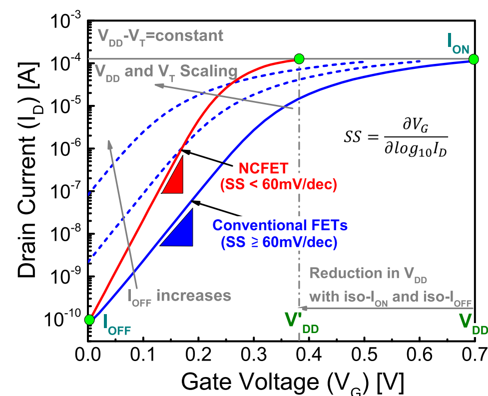

FIGURE 2. Impact of supply voltage (V_{DD}) and threshold voltage (V_T) co-scaling on the transfer characteristics of transistor. The overdrive ($V_{DD} - V_T$) is kept constant to maintain the same ON current. With V_T scaling, OFF current (I_{OFF}) starts to exponentially increase due to non-scalable sub-threshold swing (SS), which restricted V_{DD} scaling in the last decade. On the other hand, the steep SS in NCFET technology effectively mitigates this issue and achieves the same I_{ON}, as the conventional FETs at iso-I_{OFF}, but at a lower operating voltage ($V'_{DD} < V_{DD}$). In this experiment a conventional 7 nm nFinFET is studied as a baseline and then compared to NC-FinFET that has a 4 nm ferroelectric layer.

Limitations in NCFET technology process: like any other emerging technology, NCFET also faced some process-related issues and intrinsic ferroelectric limitations. One of the main process challenges is the integration of ferroelectric material in the gate stack with a high quality interface with the silicon. An inflection point occurred in 2012, after the discovery of ferroelectricity in HfO_2 based materials, which made the NCFET technology compatible with the standard CMOS technology process [20]–[22]. Subsequently, several experimental works have demonstrated NCFETs with HfO_2

based ferroelectrics exhibiting sub-60 mV/decade swing at room temperature [23]–[27]. A recent work has also proposed a method to reduce interface states between ferroelectric and silicon using a nitrided interfacial oxide layer [28].

Importantly, GlobalFoundries has recently integrated a doped HfO_2 ferroelectric layer in their state-of-the-art industrial 14 nm FinFET technology demonstrating for the first time how NCFET-based circuits can be successfully manufactured using the standard current CMOS technology [18]. Therefore, NCFET has recently become one of the few emerging technologies that is compatible with the existing CMOS manufacturing process, which may pave the way for massive production of NCFET. Additionally, there have been several other experimental works on NCFETs with the 2D MoS_2 as the active channel material which can provide additional boost over the Si channel based technology [29]–[32].

The other main limitation that is often projected is the polarization damping of ferroelectric dipoles, due to which dipoles may not respond fast enough to the applied voltage during high frequency switching events [33]–[35]. Therefore, it was questionable that whether the switching frequency of NCFETs can actually match the GHz frequency operation in modern processors. However, this concern has recently been discarded. In their experimental work, Krivokapic *et al.* [18] demonstrated that when NCFET is integrated into 14 nm FinFET technology, ring-oscillator circuits can operate at frequencies similar to those in the original (i.e., baseline) 14 nm technology. Another theoretical study has predicted the intrinsic delay due to polarization damping in NCFET to be very small ($\approx$ 270 fs) in doped HfO_2 ferroelectrics, which can be easily ignored in digital logic applications [36]. This prediction is based on the fact that the actual amount of gate charge to be switched in NCFET is very small (inversion gate charge density in a silicon FET is $\approx 1.6\ \mu C/cm^2$ [36], much smaller than the remnant polarization of the available ferroelectrics which is generally in the range of tens of $\mu C/cm^2$).

C. KEY FOCUS AREAS IN THIS WORK

In this work, we investigate the implications of NCFET technology, at the 7 nm FinFET node, starting from physics all the way up to the processor level, in the following areas:

(1) Reviving the prior trend of frequency increase in processors without increasing power densities. In other words, under the same power density constraint, how much the frequency of processor can be increased due to NCFET? This, in turn, enables the technology to achieve further improvements in performance when scaling, without exacerbating the heat generation problem.

(2) Reviving the prior trend of voltage decrease in processors without decreasing performance. In other words, under the same performance constraint, how much the voltage of processor can be decreased due to NCFET? This, in turn, enables the technology to achieve further improvements in power when scaling, without degrading performance.

(3) Continuation of Moore's law when reaching the fundamental limit of scaling. In other words, how alterations in the NCFET technology (e.g., increasing the thickness of the ferroelectric) may provide further improvements in the processor's performance without the need to scaling down the transistor dimensions.

II. NCFET EFFECTS FROM PHYSICS TO PROCESSOR LEVEL

In the following, we first explain briefly how NCFET technology works and then we describe how their effects at the physical and device levels can be modeled. Afterwards, we discuss the different case studies that our work investigates. Finally, we demonstrate how NCFET-aware cell libraries can be created towards enabling designers to analyze the effects that NCFET technology has on the performance and power of complex circuits like processors.

A. NCFET BASICS

NCFET incorporates a ferroelectric material within the gate stack of transistor (see Fig. 3(a)), which exhibits a

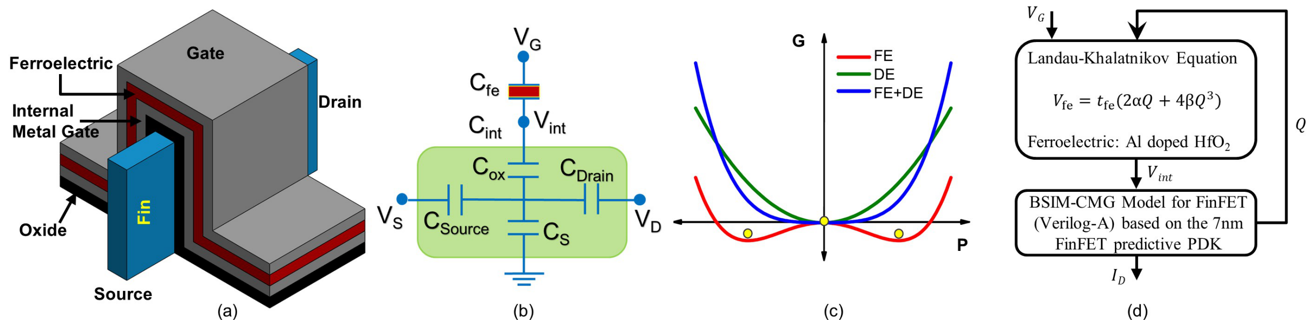

FIGURE 3. (a) Schematic of metal-ferroelectric-metal-insulator-semiconductor (MFMIS) NCFET. Presence of intermediate equipotential metal gate enables the partitioning of the full structure into two circuit components: the ferroelectric capacitor and the baseline FinFET for device modeling purpose. (b) Circuit equivalent of MFMIS type NCFET. Shaded region represent gate capacitance of the internal baseline FinFET. (c) Gibbs free energy profiles at zero external electric field as a function of polarization, for ferroelectric (FE), dielectric (DE) and the combined system (FE+DE). In an isolated ferroelectric, either of the two energy minima are occupied. However, addition of a dielectric in series with the ferroelectric produces an energy profile of the system, with a minimum at $P = 0$, where ferroelectric lies in the negative capacitance state. (d) Modeling flowchart for NC-FinFET. The L-K model of ferroelectric capacitor is solved self-consistently within the industrial BSIM-CMG model of FinFET, in order to obtain drain current (I_D) of NC-FinFET.

negative capacitance (NC) under certain constraints. The metal-ferroelectric-metal-insulator-semiconductor (MFMIS) arrangement in NCFET can be equivalently represented by a capacitor divider circuit of the ferroelectric capacitance C_{fe} and the internal baseline FET capacitance C_{int} as shown in Fig. 3(b). A negative value of C_{fe} results in voltage amplification at the internal gate, and can be expressed through the following equation:

$$A_V = \frac{|C_{fe}|}{|C_{fe}| - C_{int}} \tag{1}$$

This internal voltage amplification is responsible for suppressing *SS* beyond the Boltzmann limit (i.e., achieving a sub-60 mV/decade) [9]. Additionally, this also results in higher ON current in NCFET compared with the baseline FET at the same applied voltage [11]. Thermodynamically, any ferroelectric system in equilibrium can be described by a double well energy profile at zero applied electric field, as shown in Fig. 3(c). The energy profile is characterized by three extrema states; two with positive curvature or positive capacitance minima and one with a negative curvature or negative capacitance (NC) maximum (note that capacitance $= (\partial^2 G/\partial P^2)^{-1}$). Such an energy profile in thermodynamics is generally modeled by a Taylor series expansion of G in even powers of polarization known as the Landau-Khalatnikov (L-K) theory [37], [38]. The system always occupies either of the two states of minimum energy corresponding to a non-zero/remnant polarization at zero bias. The NC state corresponding to the energy maximum is unstable and, therefore, inaccessible in an isolated ferroelectric capacitor.

Salahuddin and Datta [9] suggested that an unstable NC state can normally be stabilized by connecting a positive dielectric capacitance in series with the ferroelectric, such that the total capacitance of the system becomes positive. They also illustrated this using the L-K model of ferroelectrics. This method ensures a stable minimum in the total energy of the system (at $P = 0$), in which the ferroelectric lies in NC state as shown in Fig. 3(c). In an NCFET structure, the internal baseline FET acts as a positive capacitance (C_{int}) (see Fig. 3(b)), which can stabilize the ferroelectric in NC state, if the total gate capacitance $= ({C_{int}}^{-1} + {C_{fe}}^{-1})^{-1}$ is positive. This condition implies that $|C_{fe}|$ must be greater than C_{int} to realize a thermodynamically stable NC state of the ferroelectric in NCFET. Note that in general, both the $|C_{fe}|$ and C_{int} can be function of applied voltages (gate voltage V_G and drain voltage V_D). Violation of the above condition, for any combination of V_G and V_D results in the hysteresis behavior in device's electrical characteristics [39]. To avoid such violation, the thickness of ferroelectric should be limited because $|C_{fe}|$ varies inversely with t_{fe}. Additionally, $|C_{fe}|$ also depends on the remnant polarization (P_r) and coercive field (E_c) values of the ferroelectric. The ferroelectric with a high remnant polarization (P_r) and low coercive field (E_c) also leads to an increase in the value of $|C_{fe}|$ [12]. This ensures that the condition of no hysteresis, i.e. $|C_{fe}| > C_{int}$, is always met in the range of operating voltages. Note that a low t_{fe}, high P_r and low E_c, all reduce capacitance matching between C_{fe} and C_{int}, thus also the ferroelectric gain according to Eq. 1. Thus, their optimum values should be carefully chosen, such that it provides a larger gain (due to NC effect), but does not lead to hysteresis behavior, which is undesirable for the logic applications.

PHYSICAL ORIGIN OF NC

Many recent experimental works employing a resistor-ferroelectric system [40]–[42] have indicated that the NC effect is actually a transient phenomenon which appears due to insufficient screening of bound polarization charges by the free charges delivered from the voltage source during polarization switching [43]. Chang *et al.* [44], [45] have explained the emergence of transient negative capacitance in resistor-ferroelectric and ferroelectric-dielectric (FE-DE) systems using the previous condition in conjugation with L-K theory [37]. However, some other works [46]–[48] based on different classical ferroelectric models have provided alternative explanations and argued that the negative capacitance may only be a result of dynamics of ferroelectric domain nucleation and growth during polarization switching and not an intrinsic effect based on the thermodynamic L-K theory. Another work has attributed the total energy minimization in FE-DE systems at $P = 0$ under a quasi-static scenario (Fig. 3(c)) to a strong coupling between FE and DE polarizations [49], which may force the whole system act like a dielectric with a positive capacitance behavior [49]. The real physical origin of NC in ferroelectrics is still under intense research.

B. PHYSICAL LEVEL: MODEL DESCRIPTION

In this work, we consider an NC-FinFET that has configuration of MFMIS as shown in Fig. 3(a). The presence of equipotential intermediate metal between the ferroelectric and the oxide insulator, enables the partitioning of full structure into two circuit components: the ferroelectric capacitor and the internal baseline FinFET. The baseline FinFET part of the device is modeled by the industry standard BSIM-CMG model, which accurately captures both the short channel and quantum mechanical effects in small geometries [50], [51]. We employ the open-source 7 nm predictive Process Design Kit (PDK) [52] for the FinFET model parameters. The ferroelectric part is modeled using L-K eqnarray[1] given by: $V_{fe} = t_{fe}(2\alpha Q + 4\beta Q^3)$, where V_{fe} is the voltage across ferroelectric, Q is the gate terminal charge per unit area, t_{fe} is the ferroelectric thickness and α and β are ferroelectric material specific parameters [9], [37]. We adopt Al doped HfO_2 as the ferroelectric, which is a CMOS technology process compatible material [21]. The experimental remnant polarization $=$ 0.05 μC/cm^2 and coercive field $=$ 1 MV/cm values of this material, obtained from [21], are used to calculate α and β

[1]Note that the dielectric constant or more precisely the behavior of polarization with the applied electric field takes the higher dielectric constant of the ferroelectric into account.

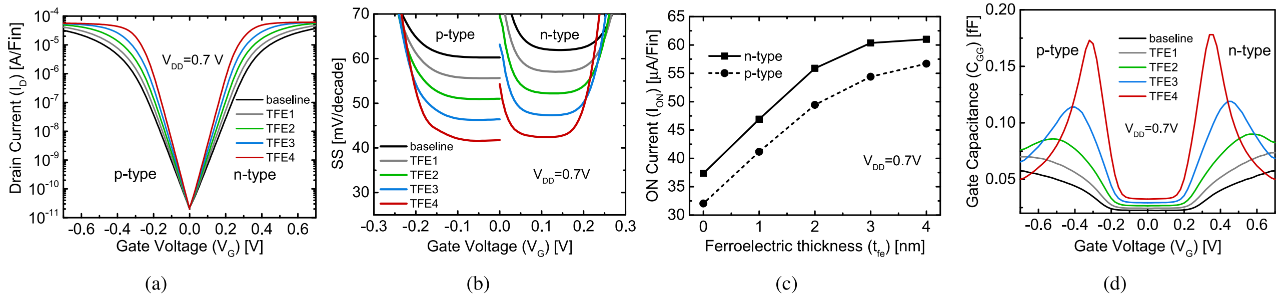

FIGURE 4. **(a) Transfer characteristics of n-type and p-type NC-FinFET for different ferroelectric thicknesses (t_{fe}) at iso-I_{OFF} condition. The I_{OFF} of both types of NC-FinFETs are matched to the corresponding baseline 7nm node FinFETs by work function tuning. (b) sub-threshold swing as a function of gate voltage for different t_{fe} values. (c) ON current variation as a function of t_{fe}. (d) Gate terminal capacitance as a function of gate bias for different t_{fe} values.**

parameters [53]. Finally, for the full device simulation, the L-K equation is solved in a self-consistent manner inside the BSIM-CMG model [51] of FinFET in Verilog-A code (see Fig. 3(d)), using a commercial SPICE simulator [54].

Note that we do not consider in this work non-idealities related to different *SS* in forward and reverse sweeps [42], [55] because the employed structure of NCFET here is MFMIS with defects free top and bottom metal electrodes of the ferroelectric with a single domain configuration. Additionally, we have used ferroelectric layers with relatively small thicknesses (i.e., maximum of 4 nm) in which a hysteresis free operation, which is essential for CMOS logic applications, is ensured.

ROLE OF INTERNAL METAL GATE

Theoretically, internal gate may provide a larger ON current than the NCFET without this gate except for very low P_r ferroelectrics as we have shown in [56]. The presence of internal gate also makes the NCFET device less susceptible to hysteresis [56]. However, some other works have shown that the existence of internal metal gate causes some other issues like destabilization of the negative capacitance state in the presence of ferroelectric leakage current [57] or domain formation [58]. Moreover, the presence of internal metal gate can also contribute as an additional source of traps which may cause the device variability of NCFET with the internal gate to be larger than without internal gate [59].

C. INVESTIGATED CASE STUDIES

We consider four different NC-FinFETs corresponding to four different ferroelectric thicknesses (t_{fe}) of 1 nm, 2 nm, 3 nm and 4 nm; termed as: TFE1, TFE2, TFE3 and TFE4, respectively. Our main focus is to investigate, how different NC-FinFET technologies (i.e., alternations in the NCFET technology itself) can ultimately impact performance and power of the processor compared to the *baseline*, which is the original/conventional 7 nm FinFET, that does not include any ferroelectric material. We refer to the baseline case with TFE0. For fair comparisons, we calibrate the four NC-FinFET devices (TFE1, TFE2, TFE3 and TFE4) through gate work-function tuning in order to acquire iso-I_{OFF} condition i.e. the same OFF current as that of the baseline 7 nm FinFET node (TFE0) at the supply voltage, V_{DD} = 0.7 V, which is the nominal voltage provided in the PDK.

The electrical characteristics of NC-FinFET and their comparison with those of baseline FinFET are shown in Fig. 4. The voltage amplification due to negative capacitance effect, at the internal gate in NC-FinFET, clearly results in lower sub-threshold swing and higher ON current in comparison to baseline FinFET, as demonstrated in Figs. (4(b) and 4(c)). It can be seen that these quantities further improve with increase in the ferroelectric thickness (t_{fe}), due to an improved capacitance matching between the baseline capacitance (C_{int}) and ferroelectric capacitance (C_{fe}), which consequently, provides higher voltage amplification [10], [39]. However, when the gate voltage (V_G) is such that C_{fe} is negative, the total gate terminal capacitance, C_{GG} exceeds C_{int} (conventional dielectric layer) and exhibits sharp peaks as shown in Fig. 4(d). Also, C_{GG} rises with increase in t_{fe}, similar to I_{ON}. Hence, in NCFET, there always exists a trade-off between conflicting I_{ON} and C_{GG} requirements, to achieve better performance gain by increasing t_{fe}. However, in our analysis, we find that the gain in I_{ON}, in general, more than compensates the undesirable increment in C_{GG}. The performance of processor typically improves with increase in t_{fe}, at least until TFE3 (i.e. t_{fe} = 3 nm). Above that ferroelectric thickness (i.e. at TFE4), the compensation effect of C_{GG} can diminish the performance improvement at high V_{DD}. Further details and discussion are presented later in Section IV and demonstrated in Fig. 10(a).

D. NCFET-AWARE CELL LIBRARIES

After incorporating the physical effects that ferroelectric layer causes in the 7 nm p-FinFET and n-FinFET devices, we characterize the 7 nm standard cell library [52] for the five studied cases (i.e., TFE0, TFE1, TFE2, TFE3 and TFE4). Each case is analyzed starting from the nominal operating voltage (V_{DD} = 0.7 V) to the minimum voltage (V_{DD} = 0.2 V) using a commercial tool for cell library characterization [60]. The tool takes the post-layout SPICE netlists of standard cells including the parasitics information as input and calculates the delay and the power information of every cell at the targeted scenario (i.e., V_{DD} and t_{fe} values), using a

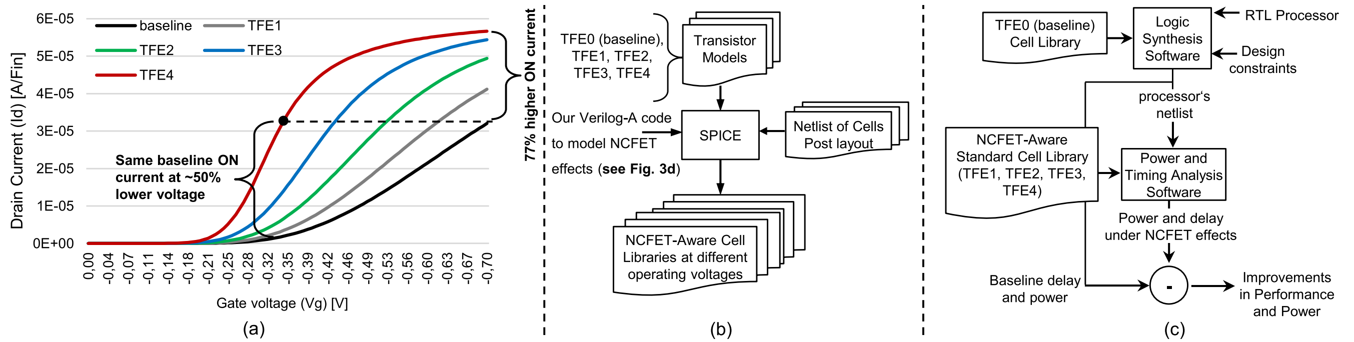

FIGURE 5. (a) The I-V characteristics of pFinFET under the effects of negative capacitance at different thickness of ferroelectric. As shown, the same ON current can be reached a lower V_{DD} when NC-FinFET is employed. Increasing the thickness of ferroelectric layer allows further reduction in the operating voltage while still achieving the same I_{ON}. (b) A general flowchart demonstrating the cell library characterization for creating NCFET-aware cell libraries at different voltages and different thicknesses of ferroelectric. (c) A general flowchart demonstrating, how the created NCFET-aware cell libraries are later used in order to analyze the performance and power of processor, towards evaluating the overall impact of NCFET technology at the processor level.

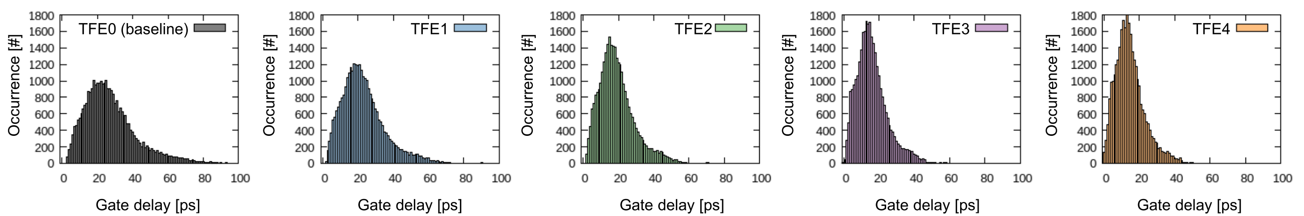

FIGURE 6. Evaluating the impact of NCFET on the delay of cells within the 7 nm FinFET standard cell library. Increasing the thickness of the ferroelectric layer provides a larger gate voltage amplification in transistors (i.e., steeper slope and higher ON current). Hence, the delay of cells become smaller.

commercial SPICE simulator [54]. For the library characterization process, we employ our developed Verilog-A FinFET model, which takes into account the negative capacitance effect as explained earlier, along with the modified transistor modelcard, which contains the baseline FinFET transistor's parameters as well as the parameters that are additionally required for the ferroelectric layer, e.g., ferroelectric thickness (t_{fe}), remnant polarization (P_r) and coercive field (E_c). Every characterized cell library consists of 121 different combinational and sequential cells, covering a wide range of cell complexity, due to the different typologies of cells (i.e., pull-up and pull-down transistor networks inside every cell), starting from an inverter, which has only two transistors to a D-FF cell, which has 26 transistors. Every cell is analyzed under different operating conditions; 7×7 input signal slews and output load capacitances. The selected ranges of operating conditions are obtained from the baseline standard cell library and scaled when considering low V_{DD} scenarios. At the end, all the calculated delay and power information of cells are stored using the standard "liberty" format, which makes the obtained NCFET-aware cell libraries compatible with the existing commercial EDA tools for circuits like logic synthesis and timing/power analysis tool flows [61]. This enables us to integrate our NCFET-aware cell libraries within the standard process flow, to evaluate the overall impact of NCFET on the performance and the power of processors. Figs. 5(b and c) summarize the method of creating NCFET-aware cell libraries and how they can be later employed to evaluate the power and the performance of a processor.

III. EFFECTS OF NCFET ON STANDARD CELLS

As explained earlier, the NCFET-aware cell libraries contain the delay and power information of every cell under the ferroelectric effects for different operating voltages. This enables us to quantify, how the NCFET technology impacts the delay, power, and capacitance of every gate. In Fig. 6, we demonstrate the delay distribution of gates in the 7 nm FinFET cell library, for five different analyzed cases: TFE0, TFE1, TFE2, TFE3 and TFE4. It can be noticed that, with increase in the thickness of ferroelectric layer, the delay distribution gets shifted towards the left side. Hence, the delay of gates at the same voltage ($V_{DD} = 0.7$ V) becomes smaller, which means, NCFET boosts the delay of gates due to the amplification of gate voltage. To demonstrate the relative delay improvement, we show in Fig. 7, the reduction in delay across the standard cell library for the four NCFET technologies relative to the baseline technology. The delay improvement due to NCFET becomes even better at lower voltages. As shown in Fig. 8, for the case of $V_{DD} = 0.4$ V, the NCFET technology can be provide delay improvement by around 40%, 60%, 80% and 90%, on average, for TFE1, TFE2, TFE3 and TFE4, respectively. This improvement is on expected lines, because the improvement in ON current due to NCFET, relative to the baseline, becomes higher at lower voltages, as can be noticed in Fig. 5(a).

It is noteworthy that adding a ferroelectric layer to the gate stack of transistor will directly increase its gate capacitance, since the ferroelectric layer exhibits a negative capacitance (see Fig. 3(b)). Therefore, the total capacitance of gate will

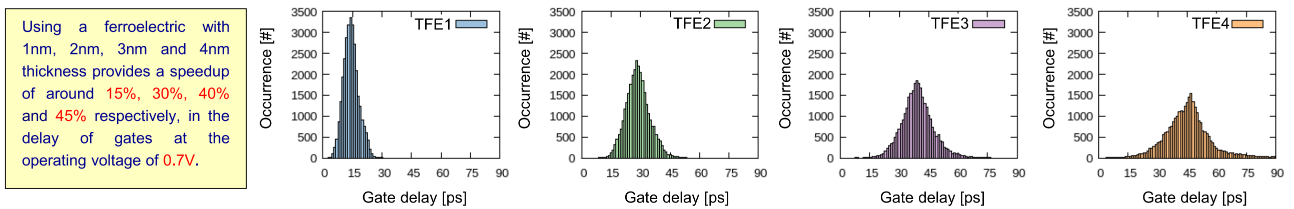

FIGURE 7. Quantifying the relative delay decrease/improvement of cells within the 7 nm FinFET standard cell library due to NCFET at $V_{DD} = 0.7\,V$.

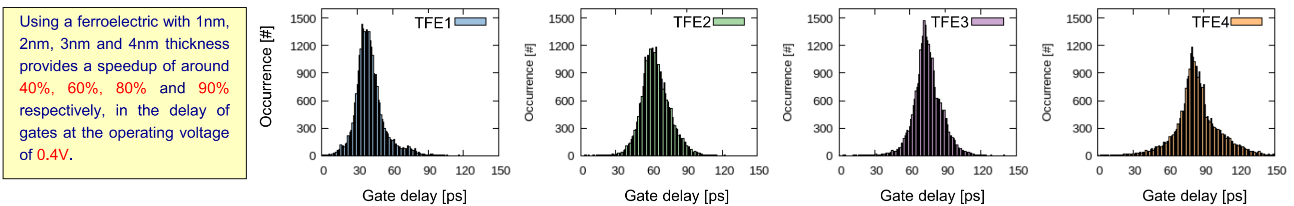

FIGURE 8. Quantifying the relative delay decrease/improvement of gates within the 7 nm FinFET standard cell library due to NCFET at $V_{DD} = 0.4\,V$.

increase due to NCFET, as demonstrated in Fig. 4(d). This of course can have a diminishing impact on the performance gain achieved by NCFET, because gates will exhibit larger capacitance to charge. In Fig. 9(a), we present the relative increase in the cells' capacitance due to NCFET, for the different ferroelectric thicknesses. For instance, the average increase in the cells' capacitance reaches around 20% and 70% when t_{fe} is 1 nm and 4 nm, respectively, for the case of $V_{DD} = 0.7\,V$. Since, NCFET provides a higher drive current and also leads to increase in the cell's capacitance, the internal power of cell will definitely increase. This is indicated in Fig. 9(b), which demonstrates the average increase in the power of cells due to NCFET for $V_{DD} = 0.7\,V$ and $V_{DD} = 0.4\,V$. It is noteworthy that regardless of the increase in the cells' power, at the end of the day, NCFET will still provide a considerable power saving for circuits compared to the baseline. This is because the same baseline performance (i.e., frequency) can be achieved at a lower voltage, which leads to quadratic saving in dynamic power ($P_{dynamic} \propto Freq \times V_{DD}^2$) and exponential saving in stand-by power, thus, compensating the side effect of NCFET with respect to power.

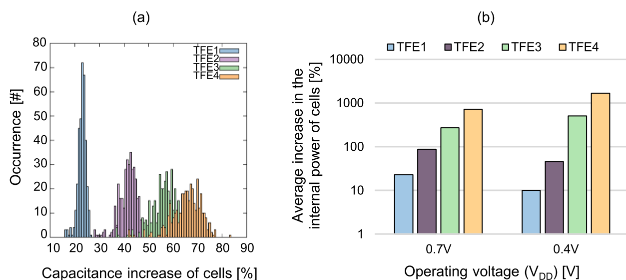

FIGURE 9. (a) Evaluating the impact of NCFET on increasing the total capacitance of cells at $V_{DD} = 0.7\,V$. As expected increasing the thickness of ferroelectric layer leads to an increase in the total cells' capacitance. (b) Evaluating the impact of NCFET on increasing the internal power of cells at $V_{DD} = 0.7\,V$ and $0.4\,V$. The average increase among all cells is used in this analysis.

IV. EFFECTS OF NCFET ON FUTURE PROCESSOR DESIGN

Since, the created NCFET-aware cell libraries are compatible with the existing commercial EDA tool flows (e.g., [61]), we can employ these tools directly without any modification for investigating the impact of NCFET technology on the performance and the power of circuits. Because our main focus is to understand how the NCFET technology can reshape the trends in processor design, we analyzed the Berkeley Out-of-Order Machine (BOOM), which is an open-source industry-competitive processor, based on the recent open source RISC-V instruction set architecture (ISA) [62]. The processor is designed to serve as the prototypical baseline processor for future micro-architectural studies for use in education, research, and industry [63], [64]. In our analysis, we employed the default settings of the BOOM processor when generating its register-transfer level (RTL) for the hardware description. As demonstrated in Fig. 5(c), we first synthesize the RTL of processor using the original 7 nm FinFET cell library. This represents our baseline to compare against. Then, we analyze the performance and the power of processor using the generated gate-level netlist, and our created NCFET-aware cell libraries, for the four different NCFET technologies. This enables us to evaluate, how the gate voltage amplification (originating from the physical level, due to the integration of ferroelectric layer within the gate stack of pFinFET and nFinFET transistors) will finally impact the overall performance and power at the processor level.

A. IMPACT OF NCFET ON COMPUTING EFFICIENCY

To investigate the potential impact of NCFET on the processor design trends, we consider the following three scenarios: **(1) Impact of NCFET on increasing the processor's frequency at the same V_{DD} (i.e. performance improvement without voltage increase):** As explained earlier, the NCFET technology provides voltage amplification for the transistor's gate caused by the integrated ferroelectric material, and this

leads to higher ON currents in pFinFET and nFinFET transistors at the same voltage as shown in Figs. (4(a) and 5(a)). Since, higher ON current results in higher speed in standard cells, as shown in Figs. (6, 7 and 8), the maximum delay of processor becomes smaller, due to NCFET. In Fig. 10(a), we show the frequency increase relative to the baseline for two different V_{DD}, the nominal voltage (0.7 V), and a near-threshold voltage (0.4 V). It can be noticed that, NCFET always provides speedup in the processor's performance. The speedup becomes larger with increase in the thickness of ferroelectric layer due to the higher voltage amplification. At lower voltage (i.e., $V_{DD} = 0.4$ V), the achieved speedup becomes even higher, which is consistent with the results presented earlier in Fig. 8. It is noteworthy that, unlike the case of $V_{DD} = 0.4$ V, increasing thickness of the ferroelectric layer from 3nm to 4nm in the case of $V_{DD} = 0.7$ V, does not lead to any further improvement in the performance. This is due to the compensation effect related to the increase in the cells' capacitance caused by the negative capacitance, as discussed earlier in Section II-C and shown in Figs. (4(d) and 9(a)). These trends are also consistent with the previous works on NCFET based digital circuits [65], [66]. Hence, selecting the optimal thickness of ferroelectric layer, such that the performance gain is maximized, is not trivial and it depends on several aspects, including the operating voltage.

(2) Impact of NCFET technology on increasing the processor's frequency within the baseline power density constraint: As explained earlier, in the introduction, due to the non-ideal voltage scaling, the frequency of processors had stopped increasing in the last decade, to avoid unsustainable on-chip power densities. In the following analysis, we investigate whether the NCFET technology will enable processor designers to increase the processor's frequency, without violating the power density constraint. The latter is considered as the baseline power density of the processor, which is at the nominal voltage ($V_{DD} = 0.7$ V) when no NCFET is employed. As a matter of fact, NCFET allows the pFinFET and nFinFET to have smaller sub-threshold swing and higher ON current than the baseline at the same voltage. Hence, the same ON current as in the baseline case, can be achieved at a lower voltage (see Fig. 5(a)). Therefore, under the same power density constraint as in the baseline case, there is prospect to operate the processor at a higher frequency. In Fig. 10(b), we demonstrate the speedup in processor performance for the four NCFET technologies. As shown in the figure, by increasing the thickness of ferroelectric, higher speedup can be achieved. The figure also shows, the corresponding operating voltage for every NCFET technology (i.e., TFE1, TFE2, TFE3 and TFE4) where the baseline power density has been met.

(3) Impact of NCFET technology on decreasing the processor's voltage under baseline frequency constraint: Last but not least, we investigate what is the minimum operating voltage at which the baseline performance (i.e., the baseline processor's frequency at nominal voltage when no NCFET is employed) can be achieved. Reduction in V_{DD} directly leads to decrease in the overall power of processor, as both static and dynamic powers get reduced at lower voltages [51]. In Fig. 10(c), we show, how the NCFET provides a noticeable reduction in the processor's power for the same performance. As can be noticed, the reduction reaches up to 54% when the thickness of ferroelectric layer is 4nm. Increasing the ferroelectric thickness leads to higher gate voltage amplification. Hence, the same ON current can be achieved at a lower voltage. As shown in the figure, in case of TFE3 and TFE4, the processor can operate at lower than the nominal voltage (i.e., 0.47 V and 0.43 V, respectively) while the baseline processor's frequency is still met. This, in turn, leads to 33% and 54% reductions in processor's power, respectively. Note that from this analysis, it becomes apparent that NCFET can still provide a considerable power reduction despite the increase in power of cells shown in Fig. 9(b), because it allows the processor to operate at a lower voltage, while still achieving the same baseline performance.

B. REWARDING EFFECTS OF NCFET

In order to put the achieved gains due to NCFET in context, now we discuss, how reductions in power density due to

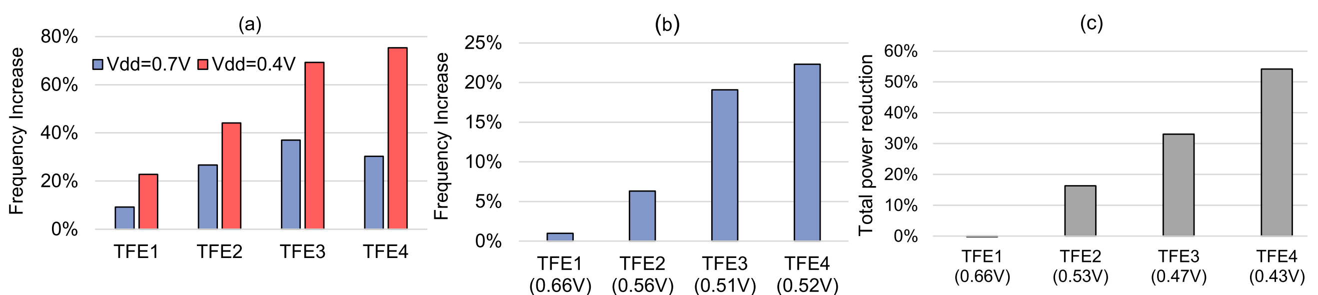

FIGURE 10. Analyzing the impact of NCFET technology at the processor level. (a) Addressing the question of what is the frequency increase due to NCFET under the same voltage constraint? (b) Addressing the question of what is the frequency increase under the same (i.e., baseline) power density constraint? The baseline refers to the power density of processor when no NCFET is employed at the nominal voltage ($V_{DD} = 0.7$ V). (c) Addressing the question of what is the minimum operating voltage along with the achieved power reduction under the same (i.e., baseline) performance (i.e., frequency) constraint? The baseline refers to the frequency of processor when no NCFET is employed at the nominal voltage of 0.7 V.

NCFET will lead to reductions in temperature as well as the role that NCFET may play in the Internet of Things (IoTs) domain, where power budgets are very restricted.

(1) Temperature Reduction: Since, processors nowadays are thermally constrained [5], we analyze further the positive consequences of reducing the total power of processor due to NCFET (see Fig. 10(c)) on temperature. Since, the processor area is the same in all the analyzed cases, the reduction in total power due to NCFET is directly related to the reduction in power density of processor. Hence, NCFET will, in principle, lead to lower operating temperatures. To evaluate this, we use a commercial multiphysics simulation software [67], in order to accurately calculate the maximum temperature of chip for the five different power densities, resulting from the four studied NCFET cases beside the original (i.e., baseline) case. Fig. 11(a) shows an overview of the simulated system. It consists of a chip on top of a printed circuit board (PCB) and under a metal heatsink. Fig. 11(b) summarizes the resulting maximum temperature for the different cases. As shown in the figure, NCFET with ferroelectric thickness more than 1 nm leads to a noticeable temperature reduction, due to the decrease in the on-chip power density. For the case of TFE4, the temperature reduction reaches 62%.

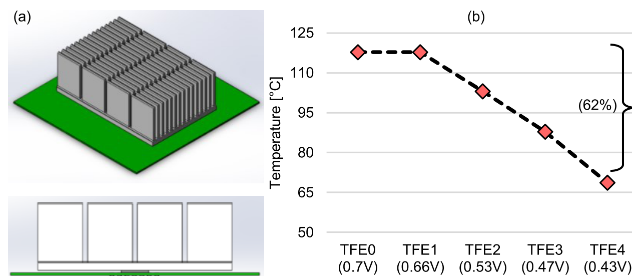

FIGURE 11. Evaluating the corresponding impact of power density reduction due to NCFET on reducing the maximum temperature of chip. (a) shows the built system in a multiphysics simulation software to conduct the required experiments. The system consists of a silicon chip that is located between a PCB and a heatsink. (b) shows the resulting reduction in temperature for every studied NCFET technology case.

Implementation details: In the aforementioned analysis, the size of heatsink is 7.8×5.2 cm with a height of 2.7 cm. The heatsink consists of several fins providing a total surface area of 64133.7mm^2. The heatsink material is aluminum with a thermal conductivity of 237.5 W/mK. We consider a thermal transfer coefficient of 70W/m^{2}K, as in the forced convection of air [68], which provides a temperature below 120°C at the maximum simulated power density (i.e., the baseline power density). The material of simulated chip is silicon anisotropic, with thermal conductivity of 124W/mK, and the thermal conductivity of PCB is 1.4W/mK. The properties of all used materials have been obtained from the engineering data, which is available in the used multiphysics software [67]. The ambient temperature of 27°C was considered in all analyzed cases. It is noteworthy that operation of circuits at lower voltage along with lower temperature can have a considerable impact on their lifetime. This is because the majority of the underlying mechanisms behind reliability degradation, e.g. Bias Temperature Instability (BTI) aging phenomenon, are stimulated by higher voltage and temperature [69]. Therefore, it is also expected that traditional aging mechanisms (e.g., BTI) will be significantly mitigated in NCFET, due to the reduction in voltage and temperature.

(2) Enabling Internet-of-Thing (IoT) Devices: IoTs has recently emerged as an attractive paradigm in which everything and everyone might be connected to internet. IoTs aim at providing variety of services such as sensing and processing data, exchanging information with other IoT devices as well as with cloud for making decisions. One of the key challenges to enable IoTs is that the vast majority of IoT devices may not be possibly powered by batteries, due to the difficulty of replacing them. Therefore, power sources through harvesting energy such as body heat, could be one of the attractive alternatives – especially for wearable medical IoT devices. However, the harvested energy from such resources is typically very low and, hence, not sufficient to operate the processor at a suitable frequency to meet required performance constraints.

Since, NCFET technology is a good candidate for ultra-low power applications, we now investigate, how much the NCFET technology will provide performance improvement for the processor, when it is operated under restricted power budgets which are harvested from a human body heat. For this purpose, we built, using a commercial multiphysics simulation software [67], a thermoelectric generator (TEG) that consists of 128 N-P couples within an area of 3 × 3 cm. The TEG device converts the difference in temperature into electrical power due to the Seebeck effect [70]. To harvest energy from the body heat, the TEG with a small heatsink above it can be located on top of the wrist of a person. This TEG converts the temperature difference between the body skin and the ambient temperature into power. In our analysis, we consider four different ambient temperatures ranging from 0°C to 25°C. In every case, we simulate the heat flux that corresponds to the generated heat from human body at that ambient temperature. The heat flux values haven been obtained from the experimental work in [71]. From the multiphysics simulation, we extract the output voltage of the TEG for the open circuit (V_{OC}). Then, the power generated by connecting a load to the TEG, is calculated using: $P_L = \frac{V_{OC}^2 R_L}{(R_{TEG} + R_L)^2}$. Here, R_{TEG} is the internal resistance of TEG and R_L is the resistance of load. The maximum power point occurs when R_L and R_{TEG} are equal. In Fig. 12(a), we show the maximum generated power for different ambient temperatures. For instance, when the ambient temperature is 15°C, the total power generated by the studied 3 × 3 cm TEG device is 232 μW.

In Fig. 12(b), the improvement in the processor's performance due to NCFET is shown for every power budget that corresponds to the maximum generated power in every ambient temperature case. Unlike the previous analysis in Fig. 10 in which a high-performance processor was studied,

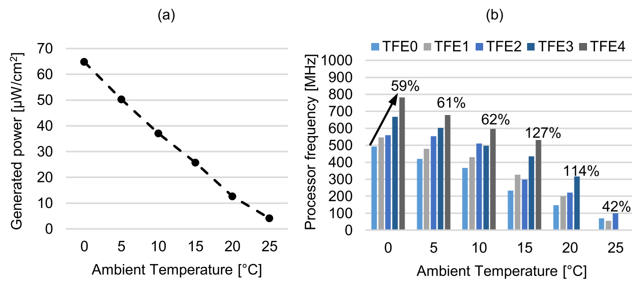

FIGURE 12. (a) Maximum harvested power from body heat using a thermoelectric generator (TEG) at different ambient temperatures. Experiments are done using a multiphysics simulation software. The TEG's area is 9 cm^2. (b) The impact of NCFET technology on improving the performance of an IoT processor, at different power budgets that correspond to the harvested energy from the body heat at different ambient temperatures.

a much simpler processor, which suits more the purpose of IoT devices, has to be considered in this analysis. To this end, we analyze the open-source 32-bit PULPino processor, which has been developed to satisfy the demands of IoT applications [72]. This processor is based on the Instruction Set Architecture of RISC-V, similar to the BOOM processor. As shown in Fig. 12(a), higher the ambient temperature is, smaller the available power budget becomes. Hence, the processor needs to operate at a low V_{DD} to fulfill the ultra-low power budget, which, in turn, leads to considerable performance loss, due to the very low operating frequency. However, for all different ambient temperatures and thus power budgets, NCFET provides a noticeable improvement in the processor's frequency. For instance, when the ambient temperature is 10°C, the NCFET with 4 nm ferroelectric thickness, can boost the processor frequency by 62%. For a smaller power budget, when the ambient temperature is 20°C, the NCFET with a 3 nm ferroelectric layer can increase the processor's performance by more than 110%. In addition, assuming that the IoT device has a performance requirement of 500 MHz, the baseline technology fails to meet such a constraint even at the lowest ambient temperature (0°C), where the harvested power is at maximum. On the other hand, the NCFET technology allows the IoT processor to meet this frequency constraint until the ambient temperature reaches near 15°C. Note that when the power budgets become very small (e.g., when the ambient temperature goes above 15°C), the NCFET technology even with thicker ferroelectric layer (i.e., TFE3, TFE4) fails to fulfill such power budgets. This is mainly due to the increase in the cells' capacitance when the ferroelectric thickness becomes large, as shown in Figs. (4(d), 9(a) and 9(b)). This, in turn, leads to increasing the power consumption of processor beyond the small available power budgets. Note that efficiency loss due to connected circuitries to TEG (e.g., DC-DC converter) is not taken into account in this analysis. However, such loss might be compensated by generating more power through e.g., increasing the size of TEG or adding a second TEG device on the bottom side of the wrist of a person.

Implementation Details: The simulated TEG device has a Seebeck coefficient of 200 V/°C [73] and a total internal resistance of 4.2 Ω. The size of heatsink is 3 × 3 cm matching the TEG surface with a thickness of merely 0.1 cm. The heatsink material is aluminum with a thermal conductivity of 237.5 W/mK. We consider the thermal transfer coefficient to be 5 W/m^{2}K, as in the natural free convection of air [68]. The heatsink has 10 fins, which provides a total surface area of 6528 mm^2. The thickness of the human skin is 1.3 mm and it thermal conductivity is 0.209 W/mK, based on [71] and [74].

V. CONCLUSION

In this work, we have analyzed the impact of NCFET technology on processor performance, based on the 7 nm FinFET. We have demonstrated that the NCFET can provide a quantum leap in computing efficiency, because it enables processors to operate at higher frequencies, without increasing the operating voltage. Additionally, NCFET can revive the prior trend of frequency, which stopped a decade ago due to the irrepressible increase in power densities, because it allows the processor to operate at a higher frequency compared to the conventional 7 nm FinFET, without increasing its power density. We have also shown, how NCFET can lead to a considerable reduction in power density, and hence, temperature, as it allows the processor to operate at a lower voltage while still be clocked at the same frequency as in the the conventional FinFET. Finally, for ultra-low power applications, such as in IoTs, NCFET can play a major role. We have shown that under very small power budgets harvested from body heat, NCFET can noticeably boost the the processor's frequency compared to the conventional FinFET technology.

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