Optimized Design and Control for Hybrid MMC With Reduced Capacitance Requirements

PENG DONG [ID], JING LYU, AND XU CAI [ID]
School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China
Wind Power Research Center, Shanghai Jiao Tong University, Shanghai 200240, China

Corresponding author: Xu Cai (xucai@sjtu.edu.cn)

ABSTRACT Reducing the capacitance of the sub-modules (SMs) and handling dc short-circuit faults are critical for the economical and reliable operation of modular multilevel converters (MMCs) in high-voltage direct current (HVDC) transmission systems. To deal with these issues, the optimized design and control for the hybrid MMC are proposed in this paper. First, the capacitor voltage fluctuations of the hybrid MMC with second-order circulating current and third-order common-mode voltage injection are analyzed. On this basis, the modulation index, required number of half-bridge SMs and full-bridge SMs, and SM capacitances are optimally designed with consideration of the operation constraints of the hybrid MMC, respectively. Further, an optimized control strategy is proposed to ensure the stable operation of the converter and to provide good dynamic performance. The capacitance requirements of the hybrid MMC with optimized design can be reduced to about 38% of those of the hybrid MMC with conventional design. The correctness of the theoretical analysis and the effectiveness of the proposed optimized design and the control strategy have been validated by the simulation and experimental results.

INDEX TERMS Modular multilevel converter (MMC), capacitance reduction, modulation index, circulating current injection, optimized design, control.

I. INTRODUCTION

The modular multilevel converter (MMC) has become one of the most promising converter topologies for high-power applications, e.g., high-voltage direct current (HVDC) transmission, large motor drives and many other important future applications, because of its modularity, scalability and low power loss [1]–[6].

So far, all the existing MMC-HVDC links operate using dc cables. With the increase of transmission voltage, capacity and distance, it is an inevitable choice to use overhead lines as dc transmission lines in consideration of economic and technological advantages. However, it is the fact that the overhead lines are prone to transient failures, e.g., pole-to-pole short-circuit fault. To cope with this problem, two technical routes have emerged. One is to install dc circuit breakers, the other is to use an MMC topology with dc fault handling capability. In view of the high cost and immaturity of dc circuit breakers, the MMC with dc fault handling capability has recently become a hot spot of research. To deal with the frequent dc faults on the overhead lines, several dc fault tolerant topologies have been proposed [7]–[11].

Although these topologies can isolate the fault current by blocking the IGBTs of the converter, it prolongs the shutdown of the overall HVDC system and loses the ability to continuously support the ac system during dc faults. Compared with the dc fault blocking capability, the dc fault ride-through capability is more practical. When a dc fault occurs, the power of the ac system may fluctuate rapidly. In this case, the converter with dc fault ride-through capability can improve the transient stability of the system through the reactive power control [12]. The full-bridge-type MMC (FB-MMC) is a typical converter topology with dc fault ride-through capability, but the cost of semiconductors is recognized as double that of half-bridge-type MMC (HB-MMC) and its power losses have been proven to be up to 70% higher than HB-MMC [13], [14], which is unacceptable.

General application of FB-MMC is limited up to now, because of increased converter power losses and cost. In order to improve these issues, the hybrid MMC topology based on half-bridge sub-modules (HBSMs) and FB sub-modules (FBSMs) has been investigated by several authors [15]–[21]. The topology and operation principle of the hybrid

MMC have been discussed in [15], which considers the operation at modulation indexes of 0.8163 and 1.633. The design of hybrid MMC adopting various different SM topologies was studied in [16]. However, the analysis was performed assuming a relatively low modulation index of 0.81 in all cases. In [17], taking into account the operating range of the dc-link voltage, a design method to determine the number of FBSMs and HBSMs in a hybrid MMC was presented. The optimized design considering the efficiency has been performed in [18]. Other works have focused on the modulation strategies [19], [20] and control strategies [21]–[23]. However, a full investigation into greatly reducing the capacitance requirements for the hybrid MMC has not yet been performed. For the HB-MMC, a second-order circulating current was injected to reduce the capacitor voltage fluctuations in [24]–[28]. These methods are mainly aimed at reducing the second-order capacitor voltage fluctuation, but the relatively larger fundamental-frequency fluctuation is not effectively suppressed. In addition, injecting a higher frequency circulating current and a common-mode voltage could reduce the fundamental-frequency voltage fluctuation [29]–[31]. These methods are convenient for motor drive applications when the motor operates at a low speed, but they are not suitable for grid-connected applications. For the FB-MMC, the energy variations and the resulting capacitor voltage fluctuations have been analyzed in [32] and the capacitor voltage fluctuations can be reduced by taking advantage of the negative voltage output capability of the FBSMs [33], [34].

In this paper, in order to greatly reduce the capacitance requirements while retaining the dc fault ride-through capability and without increasing the conduction losses of the converter, the modulation index, required number of HBSMs and FBSMs, and SM capacitances are optimally designed. On this basis, an optimized control strategy is proposed to ensure the stable operation of the converter and to provide good dynamic performance. With the optimized design and control strategy, the capacitance requirements of the hybrid MMC can be reduced to 38% of the original value. Therefore, it is especially important for offshore windfarm applications which are typically very sensitive to the dimension issue [35].

The paper is organized as follows. Section II depicts the operating principle of the hybrid MMC. The capacitor voltage fluctuations for the hybrid MMC are analyzed in Section III. On this basis, the required number of HBSMs and FBSMs and SM capacitances are optimally designed in section IV. Further, an optimized control strategy is designed step-by-step in section V. The effectiveness of the proposed optimized method is validated by simulation and experimental results in section VI, and finally, section VII concludes the study.

II. OPERATING PRINCIPLE OF HYBRID MMC
A. BASIC CONFIGURATION
Fig. 1 shows the topology of a three-phase hybrid MMC. Each leg consists of one upper and one lower arm connected in series between the dc terminals. Each arm has N SMs, comprising N_h HBSMs, N_f FBSMs and one arm inductor L.
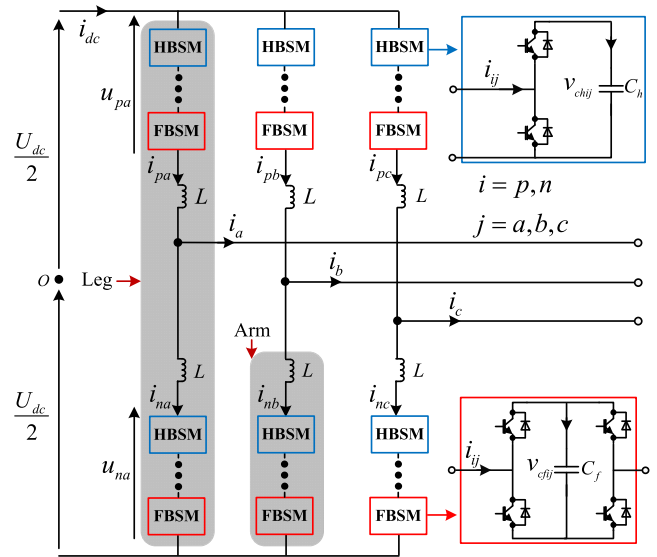

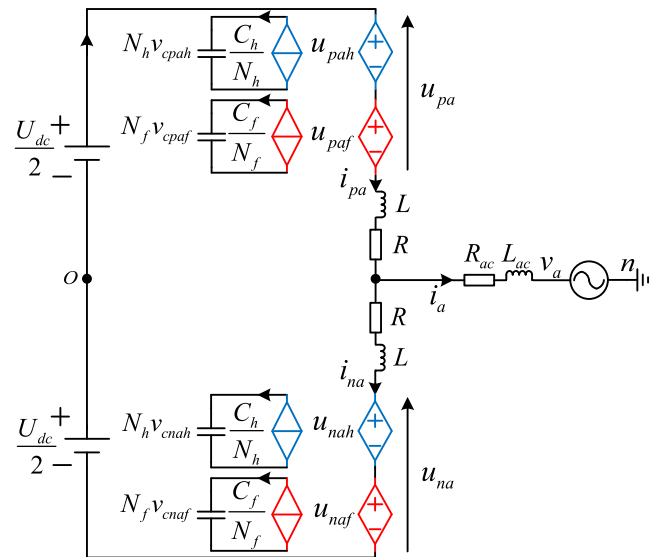**FIGURE 1.** Topology of the hybrid MMC.

FIGURE 2. Single phase average model of the hybrid MMC.

The capacitance of the HBSM is C_h and the capacitance of the FBSM is C_f.

B. OPERATING PRINCIPLE
For the sake of simplicity, one phase (phase a) is taken as an example for illustration due to the symmetry of the three-phase hybrid MMC. Fig. 2 depicts the average model of phase a, where the cascaded HBSMs and FBSMs in each arm can be equivalent to the controllable voltage source, respectively. In the figure, R is the arm equivalent resistance, L_{ac} and R_{ac} are the leakage inductance and equivalent resistance of the transformer, U_{dc} and v_a are the rated dc-link voltage and the ac-side phase voltage, respectively, v_{no} is the common-mode voltage, which is considered to be zero in this common-mode voltage, which is considered to be zero in this paper, u_{pa} and

u_{na} are the voltages generated by all the SMs in the upper and lower arms, respectively, and u_{pah}, u_{nah}, u_{paf}, and u_{naf} are the voltages modulated by the cascaded HBSMs and FBSMs in the upper and lower arms, respectively.

The upper and lower arm currents of the hybrid MMC can be expressed as

$$\begin{cases} i_{pa} = \dfrac{i_{dc}}{3} + i_{cira} + \dfrac{i_a}{2} \\ i_{na} = \dfrac{i_{dc}}{3} + i_{cira} - \dfrac{i_a}{2} \end{cases} \tag{1}$$

where i_{pa} and i_{na} are the upper and lower arm currents, respectively, i_a, i_{cira}, and i_{dc} are the ac-side current, the circulating current, and the dc-side current, respectively.

According to Kirchhoff's voltage law, the following equations can be derived from Fig. 2:

$$\begin{cases} u_{pa} = u_{pah} + u_{paf} = \dfrac{U_{dc}}{2} - e_a - u_{cira} - v_{no} \\ u_{na} = u_{nah} + u_{naf} = \dfrac{U_{dc}}{2} + e_a - u_{cira} + v_{no} \end{cases} \tag{2}$$

where e_a is the ac EMF (driving i_a), u_{cira} is the internal circulating voltage (driving i_{cira}), and can be expressed as follows:

$$\begin{cases} e_a = v_a + \left(\dfrac{L}{2} + L_{ac}\right)\dfrac{di_a}{dt} + \left(\dfrac{R}{2} + R_{ac}\right)i_a \\ u_{cira} = L\dfrac{di_{cira}}{dt} + Ri_{cira} \end{cases} \tag{3}$$

It should be noted that L and L_{ac} are large in high-power HVDC applications [36], thus the voltage drop on the inductors and the reactive power consumed by the inductors can not be ignored. Assuming that the ac EMF, the ac-side current and the circulating current in the steady state can be written as

$$e_a = e_m \cos \omega t = \frac{U_{dc}}{2} m \cos \omega t \tag{4}$$

$$i_a = i_m \cos(\omega t + \phi) \tag{5}$$

$$i_{cira} = i_{cirm} \cos(2\omega t + \theta) \tag{6}$$

where e_m and i_m are the amplitudes of the ac EMF and ac-side current, respectively, m is the modulation index, ϕ and θ are the initial phase angles of the ac-side current and the circulating current, respectively.

It's assumed that all the capacitor voltages in one arm are maintained in a close range by a balancing algorithm included in the MMC control system. Due to the symmetry, the voltages and currents in all arms are only time shifted with respect to each other. Hence, for the sake of simplicity, only the upper arm of phase a is analyzed. The voltages modulated by the cascaded HBSMs and FBSMs can be expressed as

$$\begin{cases} u_{pah} = n_{pah}N_h v_{cpah} \approx (n_{pahdc} + n_{pahac})N_h V_c \\ u_{paf} = n_{paf}N_f v_{cpaf} \approx (n_{pafdc} + n_{pafac})N_f V_c \end{cases} \tag{7}$$

where n_{pah} and n_{paf} are the insertion indices of the HBSMs and FBSMs, respectively, n_{pahdc} and n_{pahac} are the dc and ac components of n_{pah}, respectively, n_{pafdc} and n_{pafac} are the dc and ac components of n_{paf}, respectively, v_{cpah} and v_{cpaf} are

the capacitor voltages of the HBSM and FBSM, respectively, and V_c is the average dc voltage of v_{cpah} and v_{cpaf}.

By ignoring the influence of u_{cira}, the following equation can be derived from (2), (4) and (7)

$$n_{pahac}N_h V_c + n_{pafac}N_f V_c = -e_a = -\frac{U_{dc}}{2}m\cos\omega t \tag{8}$$

According to (8), the ac EMF e_a can be synthesized in many different ways. However, in order to make full use of the effective voltage output capacity of the HBSMs and FBSMs, the absolute value of the fundamental-frequency ac voltage modulated by the HBSMs should be large enough in steady-state operation and this voltage should be kept in phase with the fundamental-frequency ac voltage modulated by the FBSMs. In consequence, we can obtain

$$\begin{cases} n_{pahac1} = -n_{pahac1m}\cos\omega t \\ n_{pafac1} = -n_{pafac1m}\cos\omega t \end{cases} \tag{9}$$

where n_{pahac1} and n_{pafac1} are the fundamental-frequency components of the insertion indices of the HBSMs and FBSMs, respectively, $n_{pahac1m}$ and $n_{pafac1m}$ are the amplitudes of n_{pahac1} and n_{pafac1}, respectively.

The balance of the capacitor voltages in the HBSMs and FBSMs is the prerequisite for the normal operation of the hybrid MMC. Therefore, the amount of charge flowing into the capacitors in a fundamental-frequency cycle is zero, which can be expressed as

$$\begin{cases} \displaystyle\int_t^{t+T} (n_{pahdc} - n_{pahacm1}\cos\omega t)i_{pa}dt = 0 \\ \displaystyle\int_t^{t+T} (n_{pafdc} - n_{pafacm1}\cos\omega t)i_{pa}dt = 0 \end{cases} \tag{10}$$

where T is a fundamental-frequency cycle.

Combining (1)-(5), (7) and (10), and according to the converter input and output power balance, the following equation can be obtained

$$\frac{n_{pahac1m}}{n_{pahdc}} = \frac{n_{pafac1m}}{n_{pafdc}} = m \tag{11}$$

III. ANALYSIS OF CAPACITOR VOLTAGE FLUCTUA-TIONS FOR HYBRID MMC

The capacitor voltages of the HBSMs and FBSMs can be expressed as

$$v_{cpah} = V_c + \tilde{v}_{cpah} \tag{12}$$

$$v_{cpaf} = V_c + \tilde{v}_{cpaf} \tag{13}$$

where $\tilde{v}_{cpah}$ and $\tilde{v}_{cpaf}$ are the ac fluctuation components of the capacitor voltages of the HBSMs and FBSMs, respectively.

According to the instantaneous energy balance of the SM [37], we can obtain

$$\tilde{v}_{cpah} = \frac{1}{N_h C_h V_c}\int p_{pah}dt = \frac{1}{N_h C_h V_c}\int u_{pah}i_{pa}dt \tag{14}$$

$$\tilde{v}_{cpaf} = \frac{1}{N_f C_f V_c}\int p_{paf}dt = \frac{1}{N_f C_f V_c}\int u_{paf}i_{pa}dt \tag{15}$$

where p_{pah} and p_{paf} are the instantaneous fluctuation powers of the cascaded HBSMs and FBSMs, respectively.

A. ANALYSIS OF CAPACITOR VOLTAGE FLUCTUA-TIONS WITH THE SINUSOIDAL MODULATION

For the hybrid MMC with conventional design, the FBSMs do not output the negative voltage in normal conditions, which are equivalent to the HBSMs. Both the FBSMs and HBSMs adopt the sinusoidal modulation. In this case, ignoring the influence of u_{cira} and combining (2), (4), (7) and (11), we can derive

$$\begin{cases} u_{pah} = ku_{pa} = k(\dfrac{U_{dc}}{2} - \dfrac{U_{dc}}{2}m\cos\omega t) \\ u_{paf} = (1-k)u_{pa} = (1-k)(\dfrac{U_{dc}}{2} - \dfrac{U_{dc}}{2}m\cos\omega t) \end{cases} \quad (16)$$

where k is the ratio of the voltage modulated by the cascaded HBSMs to the entire arm voltage and the value of k depends on the ratio of the number of HBSMs to the total number of SMs in one arm, whose range is from 0 to 1.

From (14) and (15), we know that the magnitude and shape of the capacitor voltage fluctuation can be controlled by manipulating the fluctuation power of the HBSMs and FBSMs. Combining (1) and (16), the following equation can be derived as

$$\begin{aligned} p_{pa} = {} & \frac{S}{3m}\cos(\omega t + \phi) - \frac{mU_{dc}i_{cirm}}{4}\cos(\omega t + \theta) \\ & - \frac{m\cos\phi S}{6}\cos\omega t + \frac{U_{dc}i_{cirm}}{2}\cos(2\omega t + \theta) \\ & - \frac{S}{6}\cos(2\omega t + \phi) - \frac{U_{dc}mi_{cirm}}{4}\cos(3\omega t + \theta) \quad (17) \end{aligned}$$

$$\begin{cases} p_{pah} = kp_{pa} \\ p_{paf} = (1-k)p_{pa} \end{cases} \quad (18)$$

where S is the apparent power of the converter, and can be expressed as follows:

$$S = \frac{3}{2}e_m i_m \quad (19)$$

According to (14)-(18), there are large fundamental-frequency and second-order harmonic components in the instantaneous power of the cascaded HBSMs and FBSMs, which would result in large fundamental-frequency and second-order harmonic capacitor voltage fluctuations. Furthermore, the second-order harmonic fluctuation can be adjusted by the circulating current and the fundamental-frequency fluctuation can be influenced by the modulation index.

According to (17)-(18), in order to eliminate the second-order harmonic component, the circulating current that needs to be injected can be derived as

$$i_{cira} = \frac{S}{3U_{dc}}\cos(2\omega t + \phi) \quad (20)$$

After injecting the second-order harmonic circulating current expressed in (20) into the converter, the capacitor voltage fluctuations of the HBSMs and FBSMs can be obtained as

follows through combining (14), (15), (17), (18), and (20)

$$\begin{cases} \tilde{v}_{cpah} = \dfrac{kS}{3N_h C_h V_c \omega} f(m, \phi, t) \\ \tilde{v}_{cpaf} = \dfrac{(1-k)S}{3N_f C_f V_c \omega} f(m, \phi, t) \end{cases} \quad (21)$$

where $f(m, \phi, t)$ is the capacitor voltage fluctuation function of the SMs with the sinusoidal modulation, and can be expressed as follows:

$$f(m, \phi, t) = (\cos\phi \cdot A + \sin\phi \cdot B) \quad (22)$$

where

$$\begin{cases} A = (\dfrac{1}{m} - \dfrac{3m}{4})\sin\omega t - \dfrac{m}{12}\sin 3\omega t \\ B = (\dfrac{1}{m} - \dfrac{m}{4})\cos\omega t - \dfrac{m}{12}\cos 3\omega t \end{cases} \quad (23)$$

According to (21)-(23), we know that although the second-order harmonic capacitor voltage fluctuation is eliminated, the dominant fundamental-frequency component still exists. For $f(m, \phi, t)$, the coefficient of "$\sin\omega t$" is different from that of "$\cos\omega t$", so only when the converter is in pure active power operation or pure reactive power operation can the fundamental-frequency fluctuation be eliminated by adjusting the modulation index m. In high-power HVDC applications, the converter usually operates at the approximate unity power factor ($0.94 \le \cos\phi \le 1$) when transmitting the rated power. In this case, in order to greatly reduce the capacitor voltage fluctuations, the modulation index should be set close to $2/\sqrt{3}$. However, the modulation index of the hybrid MMC with the sinusoidal modulation is limited to less than 1. In order to obtain the reasonable modulation index, the ac voltage modulated by the HBSMs should be with a certain degree of distortion and the generated harmonics of this voltage should be compensated by the FBSMs in one arm. In addition, the harmonics can not have any influence on the voltage balance in the HBSMs and the FBSMs, if the arm currents are free of the corresponding harmonic components.

B. ANALYSIS OF CAPACITOR VOLTAGE FLUCTUA-TIONS WITH THIRD HARMONIC INJECTION

It is necessary to point out that if the total ac voltage of the hybrid MMC is not synthesized according to the "best" synthesis mode where the fundamental-frequency ac voltage modulated by the HBSMs is kept in phase with the fundamental-frequency ac voltage modulated by the FBSMs, the maximum value of m can reach 2 [17]. However, in this case, the waveforms with highest degrees of distortion might be generated by the HBSMs and FBSMs, thus more extra FBSMs are needed, which may increase the costs and make the dynamics of the arm more complex. In consequence, only the "best" synthesis mode is considered in this paper.

According to (4) and (11), fundamental conditions for capacitor voltage balance enforce that the same value of m must be ensured for the HBSMs, the FBSMs and the whole
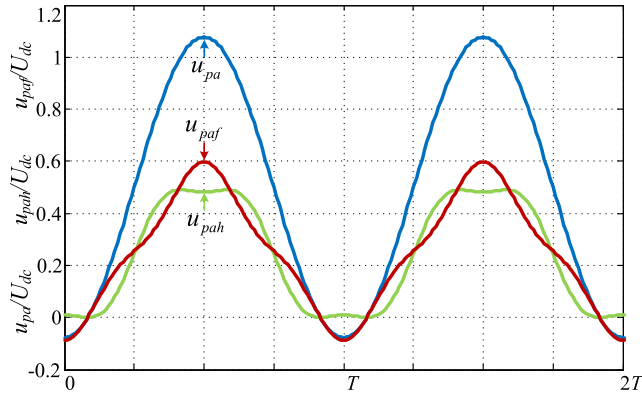
FIGURE 3. Synthesis schematic diagram of the normalized arm voltage.

FIGURE 4. Normalized peak-to-peak value of capacitor voltage fluctuation vs. power phase angle and modulation index with third harmonic injection.

hybrid MMC in steady-state operation. Hence, in order to make the modulation index m of the HBSMs reach $2/\sqrt{3}$, a third harmonic voltage should be injected into its reference voltage, which can be expressed as follows

$$u_{pah} = k(\frac{U_{dc}}{2} - e_m \cos \omega t + \frac{e_m}{6} \cos 3\omega t) \qquad (24)$$

The injected zero-sequence third harmonic voltage may produce a zero-sequence current depending on the application and grounding connection of the hybrid MMC. In order to solve this problem, the third harmonic voltage modulated by the HBSMs must be compensated by the FBSMs as shown in Fig. 3, and the reference voltage of the FBSMs can be derived as

$$u_{paf} = (1-k)(\frac{U_{dc}}{2} - e_m \cos \omega t - \frac{ke_m}{6(1-k)} \cos 3\omega t) \qquad (25)$$

In this case, the FBSM would output negative voltage, thus the dc voltage output capability and the active power conversion capability of a single FBSM are smaller than those of a single HBSM, which will cause the capacitor voltage fluctuation of the FBSM to be smaller than that of the HBSM. In consequence, we should focus on the capacitor voltage fluctuations of the HBSMs with third harmonic injection and then find the optimized modulation index for the hybrid MMC.

After injecting the second-order harmonic circulating current expressed in (20), and combining (1), (4)-(5), (14) and (24), the capacitor voltage fluctuation of the HBSMs with third harmonic injection can be obtained

$$\tilde{v}_{cpah} = \frac{kS}{3N_h C_h V_c \omega} f_{ch}(m, \phi, t) \qquad (26)$$

where $f_{ch}(m, \phi, t)$ is the capacitor voltage fluctuation function of the HBSMs with third harmonic injection, and can be expressed as follows:

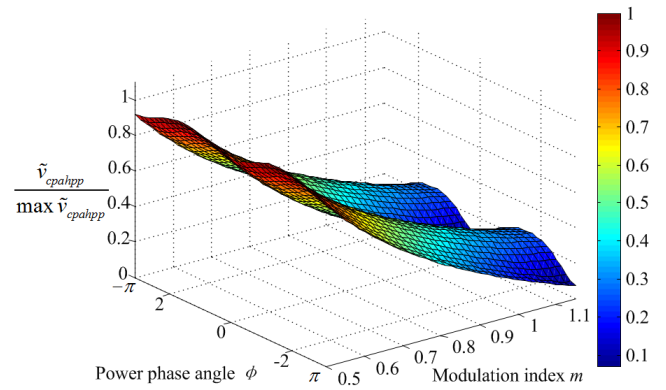$$f_{ch}(m, \phi, t) = (\cos \phi \cdot C + \sin \phi \cdot D) \qquad (27)$$

where

$$\begin{cases} C = (\frac{1}{m} - \frac{17m}{24}) \sin \omega t + \frac{1}{24} \sin 2\omega t \\ \quad - \frac{m}{18} \sin 3\omega t + \frac{1}{48} \sin 4\omega t + \frac{m}{120} \sin 5\omega t \\ D = (\frac{1}{m} - \frac{7m}{24}) \cos \omega t - \frac{1}{24} \cos 2\omega t \\ \quad - \frac{m}{12} \cos 3\omega t + \frac{1}{48} \cos 4\omega t + \frac{m}{120} \cos 5\omega t \end{cases} \qquad (28)$$

According to (26)-(28), a 3-dimensional figure can be plotted to demonstrate the influence of the power phase angle and the modulation index on the peak-to-peak value of the capacitor voltage fluctuation of the HBSMs with third harmonic injection, as shown in Fig. 4. One horizontal axis is the power phase angle ϕ, where the range is $-\pi \leq \phi \leq \pi$; another horizontal axis is the modulation index m, where the range is $0.5 \leq m \leq 2/\sqrt{3}$. The vertical axis is the ratio of the peak-to-peak value of the capacitor voltage fluctuation to the maximum peak-to-peak value of the fluctuation within the above range. From Fig. 4, it can be seen that the peak-to-peak value of the capacitor voltage fluctuation is symmetrical when the converter is in the rectifier and inverter operation and it decreases with the increase of the modulation index m for any power phase angle ϕ. Therefore, the optimized modulation index m should be selected to $2/\sqrt{3}$ to greatly reduce the capacitance requirements for the hybrid MMC.

IV. OPTIMIZED DESIGN FOR HYBRID MMC WITH REDUCED CAPACITANCE REQUIREMENTS
A. REQUIRED NUMBER OF HBSMS AND FBSMS
In order to enable the hybrid MMC to ride through the dc short-circuit fault without blocking the IGBTs, the cascaded FBSMs need to output the maximum negative voltage expected by the arm. Then the reactive power interaction between the converter and the ac power grid can still be performed during the dc short-circuit fault, which provides support for the ac power grid. Thus the number of the
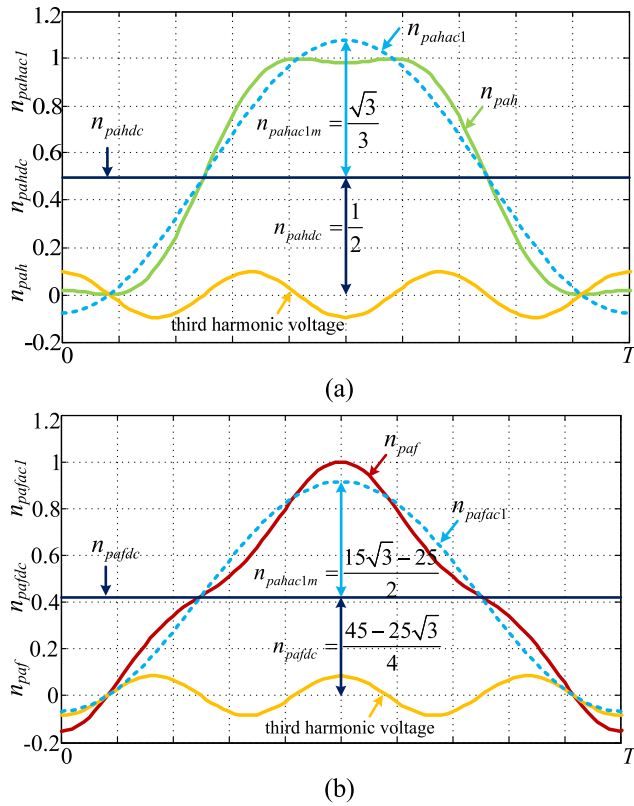
(a)

(b)

FIGURE 5. Insertion indices of the HBSMs and FBSMs.

FBSMs should be satisfied as follows:

$$N_f \geq \frac{e_m}{V_c} = \frac{\sqrt{3}U_{dc}}{3V_c} \tag{29}$$

In order to reduce the losses and costs of the converter, the number of the FBSMs should be minimum on the premise of satisfying (29). Therefore, the required number of the FBSMs in each arm is

$$N_f = ceil(\frac{\sqrt{3}U_{dc}}{3V_c}) \approx ceil(\frac{0.577U_{dc}}{V_c}) \tag{30}$$

where *ceil* is a rounding function that returns the smallest integer greater than or equal to the specified expression.

Combining (8)-(9) and (11), we can obtain

$$\begin{cases} n_{pahdc}N_hV_c + n_{pafdc}N_fV_c = \dfrac{U_{dc}}{2} \\ n_{pahac1m}N_hV_c + n_{pafac1m}N_fV_c = \dfrac{\sqrt{3}U_{dc}}{3} \end{cases} \tag{31}$$

In order to make full use of the voltage output capacity of the HBSMs, the absolute value of the dc voltage and the fundamental-frequency ac voltage modulated by the HBSMs should be maximized. Therefore, as shown in Fig. 5(a), n_{pahdc} and $n_{pahac1m}$ should be

$$\begin{cases} n_{pahdc} = \dfrac{1}{2} \\ n_{pahac1m} = \dfrac{\sqrt{3}}{3} \end{cases} \tag{32}$$

Combining (11), (24)-(25) and (29)-(32), n_{pafdc}, $n_{pafac1m}$, (shown in Fig. 5(b)) k and N_h can be derived as follows:

$$\begin{cases} n_{pafdc} = \dfrac{45 - 25\sqrt{3}}{4} \\ n_{pahac1m} = \dfrac{15\sqrt{3} - 25}{2} \end{cases} \tag{33}$$

$$k = \frac{15\sqrt{3} - 25}{2} \tag{34}$$

$$N_h = ceil(\frac{(27 - 15\sqrt{3})U_{dc}}{2V_c}) \approx ceil(\frac{U_{dc}}{2V_c}) \tag{35}$$

B. CAPACITANCE SELECTION OF HBSMS AND FBSMS

Combining (1), (4)-(5), (15), (25)-(26), (30) and (34)-(35), the capacitor voltage fluctuations of the HBSMs and FBSMs can be obtained

$$\tilde{v}_{cpah} = \frac{0.33S}{U_{dc}\omega C_h}f_{ch}(m, \phi, t) \tag{36}$$

$$\tilde{v}_{cpaf} = \frac{0.29S}{U_{dc}\omega C_f}f_{cf}(m, \phi, t) \tag{37}$$

where $f_{cf}(m, \phi, t)$ is the capacitor voltage fluctuation function of the FBSMs, and can be expressed as follows:

$$f_{cf}(m, \phi, t) = (\cos \phi \cdot E + \sin \phi \cdot F) \tag{38}$$

where

$$\begin{cases} E = (\dfrac{1}{m} - \dfrac{19m}{24})\sin \omega t - \dfrac{1}{24}\sin 2\omega t \\ \quad - \dfrac{m}{9}\sin 3\omega t - \dfrac{1}{48}\sin 4\omega t - \dfrac{m}{120}\sin 5\omega t \\ F = (\dfrac{1}{m} - \dfrac{5m}{24})\cos \omega t + \dfrac{1}{24}\cos 2\omega t \\ \quad - \dfrac{m}{12}\cos 3\omega t - \dfrac{1}{48}\cos 4\omega t - \dfrac{m}{120}\cos 5\omega t \end{cases} \tag{39}$$

According to (27) and (38), Fig. 6 can be plotted to demonstrate the influence of the power phase angle within $-0.11\pi \leq \phi \leq 0.11\pi$ ($0.94 \leq \cos \phi \leq 1$) on the peak-to-peak value of the voltage fluctuation function of the HBSMs and FBSMs. We can observe that the peak-to-peak value of the voltage fluctuation function increases with the increase of the power phase angle ϕ for a fixed modulation index m. Therefore, the capacitances of the SMs should be designed considering the operating conditions with $\phi = \pm 0.11\pi$ ($\cos \phi = 0.94$).

According to [37], the peak-to-peak value of the capacitor voltage fluctuation can not exceed 20% of the rated value. Therefore, the minimum capacitance of the HBSMs and FBSMs can be derived as

$$\begin{cases} C_h = \dfrac{1.65S}{U_{dc}V_c\omega}f_{ch}(\sqrt{3}/2, \pm 0.11\pi, t)_{pp} \\ C_f = \dfrac{1.45S}{U_{dc}V_c\omega}f_{cf}(\sqrt{3}/2, \pm 0.11\pi, t)_{pp} \end{cases} \tag{40}$$

where $f_{ch}(m, \phi, t)_{pp}$ and $f_{cf}(m, \phi, t)_{pp}$ are the peak-to-peak values of the capacitor voltage fluctuation functions of the HBSMs and FBSMs, respectively.
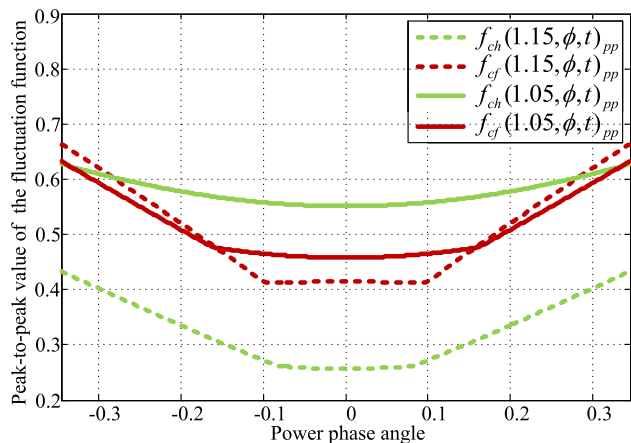
FIGURE 6. Peak-to-peak value of the voltage fluctuation function vs. power phase angle.

FIGURE 7. Comparison of capacitance requirements of the hybrid MMC with conventional and optimized design.

The above calculation is only for theoretical analysis. However, in the actual operation, taking into account the system dynamics, the transient operating conditions and the capacitor voltage fluctuations, a certain margin should be required for the modulation index m. For the hybrid MMC with the sinusoidal modulation, the theoretical maximum value of m is 1, and the typical value in actual operation is 0.9 [3]. Similarly, for the hybrid MMC with third harmonic injection, the theoretical maximum value of m is $2/\sqrt{3}$, and the typical value in actual operation should be set to 1.05. In consequence, the minimum capacitance of the HBSMs and FBSMs should be designed as follows

$$\begin{cases} C_h = \dfrac{1.65S}{U_{dc}V_c\omega}f_{ch}(1.05, \pm 0.11\pi, t)_{pp} \\ C_f = \dfrac{1.45S}{U_{dc}V_c\omega}f_{cf}(1.05, \pm 0.11\pi, t)_{pp} \end{cases} \tag{41}$$

C. COMPARISION OF CAPACITANCE REQUIREMENTS AND CONDUCTION LOSSES

According to the above analysis, we can know that the required number of the HBSMs and FBSMs should be designed under the condition of the modulation index $m = \sqrt{3}/2$, and the capacitances of the HBSMs and FBSMs should be designed under the condition of the modulation index $m = 1.05$.

The "energy-to-power ratio" is often used in engineering to measure the converter's capacitance requirements [35], which can be expressed as

$$EP = \frac{3(N_h C_h V_c^2 + N_f C_f V_c^2)}{S} \tag{42}$$

According to (30), (35), (41)-(42), Fig. 6 and [37], the "energy-to-power ratio" of the hybrid MMC with optimized design ($m = 1.05$) and with conventional design ($m = 0.9$) can be obtained, respectively

$$EP_{op} = 10\text{kJ/MVA} \tag{43}$$
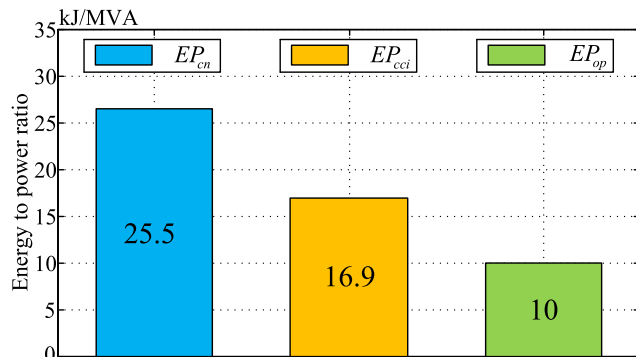
$$EP_{cn} = 26.5\text{kJ/MVA} \tag{44}$$

where EP_{op} and EP_{cn} are "energy-to-power ratio" of the hybrid MMC with optimized and conventional design, respectively.

According to (43), (44) and [25], the comparison of the capacitance requirements of the hybrid MMC with different design is presented in Fig. 7. It can be seen that the "energy-to-power ratio" of the conventional hybrid MMC injected only with the second-order circulating current EP_{cci} is reduced to about 66% of that of the hybrid MMC with conventional design EP_{cn} [25], and the "energy-to-power ratio" of the hybrid MMC with optimized design EP_{op} is reduced to about 38% of EP_{cn}.

Under the same dc-link voltage and transmission power, the upper arm current in phase a of the hybrid MMC with optimized and conventional design can be expressed as

$$i_{paop} = \frac{i_{dc}}{3} + \frac{20i_{dc}}{27\cos\phi}\cos(\omega t + \phi)$$
$$+ \frac{i_{dc}}{3\cos\phi}\cos(2\omega t + \phi) \tag{45}$$

$$i_{pacn} = \frac{i_{dc}}{3} + \frac{40i_{dc}}{63\cos\phi}\cos(\omega t + \phi) \tag{46}$$

In this paper, HiPak5SNA 1500E330305 IGBT of ABB is selected for loss calculation. For MMCs used in HVDC applications, the conduction losses are the dominant component of the converter losses. Therefore, the conduction losses are compared for the hybrid MMCs with optimized and conventional design. By adopting the method proposed in [38], the conduction losses can be calculated as shown in Fig. 8. It can be observed that under the same dc-link voltage and transmission power, the conduction losses of the hybrid MMCs with optimized and conventional design are both 0.9%, and the conduction losses of the conventional hybrid MMC injected only with the second-order circulating current is 1.03%.

V. OPTIMIZED CONTROL FOR HYBRID MMC WITH REDUCED CAPACITANCE REQUIREMENTS

Due to the drastic reduction in the capacitances of the HBSMs and FBSMs, the capacitor voltages are more susceptible to
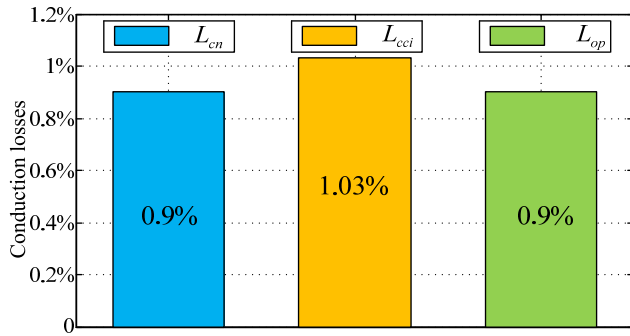
FIGURE 8. Comparison of conduction losses of the hybrid MMC with conventional and optimized design.

the disturbances, which challenges the stable operation of the converter. In order to solve this problem, the capacitor voltages should be controlled in a closed-loop manner, and a dedicated feed-forward compensation should be considered, thus allowing to choose the convergence rate of the voltage balancing. Therefore, an optimized capacitor voltage control is designed step-by-step as shown below.

Combining (1) and (2), and ignoring the influence of u_{cirj}, the instantaneous power of the cascaded SMs in the upper and lower arms can thus be expressed as

$$\frac{dw_{pj}}{dt} = (\frac{U_{dc}}{2} - e_j)(\frac{i_{dc}}{3} + i_{cirj} + \frac{i_j}{2}) \tag{47}$$

$$\frac{dw_{nj}}{dt} = (\frac{U_{dc}}{2} + e_j)(\frac{i_{dc}}{3} + i_{cirj} - \frac{i_j}{2}) \tag{48}$$

where $j = $ (a, b,c), w_{pj} (w_{nj}) is the energy stored in the cascaded SMs of the upper (lower) arm.

The addition of (47) and (48) and subtraction of (48) from (47) yield respectively

$$\frac{dw_{j\Sigma}}{dt} = \frac{1}{3}U_{dc}i_{dc} + U_{dc}i_{cirj} - e_ji_j \tag{49}$$

$$\frac{dw_{j\Delta}}{dt} = -2e_ji_{cirj} + \frac{U_{dc}}{2}i_j - \frac{2}{3}e_ji_{dc} \tag{50}$$

where $w_{j\Sigma}$ ($w_{j\Delta}$) is the sum (difference) of energy stored in the cascaded SMs of the upper and lower arms.

Because the capacitor voltage balance control is focused on regulating the dc components of the energies, only the non-alternating power terms are considered. Transforming (49) to the $\alpha\beta0$ reference frame and ignoring the losses of the converter station, the dynamics of the sum of energy stored in the cascaded SMs of the upper and lower arms can be derived from algebraic calculation as

$$\begin{cases} \frac{dw_{\alpha\Sigma dc}}{dt} = U_{dc}i_{cir\alpha dc} - \frac{1}{2}(v_\alpha i_{\alpha-} - v_\beta i_{\beta-}) = u_{sum\alpha} \\ \frac{dw_{\beta\Sigma dc}}{dt} = U_{dc}i_{cir\beta dc} + \frac{1}{2}(v_\alpha i_{\beta-} + v_\beta i_{\alpha-}) = u_{sum\beta} \\ 3\frac{dw_{0\Sigma dc}}{dt} = U_{dc}i_{dc} - \frac{3}{2}v_d i_{d+} = u_{sum0} \end{cases} \tag{51}$$

where $w_{\alpha\Sigma dc}$, $w_{\beta\Sigma dc}$ and $w_{0\Sigma dc}$ are the dc components of the sum of energy stored in the cascaded SMs of the upper and

lower arms in the $\alpha\beta0$ reference frame, $i_{\alpha-}$ and $i_{\beta-}$ are the negative sequence ac-side currents, $i_{cir\alpha dc}$ and $i_{cir\beta dc}$ are the dc components of the circulating currents, $u_{sum\alpha}$, $u_{sum\beta}$ and u_{sum0} are defined as the auxiliary control inputs in the $\alpha\beta0$ reference frame, v_d is the d-axis component of the ac-side voltage and i_{d+} is the positive sequence d-axis component of the ac-side currents in the dq reference frame.

According to (51), both $i_{cir\alpha\beta dc}$ and $i_{\alpha\beta-}$ can be used to balance the capacitor voltages among different legs. However, during the dc short-circuit fault, $i_{cir\alpha dc}$ and $i_{cir\beta dc}$ are invalid. Therefore, in order to perform seamless transition between normal operating conditions and dc-short circuit fault conditions, $i_{\alpha-}$ and $i_{\beta-}$ are used to balance the capacitor voltages. Similarly, the total capacitor voltage stored in the converter should be regulated by the positive sequence d-axis component of the ac-side current i_{d+}. By defining the auxiliary control inputs $u_{sum\alpha}$, $u_{sum\beta}$ and u_{sum0}, the non-alternating power disturbances can be compensated in a feed-forward manner. Through transforming the control input, a PI-based feedback control loop can be designed to regulate the capacitor voltages among different legs using the resulting first-order system as shown in (51). The reference of the ac-side currents can be expressed as:

$$i_{d+ref} = \frac{2}{3v_d}(U_{dc}i_{dc} - u_{sum0}) \tag{52}$$

$$\begin{bmatrix} i_{\alpha-ref} \\ i_{\beta-ref} \end{bmatrix} = \frac{2}{(v_\alpha^2 + v_\beta^2)} \begin{bmatrix} -v_\alpha & v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} u_{sum\alpha} \\ u_{sum\beta} \end{bmatrix} \tag{53}$$

where i_{d+ref} is the reference value of the positive sequence d-axis component of the ac-side current in the dq reference frame, $i_{\alpha-ref}$ and $i_{\beta-ref}$ are the reference values of the negative sequence ac-side currents in the $\alpha\beta0$ reference frame.

Transforming (50) to the $\alpha\beta0$ reference frame, the dynamics of the difference of energy stored in the cascaded SMs of the upper and lower arms can be derived from algebraic calculation as

$$\begin{bmatrix} \frac{dw_{\alpha\Delta dc}}{dt} \\ \frac{dw_{\beta\Delta dc}}{dt} \\ \frac{dw_{0\Delta dc}}{dt} \end{bmatrix} = A \begin{bmatrix} i_{cir\alpha1+} \\ i_{cir\beta1+} \\ i_{cir\alpha1-} \\ i_{cir\beta1-} \end{bmatrix} = \begin{bmatrix} u_{dif\alpha} \\ u_{dif\beta} \\ u_{dif0} \end{bmatrix} \tag{54}$$

where $w_{\alpha\Delta dc}$, $w_{\beta\Delta dc}$ and $w_{0\Delta dc}$ are the dc components of the difference of energy stored in the cascaded SMs of the upper and lower arms in the $\alpha\beta0$ reference frame, $i_{cir\alpha1+}$ and $i_{cir\alpha\beta1-}$ are the positive and negative sequence fundamental-frequency circulating currents, respectively, $u_{dif\alpha}$, $u_{dif\beta}$ and u_{dif0} are defined as the auxiliary control inputs in the $\alpha\beta0$ reference frame, and A can be expressed as

$$A = \begin{bmatrix} -e_{\alpha-} & e_{\beta-} & -e_{\alpha+} & e_{\beta+} \\ e_{\beta-} & e_{\alpha-} & e_{\beta+} & e_{\alpha+} \\ -e_{\alpha+} & -e_{\beta+} & -e_{\alpha-} & -e_{\beta-} \end{bmatrix} \tag{55}$$

According to (54), $i_{cir\alpha\beta1+}$ and $i_{cir\alpha\beta1-}$ can be used to balance the capacitor voltages between the upper and lower arms. By defining the auxiliary control inputs $u_{dif\alpha}$, $u_{dif\beta}$

and u_{dif0}, a PI-based feedback control loop can be designed to regulate the difference of energy stored in the cascaded SMs of the upper and lower arms using the resulting first-order system as shown in (54). However, there are three energies to be controlled and four ac components of the circulating current to be chosen. Therefore, it is necessary to add a constraint condition in which the reactive power interaction between the positive-sequence fundamental-frequency circulating current and the ac-side voltage is zero in order to ensure that the converter achieves the highest efficiency, that is

$$\frac{3}{2}(-v_\alpha i_{cir\beta1+} + v_\beta i_{cir\alpha1+}) = 0 \qquad (56)$$

Combining (54) and (56), the reference values of the positive and negative fundamental-frequency ac components of the circulating current can thus be expressed as:

$$\begin{bmatrix} i_{cir\alpha1+ref} \\ i_{cir\beta1+ref} \\ i_{cir\alpha1-ref} \\ i_{cir\beta1-ref} \end{bmatrix} = \begin{bmatrix} -e_{\alpha-} & e_{\beta-} & -e_{\alpha+} & e_{\beta+} \\ e_{\beta-} & e_{\alpha-} & e_{\beta+} & e_{\alpha+} \\ -e_{\alpha+} & -e_{\beta+} & -e_{\alpha-} & -e_{\beta-} \\ -e_{\beta+} & e_{\alpha+} & 0 & 0 \end{bmatrix}^{-1} \begin{bmatrix} u_{dif\alpha} \\ u_{dif\beta} \\ u_{dif0} \\ 0 \end{bmatrix} \qquad (57)$$

According to (51)-(57), the optimized capacitor voltage balance control strategy for the hybrid MMC with reduced capacitance requirements is designed as shown in Fig. 9. Fig. 9(a) depicts the block diagram of the total capacitor voltage control and the capacitor voltage balance control among different legs, the feedback value of the sum of energy stored in the cascaded SMs of the upper and lower arms contains a large double-frequency ripple. In order to eliminate the influence of the double-frequency component, a 100Hz notch filter is needed in the feedback link. The outputs of the three PI regulators are u_{sum0}, $u_{sum\alpha}$ and $u_{sum\beta}$, respectively, and the reference values of the positive sequence and negative sequence ac-side currents can be obtained according to (52) and (53), respectively. Fig. 9(b) depicts the block diagram of the capacitor voltage balance control between the upper and lower arms, the feedback value of the difference of energy stored in the cascaded SMs of the upper and lower arms contains a large fundamental-frequency ripple. In order to eliminate the influence of fundamental-frequency component, we need to add a 50Hz notch filter in the feedback link. The outputs of the three PI regulators are $u_{dif\alpha}$, $u_{dif\beta}$ and u_{dif0}, respectively, and the reference value of the positive and negative fundamental-frequency ac components of the circulating current can be obtained according to (57).

The overall control strategy proposed in this paper, as shown in Fig. 10, consists of outer loop control and inner loop control. The outer loop control includes three parts. The first part is fixed dc voltage control (corresponding to a fixed dc voltage converter station) or fixed active power control (corresponding to a fixed active power converter station), whose output is the reference value of the dc-side current. The second part is the total capacitor voltage control and capacitor voltage balance control among legs shown in Fig. 9(a), whose outputs are the reference values of the
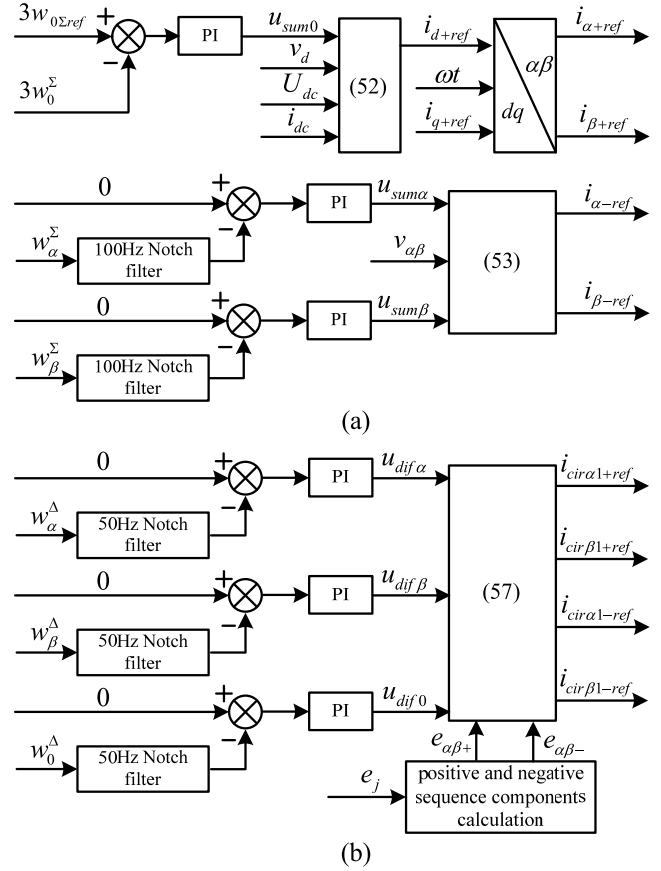

FIGURE 9. Optimized capacitor voltage control strategy: (a) total capacitor voltage control and capacitor voltage balance control between upper and lower arm, (b) capacitor voltage balance control among legs.
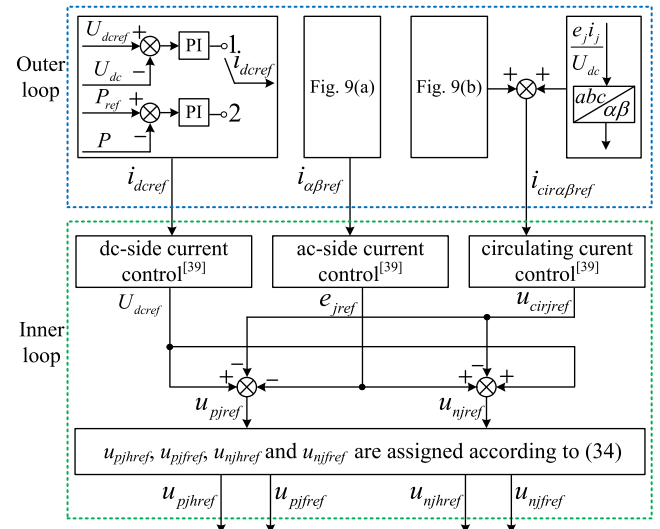

FIGURE 10. The overall control strategy for the hybrid MMC.

ac-side currents. The third part is the capacitor voltage balance control between the upper and lower arms shown in Fig. 9(b), and the reference values of the circulating currents can be obtained by adding the outputs of the capacitor voltage balance control and the reference value of the

TABLE 1. Simulation parameters of the hybrid MMC with conventional design.

Symbol	Quantity	Value
P	rated active power	1000 MW
Q	rated reactive power	200 MVar
U_{dc}	dc-link voltage	640 kV
V	ac rated rms voltage	400/342 kV
f	frequency	50 Hz
N_h	number of HBSM in one arm	10
N_f	number of FBSM in one arm	10
C_h	capacitance of HBSM	0.45 mF
C_f	capacitance of FBSM	0.45 mF
L	arm inductance	36 mH
L_{ac}	transformer leakage inductance	36 mH
R	arm resistor	1.1 Ω
L_{dc}	limiting inductance	20 mH

TABLE 2. Simulation parameters of the hybrid MMC with optimized design.

| Symbol	Quantity	Value
V	ac rated rms voltage	400/400 kV
N_f	number of FBSM in one arm	12
L_{ac}	transformer leakage inductance	52 mH
C_h	capacitance of HBSM	0.17 mF
C_f	capacitance of FBSM	0.15 mF

second-order circulating current. The inner loop control includes dc-side current control, ac-side current control, and circulating current control [39]. The reference voltages of the upper and lower arms are formed by integrating the outputs of the three current controllers linearly, then the reference voltages of the HBSMs and FBSMs in each arm are assigned according to (34).

VI. SIMULATION AND EXPERIMENTAL VERIFICATIONS
A. SIMULATION RESULTS
To verify the effectiveness of the optimized design and control for the hybrid MMC proposed in this paper, a nonlinear time domain simulation model of the hybrid MMC system shown in Fig. 11 has been built by using MATLAB/ Simulink. The ac side of the converter is connected to a three-phase ac power grid, and the dc side is connected to a current-limiting reactor and a resistive load. The converter adopts the fixed dc voltage control strategy. The simulation parameters of the hybrid MMC with conventional design are shown in Table 1. The simulation parameters of the hybrid MMC with optimized design are shown in Table 2. The parameters not listed in Table 2 are the same as those in Table 1. Considering the voltage drop on the inductors and the reactive power consumed by the inductors, the modulation index m of the hybrid MMC with conventional and optimized design is 0.9 and 1.05, respectively, and both power phase angles satisfy $\cos\phi = 0.94$.
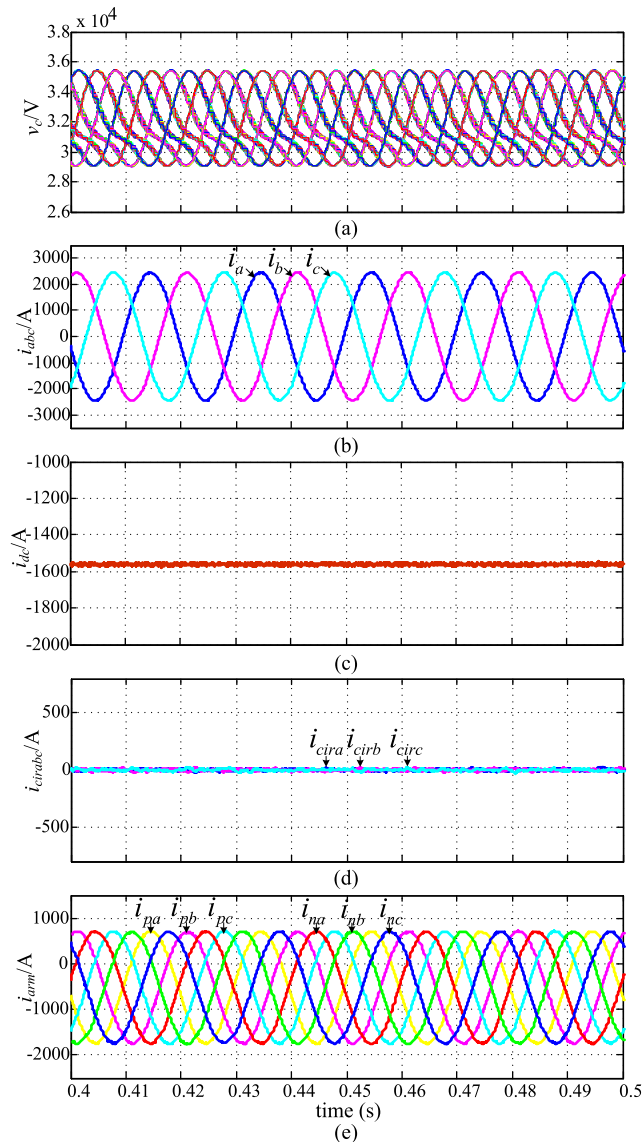
The steady-state simulation results of the hybrid MMC with conventional design when transmitting the rated active
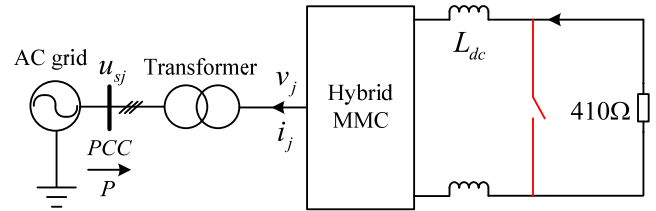
FIGURE 11. Schematic diagram of the simulated hybrid MMC system.

power and generating the rated reactive power (capacitive reactive power given as positive) are shown in Fig. 12. Fig. 12(a) shows the capacitor voltage waveforms of the HBSMs and FBSMs. It can be seen that the peak-to-peak values of the capacitor voltage fluctuations are both 6.4 kV, accounting for 20% of the rated value. Fig. 12(d) shows the waveform of the circulating current, and we can observe that the second-order circulating current is suppressed very well. Fig. 12(b), (c), and (e) show the waveforms of the ac-side, the dc-side, and the arm currents of the hybrid MMC. It can be seen that the hybrid MMC with conventional design has good steady-state performance.

The steady-state simulation results of the hybrid MMC with optimized design when transmitting the rated active power and generating the rated reactive power are shown in Fig. 13. The capacitances of HBSM and FBSM are 0.17mF and 0.15mF, respectively. Fig. 13(a) and (b) show the capacitor voltage waveforms of the HBSMs and FBSMs, respectively. It can be seen that the peak-to-peak values of the voltage fluctuations of the HBSMs and FBSMs are both 6.4 kV, accounting for 20% of the rated value, which verifies the correctness of (41) and (43). This indicates that the capacitance requirements of the hybrid MMC with optimized design can be reduced to 38% of those of the hybrid MMC with conventional design. Fig. 13(e) shows the waveform of the circulating current, and we can see that it includes the second-order harmonic components, which is consistent with (20). Fig. 13(c), (d), and (e) show the waveforms of the ac-side, the dc-side, and the arm currents of the hybrid MMC. It can be seen that the hybrid MMC with optimized design also has good steady-state performance.

The transient simulation results of the hybrid MMC with optimized design riding through the dc short-circuit fault are shown in Fig. 14. At t=0.5s, a dc short-circuit fault occurs at the dc port of the converter. Fault detection technology is a very critical issue in fault processing, but it is beyond the scope of this paper. In order to simplify the simulation, this paper monitors the dc-side current to determine whether there is a dc short-circuit fault. When the amplitude of the dc-side current is monitored to exceed 2350A (1.5pu), the controller considers that a dc short-circuit fault has occurred, then the dc-side current and the circulating currents are quickly controlled to zero. From the waveform of the dc-side current in Fig. 14(e), we can see that the fault current is cleared within 10 ms after the fault occurs, and at t=0.8s, the controller is switched to normal operation mode. The dc-link voltage quickly returns to the rated value, and the power
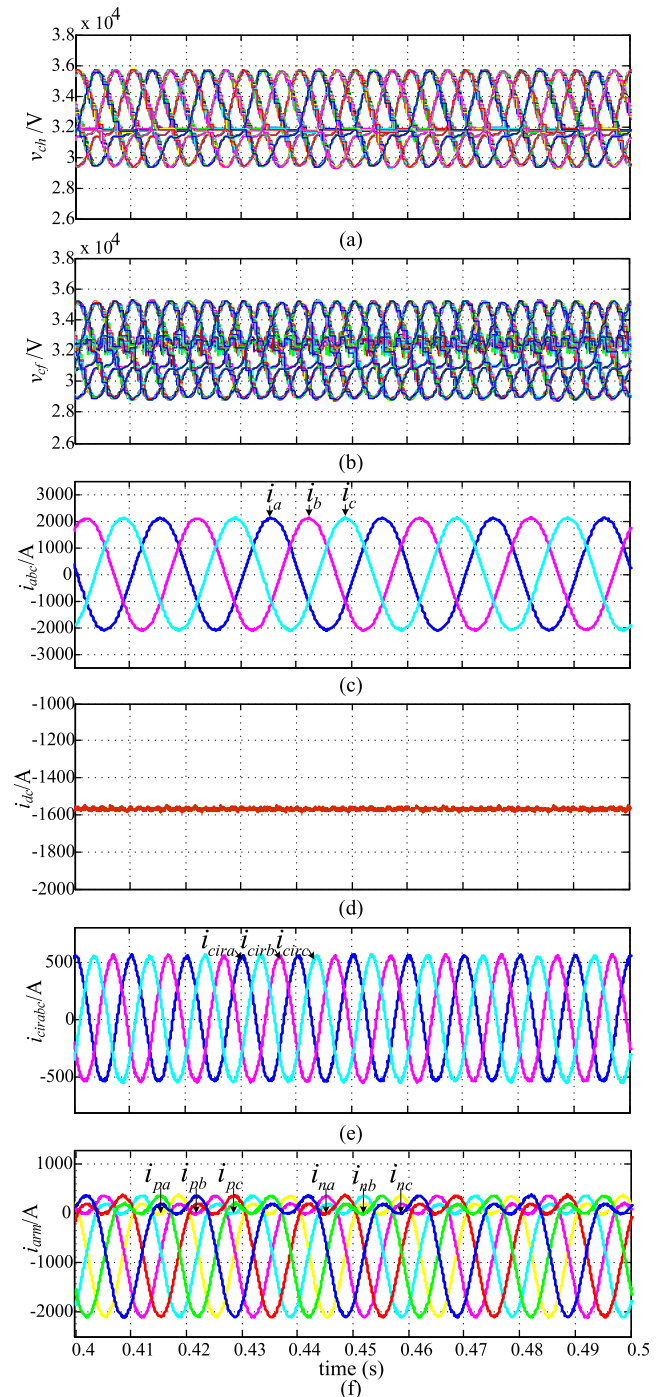
FIGURE 12. Steady-state simulation results of the hybrid MMC with conventional design. (a) Capacitor voltages of HBSMs and FBSMs. (b) AC-side current. (c) DC-side current. (d) Circulating currents. (e) Arm currents.

transmitted by the system is quickly recovered to the pre-fault value. As can be observed from the waveforms of the ac-side currents in Fig. 14(c), during the fault-ride-through period, the hybrid MMC still generates 400MVar reactive power to support the ac power grid. Furthermore, it can be observed from Fig. 14(a), (b), (f) and (g) that after the dc short-circuit fault occurs or the controller is switched to normal operation mode, the capacitor voltages, the circulating currents and the arm currents can quickly enter the new steady state, which verifies the good dynamic performance of the optimized control strategy.

B. EXPERIMENTAL RESULTS

A scaled-down three-phase hybrid MMC prototype has been built in the laboratory to further verify the effectiveness of

FIGURE 13. Steady-state simulation results of the hybrid MMC with optimized design. (a) Capacitor voltages of HBSMs. (c) AC-side current. (d) DC-side current. (e) Circulating currents. (f) Arm currents.

the optimized design and control for the hybrid MMC. Photograph of the prototype is shown in Fig. 15. Fig. 16 shows the experimental system configuration of the downscaled system. The hybrid MMC adopts the fixed dc voltage control strategy and the two-level converter adopts the fixed power control strategy. The circuit parameters of the hybrid MMC with conventional design are listed in Table 3, and the circuit parameters of the hybrid MMC with optimized design are
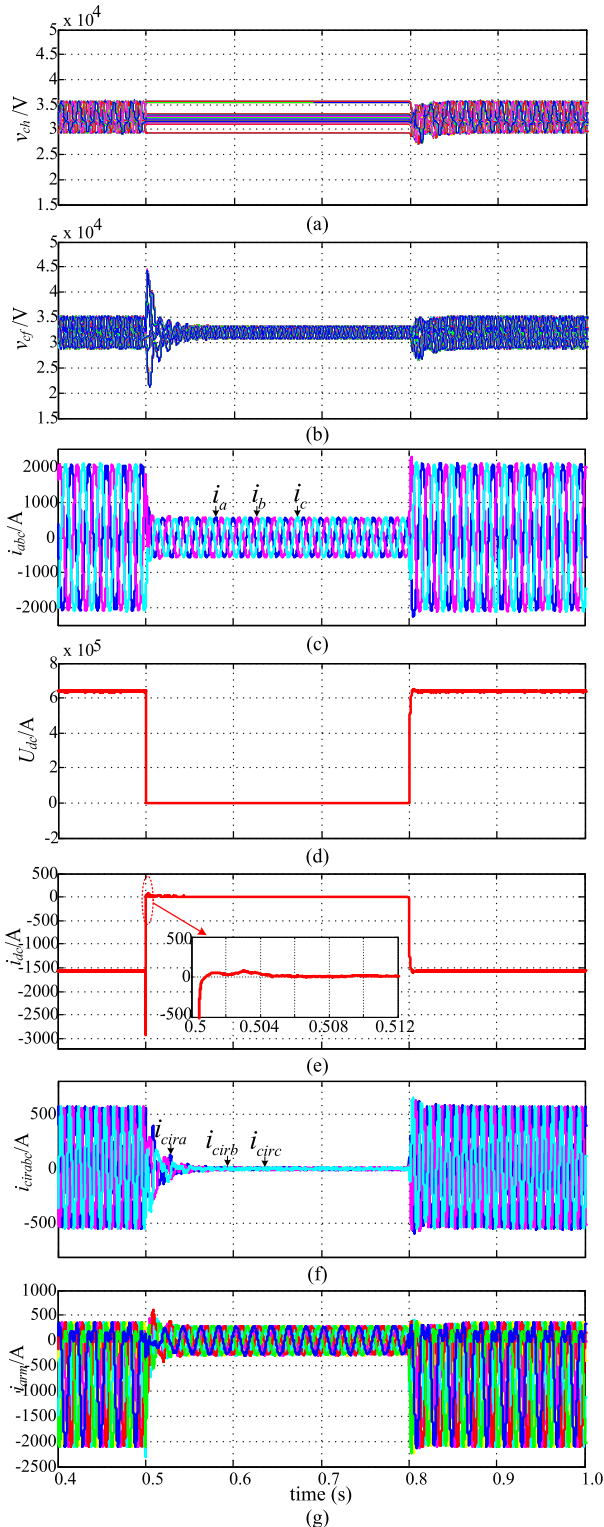
FIGURE 14. Transient simulation results of the hybrid MMC system with optimized design. (a) Capacitor voltages of HBSMs. (b) Capacitor voltages of FBSMs. (c) AC-side current. (d) DC-link voltage. (e) DC-side current. (f) Circulating currents. (g) Arm currents.

listed in Table 4. The parameters not listed in Table 4 are the same as those in Table 3. Considering the voltage drop on the inductors and the reactive power consumed by the inductors,

TABLE 3. Experimental parameters of the hybrid MMC with conventional design.

Symbol	Quantity	Value
P	active power	5 kW
Q	reactive power	800 Var
U_{dc}	dc-link voltage	300 V
V	ac rated rms voltage	380/161 V
f	frequency	50 Hz
N_h	number of HBSM in one arm	2
N_f	number of FBSM in one arm	2
C_h	capacitance of HBSM	2 mF
C_f	capacitance of FBSM	2 mF
L	arm inductance	1.5 mH
L_{ac}	ac-side inductance	2 mH
f_s	switching frequency	4000 Hz

TABLE 4. Experimental parameters of the hybrid MMC with optimized design.

Symbol	Quantity	Value
Q	reactive power	1200 Var
V	ac rated rms voltage	380/190 V
N_f	number of FBSM in one arm	3
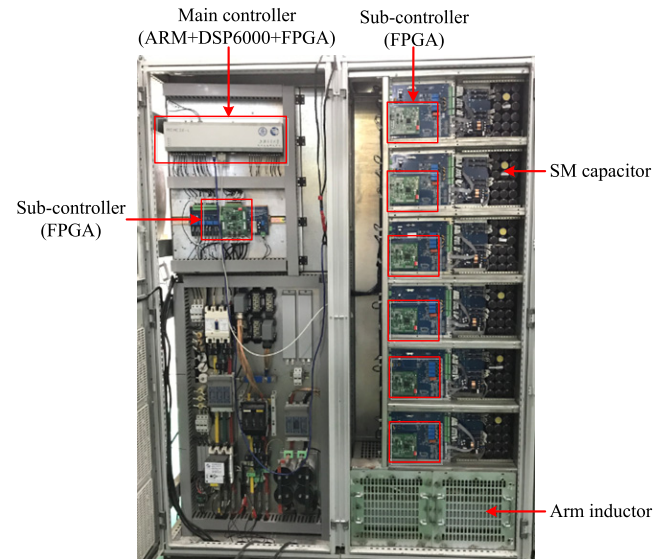
FIGURE 15. Photograph of the laboratorial three-phase hybrid MMC prototype.

the modulation index m of the hybrid MMC with conventional and optimized design is 0.9 and 1.05, respectively, and both power phase angles satisfy $\cos\phi = 0.94$. Because it is difficult to select the appropriate SM capacitor to be mounted on the prototype with optimized design. To simplify the experiment, the SM capacitance of the prototype with optimized design is 2mF, which is the same as that of the prototype with conventional design. In consequence, the peak-to-peak value of the capacitor voltage fluctuation will be used to indirectly measure the capacitance requirements of the converter.
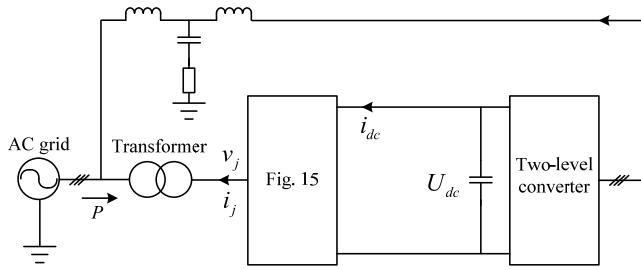
FIGURE 16. Experimental system configuration of the downscaled system.

(a)
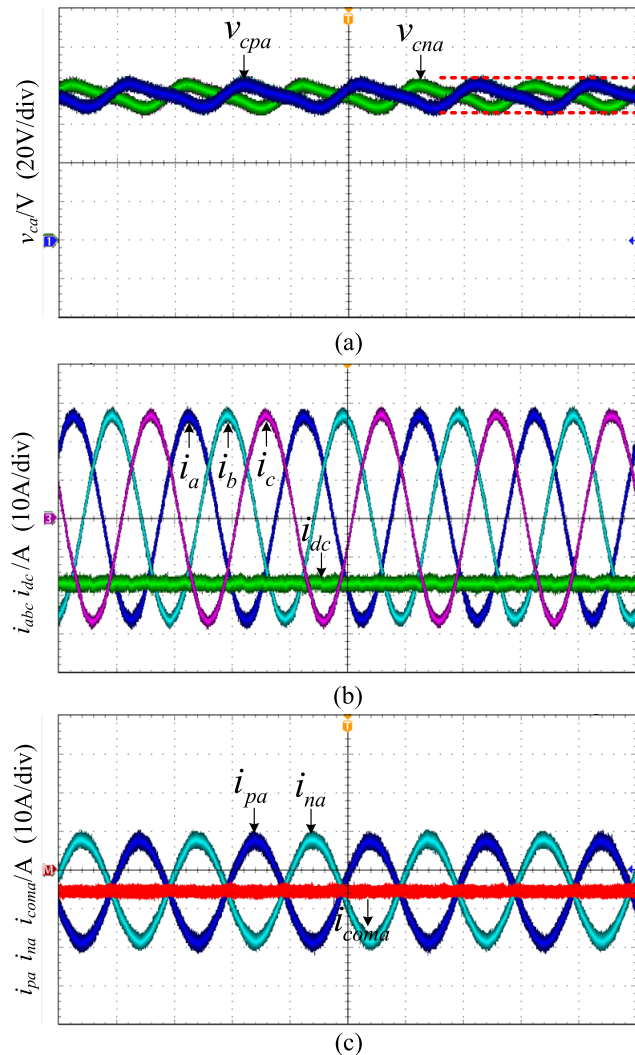

(a)

(b)

(b)

(c)

(c)

(d)

FIGURE 17. Steady-state experimental results of the hybrid MMC with conventional design. (a) Capacitor voltages of HBSMs and FBSMs of phase *a*. (b) AC- and dc-side currents. (c) Arm and common-mode currents of phase *a* 10ms/div.

FIGURE 18. Steady-state experimental results of the hybrid MMC with optimized design. (a) Capacitor voltages of HBSMs of phase *a*. (b) Capacitor voltages of FBSMs of phase *a*. (c) AC- and dc-side currents. (d) Arm and common-mode currents of phase *a* 10ms/div.

The steady-state experimental results of the hybrid MMC with conventional design are shown in Fig. 17. Fig. 17(a) shows the capacitor voltage waveforms of the HBSMs and FBSMs of phase a. It can be seen that the peak-to-peak values of the capacitor voltage fluctuations of the HBSMs and FBSMs are both 15.4V, accounting for 20.5% of the rated value, which is a little bigger than the theoretical value 20%.

Fig. 17(c) shows the waveforms of the arm and common-mode currents of phase a, where the common-mode current $i_{coma} = i_{dc}/3 + i_{cira}$, and we can observe that the circulating current is suppressed very well. Fig. 17(b) shows the waveforms of ac- and dc-side currents of the hybrid MMC. We can see that the hybrid MMC with conventional design has good steady-state performance.

The steady-state experimental results of the hybrid MMC with optimized design are shown in Fig. 18. Fig. 18(a) shows the capacitor voltage waveforms of the HBSMs. It can be seen that the peak-to-peak value of the voltage fluctuation of the HBSMs is 5.9V, accounting for 7.9% of the rated v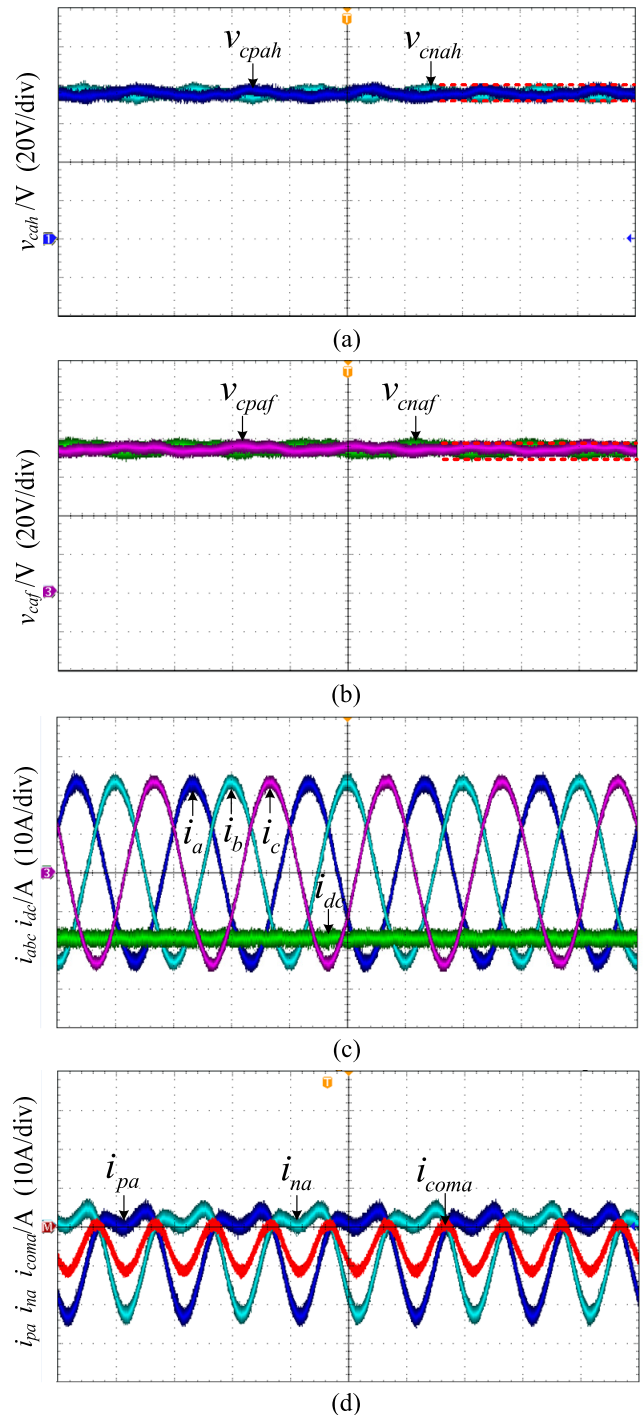alue, which is a little bigger than the theoretical value 7.6% according to (41). Fig. 18(b) shows the capacitor voltage waveforms of the FBSMs. It can be seen that the peak-to-peak value of the voltage fluctuation of the FBSMs is 4.2V, accounting for 5.6% of the rated value, which is a little bigger than the theoretical value 5.3% according to (41). This indirectly indicates that the capacitance requirements of the hybrid MMC with optimized design can be reduced to 38% of those of the hybrid MMC with conventional design. The differences between the measured values and the calculated values of the capacitor voltage fluctuations may be caused by the power losses of the prototype. Fig. 18(d) shows the waveforms of the arm and common-mode currents of phase a, and we can see that it includes the second-order harmonic components, which is consistent with (20). Fig. 18(c) shows the waveforms of ac- and dc-side currents of the hybrid MMC. It can be seen that the hybrid MMC with optimized design also has good steady-state performance. The experimental results verify the effectiveness of the proposed optimized method for the hybrid MMC.

VII. CONCLUSION

This paper proposes an optimized design and control for the hybrid MMC, which can not only greatly reduce the capacitance requirements, but also retaining the dc fault ride-through capability and without increasing the conduction losses of the converter. The main conclusions are as follows.

1) The capacitance requirements of the hybrid MMC with optimized design can be reduced to about 38% of those of the hybrid MMC with conventional design.

2) The optimized design and control are especially important for the hybrid MMC used in offshore windfarm applications which are typically very sensitive to the dimension issue.

3) The optimized control strategy can ensure the stable operation of the hybrid MMC and provide good dynamic performance.

REFERENCES

[1] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-networks and extended DC-bus-applications," in *Proc. Int. Power Electron. Conf.*, Jun. 2010, pp. 502–507.

[2] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan. 2015.

[3] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[4] J. Lv, P. Dong, G. Shi, X. Cai, H. Rao, and J. Chen, "Subsynchronous oscillation of large DFIG-based wind farms integration through MMC-based HVDC," in *Proc. Int. Conf. Power Syst. Technol.*, Chengdu, China, Oct. 2014, pp. 2401–2408.

[5] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded control system of the modular multilevel converter for feeding variable-speed drives," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 349–357, Jan. 2015.

[6] M. M. Steurer et al., "Multifunctional megawatt-scale medium voltage DC test bed based on modular multilevel converter technology," *IEEE Trans. Transp. Electrific.*, vol. 2, no. 4, pp. 597–606, Dec. 2016.

[7] D. Schmitt, Y. Wang, T. Weyh, and R. Marquardt, "DC-side fault current management in extended multiterminal-HVDC-grids," in *Proc. IEEE Int. Multi-Conf. Syst., Signals Devices*, Mar. 2012, pp. 1–5.

[8] A. Nami, L. Jiaqi, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, Jan. 2015.

[9] R. Li, J. E. Fletcher, L. Xu, D. Holliday, and B. W. Williams, "A hybrid modular multilevel converter with novel three-level cells for DC fault blocking capability," *IEEE Trans. Power Del.*, vol. 30, no. 4, pp. 2017–2026, Aug. 2015.

[10] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits," *IEEE Trans. Power Del.*, vol. 30, no. 1, pp. 385–394, Feb. 2015.

[11] G. P. Adam, I. Abdelsalam, J. E. Fletcher, G. M. Burt, D. Holliday, and S. J. Finney, "New efficient submodule for a modular multilevel converter in multiterminal HVDC networks," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4258–4278, Jun. 2017.

[12] G. Tang, Z. Xu, and Y. Zhou, "Impacts of three MMC-HVDC configurations on AC system stability under DC line faults," *IEEE Trans. Power Syst.*, vol. 29, no. 6, pp. 3030–3040, Nov. 2014.

[13] T. Jonsson, P. Lundberg, S. Maiti, and Y. Jiang-Hafner, "Converter technologies and functional requirements for reliable and economical HVDC grid design," in *Proc. CIGRÉ Canada Conf.*, Sep. 2013, pp. 1–9.

[14] R. Marquardt, "Modular multilevel converter—Impact on future applications and semiconductors," in *Proc. Power Electron. Compon. Appl.*, Apr. 2017, pp. 1–10.

[15] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1137–1146, Mar. 2015.

[16] W. Lin, D. Jovcic, S. Nguefeu, and H. Saad, "Full-bridge MMC converter optimal design to HVDC operational requirements," *IEEE Trans. Power Del.*, vol. 31, no. 3, pp. 1342–1350, Jun. 2016.

[17] V. Hofmann and M.-M. Bakran, "Optimized design of a hybrid-MMC and evaluation of different MMC topologies," in *Proc. Eur. Conf. Power Electron. Appl. (ECCE)*, Sep. 2016, pp. 1–9.

[18] V. Hofmann and M.-M. Bakran, "An optimized hybrid-MMC for HVDC," in *Proc. PCIM Europe Conf.*, Mar. 2016, pp. 1–8.

[19] S. Lu, L. Yuan, K. Li, and Z. Zhao, "An improved phase-shifted carrier modulation scheme for a hybrid modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 81–97, Feb. 2017.

[20] R. Zeng, L. Xu, L. Yao, and D. J. Morrow, "Precharging and DC fault ride-through of hybrid MMC-based HVDC systems," *IEEE Trans. Power Del.*, vol. 30, no. 3, pp. 1298–1306, Jun. 2015.

[21] S. Cui, S. Kim, J.-J. Jung, and S.-K. Sul, "Principle, control and comparison of modular multilevel converters (MMCs) with DC short circuit fault ride-through capability," in *Proc. 29th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2014, pp. 610–616.

[22] S. Cui and S.-K. Sul, "A comprehensive DC short-circuit fault ride through strategy of hybrid modular multilevel converters (MMCs) for overhead line transmission," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7780–7796, Nov. 2016.

[23] R. Picas, J. Pou, S. Ceballos, V. G. Agelidis, and M. Saeedifard, "Minimization of the capacitor voltage fluctuations of a modular multilevel converter by circulating current control," in *Proc. IEEE IECON*, Montreal, QC, Canada, Oct. 2012, pp. 4985–4991.

[24] M. Vasiladiotis, N. Cherix, and A. Rufer, "Accurate capacitor voltage ripple estimation and current control considerations for grid-connected modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4568–4579, Sep. 2014.

[25] J. Pou, S. Ceballos, G. Konstantinou, V. G. Agelidis, R. Picas, and J. Zaragoza, "Circulating current injection methods based on instantaneous information for the modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 777–788, Feb. 2015.

[26] B. Li, Y. Zhang, G. Wang, W. Sun, D. Xu, and W. Wang, "A modified modular multilevel converter with reduced capacitor voltage fluctuation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6108–6119, Oct. 2015.

[27] S. P. Engel and R. W. De Doncker, "Control of the modular multi-level converter for minimized cell capacitance," in *Proc. EPE*, Birmingham, U.K., Aug. 2011, pp. 1–10.

[28] A. J. Korn, M. Winkelnkemper, and P. Steimer, "Low output frequency operation of the modular multi-level converter," in *Proc. IEEE ECCE*, Atlanta, GA, USA, Sep. 2010, pp. 3993–3997.

[29] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation-suppression methods of floating capacitors in a new modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1943–1954, May 2013.

[30] M. Hagiwara, I. Hasegawa, and H. Akagi, "Start-up and low-speed operation of an electric motor driven by a modular multilevel cascade inverter," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1556–1565, Jul. 2013.

[31] L. Baruschka and A. Mertens, "Comparison of cascaded H-bridge and modular multilevel converters for BESS application," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 909–916.

[32] K. Ilves, S. Norrga, and H.-P. Nee, "On energy variations in modular multilevel converters with full-bridge submodules for AC-DC and AC-AC applications," in *Proc. 15th Eur. Conf. Power Electron. Appl. (EPE)*, Sep. 2013, pp. 1–10.

[33] C. Zhao, Y. Li, Z. Li, P. Wang, X. Ma, and Y. Luo, "Optimized design of full-bridge modular multilevel converter with low energy storage requirements for HVDC transmission system," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 97–109, Jan. 2018.

[34] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 77–88, Jan. 2014.

[35] Z. Xu, H. Xiao, and Z. Zhang, "Selection methods of main circuit parameters for modular multilevel converters," *IET Renew. Power Gener.*, vol. 10, no. 6, pp. 788–797, Jan. 2016.

[36] M. M. C. Merlin and T. C. Green, "Cell capacitor sizing in multilevel converters: Cases of the modular multilevel converter and alternate arm converter," *IET Power Electron.*, vol. 8, no. 3, pp. 350–360, Mar. 2015.

[37] P. S. Jones and C. C. Davidson, "Calculation of power losses for MMC-based VSC HVDC stations," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2013, pp. 1–10.

[38] P. Dong, X. Cai, and J. Lyu, "Control strategy of MMC-HVDC system under asymmetric AC grid conditions," in *Proc. CSEE*, Jun. 2018, pp. 1–12, doi: 10.13334/j.0258-8013.pcsee.171765.

PENG DONG received the B.Eng. degree in electronical engineering from the China University of Mining and Technology, Xuzhou, Jiangsu, China, in 2013. He is currently pursuing the Ph.D. degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China.

His current interests include modeling and control of modular multilevel converter and high-power electronics.

JING LYU received the B.Eng. degree in electrical engineering and automation from the China University of Mining and Technology, Xuzhou, Jiangsu, China, in 2009, and the M.Eng. and Ph.D. degrees in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2011 and 2016, respectively.

He was a Research Fellow with the Department of Engineering Cybernetics, Norwegian University of Science and Technology, Trondheim, Norway, from 2016 to 2017. He is currently an Assistant Professor with the Department of Electrical Engineering, Shanghai Jiao Tong University. His current research interests include dynamic stability of MMC-based HVDC connected wind farms/PV plants, modeling and control of modular multilevel converter, wind power converters, and impedance modeling.

XU CAI received the B.Eng. degree from Southeast University, Nanjing, China, in 1983, and the M.Sc. and Ph.D. degree from the China University of Mining and Technology, Xuzhou, Jiangsu, China, in 1988 and 2000, respectively.

He was with the Department of Electrical Engineering, China University of Mining and Technology, as an Associate Professor from 1989 to 2001. He joined Shanghai Jiao Tong University as a professor in 2002, where he has been the Director of the Wind Power Research Center since 2008. He was the Vice Director with the State Energy Smart Grid R&D Center, Shanghai, from 2010 to 2013. His special fields of interest lie in power electronics and renewable energy exploitation and utilization, including wind power converters, wind turbine control system, large power battery storage systems, clustering of wind farms and its control system, and grid integration.

● ● ●