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Analysis of Cu-Graphene Interconnects

ZI-HAN CHENG[1], WEN-SHENG ZHAO[1], (Senior Member, IEEE), DA-WEI WANG[2], JING WANG[1], LINXI DONG[1], GAOFENG WANG[1], (Senior Member, IEEE), AND WEN-YAN YIN[2], (Fellow, IEEE)

[1]MOE Key Laboratory of RF Circuits and Systems, School of Electronics and Information, Hangzhou Dianzi University, Hangzhou 310018, China
[2]Zhejiang Provincial Key Laboratory of Advanced Micro-Nano Electronic Devices and Smart Systems, Innovative Institute of Electromagnetic Information and Electronic Integration, Zhejiang University, Hangzhou 310018, China

Corresponding authors: Wen-Sheng Zhao (wsh.zhao@gmail.com) and Gaofeng Wang (gaofeng@hdu.edu.cn)

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ABSTRACT Due to its ultrathin feature, graphene has been recently proposed as diffusion barrier layer for Cu wires. This paper is geared toward developing an equivalent single-conductor (ESC) transmission-line (TL) model for analysis of Cu-graphene interconnects, i.e., Cu wires encapsulated with graphene barriers. Based on the ESC TL model, electrical performances of Cu-graphene interconnects are examined and evaluated. It is shown that the time delay and temperature rise can be reduced by replacing the conventional diffusion barriers in the Cu/low-k interconnect with the graphene barriers.

INDEX TERMS Cu-graphene interconnect, diffusion barrier layer, equivalent single-conductor (ESC) model, transfer function, time delay.

I. INTRODUCTION

Unlike transistors, the scaling of interconnect dimensions into the nanometer regime leads to a dramatic rise in Cu resistivity and a concomitant performance degradation [1], [2]. At the current technology node, the Cu effective resistivity is several times higher than its bulk value, and the interconnect delay is dominant over the gate delay.

To cope with the dominant interconnect effects, alternative materials and technologies have been continuously explored. For instance, graphene was proposed as a promising candidate, and efforts on the development of graphene interconnects were exerted on the aspects of either modeling or fabrication [3]–[7]. In order to reduce the graphene resistance, few- and multi-layer graphene materials (FLG and MLG) were used for building on-chip interconnects [8]. However, the thickness of MLG, even produced by the state-of-the art technologies, cannot satisfy the requirements, in particular, for global levels. Moreover, graphene tends to behave more like graphite as the number of layer increases [9], [10]. As these innovative solutions are immature, the conventional Cu/low-k interconnect technology may be still the most foreseeable choice for the near future technology nodes [11].

It is known that a highly resistive diffusion barrier layer can adversely reduce the effective area of conduction, and this negative impact worsens with shrinking dimensions. Hence, the barrier layer has a growing influence on the Cu effective resistivity and ultimately on the chip performance [1]. It is essential to fabricate low resistivity and ultrathin barrier layer around the Cu interconnect [12]. However, depositing an ultrathin barrier layer remains a critical challenge, and currently, the related materials and techniques to fabricate a barrier layer with thickness less than 2 nm are still challenging.

Two-dimensional (2-D) materials, including graphene, hexagonal boron nitride and molybdenum disulfide, were proposed as excellent candidates for ultimate Cu diffusion barrier layer [13]–[18]. It was experimentally found that tri-layer graphene barrier layer exhibits excellent thermal stability up to 750 °C [14]. Furthermore, the intrinsic barrier performance of 1-3 layer graphene was investigated by time-dependent dielectric breakdown (TDDB) tests [15], [18]. A lumped-element resistance network model of the Cu wire encapsulated with graphene barriers (i.e., the Cu-graphene interconnect) was presented in an earlier work [19]. Such interconnects were successfully realized [20], and it was demonstrated that the performances and reliability of the Cu wire can be enhanced by employing the graphene barriers [21]–[23]. More recently, a transfer-free and low temperature plasma-enhanced chemical vapor deposition process was developed in [24] to deposit graphene barrier directly on dielectrics, which greatly promotes this interconnect scheme

in the practical applications. As the low-temperature deposition techniques for producing graphene on Cu and dielectric have been developed [20], [17], [24], the fabrication of the Cu-graphene interconnects can be presumably compatible to the CMOS technology. In order to obtain in-depth understanding of the Cu-graphene interconnect, the electrical and thermal performance evaluation and the signal transmission analysis are needed, which is the main motivation behind this study.

The rest of this paper is organized as follows. Section II briefly describes the Cu-graphene interconnect, and an equivalent single-conductor (ESC) transmission line (TL) model is developed. Section III examines the effective resistivity of the Cu-graphene interconnect in comparison with its Cu counterpart. Then, comparative analyses of delay and bandwidth of the Cu-graphene interconnects with various physical parameters are carried out by virtue of a driver-interconnect-load (DIL) system. Section IV focuses on the signal transmission performance of coupled Cu-graphene interconnects. The electrothermal characteristics of the Cu-graphene interconnects are captured and investigated in Section V. Finally, Section VI draws some conclusions.

II. CIRCUIT MODEL

Fig. 1(a) shows a typical interconnect structure. In this figure, w and t represent the interconnect width and thickness, respectively, s is the spacing between adjacent interconnects, and h is the interlayer dielectric (ILD) thickness. The relative permittivity of the medium surrounding the conductor is denoted by ε_r. Here, it is assumed that $s = w$. Fig. 1(b) shows the schematic of Cu-graphene interconnect, i.e., Cu wire encapsulated with graphene layers. Herein, w_{Cu} $(= w-2t_g)$ and t_{Cu} $(= t-2t_g)$ are the effective width and thickness of the central Cu wire, respectively. Without loss of generality, the layer number of the surrounding graphene barriers is set as N, and the graphene thickness is $t_g = N\delta$, where the interlayer spacing δ is 0.34 nm, i.e., van der Waal's gap.

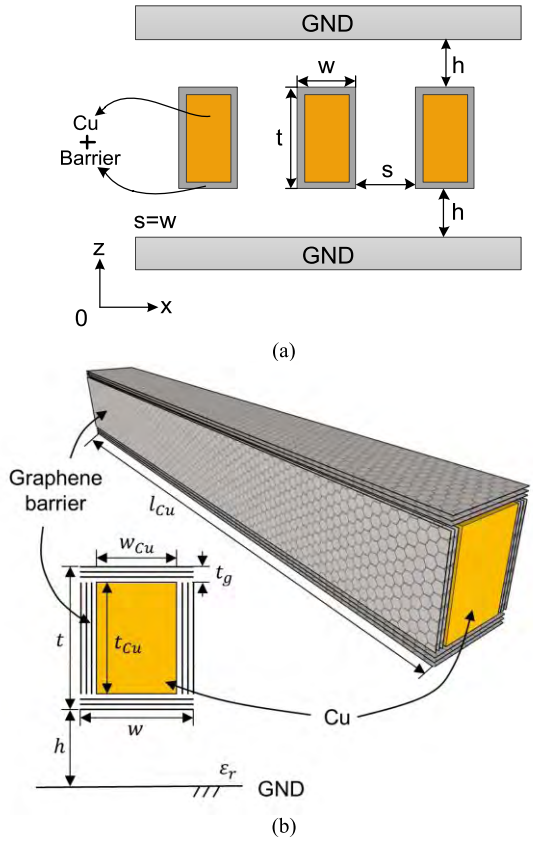

FIGURE 1. (a) Cross section of a typical interconnect structure. (b) Schematic of Cu-graphene interconnect.

The resistance network of Cu-graphene interconnect has been established in an earlier work [19], with the contact resistance between the central Cu wire and the graphene barriers being treated appropriately. It was demonstrated that the graphene barriers can help electrical conduction. With the increasing length, the contact resistance between Cu and the graphene barriers decreases. Once the length is beyond several tens of micrometers, the central Cu wire and the graphene barriers can be treated as being parallel connected at both ends. Hence, the impacts of length and contact on the electrical conduction are negligible. Under such circumstances, the Cu-graphene interconnect can be modeled with an ESC TL model, as shown in Fig. 2. In Fig. 2, R_d and C_d represent the driver resistance and the driver capacitance respectively, C_L is the load capacitance, V_{in} and V_{out} are the input and output voltages respectively, and R_{ESC}, L_{ESC}, and C_{ESC} are the per-unit-length (p.u.l.) ESC equivalent resistance, inductance, and capacitance of the Cu-graphene interconnect respectively.

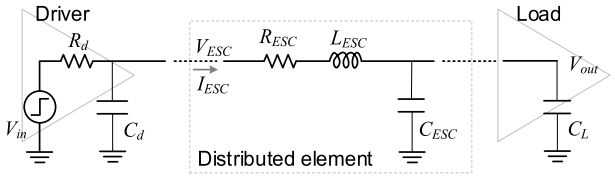

FIGURE 2. A driver-interconnect-load (DIL) system.

At any abscissa, the voltage and current in the ESC TL model satisfy [25]

$$V_{\mathrm{ESC}} = V_{\mathrm{Cu}} = V^j(i), j = t, b, l, \quad \text{and } r \tag{1}$$

$$I_{\mathrm{ESC}} = I_{\mathrm{Cu}} + \sum\nolimits_{j=t,b,l,r} \sum\nolimits_{i\in[1,N]} I^j(i) \tag{2}$$

where V_{Cu} and I_{Cu} are the voltage and the current of the central Cu respectively, and the superscripts t, b, l, and r represent the respective corresponding quantities when the graphene barrier layers on the top, bottom, left, and right surfaces of the Cu wire are considered. According to the measurements [26], [27], the central Cu wire and the graphene barriers can be assumed to be decoupled.

A. ESC RESISTANCE

The p.u.l. ESC resistance can be calculated by

$$R_{\mathrm{ESC}} = \left(\frac{1}{R_{\mathrm{Cu}}} + N \sum\nolimits_{j=t,b,l,r} \frac{1}{R_{\mathrm{gr}}^{j}} \right)^{-1} \tag{3}$$

where R_{Cu} and R_{gr}^{j} ($j = t$, b, l, and r) are the p.u.l. resistances of the central Cu and the surrounding graphene barriers, respectively. The interactions between the edges of the graphene barriers are neglected in the model as graphene is a typical anisotropic material, and its out-of-plane electrical conductivity is usually 1000 times lower than its in-plane value.

The resistance of the central Cu wire can be calculated by

$$R_{\mathrm{Cu}} = \frac{\rho_{\mathrm{Cu}}}{w_{\mathrm{Cu}} t_{\mathrm{Cu}}} \tag{4}$$

ρ_{Cu} is the effective Cu resistivity, and it can be described by the Mayadas-Shatzkes model [2]

$$\rho_{\mathrm{Cu}} = \rho_0 \left\{ \left[1 - 1.5\alpha + 3\alpha^2 - 3\alpha^3 \ln\left(1 + \frac{1}{\alpha} \right) \right]^{-1} + 0.45 \lambda_{\mathrm{Cu}} \left(1 - p_{\mathrm{Cu}} \right) \frac{w_{\mathrm{Cu}} + t_{\mathrm{Cu}}}{w_{\mathrm{Cu}} t_{\mathrm{Cu}}} \right\} \tag{5}$$

where ρ_0 is the Cu bulk resistivity, $\alpha = \lambda_{\mathrm{Cu}} R_f / \left[d_g \left(1 - R_f \right) \right]$ is a dimensionless parameter, p_{Cu} is the specularity parameter of the Cu wire (0 for fully diffusive and 1 for fully specular surfaces), λ_{Cu} is the electron mean free path (MFP) of the Cu wire, d_g is the average grain size, and R_f is the grain-boundary reflection coefficient. The Cu bulk resistivity ρ_0 can be written as [28]

$$\rho_0 = A \left(1 + \frac{BT}{\theta - CT} + D \left(\frac{\theta - CT}{T} \right)^{m} \right) \varphi \left(\frac{\theta - CT}{T} \right) \tag{6}$$

where T is the temperature, $m = 1.84$, $\theta = 310.8\mathrm{K}$, $A = 1.809 \times 10^{-8} \Omega \cdot m$, $B = -5.999 \times 10^{-3}$, $C = 0.0456 \times 10^{-3}$, $D = -6.476 \times 10^{-4}$, and the function φ is specified as

$$\varphi \left(\frac{\theta - CT}{T} \right) = 4 \left(\frac{\theta - CT}{T} \right)^{-5} \int_0^{\frac{\theta - CT}{T}} x^5 e^x \left(e^x - 1 \right)^{-2} \mathrm{d}x \tag{7}$$

The electron mean free path (MFP) of the Cu wire can be determined by $\lambda_{\mathrm{Cu}} = 6.6 \times 10^{-16} / \rho_0$ according to the theory of the electron gas.

For the graphene barriers with fully specular edges, i.e., the specularity parameter of the graphene p_{gr} is 1, the p.u.l. resistance can be given by [8]

$$R_{\mathrm{gr}} = \frac{h}{2e^2} \frac{1}{N_{ch}} \left(\frac{1}{l_{\mathrm{Cu}}} + \frac{1}{\lambda_{\mathrm{eff}}} \right) \tag{8}$$

where h is the Planck's constant, e is the electron charge, λ_{eff} is the effective electron MFP in the graphene, N_{ch} is the number of conducting channels, and l_{Cu} denotes the wire length. Note that the quantum contact resistances of the graphene barriers have been considered in (8). However, λ_{eff} decreases as p_{gr} decreases. For the graphene barriers with $p_{\mathrm{gr}} < 1$, the p.u.l. resistance can be calculated by

$$R_{\mathrm{gr}} = \frac{h}{2e^2} \frac{1}{N_{\mathrm{ch}}} \left[\sum\nolimits_i \left(\frac{1}{l_{\mathrm{Cu}}} + \frac{1}{\lambda_{i,\mathrm{eff}}} \right) \right]^{-1} \tag{9}$$

where $\lambda_{i,\mathrm{eff}}$ denotes the effective electron MFP of the ith conduction channel in graphene. The number of conducting channels N_{ch} can be obtained by adding the contributions of each conduction or valence subband [3]

$$N_{\mathrm{ch}} = \sum\nolimits_i \left(1 + \mathrm{e}^{\frac{E_i - E_F}{k_B T}} \right)^{-1} + \sum\nolimits_i \left(1 + \mathrm{e}^{\frac{E_i + E_F}{k_B T}} \right)^{-1} \tag{10}$$

where E_F is the Fermi energy and k_B is the Boltzmann's constant. Note that n-type doping and a shifted $|E_F|$ of $\sim$0.5 eV were experimentally observed in the graphene grown on Cu [29], [30]. Although E_F decreases with the distance from the Cu-carbon interface due to the interlayer screening effect [31], several doping techniques (e.g., edge doping [32]) have been continuously developed and therefore, $|E_F|$ is kept as 0.5 eV unless otherwise stated.

The effective MFP of the graphene barrier highly depends on the defects, substrate, and graphene edges. According to the Mattheissen's rule, the electron MFP of the ith conduction channel can be obtained by [4]

$$\lambda_{i,\mathrm{eff}} = \left(\frac{1}{\lambda_{i,\mathrm{edge}}} + \frac{1}{\lambda_{\mathrm{ac}}} + \frac{1}{\lambda_{\mathrm{op}}} + \frac{1}{\lambda_{\mathrm{ci}}} + \frac{1}{\lambda_{\mathrm{SPP}}} + \frac{1}{\lambda_{\mathrm{rs}}} \right)^{-1} \tag{11}$$

The edge scattering limited MFP $\lambda_{i,\mathrm{edge}}$ can be given by [3]

$$\lambda_{i,\mathrm{edge}} = \frac{w_{\mathrm{gr}}}{1 - p_{\mathrm{gr}}} \sqrt{ \left(\frac{2 w_{\mathrm{gr}} E_F}{i h v_F} \right)^2 - 1 } \tag{12}$$

where w_{gr} is the width of the graphene barrier and v_F is the Fermi velocity. Herein, fully diffusive edges (i.e., $p_{\mathrm{gr}} = 0$) are assumed for the graphene barriers. The electron MFP in graphene due to acoustic phonons λ_{ac} is given as [33]

$$\lambda_{\mathrm{ac}} = \frac{\rho_m \left(\hbar v_F v_s \right)^2}{k_B T D_{\mathrm{ac}}^2 \sqrt{\pi N_s}} \tag{13}$$

where ρ_m ($= 7.66 \times 10^{-7} \mathrm{kg/m^2}$) is the 2-D mass density of graphene, v_s is the speed of acoustic phonons, N_s is the concentration of 2-D electron gas in graphene, and D_{ac} is the acoustic deformation potential.

The effect of the optical phonons on the electron MFP can be calculated according to [33]

$$\lambda_{\mathrm{op}} = \frac{\hbar \omega_{\mathrm{op}} \rho_m v_F^2}{2 N_{\mathrm{op}} D_{\mathrm{op}}^2 \sqrt{\pi N_s}} \tag{14}$$

where $\hbar\omega_{\mathrm{op}}$ ($= 160\mathrm{meV}$) is the optical phonon energy, D_{op} ($= 2.24 \times 10^9 \mathrm{eV/m}$) is the effective electron-optical phonon coupling, and N_{op} is the phonon occupation numbers given by Bose-Einstein statics.

The electron MFP due to the charged-impurity scatterings is given by [4], [35]

$$\lambda_{\rm ci} = \frac{16\sqrt{\pi N_s}}{N_{\rm ci}} \left(\frac{\hbar v_F \varepsilon_0 \varepsilon}{Ze^2}\right)^2 \left(1 + \frac{e^2}{\pi \hbar v_F \varepsilon_0 \varepsilon}\right)^2 \quad (15)$$

where ε_0 is the permittivity in vacuum, ε is the average between the relative permittivity of the substrate and vacuum, Ze is the net charge of the impurity, and $N_{\rm ci}$ is the density of the impurity.

The electron MFP due to the surface polar phonon (SPP) scatterings is approximated by [4], [33]

$$\lambda_{\rm SPP} = \left(\sum\nolimits_{i=1,2} \frac{1}{\lambda_{{\rm SPP},i}}\right)^{-1} = \left[\sum\nolimits_{i=1,2} \left(\sqrt{\frac{\beta}{E_i}} \frac{\hbar v_F 4\pi\varepsilon_0}{e^2} \frac{e v_F}{F_i^2} \frac{e^{k_0 z_0}}{N_{{\rm SPP},i}} \frac{\hbar\sqrt{\pi}}{e}\right)^{-1}\right]^{-1} \quad (16)$$

where $\beta \approx 0.153 \times 10^{-4}$eV, $z_0 = 0.35$nm is the separation between the graphene sheet and the substrate, $k_0 \approx \sqrt{[2E_i/(\hbar v_F)]^2 + \alpha N_s}$, $\alpha \approx 10.5$, and $N_{{\rm SPP},i}$ and F_i^2 are the Bose-Einstein filling number and Froehlich constant of the ith mode respectively. Assuming the silicon dioxide dielectric is employed, v_s, N_s, D_{ac}, ε, $N_{ci}E_1$ (E_2), and F_1^2 (F_2^2) are 17.3km/s, 10^{12}cm^{-2}, 7.1eV, 2.4, 1.5×10^{11}cm^{-2}, 58.9meV (156.4meV), and 0.237meV (1.612meV), respectively [34].

The electron MFP due to the scatterings with resonant scatterers is given by [33]

$$\lambda_{\rm rs} = \frac{\sqrt{\pi N_s}}{\pi^2 N_{\rm rs}} \left[\ln\left(2a\sqrt{\pi N_s}\right)\right]^2 \quad (17)$$

where $N_{\rm rs} = 10^{10}$cm^{-2} is the concentration of the resonant scatterers and a is the bond length of graphene. Due to the charged impurity and scatterings, the net electron MFP of the graphene placing on SiO_2 substrate at 300 K is calculated to be 100.83 nm, which is much smaller than the MFP of suspending graphene ($\sim 1\ \mu$m).

B. ESC CAPACITANCE/INDUCTANCE

Fig. 3 shows the p.u.l. equivalent capacitance and inductance networks of the Cu-graphene interconnect. Taking the graphene barriers placed on the top surface for example, the parasitic circuit elements in Fig. 3 are summarized in Table 1. The elements for the other surfaces can be calculated similarly. A separation of $\delta_1 = 0.155$ nm is considered between the carbon and Cu atoms according to [36].

The p.u.l. electrostatic capacitance C_e can be given by

$$C_e = C_{\rm plate} + 2C_{\rm lowerterminal} + 2C_{\rm fringe} + 2C_{\rm upperterminal} \quad (18)$$

where $C_{\rm plate}$, $C_{\rm lowerterminal}$, $C_{\rm fringe}$ and $C_{\rm upperterminal}$ are the four major components defined in [37]. The p.u.l. magnetic inductance can be obtained by $L_e = \mu_0\varepsilon_0\varepsilon_r/C_e$. For the

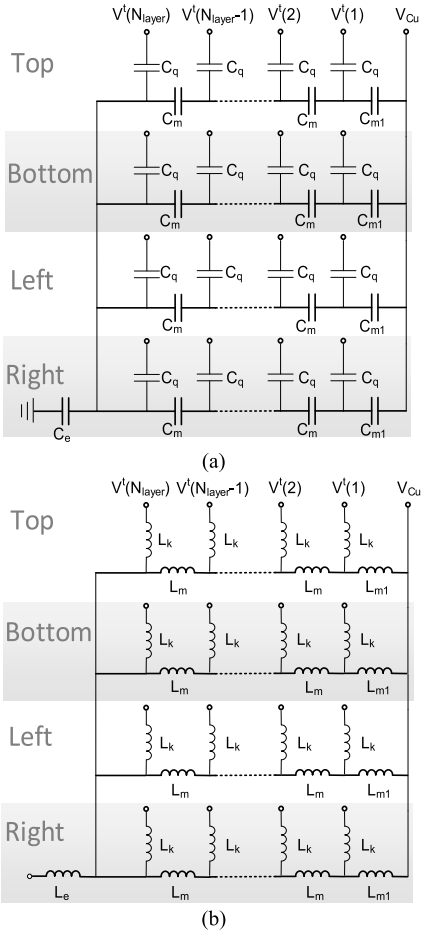

FIGURE 3. Per-unit-length (a) capacitance and (b) inductance networks of Cu-graphene interconnect..

TABLE 1. Distributed circuit parasitic elements in Fig. 3.

Comp.	Description	Model
C_q^t	Quantum capacitance of graphene layer	$200N_{ch}$ aF/μm
L_q^t	Kinetic inductance of graphene layer	$8/N_{ch}$ nH/μm
C_m^t	Electrostatic mutual capacitance between adjacent graphene layers	$\varepsilon_0 w/\delta$
L_m^t	Magnetic mutual inductance between adjacent graphene layers	$\mu_0\delta/w$
C_{m1}^t	Electrostatic mutual capacitance between Cu and graphene layer	$\varepsilon_0 w_{Cu}/\delta_1$
L_{m1}^t	Magnetic mutual inductance between Cu and graphene layer	$\mu_0\delta_1/w_{Cu}$

Cu-graphene interconnect, the p.u.l. equivalent capacitance $C_{\rm ESC}$ and equivalent inductance $L_{\rm ESC}$ can be calculated by

$$C_{\rm ESC} = \left[\left(\sum\nolimits_{j=t,b,l,r} C_{\rm rec}^j\right)^{-1} + \frac{1}{C_e}\right]^{-1} \quad (19)$$

$$L_{\rm ESC} = \left(\sum\nolimits_{j=t,b,l,r} \frac{1}{L_{\rm rec}^j}\right)^{-1} + L_e \quad (20)$$

As given in (1), the Cu wire and graphene layers are assumed to be at the same potential. $C_{\rm rec}$ and $L_{\rm rec}$ can be obtained by

applying the recursive scheme as follows [8], [25],

$$C_{\text{rec}}^{j} = C_{\text{rec}}^{N} \tag{21}$$

$$C_{\text{rec}}^{1} = C_{m1}^{j} + C_{q}^{j} \tag{22}$$

$$C_{\text{rec}}^{i} = \left[\frac{1}{C_{\text{rec}}^{i-1}} + \frac{1}{C_{m}^{j}}\right]^{-1} + C_{q}^{j}, \quad i \in [2, N] \tag{23}$$

$$L_{\text{rec}}^{j} = L_{\text{rec}}^{N} \tag{24}$$

$$L_{\text{rec}}^{1} = \left(\frac{1}{L_{m1}^{j}} + \frac{1}{L_{k}^{j}}\right)^{-1} \tag{25}$$

$$L_{\text{rec}}^{i} = \left[\frac{1}{L_{\text{rec}}^{i-1} + L_{m}^{j}} + \frac{1}{L_{k}^{j}}\right]^{-1}, \quad i \in [2, N] \tag{26}$$

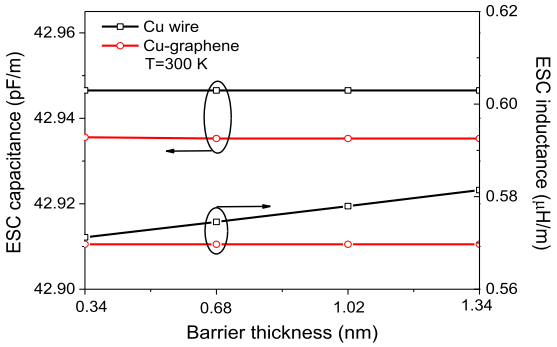

FIGURE 4. Per-unit-length ESC capacitance and ESC inductance versus barrier layer thickness at the 22 nm node.

Fig. 4 shows the p.u.l. capacitance and inductance of the Cu and Cu-graphene interconnects as functions of the barrier thickness. Here, the interconnect width and the ILD thickness are 22 nm and 39.6 nm, respectively. It is found that the capacitance is almost unchanged with the barrier thickness, while the effective inductance of the Cu-graphene interconnect appears a trend of rise with the increasing barrier thickness due to the influence of graphene kinetic inductance.

III. SIGNAL TRANSMISSION ANALYSIS

A. EFFECTIVE RESISTIVITY

Fig. 5(a) depicts the effective resistivity of the Cu-graphene interconnects versus the temperature under various barrier thicknesses in comparison to their Cu counterparts. In this figure, the used parameters are as follows: $w = 22$ nm, $t = 44$ nm, $h = 39.6$ nm, and $l_{\text{Cu}} = 1000$ μm. According to the ITRS prediction, as the interconnect width scales down to 22 nm, the barrier thickness of the Cu wire should reach 1.3 nm [12]. However, as the ITRS predictions for the barrier thickness are usually too optimistic and too challenging to achieve, the Cu wires with barrier thicknesses of 1.3 nm and 2×1.3 nm are considered as references [38]. As experimentally demonstrated in [20], by growing the graphene barrier thickness, the specularity parameter p_{Cu} of the Cu wire can increase from 0 to 0.23. In addition to reducing the surface scatterings, the capping of the graphene barriers on Cu can also increase the grain size [20], [22]. Yet it is not the main focus of the present work, d_g is herein assumed as w_{Cu}.

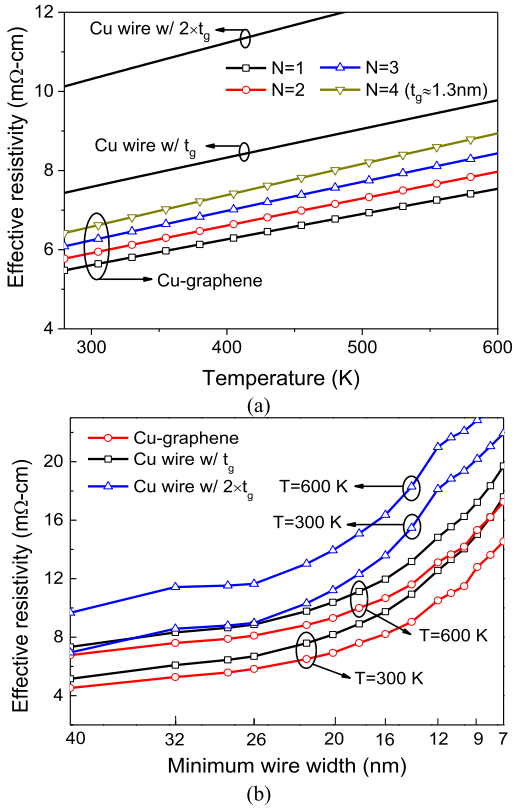

FIGURE 5. Effective resistivity of Cu and Cu-graphene interconnects versus (a) temperature and (b) technology nodes.

It can be observed from Fig. 5(a) that both the effective resistivities of the Cu and Cu-graphene interconnects increase linearly with the temperature. By introducing the graphene barriers, the effective resistivity can be significantly reduced. Although graphene can provide more conduction channels, increasing the graphene thickness would reduce the effective conduction area of the central Cu wire, thereby leading to increased resistivity. Furthermore, the effective resistivities of the Cu and Cu-graphene interconnects versus the technology node are plotted in Fig. 5(b). In this figure, the barrier thickness t_g at each technology node is selected from the ITRS prediction [12]. It can be seen that the advantage of the Cu-graphene interconnects over the conventional Cu wires become more salient as the technology is scaling down.

B. TIME DELAY

After extracting the circuit parameters in Fig. 2, 50% time delay of the DIL system can be calculated by [8]

$$\tau = \left(1.48\xi + \mathrm{e}^{-2.9\xi^{1.35}}\right)\sqrt{L_{\text{ESC}} l_{\text{Cu}} \left(C_{\text{ESC}} l_{\text{Cu}} + C_L\right)} \tag{27}$$

where

$$\xi = \frac{1}{2}\left[L_{\text{ESC}}\left(C_{\text{ESC}} + \frac{C_L}{l_{\text{Cu}}}\right)\right]^{-0.5} \times \left[\left(\frac{1}{2}R_{\text{ESC}} l_{\text{Cu}} + R_d\right) C_{\text{ESC}} + \left(R_{\text{ESC}} + \frac{R_d}{l_{\text{Cu}}}\right) C_L\right] \tag{28}$$

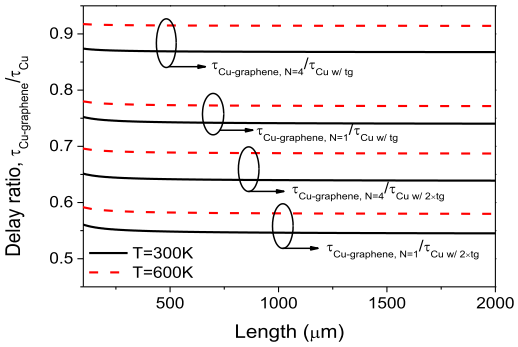

FIGURE 6. Time delay ratios of the Cu-graphene interconnects to their Cu counterparts.

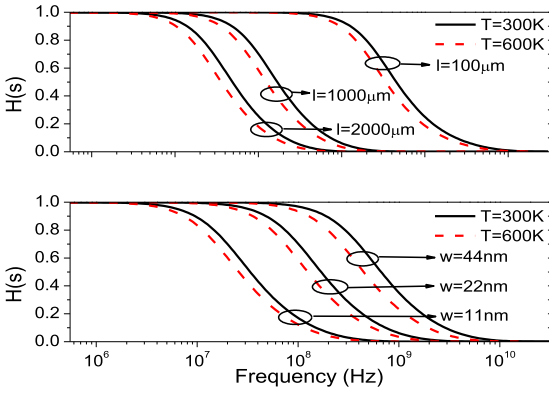

FIGURE 7. Frequency response of Cu-graphene interconnect.

Note that the driver capacitance is not considered in (27). Fig. 6 shows the time delay ratios of the Cu-graphene interconnects to their Cu counterparts. The parameters are the same as those used for producing Fig. 5(a). It can be seen that the time delay can be significantly reduced by employing the graphene barriers, and such enhancement can be further strengthened by reducing the graphene barrier thickness.

C. FREQUENCY RESPONSE

Based on the DIL system in Fig. 2, the input and output parameters can be expressed as [39]

$$\begin{bmatrix} V_{\text{in}} \\ I_{\text{in}} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_{\text{out}} \\ I_{\text{out}} \end{bmatrix} \tag{29}$$

with

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & R_d \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ sC_d & 1 \end{bmatrix} \cdot \begin{bmatrix} \cosh(\gamma l_{\text{Cu}}) & Z_0 \sinh(\gamma l_{\text{Cu}}) \\ \sinh(\gamma l_{\text{Cu}})/Z_0 & \cosh(\gamma l_{\text{Cu}}) \end{bmatrix} \tag{30}$$

$$\gamma = \sqrt{(R_{\text{ESC}} + sL_{\text{ESC}})\, sC_{\text{ESC}}} \tag{31}$$

$$Z_0 = \sqrt{\frac{R_{\text{ESC}} + sL_{\text{ESC}}}{sC_{\text{ESC}}}} \tag{32}$$

where $s = j\omega$ is the complex frequency. As $I_{\text{out}} = sC_L V_{\text{out}}$, the transfer function can be given as

$$H(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{A + BI_{\text{out}}/V_{\text{out}}} = \frac{1}{A + sBC_L} \tag{33}$$

Fig. 7 shows the (absolute) frequency responses of the Cu-graphene interconnects with various geometrical parameters. The reference parameters are as follows: $w = 22$nm, $t = 44$nm, $l_{\text{Cu}} = 1000\ \mu$m, $t_g = 1.3$ nm (i.e., $N = 4$), $h = 39.6$ nm, and all the other parameters are the same as those used for producing Fig. 5(a). It is found that the frequency response of the DIL system behaves like a low-pass filter, and the bandwidth is determined by the resistance-capacitance product [39]. As shown in Fig. 7(a), the increase in the length leads to increases in both resistance and capacitance, thereby significantly reducing the bandwidth. With the decreasing width, as shown in Fig. 7(b), the resistance of the Cu-graphene interconnect increases, thereby reducing the cut-off frequency and bandwidth. As illustrated in Fig. 5, the resistance of the Cu-graphene interconnects increases with the temperature. Therefore, the cut-off frequency and bandwidth are degraded at higher temperature.

D. TRANSIENT RESPONSE

After some mathematical manipulations, (33) can be written as

$$H(s) = \left(1 + \sum\nolimits_{i=1}^{6} a_i s^i\right)^{-1} \tag{34}$$

where the coefficients a_i ($i = 1, 2, \ldots,$ and 6) can be obtained from [40]. Hence, the step response in the Laplace domain can be obtained by

$$V_{\text{out}}(s) = V_0 \left(\frac{1}{s} + \sum\nolimits_{i=1}^{6} \frac{k_i}{s - s_i}\right) \tag{35}$$

and the transient step response is given as

$$V_{\text{out}}(t) = V_0 \left(1 + \sum\nolimits_{i=1}^{6} k_i e^{s_i t}\right) \tag{36}$$

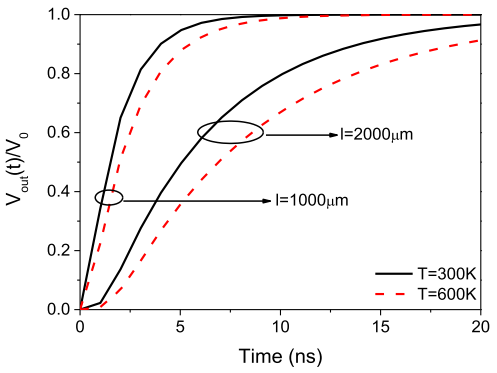

FIGURE 8. Transient step response of Cu-graphene interconnect.

Fig. 8 shows the transient step responses of the Cu-graphene interconnects, computed with various temperatures and lengths. Here, the used parameters are as follows:

$w = 22$ nm, $N = 4$, and $h = 39.6$ nm. It is found that, when the temperature and length increase, the signal transmission performance degrades, thereby resulting in longer time delay.

IV. ANALYSIS OF COUPLED CU-GRAPHENE INTERCONNECTS

Fig. 9 shows the schematic of the coupled Cu-graphene interconnects. Based on the input signals between the coupled interconnects, two phase modes including $k = 1$ and $k = -1$ (i.e., common mode and differential mode) can be decoupled. The ABCD matrix of the coupled Cu-graphene interconnects can be written as (29) with the propagation constant and characteristic impedance being expressed as

$$\gamma = \sqrt{R_{\mathrm{ESC}} + s\left(L_{\mathrm{ESC}} + kL_c\right)} \cdot \sqrt{s\left[C_{\mathrm{ESC}} + (1-k)\,C_c\right]} \tag{37}$$

$$Z_0 = \sqrt{\frac{R_{\mathrm{ESC}} + s\left(L_{\mathrm{ESC}} + kL_c\right)}{s\left[C_{\mathrm{ESC}} + (1-k)\,C_c\right]}} \tag{38}$$

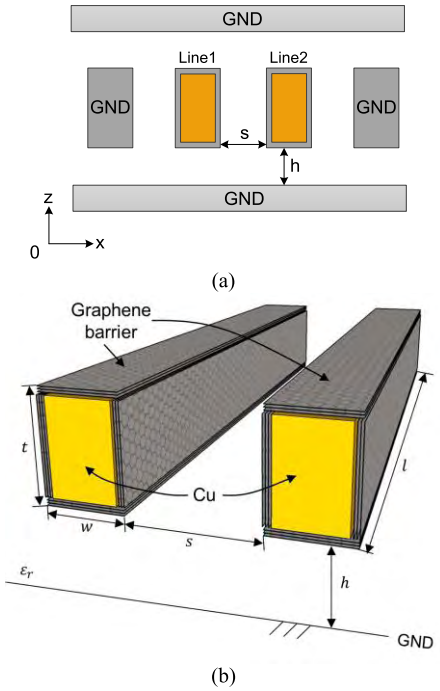

FIGURE 9. (a) Cross section and (b) schematic of coupled Cu-graphene interconnects.

where L_c and C_c are the coupling inductance and capacitance between the coupled interconnects, respectively [37]. Figs. 10 and 11 show the transfer gain and transient waveforms of the coupled Cu-graphene interconnects for different modes. It can be seen that for the $k = -1$ mode, the capacitance increases to $C_{\mathrm{ESC}} + 2C_c$, thereby decreasing the cut-off frequency and bandwidth.

V. ELECTROTHERMAL CHARACTERIZATION

In this section, the electrothermal responses of the Cu and Cu-graphene interconnects are captured and compared.

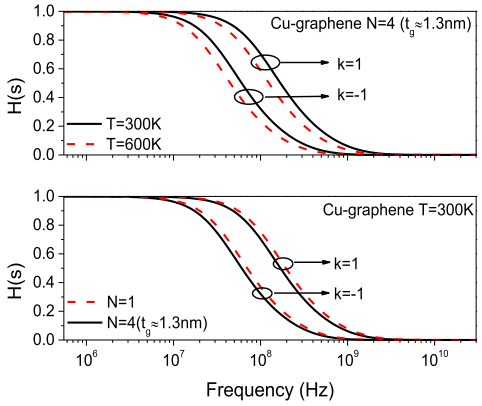

FIGURE 10. Transfer gain of coupled Cu-graphene interconnect.

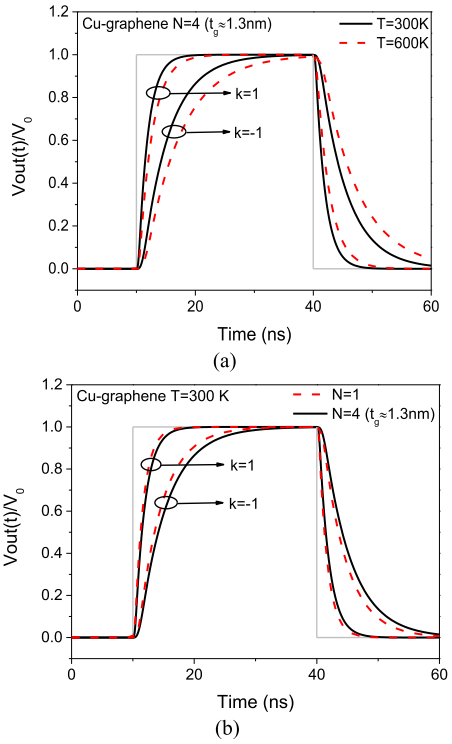

FIGURE 11. Transient waveforms of output voltages of the coupled Cu-graphene interconnects for $k = 1$ and $k = -1$ mode.

As shown in Fig. 12, an interconnect is placed above the SiO_2/Si substrate. Here, the tantalum nitride (TaN) is selected as the barrier layer for the conventional Cu interconnect to prevent atom diffusion into the surrounding dielectric material [41]. A human-metal electrostatic discharge (ESD) current is injected into the interconnect, and its waveform is expressed as [40]

$$i(t) = I_1\left(1 - \mathrm{e}^{-t/\tau_1}\right)^p \mathrm{e}^{-t/\tau_2} + I_2\left(1 - \mathrm{e}^{-t/\tau_3}\right)^q \mathrm{e}^{-t/\tau_4} + I_3\left(1 - \mathrm{e}^{-t/\tau_5}\right)^r \mathrm{e}^{-t/\tau_6} + I_4\left(1 - \mathrm{e}^{-t/\tau_7}\right)^s \mathrm{e}^{-t/\tau_8} \tag{39}$$

where the coefficients from the quadrinomial of pulse function are referred in TABLE 2. The simulation is carried out by

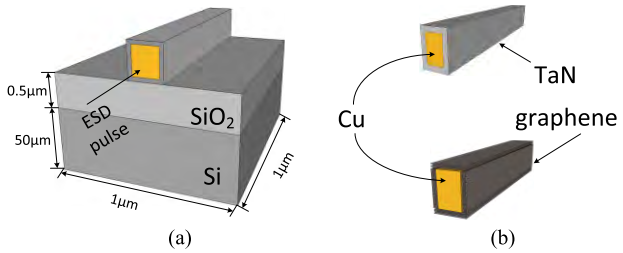

FIGURE 12. (a) Schematic of on-chip interconnect made of (b) Cu-TaN interconnect and Cu-graphene interconnect.

TABLE 2. Parameters of the pulse function.

Amplitude (mA)	Time constant (ns)	Exponential order
$I_1 = 10$	$\tau_1 = 0.641, \tau_5 = 46.62$	$p = 5$
$I_2 = 11.37$	$\tau_2 = 1.640, \tau_6 = 32.08$	$q = 4$
$I_3 = 8.73$	$\tau_3 = 7.144, \tau_7 = 16.71$	$r = 5$
$I_4 = 9.06$	$\tau_4 = 8.254, \tau_8 = 19.75$	$s = 4$

TABLE 3. Physical parameter properties of the materials involved in the simulation [41], [43]–[45].

Materials	Thermal Conductivity (W/m · K)	Density (kg/m^3)	Specific Capacity (J/kg · K)
Cu	400	8700	385
Silicon	155	2300	710
Oxide	1.38	2600	1000
TaN	3.2	14360	205
Graphene	In-plane:5000 Out-plane:10	2000	710

using the COMSOL Multiphysics. The bottom temperature of the Si substrate and the initial temperature are set as 300 K. The physical properties of the materials involved are listed in TABLE 3. For the Cu-TaN interconnects with barrier thicknesses of t_g and $2t_g$, the electrical conductivities are calculated as 1.58×10^7 S/m and 1.44×10^7 S/m, respectively, while it is 1.73×10^7 S/m for the Cu-graphene interconnect. The electrical conductivities of the horizontal and vertical graphene barriers are 4.77×10^6 S/m and 6.29×10^6 S/m, respectively. As reported in [42], the electrical resistivity of TaN ranges from 100 $\mu\Omega\cdot cm$ to $6\times10^6\mu\Omega\cdot$cm, and is chosen to be 10^6 S/m in the simulation herein.

Fig. 13 shows the maximum temperature responses of the Cu and Cu-graphene interconnects in the presence of the ESD pulse. The waveform of the ESD current density is also depicted in Fig. 13 (i.e., the dot-line curve). Here, the interconnect width and thickness are 22 nm and 44 nm, respectively, and the barrier thickness is approximately 1.3 nm. As aforementioned, the ITRS predictions are quite optimistic. Hence, the Cu wire with twice of the ITRS predicted barrier thickness is considered. It is found that the maximum temperatures of the Cu wires with barrier thicknesses of 1.3 nm and 2.6 nm reach 428.7K and 481.4 K, respectively. By utilizing the graphene barriers ($N = 4$), the maximum temperature

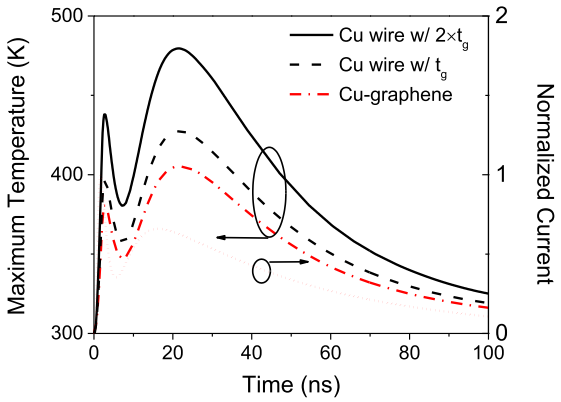

FIGURE 13. Transient maximum temperature of Cu and Cu-graphene interconnects injected with the ESD pulse.

can be reduced to 406.2K. Therefore, it can be concluded that the Cu-graphene interconnects possess superior thermal performance in comparison with the conventional Cu-TaN interconnects. This is attributed to the decreased effective resistivity.

VI. CONCLUSIONS

The Cu-graphene interconnect, which utilizes graphene as the diffusion barrier layer due to its ultrathin nature, was modeled and analyzed. The equivalent single-conductor (ESC) transmission line (TL) model of the Cu-graphene interconnect was proposed, with appropriate treatment of the capacitive and inductive couplings between adjacent graphene layers. The ESC equivalent capacitance and inductance can be extracted by using the recursive scheme. It was found that, after growing the graphene barriers, the capacitance remains almost unchanged, while the inductance slightly increases. Nevertheless, the implantation of the graphene barriers can improve the grain size and the specularity parameter of the central Cu wire, thereby resulting in significant reduction in the effective resistivity. Based on the ESC TL model, the time delays of the Cu-graphene interconnects with various physical and geometrical parameters were obtained and compared with those of their Cu counterparts. It was demonstrated that the time delay can be reduced by replacing the conventional diffusion barriers with the graphene barriers. Such trend can be further strengthened by improving the graphene quality and reducing the barrier thickness. The frequency- and time-domain analyses of the Cu-graphene interconnects were carried out subsequently. Finally, the electrothermal responses of the Cu and Cu-graphene interconnects in the presence of an ESD pulse were captured and studied. By utilizing the graphene barriers, the decreased effective resistivity leads to less Joule heat, thereby significantly reducing the temperature rise.

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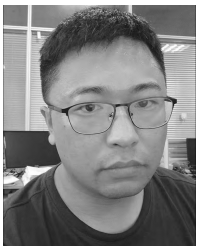
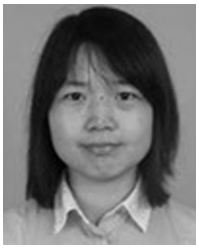
ZI-HAN CHENG received the B.E. degree from Hangzhou Dianzi University, Hangzhou, China, in 2016, where he is currently pursuing the M.E. degree with a focus on interconnect design and modeling for post CMOS electronics.



WEN-SHENG ZHAO (S'09–M'13–SM'18) received the B.E. degree from the Harbin Institute of Technology, Harbin, China, in 2008, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 2013.

He was a Visiting Ph.D. Student with the National University of Singapore, Singapore, from 2010 to 2013, and a Visiting Scholar with the Georgia Institute of Technology, Atlanta, USA, from 2017 to 2018. He is currently an Associate Professor with Hangzhou Dianzi University, Hangzhou, China. He has authored or co-authored a book, three book chapters, and over 80 papers in refereed journals and conference proceedings (including over 30 IEEE journal papers). His current research interests include 3-D integrated circuits, microwave sensor, carbon nanoelectronics, signal and power integrity, multiphysics simulation, and machine learning applications in electronic design.

DA-WEI WANG received the B.E. degree form Jilin University, Changchun, China, in 2010, and the M.E. degree from the China Academy of Telecommunications Technology, Beijing, China, in 2013. He is currently pursuing the Ph.D. degree with Zhejiang University, Hangzhou, China. His current research interests include computational electromagnetics, signal integrity analysis, and multiphysics simulation.



JING WANG received the Ph.D. degrees from the University of Science and Technology of China, Hefei, China, and from the City University of Hong Kong, Hong Kong, in 2014.

She is currently a Faculty Member with Hangzhou Dianzi University, Hangzhou, China. Her current research interests include the design and modeling of tunnel transistors.

LINXI DONG received the Ph.D. degree from Zhejiang University, Hangzhou, China, in 2004.

He is currently a Professor with Hangzhou Dianzi University, Hangzhou, China. His current research interests include the design of MEMS sensors and resonators, including the design, modeling, and fabrication of microstructures.

GAOFENG WANG (S'93–M'95–SM'01) received the Ph.D. degree in electrical engineering from the University of Wisconsin–Milwaukee, WI, USA, and the Ph.D. degree in scientific computing from Stanford University, CA, USA, in 1993 and 2001, respectively.

From 1993 to 1996, he was a Scientist at Tanner Research Inc., Pasadena, CA, USA. From 1996 to 2001, he was a Principal Research and a Development Engineer at Synopsys Inc., Mountain View, CA, USA. In the summer of 1999, he served as a Consultant at Bell Laboratories, Murray Hill, NJ, USA. From 2001 to 2003, he was the Chief Technology Officer (CTO) at Intpax, Inc., San Jose, CA, USA. From 2004 to 2010, he was the CTO at Siargo, Inc., Santa Clara, CA, USA. From 2004 to 2013, he was a Professor and the Head of the CJ Huang Information Technology Research Institute, Wuhan University, Wuhan, China. From 2010 to 2013, he was a Chief Scientist with Lorentz Solution, Inc., Santa Clara. He is currently a Distinguished Professor with Hangzhou Dianzi University, Hangzhou, China. He has over 200 peer-reviewed journal articles and holds 30 patents. His current research interests include integrated circuit and microelectromechanical system design and simulation, computational electromagnetics, electronic design automation, and wavelet applications in engineering.

WEN-YAN YIN (M'99–SM'01–F'13) received the M.Sc. degree in electromagnetic field and microwave technique from Xidian University, Xi'an, China, in 1989, and the Ph.D. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, in 1994.

Since 2009, he has been a Distinguished Professor with Zhejiang University, Hangzhou, China. His current research interests include the fields of EMC and EM protection for electronic systems and platforms, computational electromagnetics and multiphysics, 3-D ICs, advanced packaging, and nanoelectronics.