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Reliable and *Q*-Enhanced Floating Active Inductors and Their Application in RF Bandpass Filters

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ABSTRACT This paper presents three new floating active inductor (FAI)-based bandpass filter (BPF) topologies, namely, the nominal-*Q* BPF (NQF), *Q*-enhanced BPF-1 (QF_1), and *Q*-enhanced BPF-2 (QF_2). The filters utilize voltage differencing transconductance amplifier (VDTA) as an active building block and are implemented in a 45-nm CMOS process. Negative resistance techniques are used to enhance the quality factor and an addition-based current reference technique reduces the sensitivity of filter's design metrics to process, voltage, and temperature (PVT) variations. The performances of the filters are analyzed in the presence of parasitics and analytical expressions are derived. The proposed filters consume minimal power, possess a high *Q* and good dynamic range, and are reliable despite being implemented in the nanoscale regime. The NQF/QF_1/QF_2 exhibits a center frequency of 4.36/3.63/3.02 GHz, quality factor of 17.84/54/46.2, the 3-dB bandwidth of 244.4/67.22/65.36 MHz, the dynamic range of 122.49/118.58/119.46 dB, and a 1-dB compression point of −3.06/−5.48/−5.45 dBm. The filter topologies consume 0.552/0.608/0.634 mW from ±1-V supply voltage. The above-mentioned parameters translate into a figure-of-merit FOM_1(FOM_2) of 125.07 dB-Hz/mW (80.59 dB)/120.74 dB-Hz/mW (81.33 dB)/121.44 dB-Hz/mW (79.81 dB) for NQF/QF_1/QF2.

INDEX TERMS Active inductors, active filter, analog integrated circuits, integrated circuit reliability, bandpass filters.

I. INTRODUCTION

Recent trends in radio-frequency (RF) technology are pushing towards cost-effective solutions featuring high integration density, low power consumption and the ability to support diverse communication standards at different data rates and frequency bands [1]. The challenge today lies in the use of fully-integrated active (on-chip) components instead of their expensive, bulky, and passive (off-chip) counterparts. RF bandpass filter is an essential transceiver component which greatly impacts the overall system performance and performs functions like band-selection, image-rejection etc.

Several bandpass filter topologies are available in the literature such as switched-capacitor (SC) filters, active-*RC*filters, MOSFET-*C* filters, transmission-line (TL) filters, *Q*-enhanced *LC* filters, transconductance-C (g_m-*C*) filter and switched g_m-*C* N-path filter. Each of the above filter topologies suffers from one drawback or the other. SC filters suffer from clock-feedthrough problem [2] whereas; filters based on active-RC [3] and MOSFET-C [4] have limited operating frequency range due to the finite gain-bandwidth product of the op-amps used in feedback. TL filters can operate up to several gigahertz but suffer from large die area requirement and limited tunability [5]. *Q*-enhanced LC filters employ bulky tank resonators and use a negative resistor to compensate for the losses associated with spiral inductors in order to improve the effective quality factor [6]. In addition, the monolithic inductors also suffer from ohmic, eddy current and substrate losses, rendering low-quality factor ($Q < 20$) and do not obey process scaling [7], [8]. The use of emulated inductors does overcome most of the drawbacks of conventional spiral inductors such as large die area requirement, limited tunability, and difficulties in integration. However, they too have some drawbacks of their own. Active inductor-based g_m-C filters can operate at high frequencies and have low

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power consumption, but their frequency response is very sensitive to extra phase shift in the integrator leading to deviations in the filter characteristics [9]. Similarly, switched g_m-C N-path filters employ resistive feedback amplifiers which need extra LO generation circuits and also suffer from the problem of non-zero on-resistance of switches [10]. Therefore, the design of a fully-integrated high-performance RF bandpass filter remains a major challenge.

In addition to the problems mentioned above, rigorous scaling down of device dimensions to the nanoscale values has also made it extremely challenging to meet the strict performance requirements of RF bandpass filters such as high-quality factor, high compression point, low noise figure, low power, high dynamic range, reliability against PVT variations etc. Therefore, apart from filter performance parameters, impact of variations in device parameters (such as length, width, oxide thickness, channel doping concentration, and threshold voltage) and environmental parameters (such as supply voltage and temperature) on the design metrics should also be considered right from the beginning of the design cycle, rather than as an afterthought.

In view of the above, three floating active inductor-based bandpass filter topologies are presented in this paper which address the aforementioned problems and find numerous applications in building blocks of radio frequency (RF) front-ends. The proposed topologies are termed as nominal-Q BPF (NQF), Q-enhanced BPF-1 (QF_1), and Q-enhanced BPF-2 (QF_2). The proposed filter topologies take the advantage of negative resistance techniques to enhance the quality factor. Moreover, an addition-based current reference technique is used to increase the reliability of the design. The organization of the paper is as follows. Section II introduces the VDTA-based floating active inductor and the impact of parasitics on the emulated inductance. Section III presents the Q-enhancement techniques and the application of FAIs in RF bandpass filter design is discussed in Section IV. In Section V, the addition-based current reference technique for reliability enhancement is illustrated and the simulation results are provided in Section VI. Finally, the concluding remarks are given in Section VII.

II. VDTA BASED FLOATING ACTIVE INDUCTOR (FAI)

Voltage differencing transconductance amplifier (VDTA) is a tunable six-terminal modern active building block which finds its application in numerous analog signal processing applications [11], [12]. The internal structure of VDTA is composed of two floating current sources (FCS) and its terminal relationships can be characterized by the following matrix equations

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_{zc} \\ i_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_{mf} & -g_{mf} & 0 & 0 \\ \pm g_{mf} & \mp g_{mf} & 0 & 0 \\ 0 & 0 & \pm g_{mS} & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ v_{zc} \end{bmatrix}. \quad (1)$$

Here, p and n are the input terminals, z and zc are the intermediate terminals, x^- and x^+ are output terminals and g_{mF}, g_{mS} are the two Arbel and Goldminz transconductances [11].

A. CIRCUIT DESCRIPTION

The proposed floating active inductor (FAI) configuration is shown in Fig. 1 which consists of two VDTA blocks and a grounded capacitor (C_f). The terminals p and x^- are tied together and the terminals n and x^+ are shorted to ground for the first VDTA. Likewise, the terminals n and x^+ are tied together and the terminals p and x^- are shorted to ground for the second VDTA. The terminal zc is grounded for both the VDTAs and their z terminals are connected to the integrating capacitor C_f.

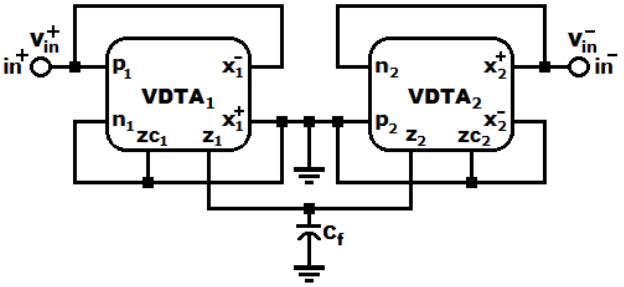

FIGURE 1. Floating active inductor (FAI) configuration.

Under ideal conditions and assuming both VDTA blocks to be matched, the input impedance (Z_{AI}) between nodes in^+ and in^- can be determined by applying KCL at nodes in^+, in^-, z and using the terminal relationship of VDTA as

$$Z_{AI}(s) = \frac{sC_f}{g_{mF}g_{mS}}, \quad (2)$$

and hence

$$L_{AI} = \frac{C_f}{g_{mF}g_{mS}}, \quad (3)$$

which can be tuned by varying the transconductances g_{mF} or g_{mS} of the VDTA.

B. IMPACT OF VDTA PARASITICS ON EMULATED INDUCTANCE

In order to evaluate the impact of parasitics on the emulated inductance, a finite parasitic conductance in parallel with a finite parasitic capacitance is associated with each VDTA terminal, i.e., p, n, z, zc, x^-, and x^+. Ideally, these parasitic conductances (G_p, G_n, G_z, G_{zc}, and G_x) and the parasitic capacitances (C_p, C_n, C_z, C_{zc}, and C_x) are zero. However, in practice, these parasitics exist and degrade the VDTA performance. The non-ideal equivalent of the proposed floating inductor is depicted in Fig. 2.

Application of KCL at nodes in^+ and in^- results in

$$i_{in} = v_{in}^+\left[G_{p_1} + G_{x_1^-} + s\left(C_{p_1} + C_{x_1^-}\right)\right] + i_{x_1}, \quad (4)$$

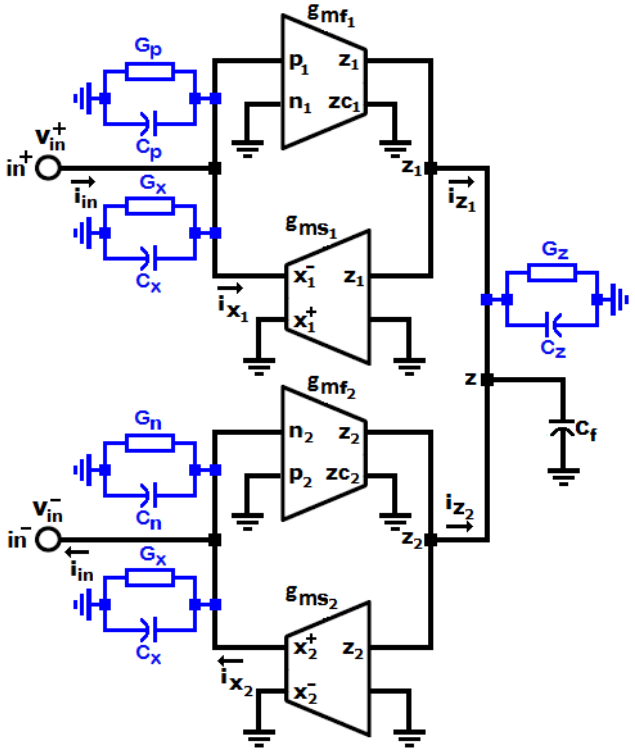

FIGURE 2. Non-ideal transconductor equivalent of FAI.

$$i_{in} = -v_{in}^{-}\left[G_{n_2} + G_{x_2^+} + s\left(C_{n_2} + C_{x_2^+}\right)\right] + i_{x_2}. \quad (5)$$

Assuming both VDTA blocks to be identically matched and substituting the value of i_x from (1) followed by the summation of (4) and (5) results in

$$2i_{in} = \left(v_{in}^{+} - v_{in}^{-}\right)\left[G_p + G_x + s\left(C_p + C_x\right)\right] + 2g_{mS}v_z. \quad (6)$$

The voltage v_z can be obtained by the KCL equation at node z and the VDTA terminal relationships as

$$v_z = \frac{\left(i_{z_1} + i_{z_2}\right)}{G_z + s\left(C_f + C_z\right)} = \frac{g_{mF}}{G_z + s\left(C_f + C_z\right)}\left(v_{in}^{+} - v_{in}^{-}\right). \quad (7)$$

The non-ideal equivalent input impedance of the active floating inductor can be evaluated from (6) and (7) as

$$Z'_{AI}(s) = \frac{2\left[sC_{fz} + G_z\right]}{\left[s^2C_{px}C_{fz} + s\left\{F_{px}C_{pz} + G_zC_{px}\right\} + G_{px}G_z + 2g_{mF}g_{ms}\right]}, \quad (8)$$

where,

$$C_{fz} = C_f + C_z, \quad C_{px} = C_p + C_x, \text{ and } G_{px} = G_p + G_x. \quad (9)$$

Here, the capacitance C_f must be chosen such that the following condition i.e., $C_f \gg C_z$ and $sC_2 \gg G_z$ is true. Equation (8) can be represented by the resonator network shown in Fig. 3 where the constituent elements have the values

$$L'_{AI} = \frac{2C_{fz}}{G_{px}G_z + 2g_{mF}g_{mS}}, \quad G'_s = \frac{G_{px}G_z + 2g_{mF}g_{mS}}{2G_z}, \quad (10)$$

$$G'_p = \frac{C_{fz}G_{px} + C_{px}G_z}{2C_{fz}}, \quad C'_p = \frac{C_{fz}G_{px} + C_{px}G_z}{2G_z},$$

$$F' = \frac{C_{fz}C_{px}}{2G_z}. \quad (11)$$

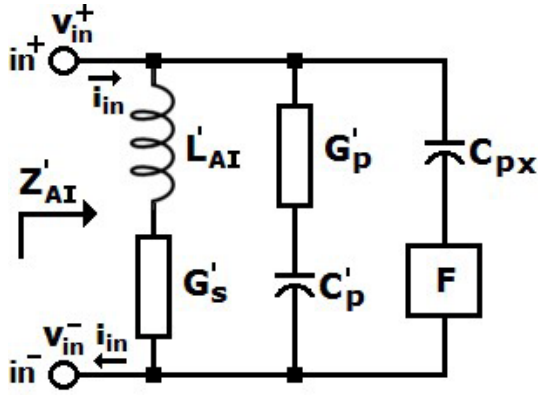

FIGURE 3. Equivalent non-ideal resonator network.

III. QUALITY FACTOR ENHANCEMENT

The most widely accepted technique for quality factor enhancement is the use of negative resistance. This negative resistance is added to the resonator network to compensate for the parasitic and excess-phase losses. Typically, both series, as well as parallel insertion of negative resistance, is possible [13]. However, series insertion of negative resistance suffers from problems related to the measurement of current through the inductor and the potential degradation of dynamic range due to the employment of current sensing resistors [14]. Therefore, the parallel insertion of negative resistance becomes the obvious choice. The complete CMOS implementation of the proposed FAI without any negative resistance is shown in Fig. 4.

A. Q-ENHANCED TOPOLOGY-1

In the first topology, a cross-coupled NMOS differential pair (M_{Q1}, M_{Q2}) is integrated across the output terminals of the FAI as shown in Fig. 5. This cross-coupled differential pair generates a negative resistance that is proportional to the transconductance of the differential pair and can be adjusted by changing the control voltage V_C.

From (8), the non-ideal equivalent input impedance of the floating active inductor can be re-evaluated as

$$Z''_{AI}(s) = \frac{2\left[sC_{fz} + G_z\right]}{2\left[s^2C_{px}C_{fz} + s\left\{G''_{px}C_{fz} + G_zC_{px}\right\} + G''_{px}G_z + 2g_{mF}g_{mS}\right]} \quad (12)$$

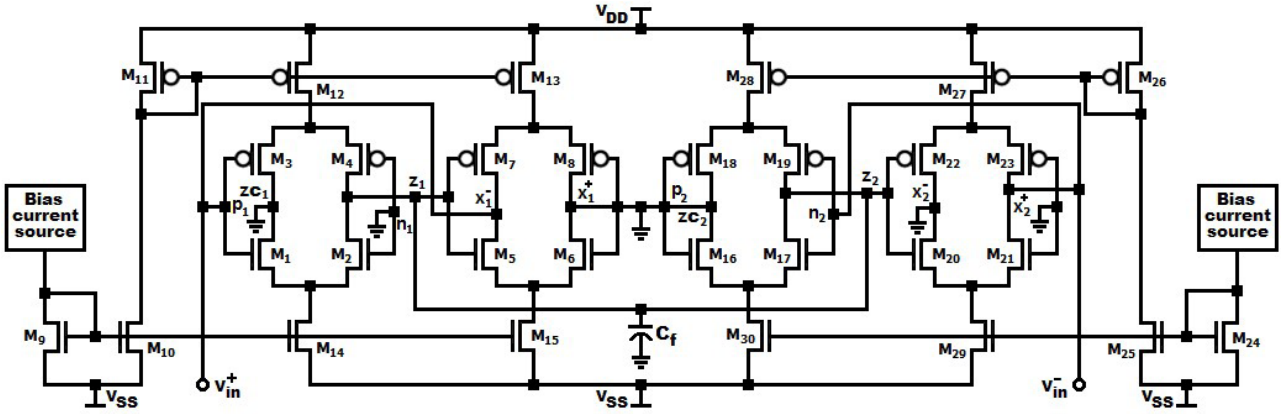

FIGURE 4. Nominal-Q topology of floating active inductor (FAI).

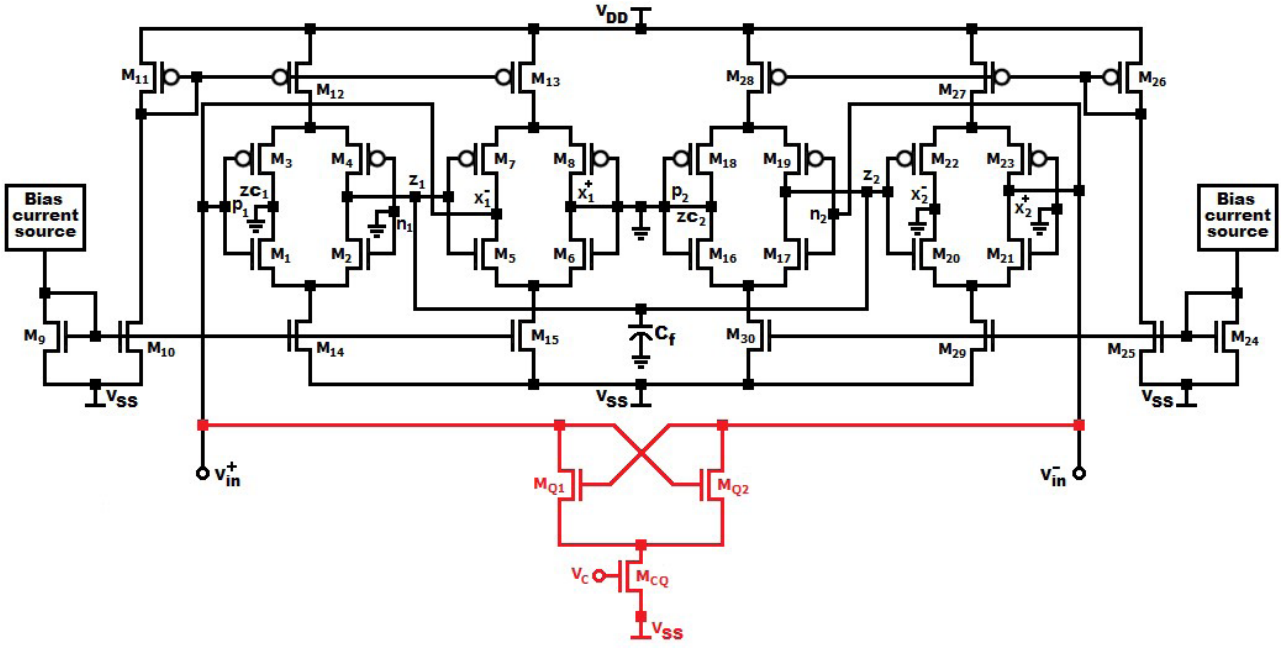

FIGURE 5. Q-enhanced topology-1 of floating active inductor (FAI).

where,

$$G''_{px} = G_{px} - G''_{nQ}, \tag{13}$$

and G''_{nQ} is the equivalent negative conductance. The equivalent resonator network derived from (12) is similar to that shown in Fig. 3 but the constituent elements are equal to

$$L''_{AI} = \frac{2C_{fz}}{G''_{px}G_z + 2g_{mF}g_{mS}}, \quad G''_s = \frac{G''_{px}G_z + 2g_{mF}g_{mS}}{2G_z}, \tag{14}$$

$$G''_p = \frac{C_{fz}G''_{px} + C_{xp}G_z}{2C_{fz}}, \quad C''_p = \frac{C_{fz}G''_{px} + C_{xp}G_z}{2G_z},$$

$$F'' = \frac{C_{fz}C_{px}}{2G_z}. \tag{15}$$

It can be observed from (14), (15) that the negative resistance topology minimizes the value of parasitic conductances G''_s and G''_p and leads to an increase in the value of the emulated inductance L''_{AI}.

B. Q-ENHANCED TOPOLOGY-2

In the second topology, separate cross-coupled NMOS differential pairs are integrated within each floating current source (FCS) block of the VDTA as shown in Fig. 6 [15]. The negative resistance presented by the transistor pairs M_{31}-M_{32}, M_{33}-M_{34}, M_{35}-M_{36} and M_{37}-M_{38}, compensate the parasitic losses associated with the terminals, z_1-zc_1, x_1^--x_1^+, z_2-zc_2 and x_2^--x_2^+ respectively. The control voltages V_{c1}-V_{c4} can be used to electronically adjust the effective negative resistance of the respective differential pair. The non-ideal

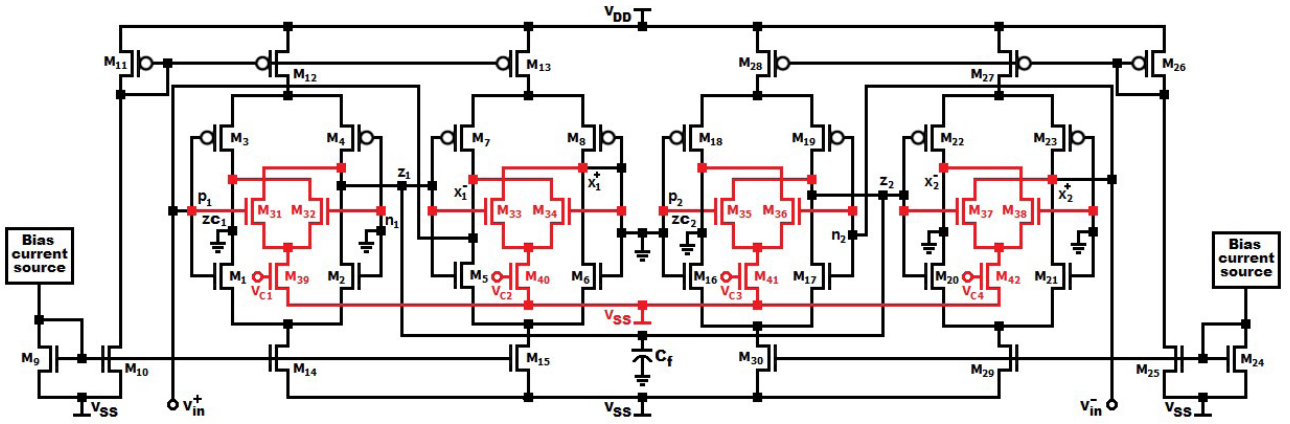

FIGURE 6. Q-enhanced topology-2 of floating active inductor (FAI).

equivalent input impedance of the second topology is determined to be

$$Z''_{AI}(s) = \frac{2\left[sC_{fz}+G''_z\right]}{\left[s^2C_{px}C_{fz}+s\left\{G'''_{px}C_{pz}+G''_zC_{px}\right\}+G'''_{px}G'''_z+2g_{mF}g_{ms}\right]}, \tag{16}$$

where,

$$G'''_z = G_z - G'''_{nQ}, \quad \text{and } G'''_{px} = G_{px} - G'''_{nQ}. \tag{17}$$

The equivalent RLC network derived from (16) has constituent elements equal to

$$L'''_{AI} = \frac{2C_{fz}}{G'''_{px}G'''_z + 2g_{mF}g_{mS}}, \quad G'''_s = \frac{G'''_{px}G'''_z + 2g_{mF}g_{mS}}{2G'''_z}, \tag{18}$$

$$G'''_p = \frac{C_{fz}G'''_{px} + C_{xp}G'''_z}{2C_{fz}}, \quad C'''_p = \frac{C_{fz}G'''_{px} + C_{xp}G'''_z}{2G'''_z},$$
$$F''' = \frac{C_{fz}C_{px}}{2G'''_z}. \tag{19}$$

As seen in topology-1, the introduction of a negative resistance network reduces the value of parasitic conductances and increases the effective emulated inductance.

IV. FAI APPLICATION IN BANDPASS FILTER DESIGN

In this section, the application of the proposed floating active inductors in second-order RF bandpass filters (BPF) is presented. The bandpass filter topologies based on the three FAI designs discussed previously are termed as nominal-*Q* BPF (NQF), *Q*-enhanced BPF-1 (QF_1), and *Q*-enhanced BPF-2 (QF_2) respectively. The basic active bandpass filter configuration utilized is shown in Fig. 7 where C_b and R_b represent the filter capacitance and resistance.

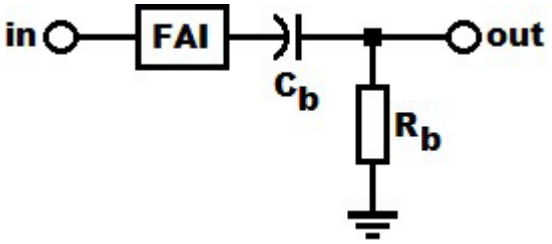

FIGURE 7. Second-order FAI based bandpass filter configuration.

A. NOMINAL-Q BPF (NQF)

The transfer function of the NQF can be approximated as

$$H_{NQF}(s) \approx \frac{s\frac{R_b}{2C_{fz}}\left(G_{px}G_z+2g_{mF}g_{mS}\right)}{s^2+s\frac{R_b}{2C_{fz}}\left(G_{px}G_z+2g_{mF}g_{mS}\right)+\frac{G_{px}G_z+2g_{mF}g_{mS}}{2C_{fz}C_b}} \tag{20}$$

The characteristic parameters i.e. resonant frequency (ω_{NQF}), bandwidth (β_{NQF}), and quality factor (Q_{NQF}) for the NQF can be calculated from (20) and are equal to

$$\omega_{NQF} \approx \sqrt{\frac{G_{px}G_z + 2g_{mF}g_{mS}}{2C_{fz}C_b}}, \tag{21}$$

$$\beta_{NQF} \approx \frac{R_b}{2C_{fz}}\left(G_{px}G_z + 2g_{mF}g_{mS}\right), \tag{22}$$

and

$$Q_{NQF} \approx \frac{1}{R_b}\sqrt{\frac{2C_{fz}}{C_b}\frac{1}{\left(G_{px}G_z + 2g_{mF}g_{mS}\right)}}. \tag{23}$$

B. Q-ENHANCED BPF-1 AND 2 (QF_1 AND QF_2)

The transfer function of the *Q*-enhanced BPF-1 and *Q*-enhanced BPF-2 (QF_1 and QF_2) can be calculated in a similar way.

Additionally, the filter design metrics for both the topologies can be computed as

$$\omega_{QF1} \approx \sqrt{\frac{G''_{px}G_z + 2g_{mF}g_{mS}}{2C_{fz}C_b}}, \tag{24}$$

$$\beta_{QF1} \approx \frac{R_b}{2C_{fz}}\left(G''_{px}G_z + 2g_{mF}g_{mS}\right), \tag{25}$$

$$Q_{QF1} \approx \frac{1}{R_b}\sqrt{\frac{2C_{fz}}{C_b}\frac{1}{\left(G''_{px}G_z + 2g_{mF}g_{mS}\right)}}, \tag{26}$$

and

$$\omega_{QF2} \approx \sqrt{\frac{G'''_{px}G'''_z + 2g_{mF}g_{mS}}{2C_{fz}C_b}}, \tag{27}$$

$$\beta_{QF2} \approx \frac{R_b}{2C_{fz}}\left(G'''_{px}G'''_z + 2g_{mF}g_{mS}\right), \tag{28}$$

$$Q_{QF2} \approx \frac{1}{R_b}\sqrt{\frac{2C_{fz}}{C_b}\frac{1}{\left(G''_{px}G''_z + 2g_{mF}g_{mS}\right)}}. \tag{29}$$

V. RELIABILITY ENHANCEMENT

Process variability arises from random fluctuations in the wafer fabrication processing steps and has a severe impact on the performance of metal-oxide-semiconductor (MOS) devices. In deep-submicron technologies, the major contributors to these device-level random fluctuations are differences in doping, ion implantation, diffusion depth and mismatch in device geometry caused by lithographic limits [16]. Apart from these, supply variations, thermal gradients, and mechanical stress can also degrade the circuit operation and induce failure.

In this section, we propose the use of an addition-based current reference as the bias current source for the active bandpass filters instead of the conventional diode-connected current reference. The proposed process, voltage, and temperature (PVT)-tolerant current source has the same loading effect as a single transistor driving the same amount of current thereby enhancing the reliability of the design without affecting its performance [17]. The conventional diode-connected current reference and the proposed addition-based current reference are shown in Fig. 8. The transistors M_{T1} and M_{T2} have equal dimensions and are matched to ensure the same amount of current through them. The total bias current I_B is the sum of the drain currents I_{T1} and I_{T3} i.e.

$$I_B = I_{T1} + I_{T3}, \tag{30}$$

where,

$$I_{T1} = \kappa_1 \left(V_{SG1} - |V_{t1}|\right)^{\alpha}, \quad I_{T3} = \kappa_3 \left(V_{SG3} - |V_{t3}|\right)^{\alpha}. \tag{31}$$

Here, V_t is the threshold voltage, α is the velocity saturation index ranging between one and two and κ is the technology-dependent transconductance coefficient.

The compensation mechanism in the proposed addition-based current reference can be explained as follows:

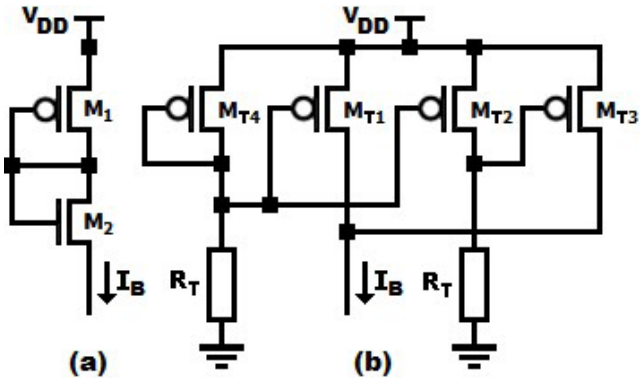

FIGURE 8. (a) Diode-connected current reference (b) Addition-based current reference.

If the current $I_{T1}(I_{T1} = I_{T2})$ increases due to either statistical or environmental variations, the gate voltage of M_{T3} increases and hence V_{SG3} decreases resulting in a lower current I_{T3}. Likewise, if the current I_{T1} decreases, the source-to-gate voltage V_{SG3} of M_{T3} increases resulting in a higher current I_{T3}. Due to this phenomenon, the effective bias current I_B $(I_{T1} + I_{T3})$ from the current reference remains stabilized and is relatively insensitive to process, voltage and temperature variations. The variation in the drain current of a single transistor ΔI_S due to process-varying parameters κ and V_t can be determined by taking partial derivatives with respect to κ and V_t resulting in

$$\Delta I_S = \left(\frac{1}{\kappa}\Delta\kappa - \frac{\alpha}{V_{SG} - |V_t|}\Delta V_t\right) I_S, \tag{32}$$

where $\Delta\kappa$ and ΔV_t are the process-dependent variations in κ and V_t. A similar exercise can be repeated for the bias current I_B from the addition-based current reference resulting in [18]

$$\Delta I_B = \left(1 + \frac{\kappa_3}{\kappa_1}\right)\Delta I_{S1} + \alpha\kappa_3 \left(V_{SG3} - |V_{t3}|\right)^{\alpha-1}\Delta V_{SG3}. \tag{33}$$

It can be observed from (33) that the proposed current reference has an additional feedback term which provides the necessary process-compensation and stabilizes the bias current. The optimum value of feedback required for making I_B completely process independent is equal to

$$\Delta V_{SG3} = -\frac{1 + \frac{\kappa_3}{\kappa_1}}{\alpha\kappa_3 \left(V_{SG3} - |V_{t3}|\right)^{\alpha-1}}\Delta I_{S1} = -\frac{1 + \frac{\kappa_3}{\kappa_1}}{g_{m3}}\Delta I_{S1}. \tag{34}$$

In addition to process variability, thermal variability in device threshold (V_t) and carrier mobility (μ) also has a significant impact on the performance of integrated circuits. This impact is even more severe for deep-submicron technologies because the difference between the supply and device threshold for short channel devices is small which makes it extremely difficult to manage the design margins.

The device threshold (V_t) exhibits a linear dependence on temperature which can be modeled as [19]

$$V_t(T) = V_t(T_0)\left[1 + \alpha_{Vt}(T - T_0)\right], \tag{35}$$

where T_0 is the reference temperature (300 K) and α_{Vt} is the threshold voltage temperature coefficient. Similarly, carrier mobility μ demonstrates a negative exponential temperature dependence governed by [20]

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-\alpha_\kappa}, \tag{36}$$

where α_κ is the mobility temperature exponent. In addition to the above, the resistance, R also exhibits a temperature dependence given by

$$R(T) = R(T_0)\left[1 + \alpha_R(T - T_0)\right], \tag{37}$$

where α_R is the temperature coefficient. The temperature induced variation in the drain current of a single transistor can be calculated as

$$\frac{\Delta I_S(T)}{I_S(T_0)} = \frac{\alpha_{Vt}|V_{t0}|}{V_{SG0} - |V_{t0}|}\Delta T - \frac{\alpha_\kappa}{T}\Delta T, \tag{38}$$

where ΔT is the change in temperature. The first-order ΔT term in the expression of ΔI_S is responsible for greater temperature shifts in the drain current I_S. Likewise, the change in the bias current from the addition-based current source due to ΔT change in temperature is equal to

$$\begin{aligned}\frac{\Delta I_B(T)}{I_B(T_0)} = &-\left(\frac{\alpha_{Vt}|V_{t0}|}{V_{SG0} - |V_{t0}|} - \frac{\alpha_\kappa}{T}\right)\\ &\cdot\left(\frac{\alpha_{Vt}|V_{t0}|}{V_{SG0} - |V_{t0}|} - \frac{\alpha_\kappa}{T} + \alpha_R\Delta T\right)\Delta T^2\\ &-\alpha_R\left(\frac{\alpha_{Vt}|V_{t0}|}{V_{SG0} - |V_{t0}|} - \frac{\alpha_\kappa}{T}\right)^2\Delta T^3.\end{aligned} \tag{39}$$

It can be seen from (39) that the first-order ΔT term in the expression of ΔI_B is zero and only higher order terms exist thereby establishing the temperature compensation effect. From the above analysis, it can be concluded that the proposed addition-based current reference is process and temperature compensated.

VI. SIMULATION RESULTS AND DISCUSSIONS

The proposed floating active inductors and the corresponding active bandpass filters are designed and simulated using the 45-nm Predictive Technology Model (PTM), developed by Nanoscale Integration and Modeling (NIMO) Group of Arizona State University (ASU) on the basis of BSIM4 CMOS technology model [21], [22]. The circuit performance and operation is evaluated using Virtuoso Analog Design Environment (ADE) of Cadence. Both the current source topologies exhibited similar performance in terms of filter design metrics as explained previously.

A. FLOATING ACTIVE INDUCTOR PERFORMANCE

The performance of the proposed floating active inductors i.e. nominal-Q FAI (L_{NQ}), Q-enhanced FAI-1 (L_{Q1}) and Q-enhanced FAI-2 (L_{Q2}) is analyzed by determining their characteristic parameters such as input impedance (Z_{AI}), emulated inductance value (L_{AI}) and self-resonance frequency (ω_{LAI}). The input impedance (Z_{AI}) essentially consists of a resistive component Re$\{Z_{AI}\}$ and an inductive reactance Img$\{Z_{AI}\}$. The frequency dependence of Z_{AI}, Re$\{Z_{AI}\}$, and Img$\{Z_{AI}\}$ for the floating active inductors are shown in Figs. 9−11 respectively. The emulated inductance value (L_{AI}) of the floating active inductor can be obtained from the imaginary component of Z_{AI} (Img$\{Z_{AI}\}$) as

$$L_{AI} = \frac{\mathrm{Im}\{Z_{AI}\}}{\omega}. \tag{40}$$

The emulated inductance (L_{AI}) and self-resonance frequencies (ω_{LAI}) values for L_{NQ}, L_{Q1}, and L_{Q2} are determined from Figs. 9−11 to be approximately 0.63, 0.98, and 1.1 μH and 8.32, 7.11, and 6.93 GHz respectively.

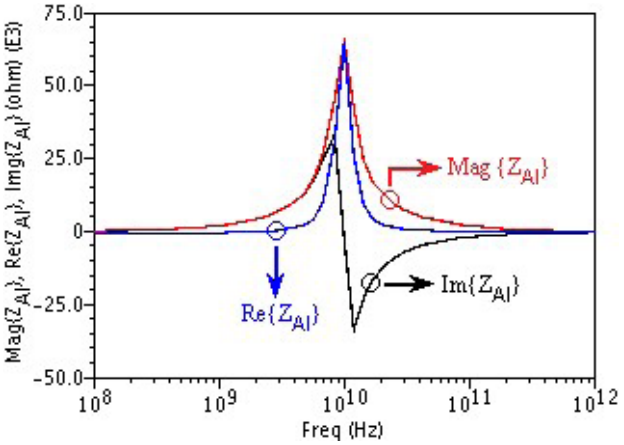

FIGURE 9. Variation of the equivalent input impedance (ZAI) of the nominal-Q floating active inductor and its resistive and reactive components.

B. PRE-LAYOUT BANDPASS FILTER PERFORMANCE

The frequency response of all the three active BPF topologies is shown in Fig. 12. As observed, the NQF exhibits a center frequency (ω_0) of 4.36 GHz, quality factor (Q_{filter}) of 17.83 and a 3-dB bandwidth (BW) of 244.4 MHz. Similarly, the QF_1(QF_2) is centered at 3.63 (3.02) GHz, exhibit quality factors of 54 (46.2) and 3-dB bandwidths of 67.22 (65.36) MHz. The NQF, QF_1, and QF_2 consume 0.552 mW, 0.608 mW, and 0.634 mW respectively from a ±1 V supply and their respective 1-dB compression points are −3.06 dBm, −5.48 dBm, and −5.45 dBm. In the case of integrated receivers employing active filters, the overall receiver performance depends significantly on the dynamic range of the filter [23]. Dynamic range is typically defined as the maximum input level that the filter can tolerate divided by the minimum input level that it can detect. The maximum

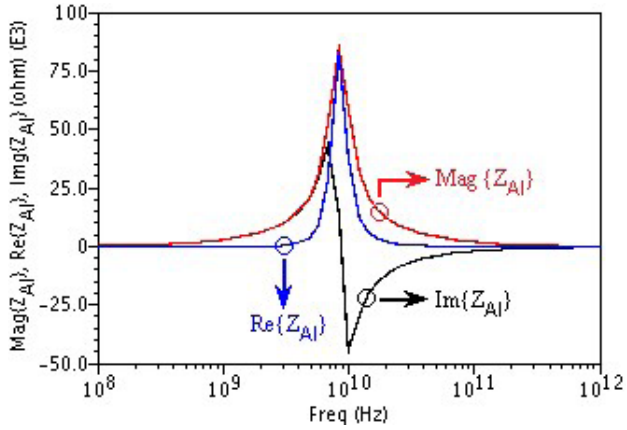

FIGURE 10. Variation of the equivalent input impedance (ZAI) of the Q-enhanced topology-1 floating active inductor and its resistive and reactive components.

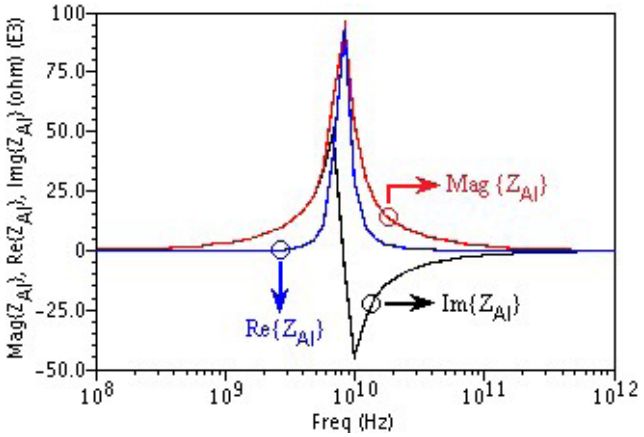

FIGURE 11. Variation of the equivalent input impedance (ZAI) of the Q-enhanced topology-2 floating active inductor and its resistive and reactive components.

TABLE 1. Noise performance of the active BPF topologies.

Filter Topology	Spot Noise @ 1-Hz Bandwidth	Integrated Noise @ 1-MHz Bandwidth	Integrated Noise @ Filter Bandwidth $\left(\frac{\pi}{2}\times BW\right)$
NQF	−125.55	−65.55	−39.71 @ 383.7 MHz
QF_1	−124.06	−64.06	−43.83 @ 105.5 MHz
QF_2	−124.91	−64.91	−44.80 @ 102.6 MHz

input level for the filter is represented by 1-dB compression point (P_{1dB}) and the minimum input level is represented by input referred noise power (P_n) in the bandwidth of interest. Mathematically, $DR = P_{1dB}/P_n$. The input referred noise power (P_n) of all the active filters are tabulated in Table 1 and are estimated at over 1-Hz, 1-MHz and the filter noise bandwidth [11]. Using the parameters in Table 1, the dynamic range (DR) of active filters NQF/QF_1/ QF_2 are calculated as 122.49/118.58/119.46 dB respectively.

In Table 2 all the filter design metrics are tabulated and compared with the state-of-the-art active bandpass filters

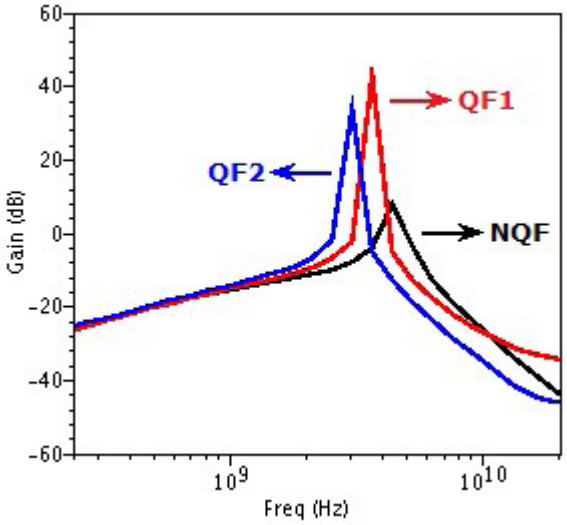

FIGURE 12. Frequency response of the proposed bandpass filter topologies.

reported in the literature. The filter performance can be evaluated and compared using a figure-of-merit (FOM). A superior filter reflects a greater FOM. Two commonly used definitions of figure-of-merit (FOM) are [11], [23], [27]

$$FOM_1 = \frac{P_{1dB}}{P_n}\frac{1}{P_{dc}}, \tag{41}$$

and

$$FOM_2 = \frac{NP_{1dBW}f_{resonant}Q_{filter}}{P_{dc}NF}. \tag{42}$$

Here, P_{dc} is dc power consumption in watts, P_{1dB} is the 1-dB compression point in dBm and P_n is the filter noise power corresponding to 1-Hz bandwidth in dBm. In addition, N is the order of the filter, $f_{resonant}$ is the resonant frequency, Q_{filter} is the quality factor of the filter, P_{1dBW} is the 1-dB compression point in watts, and NF is noise figure (not in decibels). It can be observed from Table 2 that the proposed NQF/QF_1/QF_2 achieves a FOM_1 (FOM_2) value of 125.07 dB-Hz/mW (80.59 dB)/120.74 dB-Hz/mW (81.33 dB)/121.44 dB-Hz/mW (79.81 dB) respectively.

Even though the designs mentioned in [11], [24], [26], and [10], exhibit superior performance in terms of some of the design metrics, these come at an additional cost and suffer from one drawback or the other. In [24], the 0.5-μm CMOS-SOI (silicon on insulator) technology is used which is built on an insulating layer and is regarded to be less susceptible to noise in comparison to bulk CMOS. However, it also suffers from limitations such as additional cost, self-heating, kink and history effects etc. In [26], a transformer-based filter topology is employed which suffers from integration complexities, shielding requirements, large die-area, and cost. In [10], Switched G_m-C topology based on N-path filters is utilized. The N-path filters employ resistive feedback amplifiers, need additional local generation circuits and suffer from the problems related to non-zero on-resistance of switches.

TABLE 2. Comparison with state-of-the-art active bandpass filter topologies.

References (year)→	[24] (2005)	[25] (2006)	[26] (2006)	[27] (2008)	[10] (2012)	[28] (2015)	[11] 2017	This work		
								NQF	QF_1	QF_2
Technology	0.5-µm CMOS-SOI	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	65-nm CMOS	40-nm CMOS	45-nm CMOS	45-nm CMOS	45-nm CMOS	45-nm CMOS
Inductor Topology	Spiral Inductor	Transformer	Transformer	Active Inductor	Switched Gm-C	Active RC	Active Inductor	Active Inductor	Active Inductor	Active Inductor
Filter order (N)	2	3	4	2	4	8	2	2	2	2
Center frequency (GHz)	2.5	2.368	2.03	2.44	0.4-1.2	0.14	2.511	4.36	3.63	3.02
-3 dB Bandwidth (MHz)	70	60	130	60	21	7-56	36.21	244.4	67.22	65.36
Quality factor	36	40	16	41	19-57	3-20	69	17.84	54	46.2
Filter Gain (dB)	23	−1.8	0	6	−3	0-20	72.76	9.26	38.65	43.78
Supply voltage (V)	3	1.5	1.8	1.8	1.2/2.5	1.5	±1	±1	±1	±1
Power Consumption (mW)	15	8.8	17	10.8	21.4	37.8	0.168	0.552	0.608	0.634
Noise figure (dB)	6	18	15	18	10	34-55	29.62	30.84	31.28	31.17
P_{1dB} (dBm)	−15	−20	−6.6	−15	−4.4	+12	−1.5	−3.06	−5.48	−5.45
Dynamic range (dB-Hz)	153	135	152	-	160	131	125.84	122.49	118.58	119.46
FOM_1 (dB-Hz/mW)	141	125.6	140	-	146.4	115	133.6	125.07	120.74	121.44
FOM_2 (dB)	82	78	77	81	85	45	94	80.59	81.33	79.81
Die Area (mm^2)	2.5e+3	2.25e+3	0.81e+3	30	127	320	0.413	1.373	1.690	2.028
Performance Results (*Post-Layout)	Measurement	Measurement	Measurement	Measurement	Measurement	Measurement	Simulation*	Simulation*	Simulation*	Simulation*

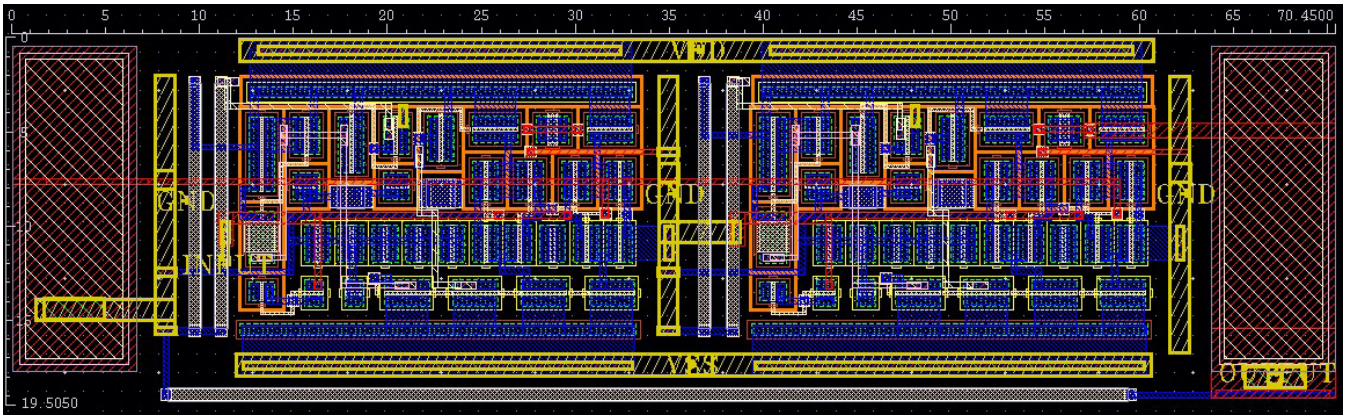

FIGURE 13. Complete physical layout of nominal-Q bandpass filter (NQF).

Finally, the filter topology in [11] is based on a grounded active inductor which requires less number of transistors for active inductor realization.

However, grounded inductors have a requirement of grounding one of the terminals thereby reducing their flexibility and diversity of applications. Further, in this work, a novel technique for reliability enhancement using addition-based current reference is employed and the performance improvement of this technique over the conventional diode-connected current reference technique used in [11] has been demonstrated.

C. POST-LAYOUT BANDPASS FILTER PERFORMANCE

Physical layouts of all three active BPF topologies are drawn and the extracted layout parasitics are used to obtain post-layout simulation results at 45-nm technology node. Due to limited space, the layout of only nominal-*Q* BPF (NQF) with addition-based current reference is shown in Fig. 13. As observed, NQF/ QF_1/QF_2 occupies an active area of 70.45 μm × 19.50μm/70.45 μm × 24 μm/70.45 μm × 28.80 μm.

A summary of the post-layout performance of the proposed active BF topologies is tabulated in Table 3 which validates the feasibility of the proposed designs.

The NQF/QF_1/QF_2 exhibits a center frequency (ω_0) of 4.06/3.48/ 2.81 GHz, quality factor (Q_{filter}) of 11.03/45.43/

TABLE 3. Post-layout performance of the active BPF topologies.

Design metrics ↓	NQF	QF_1	QF_2
Active area (mm^2)	0.0013	0.0016	0.0020
Center frequency (GHz)	4.06	3.48	2.81
-3 dB Bandwidth (MHz)	368	76.6	71
Quality factor	11.03	45.43	39.57
Noise figure (dB)	31.34	31.88	31.67
P_{1dB} (dBm)	−3.1	−5.6	−5.5
Power Consumption (mW)	0.614	0.648	0.692
Dynamic range (dB-Hz)	121.09	116.52	117.03
FOM_1 (dB-Hz/mW)	123.2	118.4	118.6
FOM_2 (dB)	77.19	79.39	77.9

39.57, 3-dB bandwidth (BW) of 368/76.6/71 MHz, consumes 0.614/0.648/0.692 mW from ±1 V supply voltage, and has a 1-dB compression point (P_{1dB}) of −3.1/−5.6/−5.5 dBm. The above parameters result in FOM_1 (FOM_2) values of 123.2 dB-Hz/mW (77.19 dB)/118.4 dB-Hz/mW (79.39 dB)/118.6 dB-Hz/mW (77.9 dB).

D. RELIABILITY PERFORMANCE

Random dopant fluctuations (RDF), oxide thickness variation (OTV), line-edge roughness (LER), line-width roughness (LWR) and metal-gate work-function fluctuations (WKF) cause a degradation in the performance of MOS devices especially in the nanoscale regime [29], [30]. To analyze the above phenomenon, process-sensitive device parameters such as channel length L, channel width W, gate oxide thickness t_{ox} and doping concentration $NDEP$ are assumed to have independent Gaussian distributions with a 3σ variation of ±10% at 45-nm technology node as suggested by the International Technology Roadmap for Semiconductor Industry (ITRS) [31]. The variability of the filter resonant frequency ω_0 is then estimated using Monte Carlo simulations of 5000 iterations to limit the inaccuracies in estimated values of σ (standard deviation) to less than 4%. The results for the same are tabulated in Tables 4-6 and the distribution of ω_0 of NQF, QF_1, and QF_2 with addition-based current reference is shown in Fig. 14. It can be seen from Tables 4-6 that the NQF with diode-connected current source shows a standard deviation (σ) of 347.5 MHz around the mean (μ) of 4.360 GHz which results into a variability (σ/μ) of 0.079. However, the values of standard deviation, mean and variability for NQF with the addition-based current reference are 111.2 MHz, 4.375 GHz and 0.025 respectively which highlight a 3.16× improvement in reliability.

TABLE 4. Monte carlo simulation results for resonant frequency of the proposed NQF topology with both current references.

Current Source	Mean (μ)	Standard Deviation (σ)	Variability (σ/μ)
Diode-connected	4.360 GHz	347.5 MHz	0.079
Addition-based	4.375 GHz	111.2 MHz	0.025

TABLE 5. Monte carlo simulation results for resonant frequency of the proposed QF_1 topology with both current references.

Current Source	Mean (μ)	Standard Deviation (σ)	Variability (σ/μ)
Diode-connected	3.615 GHz	241.6 MHz	0.066
Addition-based	3.622 GHz	57.42 MHz	0.015

Similarly, the QF_1 and QF_2 with addition-based current reference achieve a reliability enhancement of 4.4× and 4.63× respectively as compared to QF_1 and QF_2 with the diode-connected current source. In addition to Monte Carlo simulation, the filter resonant frequency ω_0 is also calculated

TABLE 6. Monte carlo simulation results for resonant frequency of the proposed QF_2 topology with both current references.

Current Source	Mean (μ)	Standard Deviation (σ)	Variability (σ/μ)
Diode-connected	2.99 GHz	526.4 MHz	0.176
Addition-based	3.01 GHz	116.1 MHz	0.038

TABLE 7. Process corner simulation results for resonant frequency of the proposed NQF topology with both current references.

Current Source	NN	FF	SS	SF	FS
Diode-connected	4.35	4.43	3.91	3.96	4.41
Addition-based	4.36	4.39	4.09	4.11	4.37

TABLE 8. Process corner simulation results for resonant frequency of the proposed QF_1 topology with both current references.

Current Source	NN	FF	SS	SF	FS
Diode-connected	3.62	3.72	3.26	3.34	3.69
Addition-based	3.62	3.69	3.39	3.42	3.68

TABLE 9. Process corner simulation results for resonant frequency of the proposed QF_2 topology with both current references.

Current Source	NN	FF	SS	SF	FS
Diode-connected	3.01	3.21	2.68	2.75	3.17
Addition-based	3.02	3.19	2.71	2.78	3.16

at all the process corners i.e. the NN, FF, SS, FS and SF corner. The process corner results for all three active BPF topologies corresponding to both current sources are tabulated in Tables 7-9. A sensitivity parameter $SP_{\omega 0}$ is defined to quantify the amount of variation in ω_0 and compare the reliability performance of active filters across different process corners. This sensitivity parameter $SP_{\omega 0}$ is equal to

$$SP_{\omega 0} = \frac{|\Delta\omega_0|}{\omega_0} = \frac{|\omega_0\,(PC) - \omega_0\,(NN)|}{\omega_0\,(NN)}, \tag{43}$$

where ω_0 (PC) is the value of ω_0 at a process corner and ω_0 (NN) is the value of ω_0 at NN corner i.e. $SP_{\omega 0}$ is defined with respect to the NN corner. The values of $SP_{\omega 0}$ at different process corners for all three filters are shown in Fig. 15. It can be seen that the sensitivity of ω_0 to process variations is much lower in case of the addition-based current source as compared to its diode-connected counterpart thereby validating its use for reliability enhancement. Similarly, to study the impact of supply voltage variations on the filter reliability, a 10% variation is assumed in the $V_{DD(SS)}$ values in accordance with the ITRS guidelines and the corresponding change in ω_0 is estimated. A similar sensitivity parameter $SV_{\omega 0}$ is defined in this case as well and is given by

$$SV_{\omega 0} = \frac{\Delta\omega_0}{\omega_0} = \frac{\omega_0\left[V_{DD(SS)}\right] - \omega_0\left[V_{DD(SS)0}\right]}{\omega_0\left[V_{DD(SS)0}\right]}. \tag{44}$$

Here, $\omega_0(V_{DD(SS)})$ is the ω_0 value at a particular supply voltage and $\omega_0(V_{DD(SS)0})$ is the value of ω_0 at the nominal supply voltage.

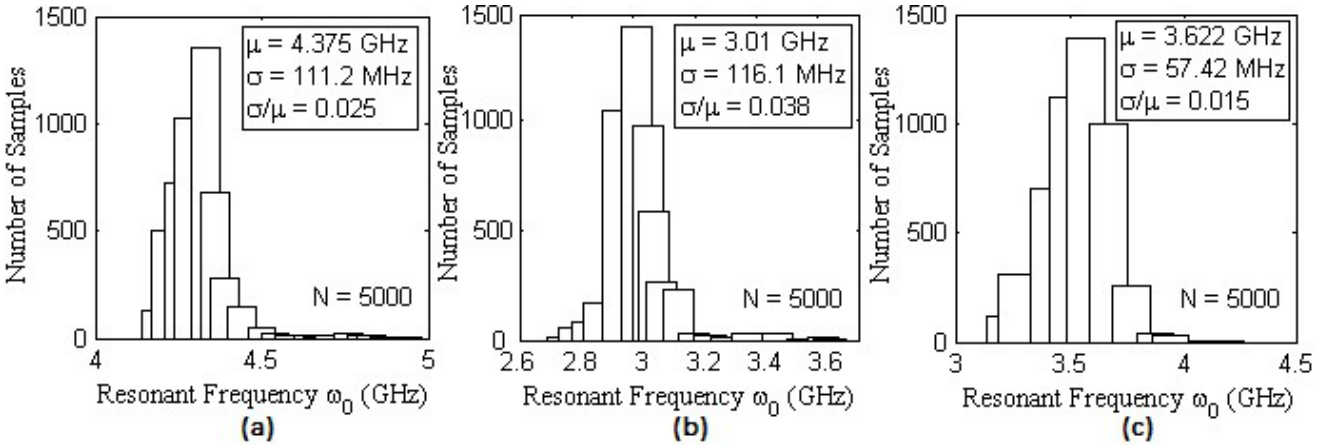

FIGURE 14. Distribution of center frequency ω_0 of (a) NQF (b) QF2 (c) QF1 with addition-based current reference.

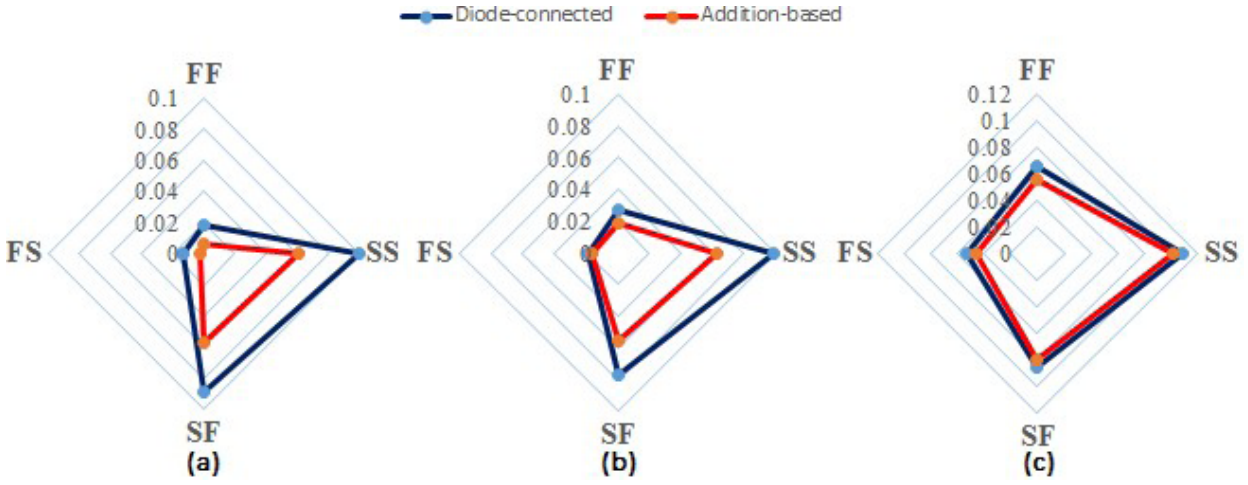

FIGURE 15. Process sensitivity of center frequency ω_0 of (a) NQF (b) QF1 (c) QF2 with diode-connected and addition-based current reference.

The parameter $SV_{\omega 0}$ quantifies the change in ω_0 due to supply voltage variation and allows for an easy comparison of the reliability performance of active filters. The variation of $SV_{\omega 0}$ with filter supply voltage for all three filters is shown in Fig. 16. It can be observed that the $SV_{\omega 0}$ values for the addition-based current source are much lower in magnitude as compared to the conventional diode-connected source. Therefore, the addition-based current reference provides greater resilience to supply voltage variations. Finally, the temperature dependence of filter design metrics is determined over the range of 0 to 100 °C. The temperature sensitivity parameter $ST_{\omega 0}$ is calculated to estimate the shift in ω_0 due to changes in operating temperature and compare the reliability of different filter topologies.

The temperature sensitivity $ST_{\omega 0}$ is equal to

$$ST_{\omega 0} = \frac{\Delta\omega_0}{\omega_0} = \frac{\omega_0(T) - \omega_0(T_0)}{\omega_0(T_0)}, \tag{45}$$

where $\omega_0(T)$ is the value of ω_0 at a specific temperature and $\omega_0(T_0)$ is the ω_0 value at room temperature (300 K). The $ST_{\omega 0}$ values at different temperatures for all three filters are shown in Fig. 17. As observed, the filters with addition-based current reference demonstrate superior reliability in the presence of temperature variations. A similar trend is also observed in the presence of process and supply voltage variations as discussed previously.

E. DESIGN SCALABILITY

The 45-nm results obtained in this work are validated by simulating the proposed topologies with TSMC's (Taiwan Semiconductor Manufacturing Company) 180-nm industry standard model parameters. The approach of validation is in-line with that adopted in [32] and [33].

The NQF/QF_1/QF_2 exhibits a center frequency (ω_0) of 3.92/3.45/ 2.83 GHz, quality factor (Q_{filter}) of 10.59/44.89/ 39.15, 3-dB bandwidth (BW) of 352/73.8/72 MHz, consumes 0.704/0.780/0.852 mW from ±1 V supply voltage, and has a 1-dB compression point ($P_{1\text{dB}}$) of −3.4/−5.8/−5.7 dBm. The above parameters result in FOM_1 (FOM_2) values of 123.89 dB-Hz/mW (76.99 dB)/118.93 dB-Hz/mW

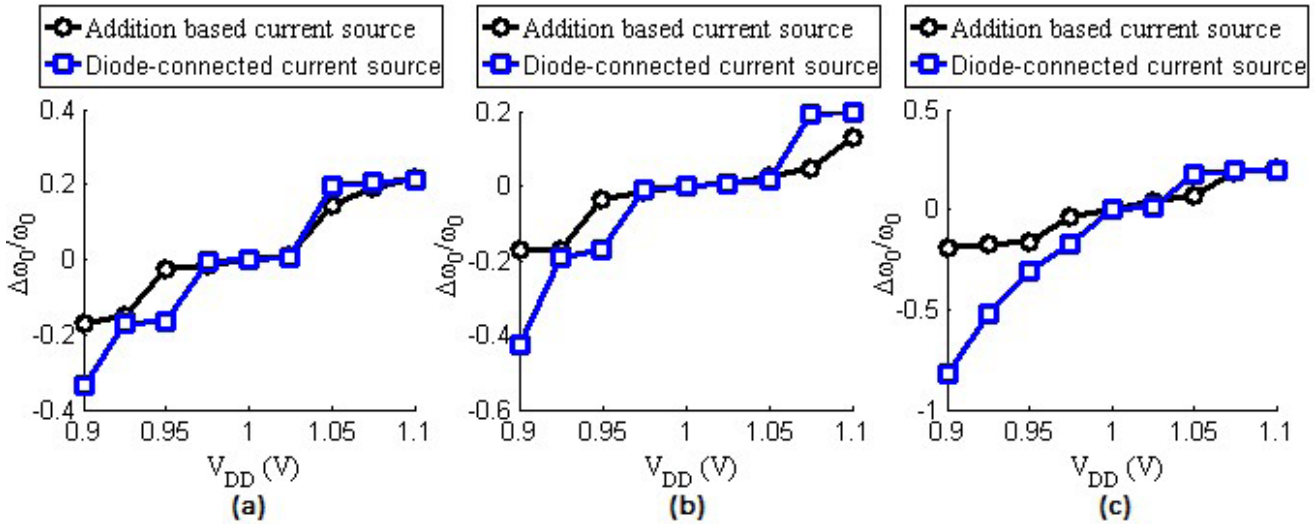

FIGURE 16. Supply voltage sensitivity of center frequency ω_0 of (a) NQF (b) QF1 (c) QF2 with diode-connected and addition-based current reference.

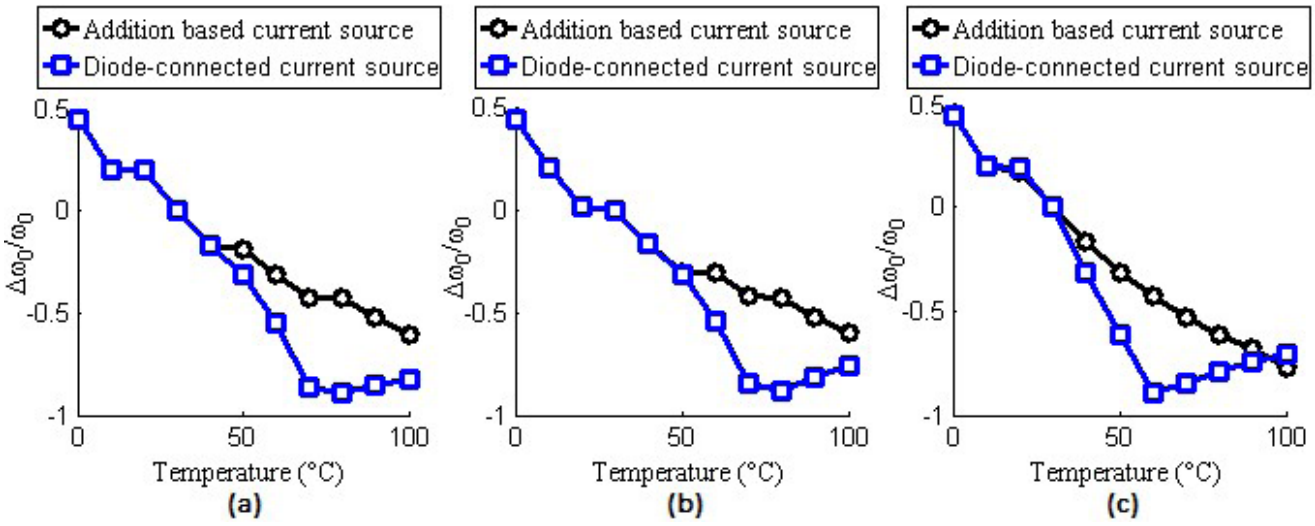

FIGURE 17. Temperature sensitivity of center frequency ω_0 of (a) NQF (b) QF1 (c) QF2 with diode-connected and addition-based current reference.

(79.97 dB)/119.12 dB-Hz/mW (77.66 dB). The FOM values obtained at 180-nm technology node agree to those obtained at the 45-nm technology node. This validates the scalability of the proposed design into ultra-deep submicron CMOS technologies such as 45-nm.

VII. CONCLUSION

Three floating active inductor-based RF bandpass filter topologies are proposed which find diverse applications in wireless transceivers, instrumentation systems such as Sonar, Seismology and medical systems such as EEGs and Electro-cardiograms. The use of an active inductor prevents the losses (metal conductance losses, substrate losses, skin and proximity effects) associated with monolithic inductors and has additional advantages such as smaller die-area, lower cost, ease of integration, high chip density etc. Negative resistance-based quality factor enhancement techniques are utilized to increase the quality factor of the proposed active filters and mitigate the effects of integrator phase error. Further, the filter reliability in the presence of process, voltage and temperature variations is improved using an addition-based current reference instead of its conventional diode-connected counterpart which ensures reliable circuit performance even in ultra-deep submicron CMOS technologies. Also, the filter characteristics are examined both at 45-nm as well as 180-nm technology node to establish the scalability of the proposed design. The circuit performance in the presence of parasitics is investigated through analytical expressions and post-layout simulation results are presented to validate the feasibility of the proposed filters.

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