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Full-Duty-Cycle Regulated Three-Level AC/AC Converter With Self-Following Flying Capacitor

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ABSTRACT The three-level (TL) AC/AC converter needs to control the output voltage as well as the voltage of flying capacitor, which makes the control circuit relatively complicated. At the same time, the ranges of the output voltage and load are limited because of the influence of the flying capacitor voltage correction on the duty cycle of the output voltage. For the applications of high-voltage and high-power conversion, a full-duty-cycle-regulated TL AC/AC converter with a self-following flying capacitor was proposed and studied, which adopts a small volume auxiliary transformer. The flying capacitor is directly supplied from the auxiliary transformer, can self-follow half of the input voltage, and does not need to be controlled by other control circuit. The proposed converter only needs to control its output voltage, which makes control strategy simple and easy to be realized. The output voltage can be regulated within the range of full-duty cycle. The capacity of an auxiliary transformer is very small, under ideal condition which only needs to supply the reactive load of the flying capacitor. The circuit operational principle was analyzed in detail, and a prototype was designed. With a simple control circuit, the experimental results were given and the full-duty-cycle regulation of the TL AC/AC converter was realized.

INDEX TERMS AC/AC converter, three-level, self-following flying capacitor, auxiliary transformer, full-duty-cycle regulation.

I. INTRODUCTION

AC/AC conversion technology is widely used in power electronics, power systems, energy transportation, industrial control, mechanical electronics, and renewable energy power generation. In high voltage and high power transmission and distribution and industrial applications, under the existing technology level of power electronic devices, one of the effective means to achieve high voltage and high power conversion with high frequency and low electromagnetic interference is to look for breakthroughs of control method and circuit topology. The multilevel technology is to achieve high voltage and high power output by improving the topology of converter. It does not require buck-boost transformer or voltage equalization circuit, nor does it have the problems of series voltage equalization and parallel current sharing caused by series and parallel connection of components. As the number of output voltage level increases, the harmonics of output voltage of converter are small, it is easy and convenient to design filter, and the voltage stress of switch is low [1]–[4]. Therefore, the multilevel conversion technique is regarded as a representative and more ideal solution to high voltage and large power conversion. And it has been widely used in rectifiers [8]–[10], inverters [5]–[7], and DC/DC converters [11]–[13].

For multilevel AC/AC converters at present, multilevel matrix converters [14]–[16] and multilevel AC-DC-AC converters [17]–[19] have been studied in more depth, but the research on multilevel PWM AC/AC converters is relatively rare. According to the multilevel topology proposed by TAEMYNARD, which uses flying capacitor for voltage equalization [20], a TL PWM AC chopper (Buck type TL AC converter) was proposed [21], on the basis of which a clock-interleaved constant frequency integration control strategy was proposed that realized the closed-loop control of the output voltage [22]. By adopting a double-closed-loop

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control strategy of flying capacitor voltage and output voltage [23], the voltage of flying capacitor could be controlled, but its front stage circuit cannot realize full-duty-cycle regulation of the output voltage.

Usually the TL AC/AC converter with flying capacitor has two control targets: the output voltage and the flying capacitor voltage, which makes the control circuit relatively complex and the range of output voltage and load are limited [23]–[25]. In this paper, a full-duty-cycle regulated TL AC/AC converter with self-following flying capacitor was proposed. The voltage of flying capacitor directly supplied by a small volume auxiliary transformer can self-follows half of the input voltage, and does not need to be controlled by other control circuit. Therefore, the converter has only one control target, and its control strategy is simple and easy to implement. The output voltage can be regulated within the range of full-duty-cycle. The capacity of the auxiliary transformer is small, under ideal condition which only needs to satisfy the reactive load of flying capacitor.

The paper was arranged as follows. In Section II, the principle of the double-target control strategy and the reason why it can not achieve full-duty-cycle regulation were analyzed. In Section III, the topology of full-duty-cycle regulated TL AC/AC converter with self-following flying capacitor was proposed, its switching modality and operational principle were analyzed and the capacity of the auxiliary transformer were calculated. In Section IV the control strategy were presented. In Section V, a prototype was fabricated and experimental results were given. Conclusions were obtained in Section VI.

II. DOUBLE-TARGET CONTROL STRATEGY AND ITS LIMITATION

Buck type TL AC/AC converter, as shown in Fig. 1, is mainly composed of four AC switches (S_1, S_2, S_3, S_4), flying capacitor C_y, output filter inductor L_f, and output filter capacitor C_f. Each AC switch consists of two switches in reverse series.

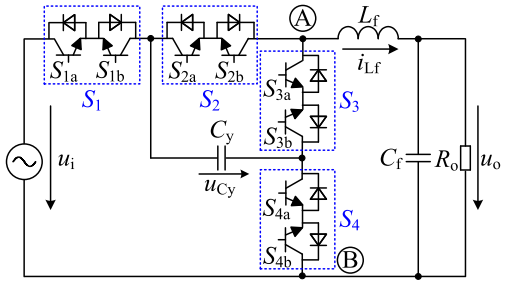


FIGURE 1. Buck type TL AC/AC converter.

For the Buck type TL AC/AC converter, the clock-interleaved constant strategy [22] and the double-closed-loop control method for output voltage and flying capacitor voltage [23], [24] are all double-target control strategy, which essentially uses one duty cycle to control two targets. On the premise of ensuring the output voltage control accuracy, the error of the flying capacitor voltage will be large. The voltage of the flying capacitor cannot follow well with half of the input voltage.

With double-target control strategy, when using one duty cycle to control the output voltage and the flying capacitor voltage, the duty cycle of S_1 is $(D + d)$, that of S_2 is $(D\text{-}d)$, that of S_3 is $[(1 - D) + d]$, and that of S_4 is $[(1 - D) - d]$ (D is the duty cycle of the converter to regulate the output voltage u_o, and d is the duty cycle offset to correct the flying capacitor voltage u_{Cy}). Assuming the input voltage is $u_i = U_{im} \sin \omega t$, the output filter inductor current $i_{Lf} = I_{fm} \sin(\omega t - \varphi)$, U_{im} and I_{fm} are the amplitudes of u_i and i_{Lf}, $\omega = 2\pi f$, f is the fundamental frequency, φ is the output impedance angle.

During one switching period T_s, the electricity difference in charging and discharging of the flying capacitor is

$$\Delta Q = \int_{t_1}^{t_2} i_{Lf} dt - \int_{t_3}^{t_4} i_{Lf} dt \tag{1}$$

t_1 to t_2 is the charging period of flying capacitor

$$t_2 - t_1 = \begin{cases} (D + d) \cdot T_s \\ (1 - D + d) \cdot T_s \quad D \geq 0.5 \end{cases} \tag{2}$$

t_3 to t_4 is the discharging period of flying capacitor

$$t_3 - t_4 = \begin{cases} (D - d) \cdot T_s & D < 0.5 \\ (1 - D - d) \cdot T_s & D \geq 0.5 \end{cases} \tag{3}$$

Because the switching frequency f_s is much larger than the input voltage frequency f. Therefore, during each switching period, i_{Lf} can be almost considered unchanged. Substituting (2) and (3) into (1)

$$\Delta Q = 2 i_{Lf} T_s d \tag{4}$$

Ignoring the high frequency current component in the flying capacitor, it can be considered that the charging and discharging of the flying capacitor are from the low frequency current component i_{Cy}

$$\Delta Q = \int_0^{T_s} i_{Cy} dt \tag{5}$$

In each switching period, i_{Cy} is also approximately constant. Combining (4) and (5)

$$d = \frac{i_{Cy}}{2 i_{Lf}} \tag{6}$$

When controlling the voltage of the flying capacitor to follow half of the input voltage, the i_{Cy} should be

$$\begin{aligned} i_{Cy} &= I_{cm} \sin(\omega t + 90^\circ) \\ &= U_{im} \pi f c_y \sin(\omega t + 90^\circ) \end{aligned} \tag{7}$$

where I_{cm} is the amplitude of i_{cy}.

The output voltage is determined by D. Assuming the total output impedance is Z_o (including the reactance of the output filter inductor and capacitor, the former is much smaller than

the latter, which can be ignored under no load condition), then i_{Lf} is

$$\begin{aligned} i_{Lf} &= I_{fm}\sin(\omega t-\varphi) \\ &= \frac{DU_{im}\sin(\omega t-\varphi)}{|Z_o|} \end{aligned} \tag{8}$$

Substituting (7) and (8) into (6)

$$d = \frac{\pi f C_y |Z_o| \sin(\omega t+90°)}{2D\sin(\omega t-\varphi)} \tag{9}$$

According to (9), d is influenced by some parameters such as D, C_y, $|Z_o|$ and φ.

When the circuit operates under no load condition, (9) can be simplified as

$$\begin{aligned} d &= \frac{\pi f C_y \sin(\omega t+90°)}{4D\pi f C_f \sin(\omega t+90°)} \\ &= \frac{1}{4D}\cdot\frac{C_y}{C_f} \end{aligned} \tag{10}$$

In (10), $d > 0$, assuming $k = C_y/C_f$, the range of d is limited by two parameters, D and k. And the duty cycle of each switch must satisfy the inequality group as shown in (11).

$$\begin{cases} 0 < D+d < 1 \\ 0 < D-d < 1 \\ 0 < (1-D)+d < 1 \\ 0 < (1-D)-d < 1 \end{cases} \tag{11}$$

According to different values of k, when the circuit operates under no load, the feasible value range curves of D are shown by the solid line in the shaded area of Fig. 2.

It can be seen from Fig. 2 that the range of D is limited by the value of k. The smaller the value of k is, the narrower the limited range of D is. The value of k is affected by C_y. If the flying capacitor C_y is too small, the voltage ripple on the flying capacitor will be too large, and the voltage stress of the switch will become large.

When the circuit is operating under load, the limited range of D also exists. When $D < 0.5$, $-D < d < D$. Assuming $\pi f C_y|Z_o|/2 = \delta$, From (9) we can get

$$D > M = \sqrt{\left|\frac{\delta\sin(\omega t+90°)}{\sin(\omega t-\varphi)}\right|} \tag{12}$$

Combined with (12), after the values of C_y, L_f, and C_f are determined, the curves of M with different resistive loads R_o are shown in Fig.3. Here, $C_y = 3.3\mu$F, $C_f = 4.4\mu$F, and $k = 3/4$, curve 1 in Fig. 3 is an M curve in the case when the circuit with no load, corresponding to the point G in Fig. 2. Curves 2, 3, and 4 in Fig. 3 are M curves when R_o is 5kΩ, 300Ω, and 50Ω, respectively. As R_o increases, the corresponding M curve becomes closer to curve 1 in Fig. 3. When $D = 0.3$, $R_o = 300\Omega$, during one input voltage period, (12) holds true during $\theta_1-\theta_2$ and $\theta_3-\theta_4$, the flying capacitor voltage can be regulated normally. During $\theta_2-\theta_3$ and $\theta_4-\theta_5$,

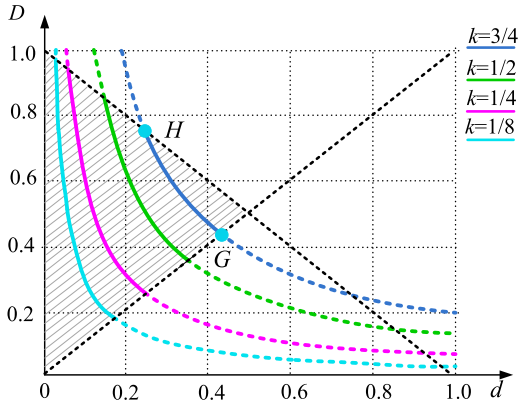


FIGURE 2. Feasible curves of D at different k under no load.

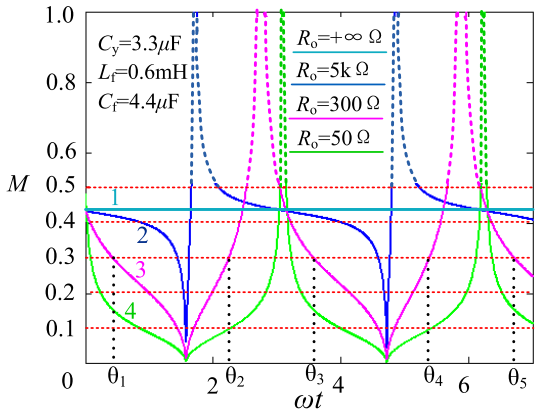


FIGURE 3. Curves of M with different R_o.

the situation is just the opposite. As D decreases, the range that satisfies (12) becomes smaller, and the range during which (12) does not hold true becomes larger.

Similarly, When $D \geq 0.5$, $-1+D < d < 1-D$. From (9) we get

$$D < N = \frac{1+\sqrt{\left|\frac{\delta\sin(\omega t+90°)}{\sin(\omega t-\varphi)}\right|}}{2} \tag{13}$$

Combined with (13), the curves of N with different R_o are shown in Fig.4. Curve 5 in Fig. 4 is an N curve in the case when the circuit with no load, corresponding to the point H in Fig. 2. Curves 6, 7, and 8 in Fig. 4 are N curves when R_o is 5kΩ, 300Ω, and 50Ω, respectively. As R_o increases, the corresponding N curve becomes closer to curve 5 in Fig. 4. When $D = 0.8$, $R_o = 300\Omega$, during $\theta_6-\theta_7$ and $\theta_8-\theta_9$, (13) holds true, and the flying capacitor voltage can be regulated normally. During $\theta_7-\theta_8$ and $\theta_9-\theta_{10}$, the situation is just the opposite. As D increases, the range that satisfies (13) becomes smaller, and the range that does not satisfy (13) becomes larger.

From the analysis above, under the double-target control strategy, the range of D is limited, and the converter cannot be full-duty-cycle regulated.

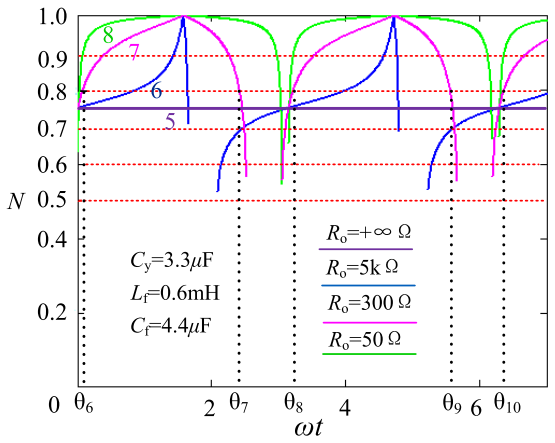


FIGURE 4. Curves of N with different R_o.

III. CIRCUIT TOPOLOGY AND OPERATIONAL PRINCIPLE

A. CIRCUIT TOPOLOGY

If we do not change the basic topology of Buck type TL AC/AC converter but only improve the control strategy by using D and its offset d to control the output voltage and the flying capacitor voltage, it is difficult to achieve full-duty-cycle regulation of the output voltage. To achieve full-duty-cycle regulation of the output voltage, based on the circuit topology of original Buck type TL AC/AC converter, a full-duty-cycle regulated TL AC/AC converter with self-following flying capacitor is proposed, as shown in Fig.5.

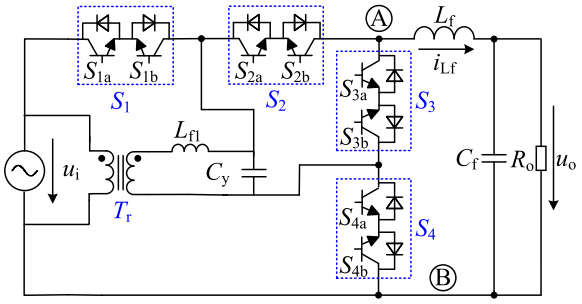


FIGURE 5. Full-duty-cycle regulated TL AC/AC converter with self-following flying capacitor.

A small volume auxiliary transformer T_r with a 2:1 turn ratio is used to directly supply voltage to the flying capacitor so that it can self-follow half of the input voltage. In order to prevent the high frequency current generated by the high frequency charging and discharging of the flying capacitor from flowing into the secondary side of the auxiliary transformer, a small inductor L_{f1} should be added between the flying capacitor and the secondary side of the transformer. The leakage inductance of the secondary side of the transformer may also be used for filtering.

When the converter works under different load, according to the polarity of u_i and i_{Lf} in one input voltage period, it can be divided into four different working stages, which are A($u_i > 0$, $i_{Lf} < 0$), B($u_i > 0$, $i_{Lf} > 0$), C($u_i < 0$, $i_{Lf} > 0$), and D($u_i < 0$, $i_{Lf} < 0$).

B. SWITCHING MODE

When $u_i > 0$, group-a switches (S_{1a}, S_{2a}, S_{3a}, S_{4a}) are on or off at a high frequency, group-b switches (S_{1b}, S_{2b}, S_{3b}, S_{4b}) are on constantly; when the input voltage $u_i < 0$, group-a switches are on constantly, group-b switches are on or off at a high frequency. When the switch is turned on and off at high frequency, the converter has four switching modes. For the convenience of analysis, the working stage B is taken as an example. The four equivalent switching mode circuits are shown in Fig.6. (At this time, group-b switches are on constantly, which are represented by short lines).

When $D < 0.5$, the control signals of switches in each switching mode are shown in Fig.7. During one switching period T_s, the operating mode sequence of the converter is switching mode 1 ($t_5 - t_6$), switching mode 3 ($t_6 - t_7$), switching mode 2 ($t_7 - t_8$), and switching mode 3 ($t_8 - t_9$). The waveform of front end voltage u_{AB} of the filter inductor and its current i_{Lf} are also shown in Fig. 7.

When $D > 0.5$, the control signals of switches in each switching mode are shown in Fig.8. During one T_s, the operating mode sequence of the converter is switching mode 4 ($t_{10} - t_{11}$), switching mode 1 ($t_{11} - t_{12}$), switching mode 4 ($t_{12} - t_{13}$) and switching mode 2 ($t_{13} - t_{14}$). The waveform of u_{AB} and i_{Lf} at $D > 0.5$ are also shown in Fig. 8.

Especially, when $D = 0.5$, the operating mode of converter only changes between switching mode 1 and 2.

C. OUTPUT FILTER

When $D < 0.5$, as shown in Fig. 7, when the circuit operates in switching mode 1 and 2, $u_{AB} = u_i - u_{Cy} = u_i/2$, and the increment of i_{Lf} is

$$\Delta i_{(Lf+)} = \frac{(\frac{1}{2}u_i - u_o)DT_s}{L_f} \tag{14}$$

When the circuit operates in switching mode 3, $u_{AB} = 0$, the reduction of i_{Lf} is

$$\Delta i_{(Lf-)} = \frac{u_o}{L_f}\left(\frac{1}{2} - D\right)T_s \tag{15}$$

When the converter is operating in steady state, the increment of i_{Lf} is almost equal to its reduction during one T_s, ie $\Delta i_{(Lf+)} = \Delta i_{(Lf-)}$. So we can get the input-output relationship of the converter when $D < 0.5$

$$u_o = Du_i \tag{16}$$

Substituting (16) into (14) and (15)

$$\Delta i_{(Lf\pm)} = \frac{(1-2D)D}{2}\frac{u_i T_s}{L_f} \tag{17}$$

For $D < 0.5$, when the input voltage u_i takes the amplitude U_{im} and D takes 0.25, the output filter inductor current

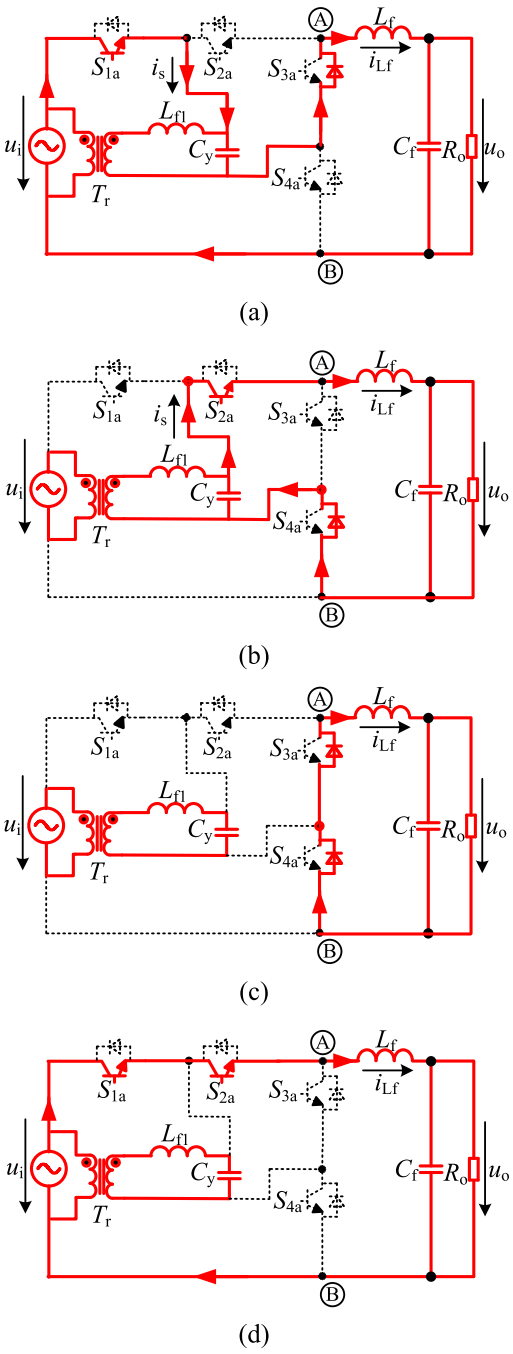


FIGURE 6. Equivalent circuit of four switching modes. (a) switching mode 1, (b) switching mode 2, (c) switching mode 3, (d) switching mode 4.

ripple Δi_{Lf} obtains the maximum value $\Delta i_{\mathrm{Lf\text{-}max}}$, which needs to be smaller than the allowed maximum current ripple ΔI_{Lf}

$$\Delta i_{Lf-\max} = \frac{U_{\mathrm{im}} T_{\mathrm{s}}}{16 L_{\mathrm{f}}} \leq \Delta I_{\mathrm{Lf}} \tag{18}$$

The output filter inductance calculation formula can be obtained

$$L_{\mathrm{f}} \geq \frac{U_{\mathrm{im}} T_{\mathrm{s}}}{16 \Delta I_{\mathrm{Lf}}} \tag{19}$$

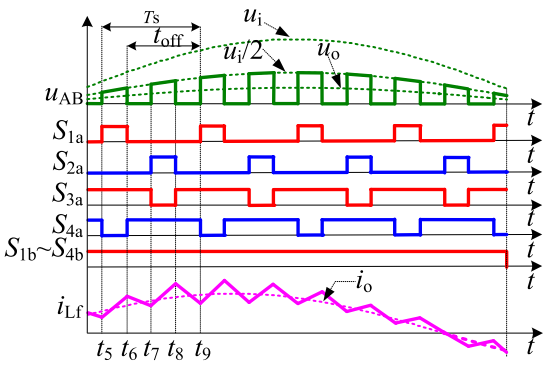


FIGURE 7. Control signals of switches, u_{AB}, and i_{Lf} when $D < 0.5$.

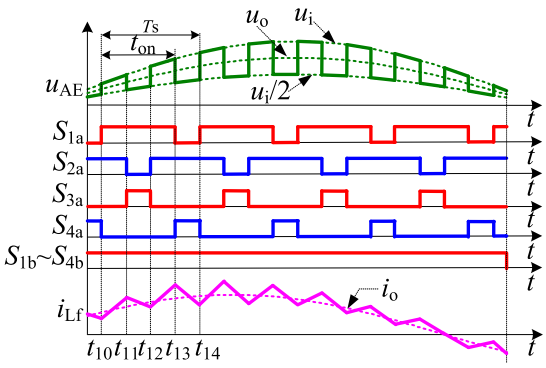


FIGURE 8. Control signals of switches, u_{AB} and i_{Lf} when $D > 0.5$.

When $D > 0.5$, as shown in Fig. 8, when the circuit operates in switching mode 4, $u_{\mathrm{AB}} = u_{\mathrm{i}}$, and the increment of i_{Lf} is

$$\Delta i_{(\mathrm{Lf}+)} = \frac{(u_{\mathrm{i}} - u_{\mathrm{o}})}{L_{\mathrm{f}}} \left(D - \frac{1}{2} \right) T_{\mathrm{s}} \tag{20}$$

When the circuit operates in switching mode 1 and 2, $u_{\mathrm{AB}} = u_{\mathrm{i}} - u_{\mathrm{Cy}} = u_{\mathrm{i}}/2$, and the reduction of i_{Lf} is

$$\Delta i_{(\mathrm{Lf}-)} = \frac{\left(u_{\mathrm{o}} - \frac{1}{2} u_{\mathrm{i}} \right)}{L_{\mathrm{f}}} (1 - D) T_{\mathrm{s}} \tag{21}$$

Similarly, $\Delta i_{(\mathrm{Lf}+)} = \Delta i_{(\mathrm{Lf}\text{-})}$. The input-output relationship of converter when $D \geq 0.5$ is obtained as same as (16). Substituting (16) into (20) and (21)

$$\Delta i_{(\mathrm{Lf}\pm)} = \frac{(1 - D)(2D - 1)}{2} \frac{u_{\mathrm{i}} T_{\mathrm{s}}}{L_{\mathrm{f}}} \tag{22}$$

For $D \geq 0.5$, when u_{i} takes the amplitude U_{im} and D takes 0.75, Δi_{Lf} obtains the maximum value $\Delta i_{\mathrm{Lf\text{-}max}}$, which is the same as (18). Therefore, when $D \geq 0.5$, the output filter inductance calculation formula is the same as equation (19).

The output filter capacitor C_{f} is used to filter out the harmonic components in the output voltage. Generally, the larger the C_{f} is, the smaller the THD (total harmonic distortion) of the output voltage is, but the reactive current component and the volume and weight of the converter will correspondingly increase. The output filter capacitor current i_{c} is the

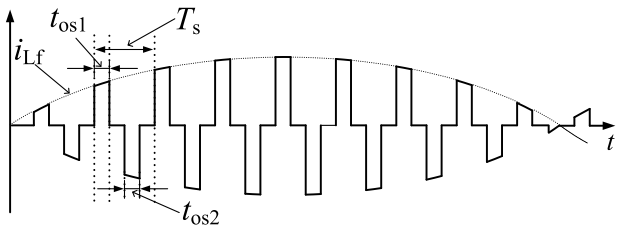


FIGURE 9. Schematic waveform of i_s.

difference between the i_{Lf} and the output load current i_o. The i_o is approximately constant during one T_s. When $D < 0.5$, the voltage ripple Δu_{Cf} on C_f is

$$\begin{aligned}\Delta u_{Cf} &= \frac{1}{C_f}\int_{\frac{1}{2}DT_s}^{\frac{1}{2}DT_s+\frac{1}{4}T_s}(i_{Lf}-i_o)dt \\ &= \frac{(1-2D)\,Du_iT_s^2}{32C_fL_f}\end{aligned} \tag{23}$$

When u_i takes the amplitude U_{im} and D takes 0.25, the output filter capacitor voltage ripple obtains the maximum value, which needs to be smaller than the maximum output filter capacitor voltage ripple ΔU_{cf} allowed, the C_f calculation formula can be obtained

$$C_f \geq \frac{U_{im}T_s^2}{256\Delta U_{Cf}L_f} \tag{24}$$

When $D \geq 0.5$, similarly the formula for calculating the C_f is the same as (24).

D. AUXILIARY TRANSFORMER

During one T_s, the flying capacitor has charging and discharging processes. The schematic waveform of the current i_s flowing through the switches to the flying capacitor is shown in Fig. 9. (Specify that the direction of i_s in switching mode 1 is positive). The i_s is a high-frequency chopping current with an envelope of $\pm i_{Lf}$. t_{os1} is the time when the switches are in switching mode 1, and t_{os2} is the time when the switches are in switching mode 2.

In an ideal state, t_{os1} and t_{os2} are exactly equal, then the flying capacitor is charged and discharged in balance during one switching period.

In the actual circuit operation, t_{os1} and t_{os2} cannot be completely equal due to the characteristics of the switches and the difference between the control circuits and the drive circuits. The fundamental current i_1 in i_s flowing into the flying capacitor is very small, which is

$$i_1 = \frac{(t_{os1}-t_{os2})}{T_s}I_{fm}\sin(\omega t-\varphi) \tag{25}$$

The secondary side of the auxiliary transformer is connected in parallel across the flying capacitor, the fundamental current i_c flowing through the flying capacitor is as shown in (7).

According to (7) and (25), the auxiliary transformer secondary current i_T can be obtained

$$\begin{aligned}i_T &= i_{Cy}-i_1 \\ &= I_{cm}\sin(\omega t+90^\circ) \\ &\quad -\frac{(t_{os1}-t_{os2})}{T_s}I_{fm}\sin(\omega t-\varphi)\end{aligned} \tag{26}$$

From the above analysis, when the voltage of the flying capacitor deviates from half of the input voltage, the auxiliary transformer can absorb or provide energy so that the flying capacitor voltage can self-follow the half of the input voltage steadily.

In an ideal state, when the converter is working stably, the auxiliary transformer only needs to provide the reactive load Q of the flying capacitor, which is

$$Q = \frac{U_{im}^2\omega C_y}{8} \tag{27}$$

In the actual circuit design, in order to facilitate the calculation, combined with (26), a margin coefficient h which is slightly larger than 1.0 is added to (27). The auxiliary transformer capacity S is estimated

$$S = hQ = \frac{hU_{im}^2\omega C_y}{8} \tag{28}$$

The selection of the capacitance value of the flying capacitor should consider that the voltage ripple on the flying capacitor formed by the high-frequency pulse current i_s should not be excessively large, otherwise the voltage stress across the switches will become large. However, if the capacitance of the flying capacitor is too large, the capacity of the auxiliary transformer will increase. When $D < 0.5$, the flying capacitor charging time $t_{os1} = DT_s$; when $D \geq 0.5$, $t_{os1} = (1-D)T_s$. In order to make the converter work in any state to meet the flying capacitor voltage ripple requirements, take $t_{os1} = 0.5T_s$. The capacitance of the flying capacitor can be calculated as follow

$$C_y \geq \frac{I_{fm}T_s}{2\Delta U_{Cy}} \tag{29}$$

where ΔU_{Cy} is the maximum ripple pulse allowed on the flying capacitor voltage.

The filter inductor L_{f1} of auxiliary transformer secondary side is mainly used to prevent the high-frequency current component caused by the flying capacitor voltage ripple from entering the secondary side of the transformer. The inductance of L_{f1} can be calculated as follow

$$L_{f1} \geq \frac{\Delta U_{Cy}T_s}{2\Delta I_T} \tag{30}$$

where ΔI_T is the maximum ripple current allowed of the secondary side of the auxiliary transformer.

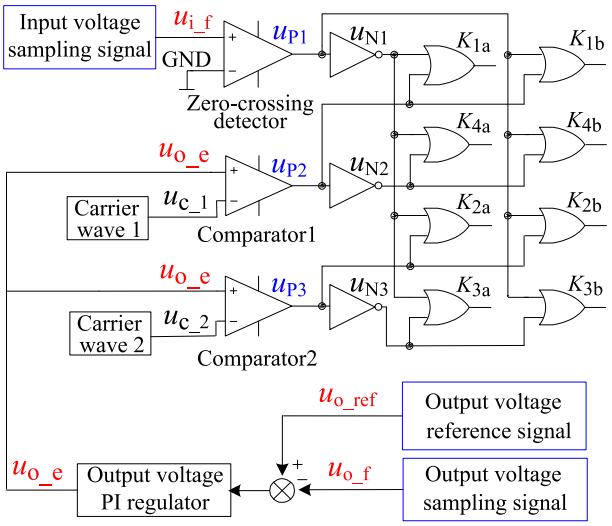


FIGURE 10. Block diagram of control strategy.

TABLE 1. Experimental parameters.

Parameter	Value	Unit
amplitude of input voltage U_{im}	$300\sqrt{2}$	V
fundamental frequency f	50	Hz
switching frequency f_s	23	kHz
power switch	IRFP460A(500V/20A)	
T filter inductor L_{fl}	0.2	mH
output filter inductor L_f	0.6	mH
flying capacitor C_y	3.3	μF
output filter capacitor C_f	4.4	μF
rated input voltage of T_r	300	V
input/output turn ratio of T_r	2:1	/
capacity of T_r	50	VA
maximum output capacity	1200	VA

IV. CONTROL STRATEGYIV

Since the presence of the auxiliary transformer ensures that the voltage of the flying capacitor can self-follow half of the input voltage steadily without any control. We just need to control the output voltage, which is simple and easy to be implemented. As shown in Fig. 10, the control block diagram only contains four parts: input voltage polarity detector, output voltage error adjustment, carrier modulation, and logic modulation.

The positive signal u_{P1} of the input sampling voltage u_{i_f} is generate by use of a zero-crossing detector. After the output voltage feedback signal u_{o_f} is compared with the output voltage reference signal u_{o_ref}, the error amplified signal u_{o_e} is obtained by the output voltage PI regulator; and then the high frequency PWM signal u_{P2} and u_{P3} are obtained after being modulated by the carrier wave u_{c_1} and the carrier wave u_{c_2} (with a phase difference of 180° from u_{c_1}), respectively. Reverse u_{P1}, u_{P2}, and u_{P3}, and get their negative signals u_{N1}, u_{N2}, and u_{N3}. Signals u_{P1} and u_{N1} are modulated with u_{P2} and u_{N2} in logical OR mode, and control signals K_{1a}, K_{1b}, K_{4a}, and K_{4b} are obtained for controlling switches S_{1a}, S_{1b}, S_{4a}, and S_{4b}, respectively. Signals u_{P1} and u_{N1} are modulated

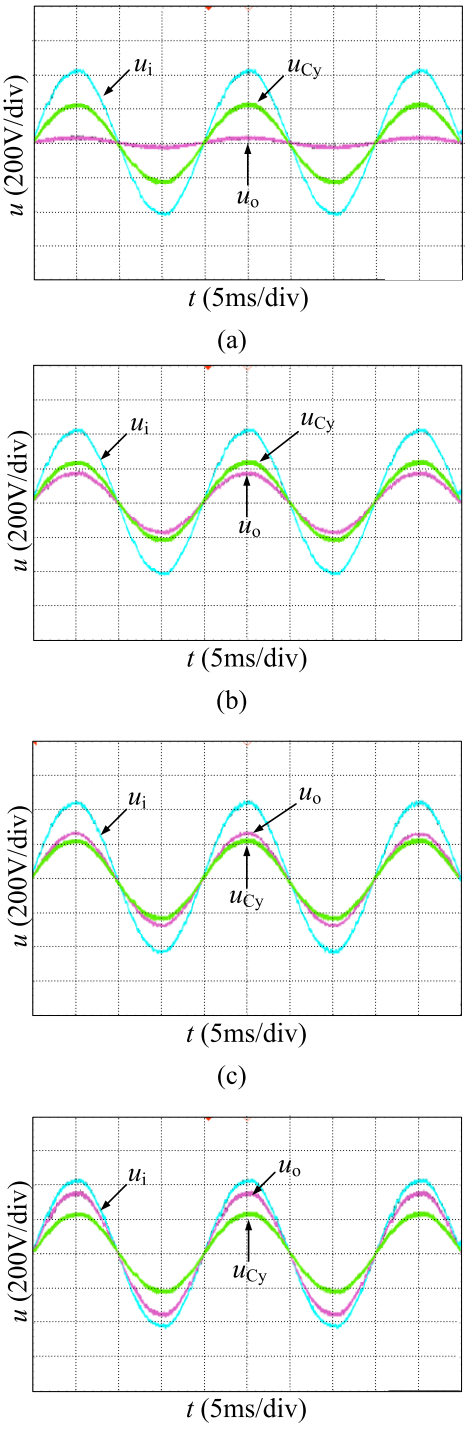


FIGURE 11. Experimental waveforms of u_i, u_{Cy}, and u_o at different D. (a) $D = 0.1$, (b) $D = 0.4$, (c) $D = 0.6$, (d) $D = 0.9$.

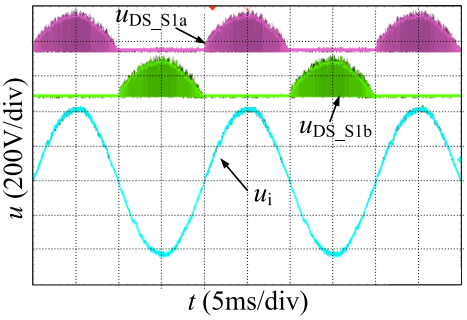
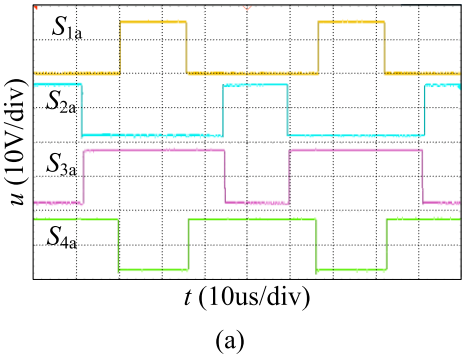


FIGURE 12. Experimental waveforms of u_{DS_S1a} and u_{DS_S2a}.



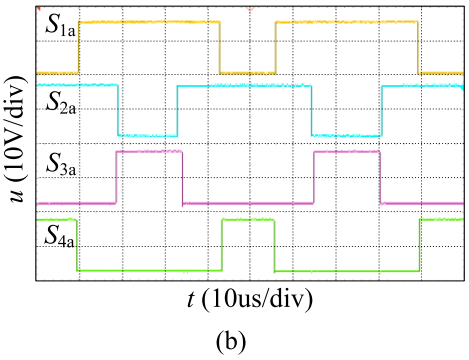


FIGURE 13. The control signal of *S*1a-*S*4a. (a) $D < 0.5$, (b) $D > 0.5$.

with u_{P3} and u_{N3} in logical OR mode, and control signals K_{2a}, K_{2b}, K_{3a}, and K_{3b} are obtained for controlling switches S_{2a}, S_{2b}, S_{3a}, and S_{3b}, respectively.

V. EXPERIMENTAL RESULTS

In order to verify the analysis above, a prototype of full-duty-cycle regulated TL AC/AC converter with self-following flying capacitor was fabricated and tested in the lab. The specifications of the prototype are as follows in TABLE 1:

Fig. 11 shows the experimental waveforms of input voltage u_i, the flying capacitor voltage u_{Cy}, and output voltage u_o when D is 0.1, 0.4, 0.6, 0.9, respectively.

As can be seen from Fig. 11, the output voltage u_o is stable at different duty cycles, and the voltage of the flying capacitor u_{Cy} self-follows half of the input voltage (u_i/2) steadily; The output voltage u_o depends on the duty cycle D,

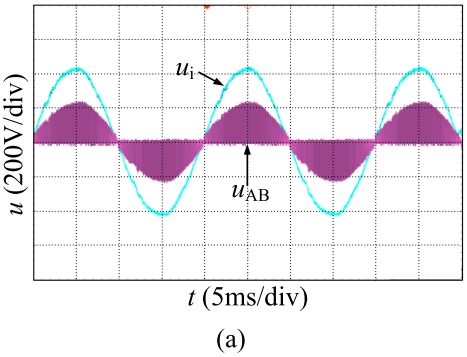


FIGURE 14. Experimental waveforms of u_{AB} and u_i when $D < 0.5$. (a) waveforms at low frequency, (b) waveforms at high frequency.

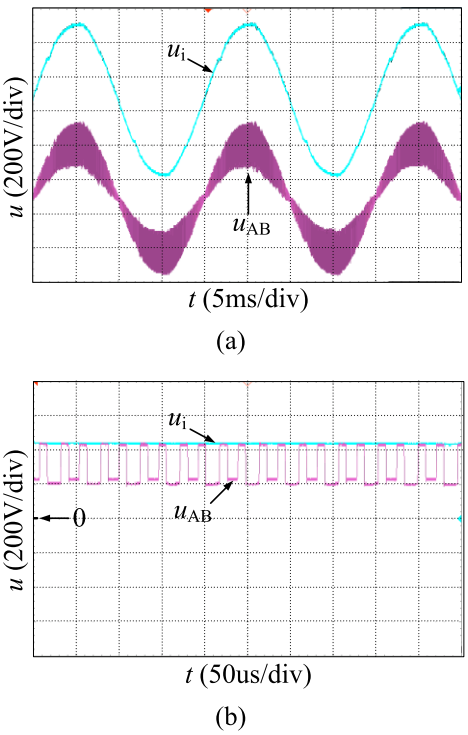


FIGURE 15. Experimental waveforms of u_{AB} and u_i when $D > 0.5$. (a) waveforms at low frequency, (b) waveforms at high frequency.

and the output voltage phase is the same as the input voltage phase.

Fig. 12 is the experimental waveform of the voltage stress of the switch S_{1a} and S_{1b}.

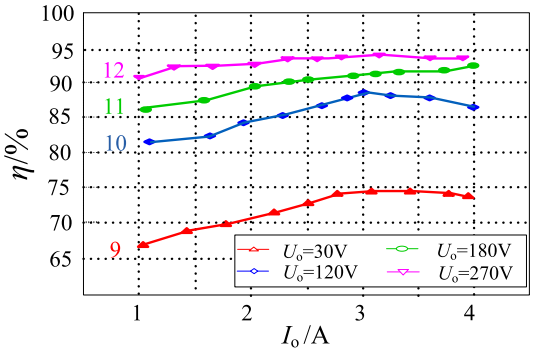


FIGURE 16. Efficiency curves at different output voltages.

As can be seen from Fig. 12, when the circuit is stable, the maximum voltage stress of the switches is $u_i/2$ due to the presence of the flying capacitor, which is half of the voltage stress of Buck type two-level AC converter.

Fig. 13 is the experimental waveform of the control signal of the switch S_{1a}, S_{2a}, S_{3a} and S_{4a}. The control signals of S_{1a} and S_{2a} have phase difference of 180°, the S_{1a} and S_{4a} control signals are complementary, so are the control signals of S_{2a} and S_{3a}.

Fig. 14 shows the experimental waveform of the u_{AB} and its expansion experimental waveform when $D < 0.5$, while Fig. 15 does these when $D > 0.5$.

As we can see from Fig. 14 and Fig. 15, when $D < 0.5$, u_{AB} changes between 0 and $u_i/2$. When $D > 0.5$, u_{AB} changes between u_i and $u_i/2$. When $D = 0.5$, it can be analyzed that u_{AB} is in a critical state between Fig. 14(a) and Fig. 15(a), namely, $u_{AB} = u_i/2$ constantly.

Fig. 16 shows the efficiency curves for four different output voltages. Curves 9, 10, 11 and 12 are efficiency curves when the output voltage is 30V, 120V, 180V, and 270V, respectively. It can be clearly seen from Fig. 16, higher the output voltage is (or larger the duty cycle is), higher the efficiency will be.

VI. CONCLUSION

1) For Buck type TL AC/AC converter with flying capacitor, the limitation of the double-target control strategy is that the output voltage can not be full-duty-cycle regulated. The proposed full-duty-cycle regulated TL AC/AC converter with self-following flying capacitor adopts a small volume auxiliary transformer, then its flying capacitor voltage is directly supplied from the auxiliary transformer and can self-follow half of the input voltage, which greatly simplifies the control circuit and its output voltage can be regulated within the range of full-duty-cycle.

2) The parameters of auxiliary transformer and output filter are deduced theoretically, and the corresponding formulas are given, and it is concluded that the auxiliary transformer capacity only needs to be slightly larger than the reactive load of the flying capacitor.

3) Experiments verify the correctness and feasibility of this circuit topology and control strategy. Experimental results show that by using this kind of circuit topology and control strategy of TL AC/AC converter, the voltage stress of the switch is halved, the output voltage can be adjusted within full duty cycle, and the structure is simple. The control strategy is easy to implement, which only needs to control the output voltage, and the output waveform is of good quality. In addition to the buck type circuits, the strategy of using auxiliary transformers can be equally applicable to other types of multilevel circuits.

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