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A 5-Gb/s 66 dB CMOS Variable-Gain Amplifier With Reconfigurable DC-Offset Cancellation for Multi-Standard Applications

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ABSTRACT This paper proposes a variable gain amplifier (VGA) with reconfigurable DC-offset cancellation (DCOC) for multi-standard applications. In this design, a cell-based design method and some bandwidth extension technologies are adopted to achieve a high data rate and a wide gain control range simultaneously. In addition, the DCOC having a tunable lower-cutoff frequency can make an optimum compromise between BER and SNR according to the specified baseband standard. The measurements show that the VGA achieves a gain control range from −6 dB to 60 dB, a bandwidth beyond 3 GHz, and a tunable lower-cutoff frequency from 0 to 300 kHz. When entering a 2^{23}-1 pseudo-random bit sequence signal at 5 Gb/s, the VGA consumes 17 mW from a 1.2-V supply and the output data peak-to-peak jitter is less than 40 ps. The VGA is fabricated in a 90-nm CMOS process with a chip size (including all pads) of 0.52×0.5 mm^2.

INDEX TERMS CMOS VGA, cell-based design, high data rate, reconfigurable, multi-standard applications.

I. INTRODUCTION

RCENTLY, the development of wireless transceivers with high data transfer rate has attracted increasing attention from both the industry and the academia [1]. Among them, the variable-gain amplifier (VGA) as a key module is allocated between RF front-end and baseband circuit to maintain the input signal amplitude within a reasonable range, which can effectively enhance the entire system dynamic range and linearity. In most broadband receivers, the VGA usually operates at low frequency but high data rate (Gb/s). For such applications, a thoughtful circuit design is needed for the VGA to ensure sufficient gain range and wide bandwidth

Fabrication of VGAs in CMOS process remains attractive for low price and ease of integration. However, compared with the high-speed III-V processes such as GaAs or InP, the inferior driving capability and the intrinsic large substrate loss of CMOS severely restrict the design of a high-gain broadband amplifier [2]. For the VGA, these drawbacks have greater impact. Particular limitations are the gain and control range in a broadband VGA. Besides, the dc offset at the input of the VGA is another critical issue, which needs to be eliminated to avoid saturating the following stages [3]. Therefore, a dc-offset cancellation (DCOC) is required, especially for high gain VGAs [4]. In DCOC, the lower-cutoff frequency (f_L) is a key specification for baseband standards [5]. For example, some signals (i.e., random binary or M-ary data) gather the most of energy at dc of the spectrum, they may be corrupted if filtered with a high f_L [6]. However, a low f_L close to dc may also cause temporary data loss under wrong initial conditions and a long loop settling time [5]. To solve this contradiction, f_L should better be adjusted according to the given system requirements. Until now, studies have rarely focused on the DCOC tuning scheme in the VGA design. In [7]–[9], digitally-assisted DCOC methods are provided with an adjustable f_L. Nevertheless, an ADC and a DAC are indispensable in the DCOC loop, which makes them unsuitable for high-speed (multi-Gb/s) applications and often consumes a relatively high dc power with increased data rate. Although there are some reconfigurable RF front-end techniques for broadband interface, some insufficiencies have

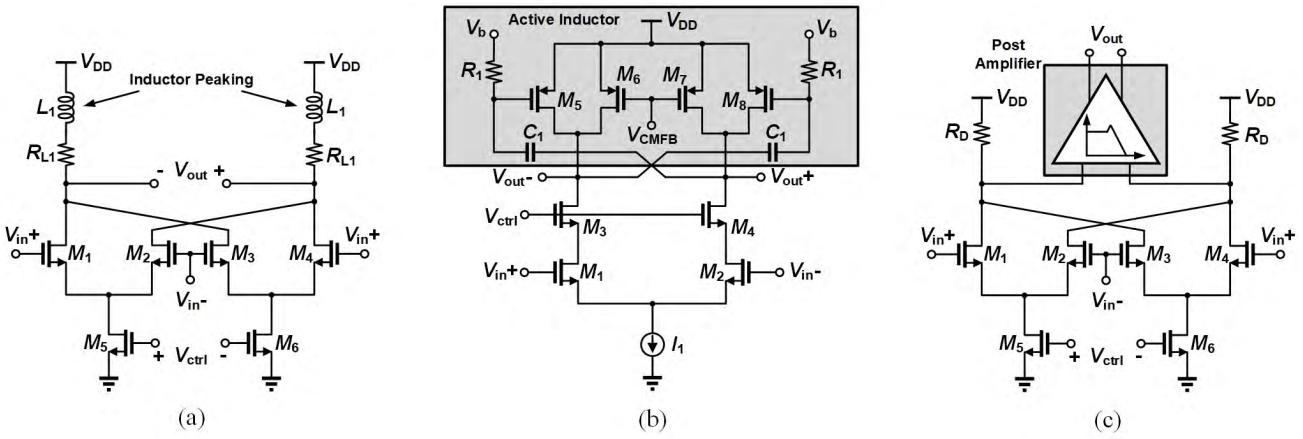


FIGURE 1. (a) Gilbert core with peaking inductor load, (b) differential cascode structure using active inductor load, and (c) Gilbert core using gain-peaking post amplifier for a fast speed.

not been solved. In [10], an active RC filter with an array of switched binary-weighted capacitors is adopted. However, it needs a lot of duplicated components to ensure a certain degree of redundancy and thus occupies a large chip area. To resolve this problem, a dual-mode complex filter [11] is realized by the opamp-based RC filter, which only requires less than 20% area occupation for the tuning components. However, it causes a more complex circuit implementation due to the high-order filters. In [12], a programmable complex integrator based on the current division network (CDN) is proposed. It has wider tuning range and higher tuning resolution, but at cost of additional power consumption and more loss in signal path owing to the use of two opamps per integrator.

In this paper, a CMOS VGA with reconfigurable DCOC is presented. By adopting a cell-based design method [13], the limitation on gain-bandwidth product (GBW) of each cascaded variable gain cell is alleviated. Thus, the gain and bandwidth of the whole VGA can be improved simultaneously. Meanwhile, other broadband technologies like the second-order active feedback and the neutralization capacitance are incorporated in the unit variable gain cell (VGC) to further enhance the bandwidth. Besides, the VGA features a reconfigurable DCOC with a voltage controlled lower-cutoff frequency, making it suitable for multi-standard applications.

II. CIRCUIT DESIGN AND ANALYSIS

Conventionally, most of wideband VGAs [14]–[16] are realized in a single variable gain stage with cascading one or several fixed gain stages. In this way, the gain range and the bandwidth are mainly determined by the variable gain stage. Besides, in order to make a gain control more efficient and not affecting the common-mode output voltage, the variable gain stage often adopts the Gilbert structure. However, it suffers from a high parasitic capacitance at the output node owing to the cross-coupled differential transistors. To eliminate this effect, Fig. 1 reviews some high-speed Gilbert structures. In Fig.1 (a), a pair of series inductors is adopted as an inductive peaking at the output load terminal [14]. This method can significantly improve the bandwidth. However, an excessive chip area may be required due to the introduction of on-chip inductors, especially when cascading multi-stage of such amplifier. To alleviate the area problem, the active inductor is an alternative to suppress the affect of the parasitic capacitance by introducing impedance peaking at the -3 dB frequency [17]. Fig. 1(b) shows the typical implementation. R_1 and C_1 together construct a high-pass network so that the high-frequency signal can be bypassed to the gate of transistors M_{5-8}, leading to positive feedback in this active load and thus a gain compensation at high frequency. Although the active inductor can save chip area, it introduces large noise, nonlinearity and additional load capacitance. In addition, since the gain-control transistors M_{1-2} operate in the triode region, extra nonlinearity may be brought when there is a large signal input, particularly at low-gain state [16]. Fig. 1(c) shows another way to make up the gain loss in high frequency. By introducing peaking in the post amplifiers rather than in the load of the gain core itself [15], a flat frequency response can be achieved if the compensated peaking is situated right in the -3 dB frequency of the variable gain core. However, due to the existence of process and temperature variations, there may be an intolerable peaking for cascaded stages of post amplifiers. Therefore, it is difficult to realize a large gain and gain control range while maintaining a high-speed operation only by using a single variable gain stage.

A. ANALYSIS OF THE CELL-BASED DESIGN METHOD

For any active device, its GBW is inherently fixed. In other words, if a single-stage amplifier achieves a high gain, then its bandwidth is limited. To solve this contradiction, the single-stage amplifier can be regarded as an individual cell for compromising its gain and bandwidth. Then, making several identical cells cascaded to obtain a high gain and a wide bandwidth simultaneously. Generally, such a cell-based

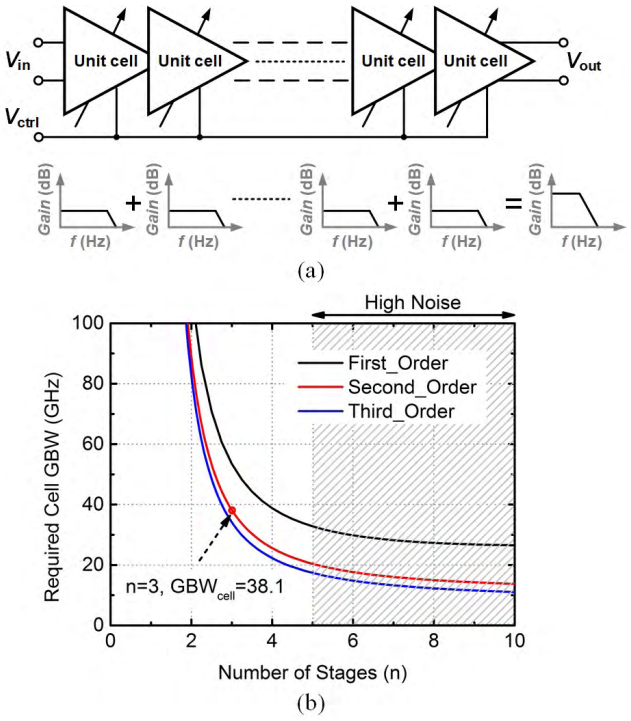


FIGURE 2. **(a) The architecture of the cell-based VGA, and (b) the required GBW vs. the number of stages for A_{tot} = 50 dB and BW_{tot} = 4 GHz.**

design method has often been employed in an amplifier requiring a wide bandwidth [18]. If this method is applied to the design of a broadband VGA, there is more space for implementation of a large gain control range by adopting a multi-stage structure. Fig. 2 shows the architecture of this cell-based VGA. Assuming that the VGA consists of n VGCs with mth-order Butterworth frequency response, the required GBW of each VGC is [2]

$$GBW_{VGC} = \frac{BW_{tot}}{\sqrt[2m]{\sqrt[n]{2}-1}}\sqrt[n]{A_{tot}} \tag{1}$$

where $A_{\rm tot}$ is the overall gain of the cascaded VGCs, $BW_{\rm tot}$ is the overall bandwidth. If $A_{\rm tot}$ = 50 dB and $BW_{\rm tot}$ = 4 GHz are targeted, the required $GBW_{\rm VGC}$ under m = 1, 2, 3 is a decreasing function of stage n as shown in Fig. 2(b). Note that the required $GBW_{\rm VGC}$ can be alleviated rapidly if using large n and m. However, with the maximum number of stage and order, some practical factors also need to be considered, i.e., power consumption and noise. Power consumption increases with the large n and m. In addition, it results in a reduced gain per stage due to a fixed total gain and thus makes a rapid noise accumulation from the gain stages. As a result, the input-referred noise figure (NF) of the whole VGC stage is significantly degraded. This effect can be quantified by [19]

$$\frac{NF_\infty - 1}{NF_p - 1} = \frac{1}{1 - 1/A_p} \tag{2}$$

where NF_∞ denotes the NF of an infinite number of cascaded gain stages, $NF_{\rm p}$ is the NF of each gain stage and $A_{\rm p}$ is the gain of each stage. Therefore, n = 3 and m = 2 are chosen to trade-off power consumption, GBW, and NF in this design.

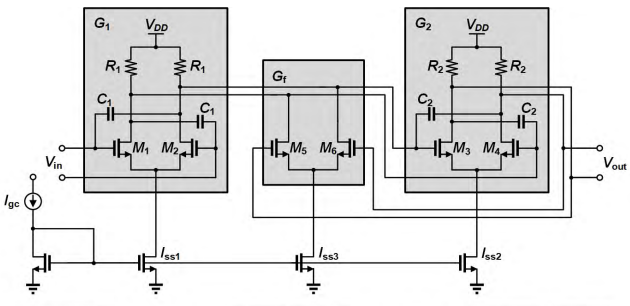
It is significant to note that the gain range of the VGA can be enlarged effectively by cascading multiple VGCs, but there still exists some challenges in implementation of such a cell. Firstly, the gain error of each cell must be as small as possible to keep the whole accumulated error not exceed the accepted value. Secondly, since a very wideband cell is required due to the gain-bandwidth tradeoff, then some broadband techniques are indispensable for the cell design. Thirdly, the cell should be designed with low power consumption and minimum chip occupation, or else that the total cost of the entire VGA will be excessive. Accordingly, a simple topology is preferred while it is helpful to achieve a wide bandwidth owning to the inherently less parasitic capacitance.

B. DESIGN OF THE VGC WITH EXTENDED BANDWIDTH

The bandwidth of the overall cascaded VGCs is given by

$$BW_{tot} = BW_{cell}\sqrt[2m]{\sqrt[n]{2}-1} \tag{3}$$

where $BW_{\rm cell}$ is the bandwidth of unit VGC. Note that the total bandwidth of the VGA will decrease with the number of n. Thus, each VGC should have a sufficient bandwidth space to allow for this shrinkage. To enhance the bandwidth of the VGC without sacrificing large chip area or voltage headroom, a second-order gain structure with active feedback is employed. Fig. 3 shows the schematic, where G_1, G_2 are the gain stages and $G_{\rm f}$ is the feedback stage. The $G_{\rm f}$ consists of a differential pair ($M_5 \sim M_6$) with a shared resistive load R_1 to make a trade-off between bandwidth and gain.



Parameter	$W/L_{1\text{-}4}$	$W/L_{5\text{-}6}$	$W/L_{ss1\text{-}ss2}$	W/L_{ss3}	R_1, R_2	C_1	C_2
Value	40μm/0.1μm	4μm/0.1μm	30μm/0.5μm	4μm/0.5μm	408 Ω	28 fF	26 fF

FIGURE 3. **Schematic of the 2-order VGC using active feedback.**

For the convenience of analysis, both the gain and feedback stages can be expressed by the single-pole response functions:

$$G_1(s) = G_2(s) = \frac{G_m R}{1 + sRC} \tag{4}$$

$$G_f(s) = \frac{G_{mf} R}{1 + sRC} \tag{5}$$

where R is the resistive load, C is the parasitic capacitance of the differential pairs, and the corresponding transconductances of the stages are $G_{\rm m}$ and $G_{\rm mf}$. Since a fraction of

output signal is returned to the input of G_1 by G_f, the transfer function of the second-order VGC is thus given by

$$H_{2nd}(s) = \frac{G_m^2 R^2}{(1+sRC)^2 + G_m G_{mf} R^2} = \frac{A_0^2}{(1+s/\omega_0)^2 + A_0\beta} \quad (6)$$

where $\omega_0 = 1/RC$, $A_0 = G_m R$ and $\beta = G_{mf} R$. So the first dominant pole is

$$\omega_{p1} = -\omega_0(1+\sqrt{A_0\beta}) \quad (7)$$

Since the −3 dB bandwidth is determined by the first dominant pole, the bandwidth can be effectively enhanced by using a large feedback gain β. However, considering that the associated gain peaking is also in proportion with the feedback gain β [2], the ratio of feedback should be selected within a reasonable range. Otherwise, the accumulated gain peaking (when multiply VGCs are cascaded) becomes serious, which will cause system instability. Thus, other methods need to be employed to further optimize the bandwidth. Note that the ω_0 is inversely proportional to capacitive loads C. By reducing the input capacitance of G_1, G_2 can reduce the capacitive load of the previous stage and then enhance the bandwidth. Therefore, two pairs of neutralization capacitance are placed in parallel with the differential transistors $M_1 \sim M_2/M_3 \sim M_4$. These neutralization capacitances are realized by exploiting the Miller-effect. The effective input capacitance seen at the input of G_1, G_2 is given by

$$C'_{eff-in} = C_{in} + (1-A)C_1 \quad (8)$$

where A is the gain of G_1, G_2, C_{in} is the original input capacitance of G_1, G_2, C'_{eff-in} is the effective input capacitance. If $A > 1$, the Miller capacitance $(1\text{-}A)C_1$ becomes negative, leading to a reduced C'_{eff-in}.

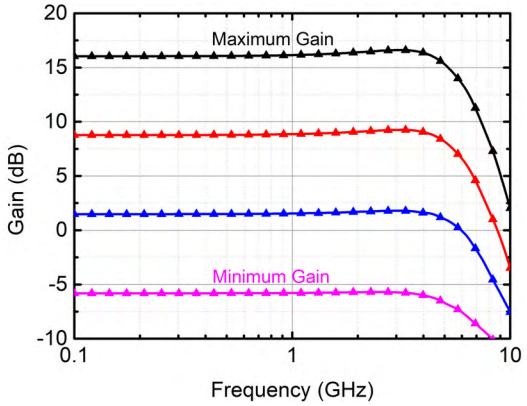


FIGURE 4. Simulated frequency response of the optimized VGC.

Fig. 4 shows the simulated frequency response of the optimized VGC, where the bandwidth is beyond 5 GHz with a maximum gain of 16 dB. Besides, the stability problem of each VGC also needs to be considered due to the introduction of the feedback structure. The simulated open-loop phase

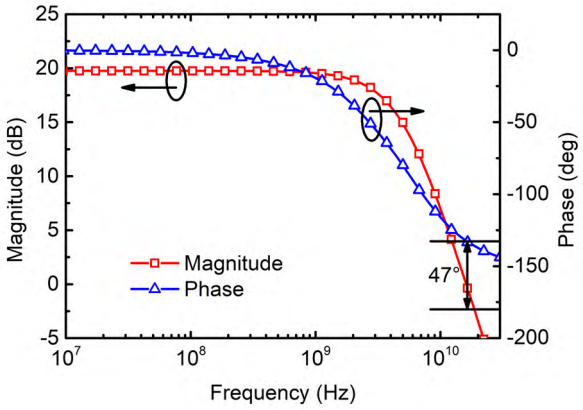


FIGURE 5. Simulated frequency response of the VGC at maximum gain.

margins of the VGC at all gain states are beyond 45 degrees while the maximum gain is about 47 degree as shown in Fig. 5, which can ensure a sufficient stability.

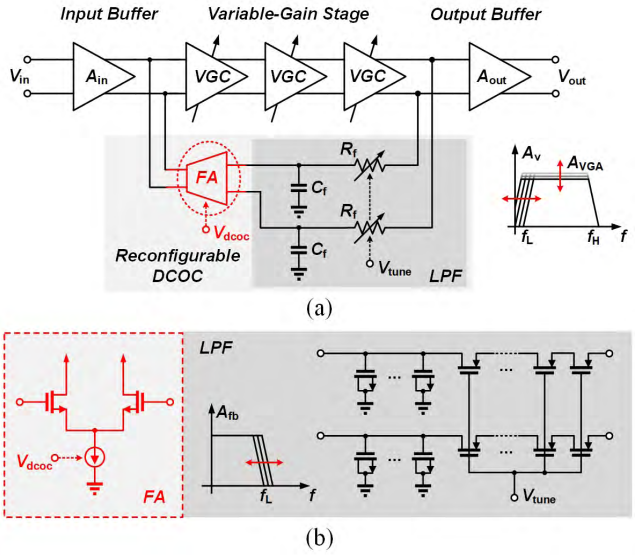


FIGURE 6. (a) Block diagram of the proposed VGA and (b) sub-circuits of the reconfigurable DCOC.

C. PROPOSED DCOC WITH TUNABLE LOW-CUTOFF FREQUENCY

Fig. 6(a) shows the block diagram of the proposed VGA, including an input buffer, a three-stage VGC, a reconfigurable DCOC and an output buffer. The input buffer employs a differential common-source amplifier with a gain of 13.1 dB. The output buffer is designed for the practical application and measurement requirements with a gain of 0 dB. Since it needs to provide a large current to keep an adequate output swing for an input impedance of 50-Ω, a f_T doubler topology [18] is adopted to relax the limited bandwidth owing to using large-size transistors. The reconfigurable DCOC in this VGA comprises a LPF and a feedback amplifier (FA)

as shown in Fig. 6(b). The LPF extracts the dc component from output of the variable gain stage and then transfers it to the FA for generating a correction current. Generally, the values of componentsC_f and R_f in LPF design are very large as the frequencies tend to dc. To avoid excessive chip size and facilitate control, multiple NMOS transistors in parallel are used to construct a large shunt capacitor and several PMOS transistors operating in triode region are also cascaded to realize an adjustable resistor that can cover the required frequency range. The large shunt capacitance C_f is designed to have a fixed value. The source and drain of the NMOS transistor are connected to ground as the bottom plate of the equivalent capacitor while the gate is used as the top plate. The channel resistance R_{on} from drain to source in the PMOS transistor is linear and can be controlled by its gate voltage V_{tune} [20]. It follows that,

$$R_{on} = \frac{1}{\mu_p C_{ox} \frac{W}{L}(V_{DD} - V_{tune} - |V_{TH}|)} \tag{9}$$

where μ_p is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W/L is the aspect ratio of the PMOS transistors and V_{TH} is the threshold voltage. By changing the control voltage V_{tune}, the value of R_{on} changes and then the f_L of the VGA can be varied.

In addition, the DCOC function is controlled by a MOS switch. When $V_{dcoc} = 1.2$ V, the DCOC does not work. The VGA exhibits a low-pass characteristic and thus the dc component is permitted to enter the baseband. When $V_{dcoc} = 0$ V, the DCOC function is enabled. By tuning the f_L, the receiver front-end interface can be configured flexibly according to the specified baseband standard. As a result, the whole circuit can achieve an improved SNR and a high efficiency in baseband processing without sacrificing the BER specification.

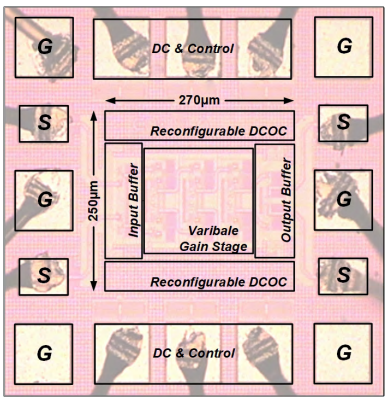


FIGURE 7. Die photo of the fabricated VGA.

III. MEASUREMENT RESULTS

Fig. 7 shows a die microphotograph of the proposed design. Fabricated in a 90-nm CMOS process, the chip size of the VGA is 0.52×0.5 mm^2, including all the measurement pads. The circuit has been measured by Chip-on-Board (COB). Under a 1.2-V supply voltage, the VGA consumes a total dc power of 17 mW.

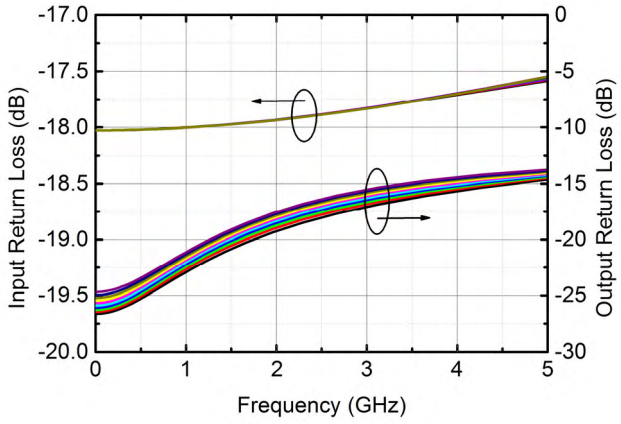


FIGURE 8. Measured return loss vs. various control currents I_{gc} at input and output ports.

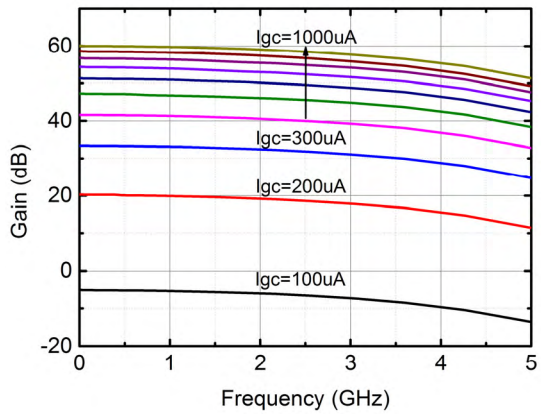


FIGURE 9. Measured voltage gain in various control currents I_{gc} vs. frequency.

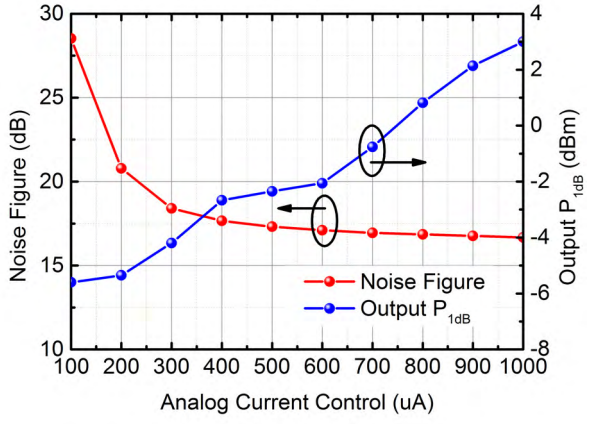


FIGURE 10. Measured NF and OP_{1dB} at 1 GHz vs. various control currents I_{gc}.

Fig. 8 shows the measured return loss vs. control current I_{gc} at input and output ports. The values of these two ports are better than 10 dB within the entire operating frequency range. Fig. 9 shows the measured tunable gain range from −6 to 60 dB with a −3 dB bandwidth beyond 3 GHz.

TABLE 1. Performance comparison of the state-of-the-art VGAs.

Ref.	Tech.	Control mode	Freq. (GHz)	Gain range (dB)	Data rate (Gb/s)	NF (dB)	Jitter (pp)	OP_{1dB} (dBm)	Reconfig. DCOC	Power (mW)	Chip Area (mm^2)
[15] 2012 JSSC	0.13-μm SiGe BiCMOS	Analog voltage	0.0002-7.5	-10 to 30	5	--	40 ps	-	N	72*@1.2V	1*
[21] 2012 TCSI	90-nm CMOS	Analog voltage	0.0002-2.2	-10 to 50	-	17 to 30	-	-3	N	2.5 @1.0V	0.7
[22] 2013 RFIC	65-nm CMOS	Digital current	0.02-1	+3 to +31	-	6 to 21	-	0	N	48 @1.1V	1**
[23] 2014 TMTT	0.18-μm SiGe BiCMOS	Digital current	0.003-1.17	-1.4 to 30.2	2	24 to 52	-	-10	N	35 @1.8V	0.25***
[24] 2016 MWCL	65-nm CMOS	Analog current	(0~0.0002) -4	-39.4 to 20.2	-	10 to 27	-	-9.8	Y	26 @1.2V	0.32
[16] 2016 JSSC	0.13-μm CMOS	Analog voltage	0.0001-5	-15 to 25	10	-	44 ps	-	N	50 @1.2V	1.07
[25] 2016 TMTT	65-nm CMOS	Analog voltage	0.0004-2	2 to 24	-	24 to 29	-	1.8	N	3.5*** @ 1.2V	0.01***
This work	**90-nm CMOS**	**Analog current**	**(0~0.0003) -3.3**	**-6 to 60**	**5**	**15.2 to 29**	**39 ps**	**3**	**Y (0-300kHz)**	**17 @1.2V**	**0.26**

*=With Temperature Compensation Block; **=With Digital Control; ***= VGA core only

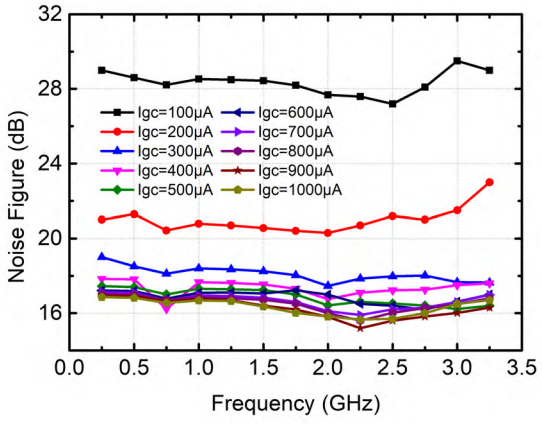


FIGURE 11. Measured NF vs. frequency under various control currents I_{gc}.

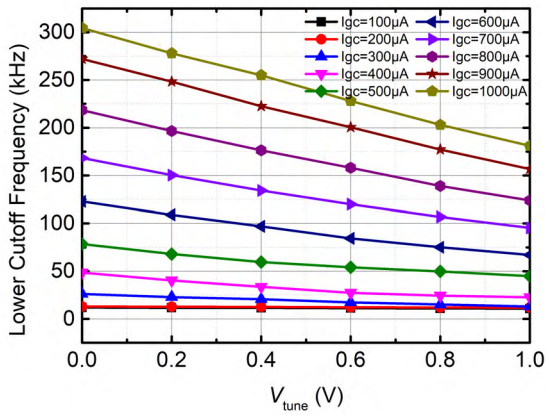


FIGURE 12. Measured f_L of the reconfigurable DCOC vs. V_{tune} at different gains.

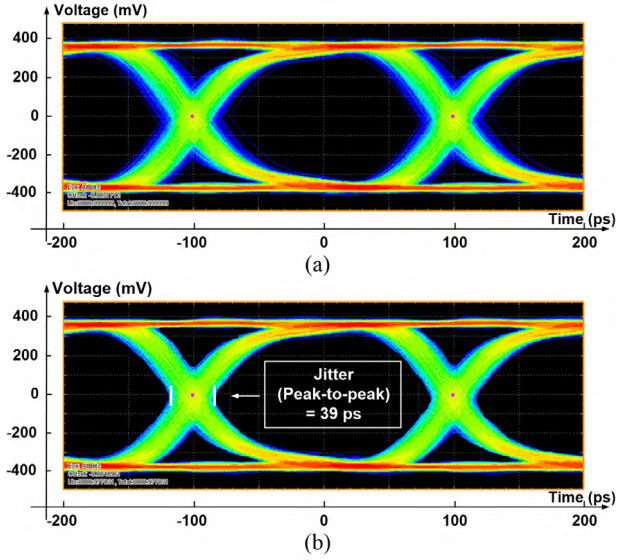


FIGURE 13. Measured output eye diagram at (a) 5 mVpp, (b) 20 mV_{pp}, 5 Gb/s 2^{23}-1 PRBS input data (Horizontal scale: 50 ps/div, Vertical scale: 100 mV/div).

Fig. 10 shows the NF and output P_{1dB} with control current I_{gc} ranging from 100 μA to 1000 μA in 100 μA steps at 1 GHz. The NF is from 16.7 to 33.5 dB and the OP_{1dB} is 3 dBm at maximum gain (I_{gc} =1000 μA). Moreover, Fig. 11 shows the NF vs. frequency under various control currents I_{gc}. The lower cutoff frequency f_L of the reconfigurable DCOC is verified by varying the V_{tune} from 0 to 1 V after activating this function (V_{dcoc} = 0 V). The obtained f_L at different gains are shown in Fig. 12. The output eye diagram and data jitter of the VGA are characterized by a Tektronix AWG7000 arbitrary waveform generator and a Tektronix MSO71604C oscilloscope. Fig. 13 shows the output eye diagrams under 5 Gb/s 2^{23}-1 PRBS signals with different input swings. Both of them have a vertical eye opening larger than 300 mV. Under an input signal level of 20 mV, the peak-to- peak jitter for 5 Gb/s is 39 ps.

Table 1 summarizes and compares the performance of this VGA with other previous reported works [15]–[16], [21]–[24]. The proposed VGA has wider bandwidth,

larger gain and gain control range as compared to the works [21]–[24]. Although the design in [15] and [16] has an excellent data rate than the proposed VGA design, they occupy a relatively large power consumption and chip area. Moreover, this work realizes a reconfigurable DCOC, attaining a tunable lower cutoff frequency range.

IV. CONCLUSION

A CMOS variable gain amplifier with reconfigurable DCOC for multi-standard applications has been demonstrated in this work. Since a cell-based design method and some bandwidth extension technologies are adopted, a gain control range of 66 dB and a data rate up to 5 Gb/s are achieved simultaneously with a small data jitter of 39 ps. Moreover, the reconfigurable DCOC with tunable f_L from 0 to 300 kHz provides an optimum compromise between BER and SNR requirements of the specified baseband standard. Accordingly, the VGA can be well utilized in high-speed transceiver systems sustaining multiple baseband standards. Meanwhile, its design concepts with non-passive inductor topology can be also easily migrated to more advanced CMOS technologies (e.g., 40 nm or 28 nm) for further improving bandwidth and data rate without robustness concerns and sacrificing other performances.

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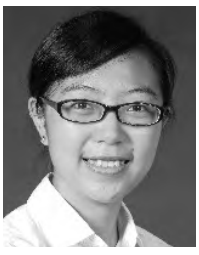

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