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A New Circuit Design of Two-Switch Buck-Boost Converter

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ABSTRACT A conventional two-switch buck–boost (TSBB) converter can operate in buck, boost, and buck–boost modes. This paper introduces a new topology for a two-switch buck–boost converter with the same operation modes. However, the proposed TSBB converter has fewer conductions and switching components than the conventional TSBB converter, which reduces the power losses.

INDEX TERMS Converter, buck converter, boost converter, buck–boost converter, TSBB converter, voltage stress, switching loss, conduction loss, MOSFET, switch, diode, inductor current.

I. INTRODUCTION

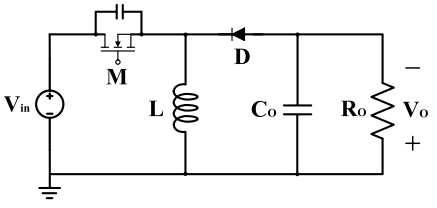
Many electric systems use DC/DC converters. These converters are applied in various portable devices such as laptop computers and mobile phones, as well as power systems such as direct-current (DC) micro grids, high voltage DC (HVDC) systems, and energy storage systems (ESS). The conversion efficiency of DC/DC converters is a key factor in maintaining long device life and reducing energy consumption. Therefore, it is necessary to develop high efficiency DC/DC converters [1], [2].

A single-switch buck–boost (SSBB) converter can either step-up or step-down input voltages. An SSBB converter is composed of a single switch, diode, and inductor and has a highly simple structure. The step-up or step-down input voltages of the SSBB converter is determined by the duty ratio of the switch. Using the duty ratio D of the switch, equation (1) describes the output-to-input voltage conversion ratio of an SSBB converter in the continuous conduction mode (CCM).:

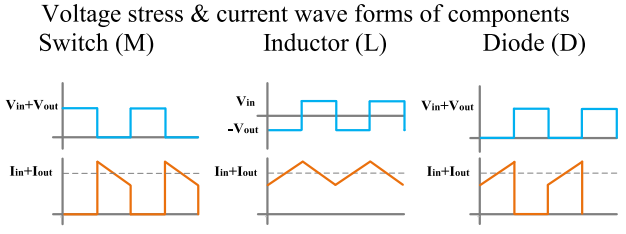
$$\frac{V_{out}}{V_{in}} = -\frac{D}{1-D} \tag{1}$$

As shown in equation (1), an SSBB converter is known as inverting or negative buck–boost converter. This equation shows that D determines whether the output voltage is higher or lower than the input voltage. If D is greater than 0.5, the output voltage is larger than the input voltage, and the converter steps up the input voltage. If D is less than 0.5, the output voltage is lower than the input voltage, and the converter steps step down the input voltage [3].

Fig. 1(a) shows a circuit diagram of an SSBB converter, and Fig. 1(b) shows the voltage stresses and current wave forms of the SSBB converter components in CCM. However, SSBB converters have several disadvantages. The polarity



(a)



(b)

FIGURE 1. Circuit diagram of (a) single switch buck–boost (SSBB) converter and (b) voltage stresses and current wave forms of SSBB converter components in CCM.

of the output voltage of an SSBB converter is opposite that of the input voltage, which can be seen in the equation (1). Therefore, an inverting or negative buck–boost converter is not appropriate for applications that require a positive output voltage. The voltage stresses of components of an SSBB converter are the sum of the input voltage and output voltage.

Several types converters have been proposed to solve the inverting output problem, such as single-end primary inductor converter (SEPIC), zeta converter, and two-switch buck-boost (TSBB) converter. These converters have a positive or non-inverting output voltage. However, compared with a basic inverting buck-boost converter (the SSBB), all three of these non-inverting converters require additional power components. The zeta converter and the SEPIC converter have an additional inductor and capacitor, while the TSBB converter has an additional MOSFET and diode [3]–[5].

Fig. 2 shows a circuit diagram of the three types of non-inverting converters. Because the zeta converter and SEPIC converter have an additional inductor and capacitor, they have larger size, resulting in higher losses in the energy conversion and low power density. Hence, these converters are not suitable for larger power applications [4], [5].

A TSBB is based on a simplified cascade connection of a buck converter and boost converter. Fig. 2 (d) shows the voltage stress and current wave form of the TSBB in buck–boost mode. Although a TSBB converter has additional components compared to an SSBB converter, the TSBB converter has the same polarity of the output voltage as the input voltage, lower voltage stress of the components, a simple structure, and easy miniaturization. For these reasons, the TSBB converter has been widely applied in power applications. A TSBB converter can be operated in buck, boost, and buck–boost mode by controlling the active switches M_1 and M_2. If M_1 and M_2 are switched on and off simultaneously, the TSBB converter behaves like an inverting buck–boost converter and is the same as an SSBB converter. To operate in buck mode, M_1 is controlled, and M_2 is always in the OFF state. When M_1 is always ON and M_2 is controlled, the TSBB converter operates in boost mode. In contrast, an SSBB converter only operates in buck–boost mode [2], [4], [6]. However, the TSBB converter still has the disadvantages resulting from the additional components compared with an SSBB converter. When the switches are turned on, conducting components are L and M_1 or M_2. When the switches are turned off, the conducting components are L and D_1 or D_2. Thus, one additional switch and diode are conducting in each subperiod, and the conventional TSBB converter has higher conduction and switching losses [2], [4], [6], [7]. To solve these problems, this paper proposes a new TSBB topology. The proposed converter has a single inductor, two switches, and two diodes. It can operate in buck mode, boost mode, and buck–boost mode like a conventional TSBB converter. The voltage stresses can also be lower than that of the SSBB converter, or the number of conducting components can be reduced compared to a conventional TSBB converter in each mode. As a result, the proposed TSBB converter has lower power losses and higher efficiency than a conventional TSBB converter.

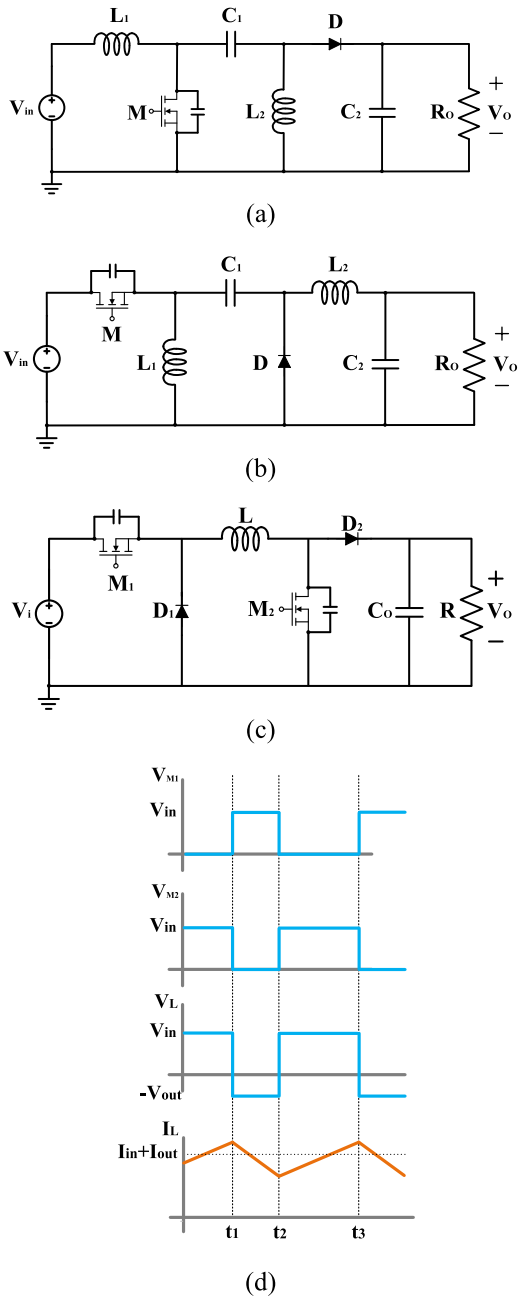


FIGURE 2. Circuit diagram of (a) single-end primary inductor converter (SEPIC) (b) zeta converter (c) two-switch buck–boost Converter (TSBB) and (d) voltage stresses and current wave forms of TSBB converter components in buck–boost mode.

Section II discusses the operational principles of the conventional TSBB converter and the proposed TSBB converter in buck, boost, and buck-boost modes. Section III shows the analysis of the power loss, conduction loss, switching loss, and voltage stress. Experimental results are shown in Section VI, and conclusions are presented in Section V.

II. OPERATION PRINCEPLES

A. CONVENTIONAL TSBB CONVERTER

The conventional TSBB converter has a single inductor, two switches, and two diodes. It is a cascaded combination of a buck converter and a boost converter. A circuit diagram of a conventional TSBB converter is shown in Fig. 2 (c). The conventional TSBB converter can change operation modes by controlling the gate signals of switches M_1 and M_2. Table 1 shows a control scheme to determine the converter's modes.

TABLE 1. Switch operation of a conventional TSBB converter in each mode.

Mode	Switch operation	
	M_1	M_2
Buck	On	Off
	Off	Off
Boost	On	On
	On	Off
Buck–boost	On	On
	Off	Off

B. PROPOSED TSBB CONVERTER

Fig. 3 shows a circuit diagram of the proposed TSBB converter. The voltage conversion ratio of the proposed converter in CCM is:

$$V_o = \frac{d_1}{1 - d_2} V_{in} \tag{2}$$

where d_1 and d_2 are the duty cycles of switch M_1 and M_2, respectively. If d_2 is 0, the converter operates in buck mode. In this mode, M_2 is always off and M_1 is controlled to regulate the output voltage. If d_1 is 1, the converter operates in boost mode, M_1 is always on, and M_2 is controlled to regulate the output voltage. If M_1 is always off and M_2 is switched, the converter operates in buck–boost mode, and the duty ratio of d_1 and d_2 is the same. When the duty ratio is less than 0.5, a conventional TSBB converter operates in step down input voltages. When the duty ratio is higher than 0.5, it operates in step up input voltages. Table 2 presents the switch control scheme of the proposed converter in each mode [2], [6], [7].

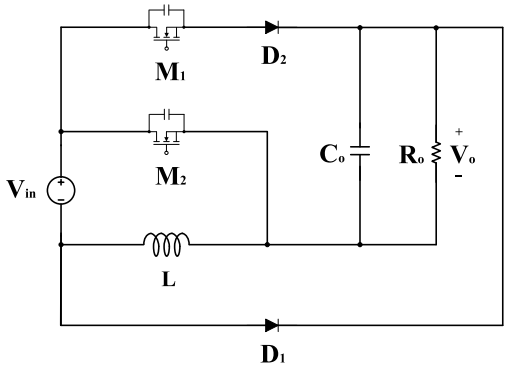


FIGURE 3. Circuit diagram of the proposed TSBB converter.

TABLE 2. Switch control scheme of the proposed TSBB converter in each mode.

Mode	Switch Operation	
	M_1	M_2
Buck	On	Off
	Off	Off
Boost	On	On
	On	Off
Buck–boost	Off	On
	Off	Off

Table 3 (a) presents the conducting semiconductors of the conventional TSBB and the proposed TSBB converter, and Table 3 (b) shows the switching semiconductors. The tables show that the proposed converter has fewer conductors and semiconductors than the conventional converter. Section III discusses the power loss in terms of the conduction loss, switching loss, and voltage stress [2], [6], [7].

TABLE 3. Conducting and switching semiconductors of a conventional TSBB and the proposed TSBB converter: (a) conducting semiconductors and (b) switching semiconductors.

Mode	Subinterval	Conventional TSBB converter	Proposed TSBB converter
Buck	subinterval 1	M_1, D_2	M_1, D_2
	subinterval 2	D_1, D_2	D_1
Boost	subinterval 3	M_1, M_2	M_2
	subinterval 4	M_1, D_2	M_1, D_2
Buck–boost	subinterval 5	M_1, M_2	M_1
	subinterval 6	D_1, D_2	D_1

(a)

Mode	Conventional TSBB converter	Proposed TSBB converter
Buck	M_1, D_1	M_1, D_1, D_2
Boost	M_2, D_2	M_2, D_2
Buck–boost	M_1, M_2, D_1, D_2	M_2, D_1

(b)

Fig. 4 shows the current flows of the proposed TSBB converter circuit in buck mode, boost mode, and buck–boost mode.

The red lines indicate the current path in each subinterval, and the conducting and switching semiconductors can be observed. For example, in buck mode, the current path of subinterval 1 passes M_1 and D_2, and the current path of subinterval 2 passes D_1. Therefore, in the whole buck mode period, the conducting semiconductors are M_1, D_1, and D_2, and the switching semiconductors are M_1, D_1, and D_2.

TABLE 4. Comparison of component voltage stress in each TSBB converter.

Type	mode	M_1	M_2	D_1	D_2
The single switch buck–boost converter	buck–boost	$V_{in} + V_{out}$	N/A	$V_{in} + V_{out}$	N/A
The conventional TSBB converter	buck	V_{in}	V_{out}	V_{in}	N/A
	boost	N/A	V_{out}	V_{in}	V_{out}
	buck–boost	V_{in}	V_{out}	V_{in}	V_{out}
The proposed TSBB converter	buck mode	$\frac{C_{D2}}{C_{M1}+C_{D2}}V_{in}$	$V_{in}+V_{out}$	V_{in}	V_{out}
	boost	N/A	V_{out}	$V_{in}+V_{out}$	V_{out}
	buck–boost	$\frac{C_{D2}}{C_{M1}+C_{D2}}V_{in}$ OR $\frac{C_{D2}}{C_{M1}+C_{D2}}V_{out}$	$V_{in}+V_{out}$	$V_{in}+V_{out}$	$\frac{C_{M1}}{C_{M1}+C_{D2}}V_{in}$ OR $\frac{C_{M1}}{C_{M1}+C_{D2}}V_{out}$

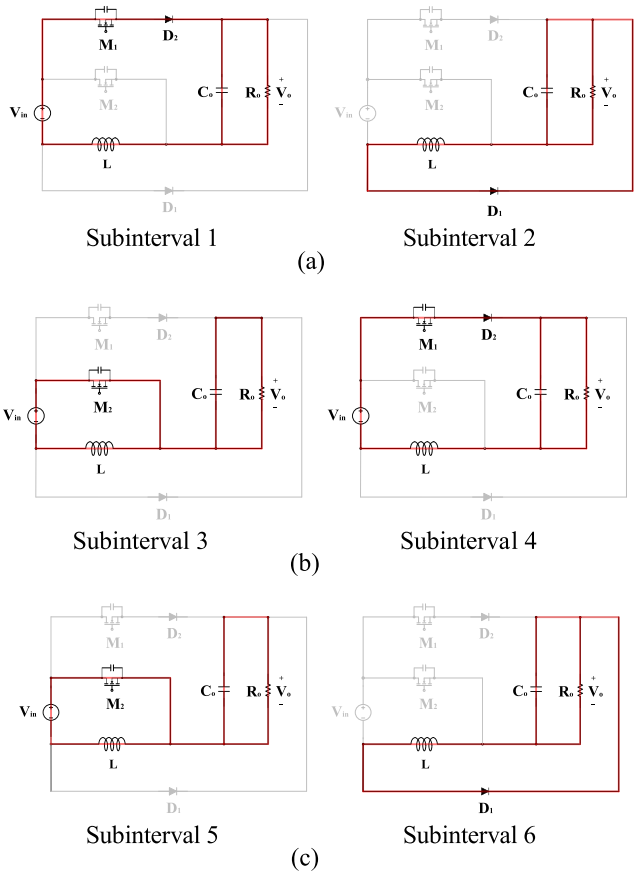


FIGURE 4. Operation mode of the proposed TSBB converter. (a) Buck mode. (b) boost mode. (c) Buck-boost mode.

III. ANALYSIS OF POWER LOSS, CONDUCTION LOSS, SWITCHING LOSS, AND VOLTAGE STRESS

As shown in Table 4, the conventional TSBB converter has lower voltage stress than an SSBB converter. However, the conventional TSBB converter has additional semiconductors, resulting in reduced voltage stresses and more power dissipation [2]–[7]. The circuit configurations of the single SSBB converter, conventional TSBB converter, and proposed TSBB converter include resistors, inductor, capacitors, switches, and diodes. The resistors, inductors, and capacitors are common to all of the circuits. However, the TSBB converters have additional components (a switch and diode). This paper focuses on the power loss of the MOSFET switches and diodes.

The power loss in switch mode operation can be divided into three parts: conduction loss, switching loss, and leakage (blocking) loss. Usually, leakage loss can be ignored. Therefore, the power loss can be simply expressed by equation (3) based on the semiconductors:

$$P_{loss} = P_c + P_{sw} + P_{leak} \approx P_c + P_{sw} \tag{3}$$

where P_{loss} is the total power losses in the semiconductors, P_{con} is the conduction loss, P_{sw} is the switching loss, and P_{leak} is the leak loss [8]. Normally, conduction loss occurs during the current flow through the MOSFET switches or diodes, and switching loss comes from the dynamic voltages and currents of the MOSFET switches or diodes during the on or off time. For the power MOSFET switch and diode, the power loss is expressed by equations (4) and (5), respectively:

$$P_{loss,M} = P_{c,M} + P_{sw,M} \tag{4}$$

$$P_{loss,D} = P_{c,D} + P_{sw,D} \tag{5}$$

where $P_{loss,M}$ is the total power loss, $P_{c,M}$ is the conduction loss, and $P_{sw,M}$ is the switching loss of the power MOSFET. For the diode, $P_{loss,D}$ is the total power losses, $P_{c,D}$ is the conduction loss, and $P_{sw,D}$ is the switching loss [8]–[10].

In equation (4), the power MOSFET losses are split into conduction losses and switching losses. The power MOSFET conduction losses can be simply decided based on the drain-to-source resistance in the ON state ($R_{DS,on}$).

$$v_{DS}\,(i_{DS}) = R_{DS,on}\,(i_{DS}) \cdot i_{DS} \tag{6}$$

where v_{DS} and i_{DS} are the drain-to-source voltage and current of the power MOSFET.

$$P_{c,M}(t) = v_{DS}(i_{DS}) \cdot i_{DS}(t) = R_{DS,on} \cdot i_{DS}^2(t) \tag{7}$$

$$\begin{aligned} P_{c,M} &= \frac{1}{T_{sw}} \int_0^{T_{sw}} P_{CM}(t)\, dt \\ &= \frac{1}{T_{sw}} \int_0^{T_{sw}} R_{DS,on} \cdot i_{DS}^2(t)\, dt = R_{DS,on} \cdot I_{DS,rms}^2 \end{aligned} \tag{8}$$

T_{sw} is the switching period, and $I_{DS,rms}$ is the root mean square (rms) value of the power MOSFET's on-state current. The instantaneous conduction losses of the power MOSFET can be determined by multiplying the current and voltage as shown in equation (7). Consequently, the power MOSFET's conduction losses are simply expressed by equation (8) [2], [8]–[11].

It is more difficult to calculate the switching losses of the components due to the nonlinear characteristics. The power MOSFET has parasitic capacitances and the inductive load of power electric converters. Therefore, a linear approximation is normally used. The linear method assumes that the drain current and drain-to-source voltage waveforms are linear during the rising and falling edge in the switching transition periods.

The power MOSFET's switching losses are expressed in equation (9):

$$P_{sw,M} = \frac{1}{2} v_{DS} \cdot i_{DS} \left(t_{on} + t_{off}\right) \cdot f_{sw} + \frac{1}{2} C_{oss} \cdot v_{DS}^2 \cdot f_{sw} \tag{9}$$

where f_{sw}, C_{oss}, t_{on}, and t_{off} are the switching frequency, output capacitance, and the power MOSFET's turn-on times and turn-off times.

Fig. 6 shows the switching loss and conduction loss of the power MOSFET [8]. If i_{DS} and v_{DS} have linear waveforms in the transient periods for switching on and off, the first term of equation (9) calculates the power MOSFET switching losses as triangular areas made by i_{DS} and v_{DS} during the transient periods [2], [8]–[11], [17]. The second term in equation (8) represents the output capacitance losses. This loss term is the energy stored in the output capacitance when the power MOSFET is turning off, which is internally dissipated through Joule heating when the power MOSFET turns on. Fig. 5 shows the three interelectrode capacitances [2], [11]. C_{oss} is the output capacitance given by equation (10):

$$C_{oss} = C_{gd} + C_{ds} \tag{10}$$

Due to the minor difference between them, C_{oss} during turn-on discharging and turn-off charging is almost canceled out. As a result, equation (9) can be simply expressed as equation (11):

$$P_{sw,M} = \frac{1}{2} v_{ds} \cdot i_{ds} \left(t_{on} + t_{off}\right) \cdot f_{sw} \tag{11}$$

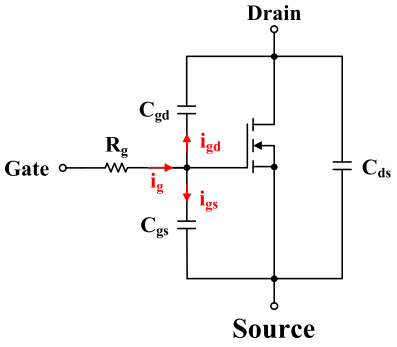


FIGURE 5. Equivalent circuit for the power MOSFET with parasitic capacitances and internal gate resistance.

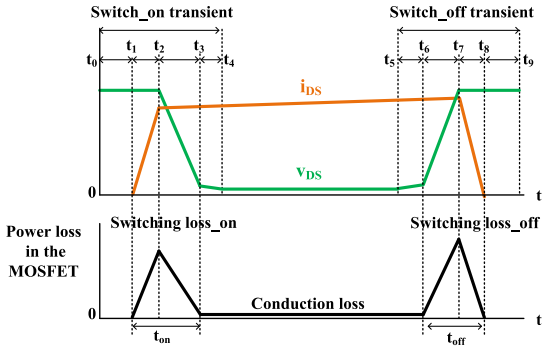


FIGURE 6. Power MOSFET losses in the transient switching period.

Therefore, the total losses of the power MOSFET are finally presented by equation (12):

$$\begin{aligned} P_{loss,M} &= P_{c,M} + P_{sw,M} \\ &= R_{DS,on} \cdot I_{D,rms}^2 + \frac{1}{2} v_{ds} \cdot i_{ds} \left(t_{on} + t_{off}\right) \cdot f_{sw} \end{aligned} \tag{12}$$

If the diode path is in the on-state, the diode presents a forward voltage drop ($v_{fw,D}$) and on-state resistance (R_D) [8]–[13].

$$P_{c,D}(t) = v_D(t) \cdot i_f(t) = v_{fw,D}(t) \cdot i_f(t) + R_D \cdot i_f^2(t) \tag{13}$$

$$\begin{aligned} P_{c,D} &= \frac{1}{T_{sw}} \int_0^{T_{sw}} P_{c,D}(t)\, dt \\ &= \frac{1}{T_{sw}} \int_0^{T_{sw}} v_{fw,D}(t) \cdot i_f(t) + R_D \cdot i_f^2(t)\, dt \\ &= v_{fw,D} \cdot I_{f,ave} + R_D \cdot I_{f,rms}^2 \end{aligned} \tag{14}$$

where v_D, i_f, $I_{f,ave}$, and $I_{f,\mathrm{rms}}$ are the voltage across the diode, current through the diode, average diode current, and rms diode current, respectively.

Fig. 7 shows the power losses current and voltage waveforms of a diode during the turn-off phase. The reverse recovery process leads to switching loss associated with the diode turn-off transition. Although the diode also has turn-on losses, they are normally negligible. If reverse voltage is applied to the diode (i.e., at t_1), the diode turns off, and the forward current If decreases. The diode voltage remains the forward voltage drop V_f [8], [14]–[17].

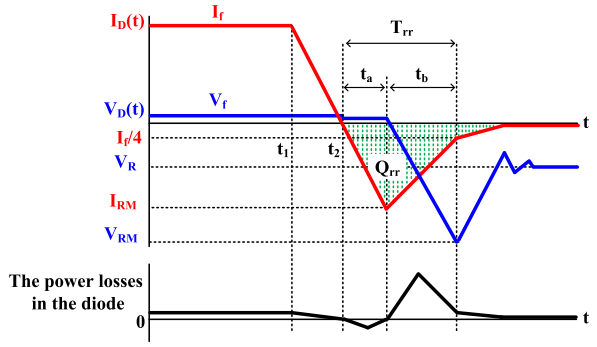


FIGURE 7. Current and voltage waveforms of a diode during turn-off phase.

After the diode current reaches zero, the diode continues to conduct in the reverse direction. The current flows in reverse during the reverse recovery time T_{rr}. The reverse recovery time is generally defined as the time between the current becoming zero and the current decreasing to 25% of the maximum reverse current I_{RM}. Therefore, T_{rr} is expressed by equation (15).

$$t_{rr} = t_a + t_b \tag{15}$$

During the interval of t_a, the charges stored in the depletion area are removed, and the diode voltage almost remains at V_f. During the interval of t_b, the charges from the semiconductor area are removed. In this interval, the reverse voltage reaches the maximum reverse voltage V_{RM} and oscillates around the reverse voltage V_R. Q_{rr} is the reverse recovery charges that are defined as the integral of the current flowing through the diode during interval T_{rr} [8]–[17].

Equation (16) shows Q_{rr} without considering the ratio t_b/t_a, which is called the snappiness factor S.

$$Q_{rr} = \int_{t_a}^{t_b} I_D(t)\,dt \cong \frac{1}{2} I_{RM} t_a + \frac{1}{2} I_{RM} t_b = \frac{1}{2} I_{RM} t_{rr} \tag{16}$$

The general diode turn-off switching losses are expressed in equation (17):

$$P_{sw,off} = \frac{1}{T_{sw}} \int_{t_1}^{t_b} V_D(t)\, I_D(t)\, dt \approx Q_{rr} \cdot V_{Drr} \cdot f_{sw} \tag{17}$$

where V_{Drr} is the voltage across the diode during reverse recovery, and f_{sw} is the switching frequency. Therefore, the total losses of the power diode are represented by equation (18):

$$\begin{aligned} P_{loss,D} &= P_{c,D} + P_{sw,D} \\ &= v_{fw,D} \cdot I_{f,ave} + R_D \cdot I_{f,rms}^2 + \frac{1}{2} I_{RM} \\ &\quad \cdot t_{rr} \cdot V_{Drr} \cdot f_{sw} \end{aligned} \tag{18}$$

The power losses in the three modes were compared. Table 3 shows the conducting and switching components in each mode. Table 4 shows the voltage stresses of each component, which give information about the conduction losses and switching losses of each component [8]–[17].

A. BUCK MODE ANALYSIS

In the following equations, the subscript notations have the following meanings: the first subscript means the type of loss, the second means the type of converter or component, and the third means the number of the subintervals. ''Conv.'' and ''Prop.'' mean ''conventional'' and ''proposed,'' and M and D indicate the MOSFET and diode, respectively.

From Table 3, the conduction losses of each converter are:

$$P_{c,Conv.} = P_{c,M1,1} + P_{c,D2,1} + P_{c,D1,2} + P_{c,D2,2} \tag{19}$$

$$P_{c,Prop.} = P_{c,M1,1} + P_{c,D2,1} + P_{c,D1,2} \tag{20}$$

The switching losses are associated with their voltage stresses, unlike the conduction losses. The voltage stresses on the components are shown in Table 4. The switching losses can be expressed by:

$$P_{sw,Conv.} = P_{sw,M1}(V_{in}) + P_{sw,D1}(V_{in}) \tag{21}$$

$$\begin{aligned} P_{sw,Prop.} &= P_{sw,M1}\left(\frac{C_{D2}}{C_{M1}+C_{D2}} V_{in}\right) + P_{sw,D1}(V_{in}) \\ &\quad + P_{sw,D2}\left(\frac{C_{M1}}{C_{M1}+C_{D2}} V_{in}\right) \end{aligned} \tag{22}$$

When comparing equation (19) and (20) to equation (21) and (22), it can be seen that the proposed converter has one less conduction component and one more switching component. Therefore, the proposed TSBB converter is obviously more advantageous than the conventional TSBB converter for conduction losses.

In the switching losses, $P_{sw,D1}(V_{in})$ is a common term for conventional TSBB converter and proposed TSBB converter. And $P_{sw,M1}(V_{in})$ of the conventional TSBB converter can be compared to the sum of $P_{sw,M1}(\frac{C_{D2}}{C_{M1}+C_{D2}} V_{in})$ and $P_{sw,D2}(\frac{C_{M1}}{C_{M1}+C_{D2}} V_{in})$ of the proposed converter.

First, $P_{sw,M1}(\frac{C_{D2}}{C_{S1}+C_{D2}} V_{in})$ is clearly smaller than $P_{sw,M1}(V_{in})$. However, it is unclear whether the sum of $P_{sw,M1}(\frac{C_{D2}}{C_{M1}+C_{D2}} V_{in})$ and $P_{sw,D2}(\frac{C_{M1}}{C_{M1}+C_{D2}} V_{in})$ is larger than $P_{sw,M1}(V_{in})$ because $P_{sw,D}$ depends on the diode reverse recovery. If reverse recovery is not dominant, $P_{sw,prop}$ can be less than $P_{sw,TSBB}$. Consequently, in buck mode, the relative efficiency of the proposed TSBB converter over the conventional TSBB converter depends on the properties of the components, and the total power losses will show no difference or are expected to be small.

B. BOOST MODE ANALYSIS

By using the same rules for the buck mode analysis, the conduction and switching losses can be expressed by:

$$P_{c,Conv.} = P_{c,M1,3} + P_{c,M2,3} + P_{c,M1,4} + P_{c,D2,4} \tag{23}$$

$$P_{c,Prop.} = P_{c,M2,3} + P_{c,M1,4} + P_{c,D2,4} \tag{24}$$

$$P_{sw,Conv.} = P_{sw,M1}(V_{out}) + P_{sw,D2}(V_{out}) \tag{25}$$

$$P_{sw,Prop.} = P_{sw,M2}(V_{out}) + P_{sw,D2}(V_{out}) \tag{26}$$

From Table 3 and equations (23)-(26), the proposed TSBB converter has one less conduction MOSFET component and

the same switching components as the conventional TSBB converter. Therefore, the proposed TSBB converter is obviously more advantageous than the conventional TSBB converter for the conduction losses. However, the proposed TSBB converter operates with a special MOSFET on-off operation. Although MOSFETS M_1 and M_2 are alternatively switched in the conventional TSBB converter, the proposed TSBB converter only switches M_2, and M_1 stays on during either subinterval 3 or subinterval 4. When M_2 stays in the on-state, currents cannot flow through M_1 due to reverse voltage across D_2. Although the proposed converter is advantageous in the conduction loss due to the small number of conduction components, M_1 is kept on continuously the proposed converter during either subinterval 3 or subinterval 4. This situation leads to continuous gate drive loss. As a result, the power efficiency of the proposed converter is expected to be similar to that of the conventional TSBB converter.

C. BUCK-BOOST MODE ANALYSIS

The conduction and switching losses can be expressed by:

$$P_{c,Conv.} = P_{c,M1,5} + P_{c,M2,5} + P_{c,D1,6} + P_{c,D2,6} \quad (27)$$

$$P_{c,Prop.} = P_{c,M2,5} + P_{c,D1,6} \quad (28)$$

$$P_{sw,Conv.} = P_{sw,M1}(V_{in}) + P_{sw,M2}(V_{out}) + P_{sw,D1}(V_{in}) + P_{sw,D2}(V_{out}) \quad (29)$$

$$P_{sw,Prop.} = P_{sw,M2}(V_{in} + V_{out}) + P_{sw,D1}(V_{in} + V_{out}) \quad (30)$$

From Table 3. and equations (27)- (30), the proposed TSBB converter has two fewer conduction components (one MOSFET and diode). Also, the proposed TSBB converter has fewer switching components than the conventional TSBB converter, but the proposed TSBB converter has large voltage stress. The voltage stress of the proposed is $V_{in} + V_{out}$ for the MOSFET switch and diode, respectively. In the conventional converter, V_{in} and V_{out} are connected to the two switches and two diodes separately. Thus, although the proposed converter has fewer switching components, the switching losses are similar. However, the conduction losses are clearly larger in the conventional TSBB converter.

Consequently, the proposed converter will exhibit better efficiency in buck–boost mode. Taken together, analysis of the buck, boost, and buck–boost modes show that the conduction losses of the proposed converter are obviously more advantageous than the conventional converter in all operation modes. The proposed converter is expected to have a lower switching loss in boost mode and a similar loss to the conventional converter in buck and buck–boost modes. Overall, the proposed converter is expected to have better efficiency characteristics because it has less power losses than the conventional converter.

IV. EXPERIMENT CONDITIONS AND RESULTS

For the experiment, a PWM waveform was generated by an Arduino Nano, and the generated PWM signal was transferred to an optocoupler MOSFET gate drive IC HCPL A J312. Then, buck, boost, and buck–boost mode operations were selectively performed by controlling the switching operation of the MOSFET switches. To compare the power efficiency of each converter, the same components were used. The detailed specifications of the devices are shown in Table 5.

TABLE 5. Detailed specifications of components for each converter.

Component	Specifications
PWM generator	Arduino Nano
Gate Drive IC Optocoupler	HCPL A J312
MOSFET	RCX510N25 (V_{DS}=250 V, I_D=51 A, R_{dson}=48 mΩ)
Diode	RF2001T3D (V_{RM}=350 V, I_O=20 A, V_F=1.3 V)
Inductor	CH270125/250-μH
Capacitor	100YXG820MEFC18X40/820-μF

The switching frequency generated by the Arduino Nano was $f_{sw} = 100$kHz. The input voltage of the buck mode and buck–boost mode step-down is 72V, and the duty ratios are $D_{buck} = 0.67$ and $D_{b/b\ step\ down} = 0.4$. The input voltage of the boost mode and buck–boost mode step-up is 36V, and the duty ratios are $D_{boost} = 0.25$ and $D_{b/bstepup} = 0.57$. The full-load current is 3.125A at the output voltage of $V_{out} = 48$V.

Fig. 8 shows the waveform of the PWM and inductor current of the proposed TSBB converter in each mode. The load condition for the power efficiency measurement was precisely controlled by the electronic load to change the load current from 10% to 100%. Table 6 shows the measured voltage stresses on the components. Fig 9. shows the measured efficiency in each mode.

TABLE 6. Experimental voltage stresses on semiconductors.

Converter	Operation mode	M_1	M_2	D_1	D_2
The conventional TSBB converter	buck	71	47	71	0
	boost	0	48	34	46
	buck–boost step down	71	48	71	47
	buck–boost step up	37	45	35	44
The proposed TSBB converter	buck mode	71	119	71	0
	boost mode	0	47	82	47
	buck–boost step down	78	121	118	96
	buck–boost step up	46	82	80	73

In buck mode, Fig 9. (a) shows that the power efficiency of the proposed TSBB converter was generally higher than that of the conventional TSBB converter. Because the conduction loss of the proposed TSBB converter is obviously lower than that of the conventional TSBB converter due to the fewer conduction components. Also, it seems that there

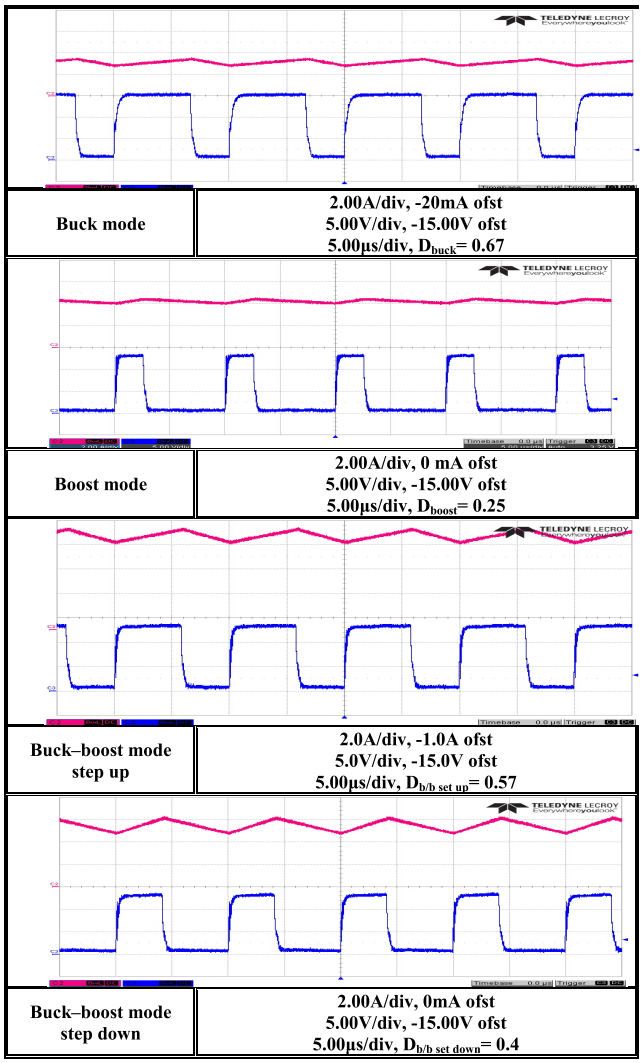


FIGURE 8. Waveform of the PWM of the MOSFET switch and inductor current of the proposed TSBB converter in buck, boost, buck–boost step-down, and buck–boost step-up modes.

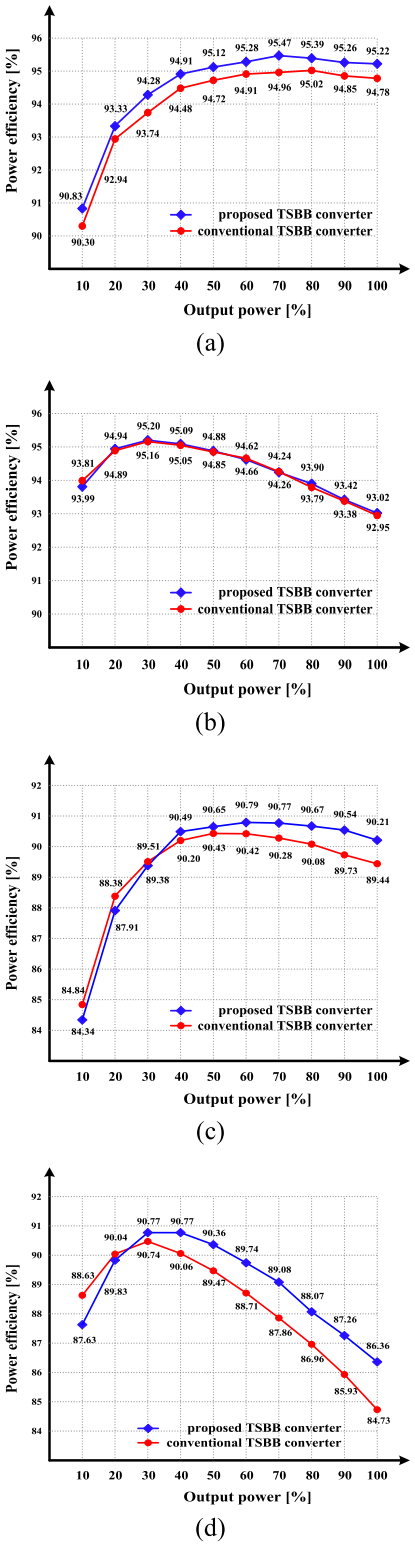


FIGURE 9. Power efficiency at $V_{out} = 48V$, $f_{sw} = 100kHz$ according to the load current. (a) buck mode $V_{in} = 72V$, (b) boost mode $V_{in} = 36V$, (c) buck-boost mode step down $V_{in} = 72V$, (d) buck-boost mode step down $V_{in} = 36V$.

was no remarkable difference between $P_{sw,M1}(V_{in})$ and the sum of $P_{sw,M1}(\frac{C_{D2}}{C_{M1}+C_{D2}}V_{in})$ and $P_{sw,D2}(\frac{C_{M1}}{C_{M1}+C_{D2}}V_{in})$ in the switching loss.

In buck mode, the proposed TSBB converter has efficiencies over 94.91% up to 95.47%, but the conventional TSBB is less than 95% at the 40% to 100% load range.

In boost mode, Fig 9. (b) shows that the power efficiency of the proposed TSBB converter was almost the same as that of the conventional converter. The conduction loss of the proposed TSBB converter is clearly lower than that of the conventional TSBB converter due to the fewer conduction components. However, the constant on-state condition seems to have offset the advantage of the conduction losses of the proposed TSBB converter.

In buck–boost mode, Fig 9. (c) shows that the power efficiency in the conventional and proposed TSBB converters was lower than in their buck mode or boost mode. This occurred because the inductor current in buck–boost mode is larger than in their buck mode or boost mode, as obviously shown in the third and fourth pictures of Fig. 8.

In buck–boost mode step-up and step-down, the power efficiency of the proposed TSBB converter is larger than that of the conventional TSBB converter at the 40% to 100% load range. Because the proposed TSBB converter has fewer conduction and switching components than the conventional TSBB converter, but the proposed TSBB converter has large voltage stress. In the proposed converter, the voltage stress $V_{in} + V_{out}$ is applied to two devices, while the voltage stress of the conventional converter V_{in} and V_{out} is divided among four devices. Therefore, when the load range is less than 40%, the efficiency of the proposed TSBB converter seems to be worse than that of the conventional TSBB converter. In other words, When the load current decreases, the influence of the voltage increases, and the voltage stress term is considered to be a more important factor.

V. CONCLUSION

In this paper, a new two-switch buck–boost converter topology was proposed. The proposed TSBB converter has a single inductor, two switches, and two diodes. It can operate in buck mode, boost mode, and buck–boost mode like a conventional TSBB converter. The proposed TSBB converter features fewer conduction or switching components than a conventional TSBB converter. Therefore, the proposed TSBB converter can be expected to have higher efficiency than the conventional TSBB converter. This was experimentally confirmed with a 150-W prototype TSBB converter. This paper also analyzed the relationship between the voltage stress and power efficiency. As the voltage stress on the components increases, the power efficiency decreases. Also, it can be confirmed that the influence of the voltage stress is increased in the region where the load range is small.

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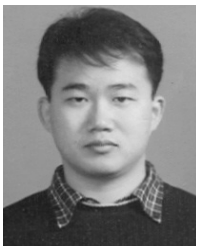

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