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High-Efficiency CMOS RF-to-DC Rectifier Based on Dynamic Threshold Reduction Technique for Wireless Charging Applications

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ABSTRACT This paper presents a high-efficiency CMOS rectifier based on an improved dynamic threshold reduction technique (DTR). The proposed DTR consists of a clamper circuit that biases the gates of pMOS diode switches through a capacitor and diode-connected pMOS transistor. The clamper is used to insert a negative dc level to the input RF signal; therefore, more negative RF signal can be obtained to bias the gates of the main rectifying pMOS devices during its conduction phase. This mechanism reduces the threshold voltage of the main pMOS transistors and increases their sensitivity to the RF input signal. The proposed rectifier is implemented in a 0.18-μm CMOS technology and tested. The measurement shows a peak power conversion efficiency of 86% and an output voltage of 0.52 V at an input power of −16.5 dBm and an input frequency of 402 MHz. The core area of chip excluding measurement pads is 0.024 mm^2.

INDEX TERMS Clamper, CMOS technology, dynamic threshold reduction, power conversion efficiency, rectifier.

I. INTRODUCTION

The applications of wireless power transfer as RFIDs, biomedical devices, and wireless sensor networks have greatly attracted the attention from academia and industry [1]. There are two common types of wireless power techniques, radiated (far-field technique) [2], [3] and non-radiated (near-field technique) [4], [5]. In far-field wireless power transfer, the power is transferred in longer distances through electromagnetic radiation like a laser beam or microwaves, such as wireless powered drone aircraft and solar power satellite. Near-field wireless power transfer (WPT) systems become popular as they are safe and provide high efficiency for short and mid-range applications. Near-field WPT systems work through transferring power either by employing inductive coupling coils, or capacitive coupling electrodes through a magnetic field, or electric field, respectively, for short distance. The near-field type applications are widely found in our daily life, such as wireless toothbrush charger, wirelessly charged cars, implantable medical devices like implanted hearing-aid, heart pacemakers, and blood flow monitor, and radio frequency identification (RFID) tags. RF energy harvesting is one of the conventional methods of wireless power extraction. A rectifier is the main block in the RF energy harvesting system that converts a received RF energy into DC power. Therefore, various types of rectifier topologies in Complementary Metal-Oxide Semiconductor (CMOS) technology have been proposed [1], [6]–[24].

The rectifier's power conversion efficiency (PCE) at low input power is a dominant factor of the RF energy harvesting systems [7]. As the RF energy available in the environment is very weak, designing a rectifier of high PCE at very low input power is a major challenge in CMOS technology

due to the power dissipated because of the threshold voltage [6], [7]. Different schemes were proposed to reduce the effect of threshold voltage required to turn on the rectifying transistors [6]–[18]. Some of these techniques control the threshold voltage using the body effect [8], [10]. Other techniques compensate the threshold voltage by applying an external driving circuit to the gate of the switching transistors [6], [7], [12]–[17].

The objective of this research is to improve the sensitivity, and the PCE of the CMOS rectifier to be suitable for ultra-low power requirements needed for applications such as biomedical electronic devices [19], and RFIDs. This goal is achieved by applying a dynamic threshold reduction (DTR) technique by gate biasing of the PMOS switches with an external clamper circuit. This clamper circuit is biased from the RF signal, then generates the RF signal shifted by a negative DC voltage that used to turn-on the main rectifying PMOS switches. This technique mitigates the threshold voltage effect of the PMOS rectifying devices. Hence, the dynamic power dissipated by the rectifying devices during their on-state is decreased. Consequently, the rectifier can operate at lower input power with improved PCE and higher voltage conversion ratio (VCR).

Another approach using bootstrapping circuit technique to reduce the threshold voltage of rectifying PMOS transistors was proposed [12]. In this technique, the output DC voltage is used to reduce the threshold voltage effect of rectifying PMOS transistors where the bootstrapping capacitor is charged up from the DC output voltage via another diode-connected transistor. The charges stored on this bootstrapping capacitor are then simultaneously applied to the gate of the main rectifying PMOS transistor. In contrast to the proposed DTR rectifier; the bootstrapping capacitor is charged up directly from the RF input power which decreased to more negative value by a clamper circuit and used to bias the rectifying PMOS switches. This technique [12] requires high voltage, and much higher RF input power than the proposed rectifier. Besides, the bootstrapping technique is restricted to low operating frequencies up to 60 MHz, and requires a large die area about 25 times of this work.

This paper is organized as follows: Section II describes the proposed full-wave rectifier design. Section III shows the proposed device's measurement setup and results. Finally, conclusions are presented in Section IV.

II. PROPOSED RECTIFIER DESIGN

In this work, we utilize a threshold reduction technique that alleviates the impact of turning on the PMOS transistors of the conventional differential drive rectifier (DDR) [20] with low input power to achieve high efficiency and sensitivity. The basic concept of the proposed PMOS rectifier depends on using a bootstrapping clamper circuit to bias the gates of PMOS rectifying devices. This clamper circuit consists of a capacitor and diode-connected PMOS transistor as shown in Fig. 1. The clamper circuit gives more negative gate voltage for each PMOS switch during the on-state, and a positive gate voltage during the off-state. In consequence, the rectifier

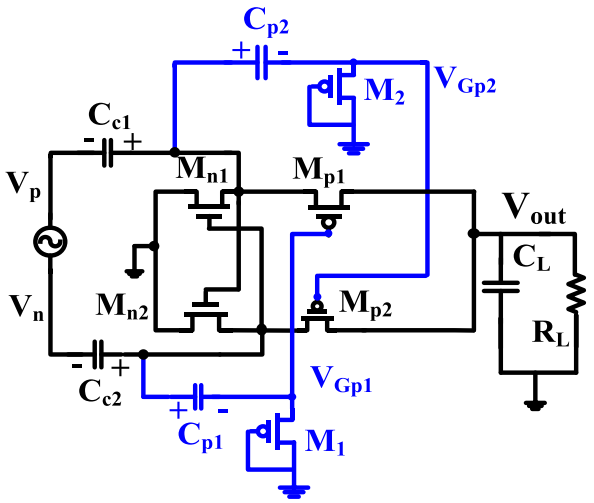

FIGURE 1. Schematic of the proposed rectifier based on PMOS transistors.

turns-on at lower input power than the conventional one. The operation principle of the proposed rectifier was developed in [21]. In this paper, the design challenges of the proposed bootstrapping circuit in [21] are treated. The pulled current from the RF generator passing through the clamper circuit should be minimum to enable the rectifier working almost at the total input power. Hence, the equivalent on-state resistance R_{on} of the MOS device used in the clamper circuit should be large. This is possible by utilizing diode-connected PMOS type transistor, which has larger on-state resistance than that of the NMOS type. The rectifier operation description during one period of the input voltage is shown in Fig. 2.

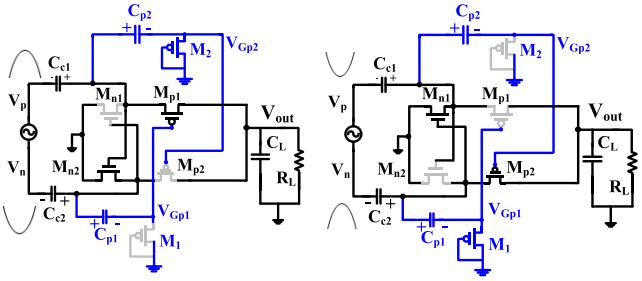

FIGURE 2. Basic operation of the proposed rectifier: (a) During the positive half cycle and (b) During the negative half cycle.

The coupling capacitor C_{c1} will charge during the negative half cycle of the input voltage to V_{Cc1} as given in (1).

$$V_{Cc_1} = V_p - V_{DS(M_{n1})} \tag{1}$$

The bootstrapping capacitor C_{p2} will charge in the on-state of the diode transistor M_2, at the positive half cycle of the input voltage to V_{Cp2} as indicated in (2).

$$V_{C_{p2}} = 2V_p - V_{DS(M_{n1})} - V_{SD(M_2)} \tag{2}$$

where, V_p is the differential input voltage, $V_{DS(Mn1)}$ and $V_{SD(M2)}$ are the drain to source voltage of the rectifying transistor M_{n1}, and the source to drain voltage of the auxiliary transistor M_2 respectively. The gate bias voltages (V_{Gp2}, V_{Gn2}) of PMOS transistor M_{p2} and NMOS transistor M_{n2} of the conventional rectifier [20], and the proposed rectifier are compared over one period of the input signal voltage. The gate bias voltages of PMOS transistor M_{p2} and NMOS transistor M_{n2} of the conventional rectifier [20], are equal as shown by (3) for the positive half cycle, and by (4) for the negative half cycle of the input voltage respectively.

When, $V_p > 0$, M_{p2} is off, and M_{n2} is on:

$$V_{G_{n2}} = V_{G_{p2}} = 2V_p - V_{DS(M_{n1})} \tag{3}$$

When, $V_p < 0$, M_{p2} is on, and M_{n2} is off:

$$V_{G_{n2}} = V_{G_{p2}} = -V_{DS(M_{n1})} \tag{4}$$

The gate voltages of the transistors M_{p2} and M_{n2} of the proposed rectifier are illustrated in (5), and in (6) respectively in the positive half cycle. It is notable that the NMOS transistor M_{n2} conducts with gate bias voltage higher than its threshold value. At the same time, the PMOS transistor M_{p2} is off because of its positive gate voltage.

When, $V_p > 0$, M_{p2} is off, and M_{n2} is on:

$$\begin{aligned} V_{G_{p2}} &= V_p + V_{Cc_1} - V_{C_{p2}} \\ V_{G_{p2}} &= V_{SD(M_2)} \end{aligned} \tag{5}$$

$$\begin{aligned} V_{G_{n2}} &= V_p + V_{Cc_1} \\ V_{G_{n2}} &= 2V_p - V_{DS(M_{n1})} \end{aligned} \tag{6}$$

The gate bias voltages of the same transistors M_{p2} and M_{n2} are analyzed in the negative half cycle of the input voltage as indicated in (7) and (8) respectively.

When, $V_p < 0$, M_{p2} is on, and M_{n2} is off:

$$\begin{aligned} V_{G_{p2}} &= -V_p + V_{Cc_1} - V_{C_{p2}} \\ V_{G_{p2}} &= -2V_p + V_{DS(M_2)} \end{aligned} \tag{7}$$

$$\begin{aligned} V_{G_{n2}} &= -V_p + V_{Cc_1} \\ V_{G_{n2}} &= -V_{DS(M_{n1})} \end{aligned} \tag{8}$$

Fig. 3 presents the simulation results of the proposed rectifier performed in the settling time, which show the variation of gate voltages of the two rectifying transistors M_{n2} and M_{p2} with time.

It is clear that the gate bias voltage of the PMOS transistor M_{p2} of the proposed rectifier becomes more negative than its corresponding value of the conventional rectifier [20], and hence conducts with a lower input voltage. Consequently, a higher PCE at low RF input power can be obtained by the proposed rectifier.

The DC output voltage (V_{out}) achieved by the proposed rectifier is given by (9).

$$\begin{aligned} V_{out} &= V_p + V_{Cc_1} - V_{SD(M_{p1})} \\ V_{out} &= 2V_p - V_{DS(M_{n1})} - V_{SD(M_{p1})} \end{aligned} \tag{9}$$

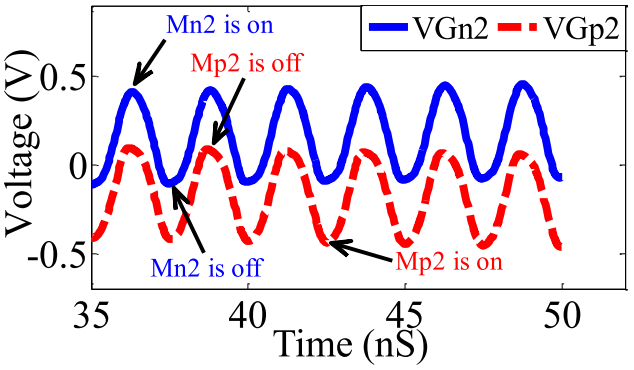

FIGURE 3. Gate voltages of M_{n2} and M_{p2} of the proposed PMOS rectifier.

The other half circuit (consisting of C_{c2}, C_{p1}, M_1, M_{n1}, and M_{p1}) will operate in the same manner and gives the same value of the output voltage. The body terminals of all transistors are connected to the source terminals in order to avoid the bulk effect.

III. MEASUREMENT AND DISCUSSION

A. CHIP IMPLEMENTATION AND MEASUREMENT SETUP

The proposed rectifier is implemented and fabricated in 0.18 μm CMOS technology. Fig. 4 shows the microphotograph of the fabricated chip and enlarged view of the same chip excluding the pads on the right side. The rectifier occupies a core area of 327 μm $\times$ 74 μm including the bootstrapping capacitors. The design area with the input and output pads is 420 μm $\times$ 460 μm. Transistor sizes W/L (μm/μm) are 60/0.18 for (M_{n1}, M_{n2}), 160/0.18 for (M_{p1}, M_{p2}), and 1.5/0.45 for (M_1, M_2). Capacitors C_{p1}, C_{p2}, C_L are used with 2 pF respectively.

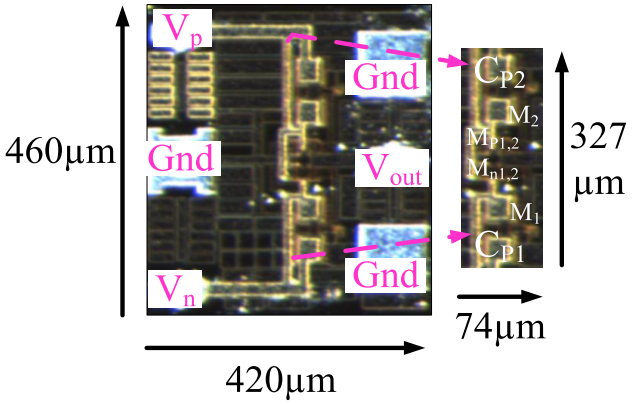

FIGURE 4. Microphotograph of the fabricated chip and enlarged view without test pads on the right side.

The RF measurements are carried out using Agilent's vector network analyzer (N5222A) with a single tone of 402 MHz frequency as one of medical implantable communication service band (MICS) at sweeping input power levels and a digital voltmeter to record the output DC voltage. Cable calibration has been done to measure the input

reflection coefficient $|S_{11}|$ under test. The net input power levels have been calculated after subtracting the reflection and transmission losses.

An off-chip parallel resistor and capacitor load is connected to the DC output terminal to emulate the DC output voltage. The measurement setup is shown in Fig. 5. A Mini-Circuits' coaxial RF power splitter/combiner (2 Way-180° 50Ω, 50 to 1000 MHz) is utilized to convert the RF single-ended signal into a differential signal. The coupling capacitors (C_{c1}, C_{c2}) are placed off chip, and each has a value of 21 pF.

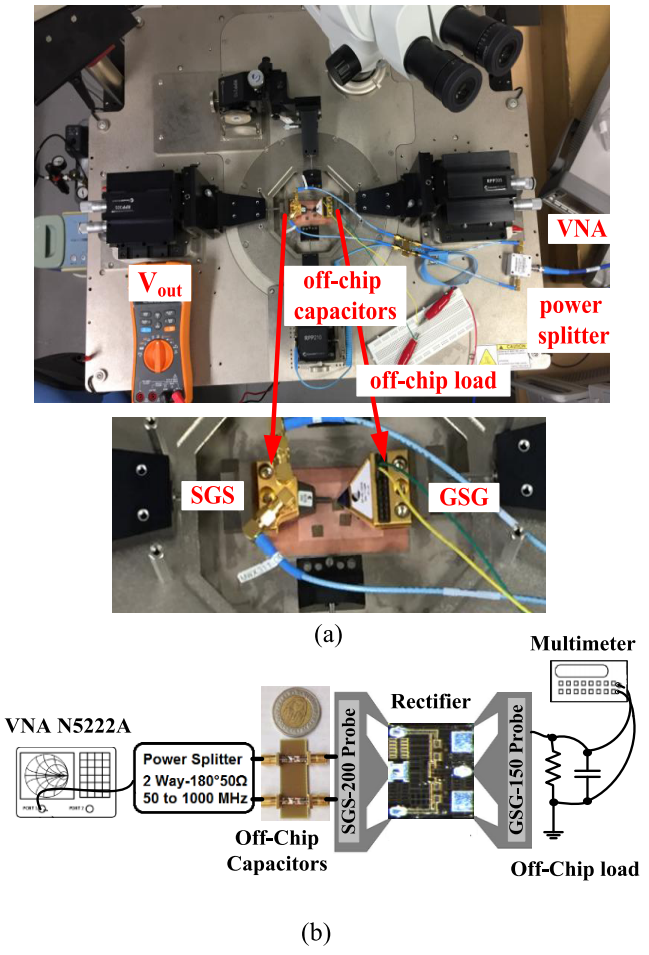

FIGURE 5. (a) Photograph of the RF-measurement setup, and (b) Diagram of the measurement test bench.

B. MEASUREMENT RESULTS

The performance of the proposed rectifier is taken in terms of the PCE and the output DC voltage versus the RF input power in dBm. The rectifier was driven by a 402 MHz single tone, while loaded with a 10 kΩ load resistor which is an optimal load for this design. The PCE of the rectifier is measured after excluding the reflection and transmission losses using the following equations (10) to (13) [7], [22], [23].

$$PCE = \frac{P_{out}}{P_{Rect}} \times 100 \tag{10}$$

$$P_{out} = \frac{V_{out}^2}{R_L} \tag{11}$$

$$P_{Splitter(watt)} = P_{S(watt)} \times (1 - |S_{11}|^2) \tag{12}$$

$$P_{Rect(dBm)} = P_{Splitter(dBm)} - IL_{dB} \tag{13}$$

Where P_{out} is the DC output power of the rectifier. V_{out} is the measured DC output voltage. P_{Rect} is actual input power delivered to the rectifier. P_S is the single-ended RF power output from the VNA port. $P_{splitter}$ is the actual input power of the splitter. IL is the insertion loss due to the connections from the signal source to the rectifier. The difference of performance between the proposed rectifier and the NMOS rectifier [21] is illustrated in Fig. 6. The PMOS rectifier achieved a measured peak PCE of 86%; while, the maximum PCE of NMOS rectifier [21] was 83%.

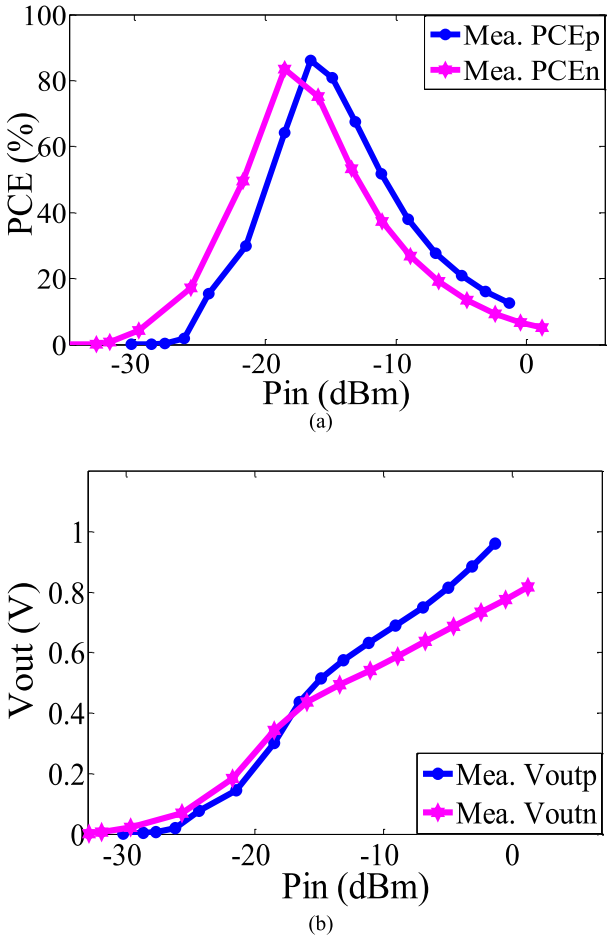

FIGURE 6. Measurement results of the two proposed rectifiers at 402 MHz. (a) The PCE, and (b) The DC output voltage.

The PCE of the NMOS rectifier is decreased and moved to the left at lower input power than the PMOS rectifier. This is because the carrier mobility difference between the NMOS and PMOS diode-connected transistors. Therefore, the equivalent on resistance of the external tansistors (M_1, M_2) of the PMOS rectifier is higher than that of the NMOS rectifier. Therefore, the bootstrapped circuit built by PMOS

transistors will draw small current and low power which makes the input power losses smaller and the PCE higher.

The performance of the proposed PMOS rectifier is also measured at 953 MHz input signal where ultra-high frequency (UHF) RFIDs utilize the UHF band (860–960) MHz [20], with 10 kΩ load as shown in Fig. 7. The measured PCE is computed 70% at RF input power of −16.8 dBm.

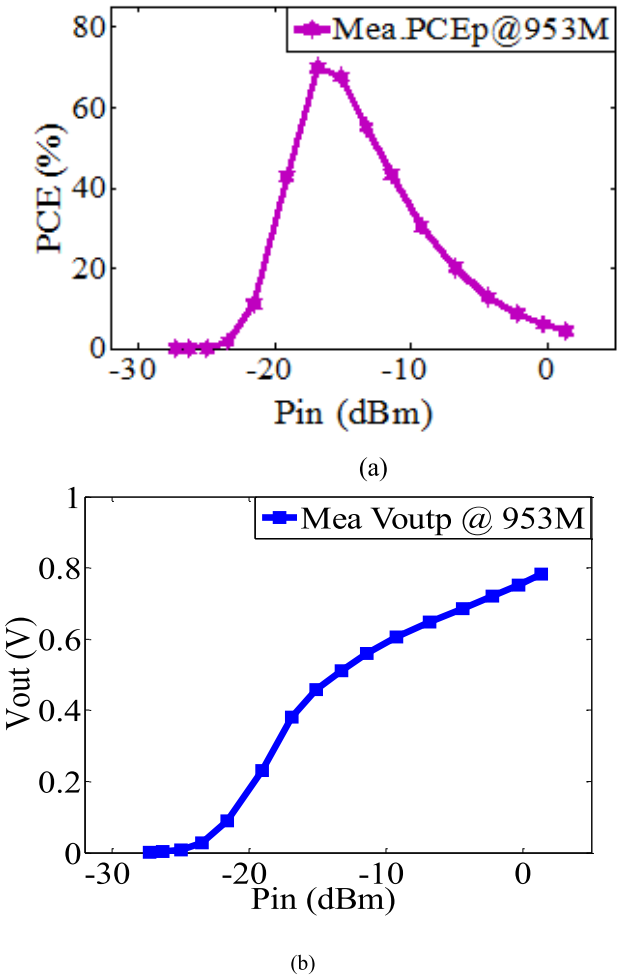

FIGURE 7. Measurement results of the proposed rectifier at 953 MHz (a) PCE, and (b) DC output voltage.

All rectifiers are non-linear system. The input impedance of a rectifier circuit is a function of input power and input signal frequency. On the other hand, the output impedance of input signal source (at a measurement system) is almost a constant. Thus, the peak PEC of a rectifier depends on the input power and input signal frequency. As the input frequency increases, the parasitic resistance caused by all the metal paths will also increase due to the skin effect. This leads the phenomenon that the peak PEC of the proposed rectifier decreased with increasing the input signal frequency.

The basic circuit of the proposed PMOS rectifier without DTR is similar to the previously proposed CMOS rectifier [20], hence the PCE of the proposed rectifier with DTR technique is compared to the conventional rectifier [20] without DTR technique at 402 MHz and 953 MHz as shown in Fig. 8. As we did not fabricate the proposed rectifier without DTR, the comparison is made with simulation results only. The proposed DTR rectifier achieves 88% at −15 dBm and 73% at −14.8 dBm at 402 MHz and 953 MHz respectively. While the rectifier [20] without DTR results 72% at −12.55 dBm and 68% at −12.5 dBm at 402 MHz and 953 MHz respectively. However, the measured PCE of proposed rectifier is 70% at 953 MHz which is 16% lesser than that of the same circuit at 402 MHz but still demonstrates the superiority of the proposed DTR even at 953 MHz compared to the rectifier without DTR [20].

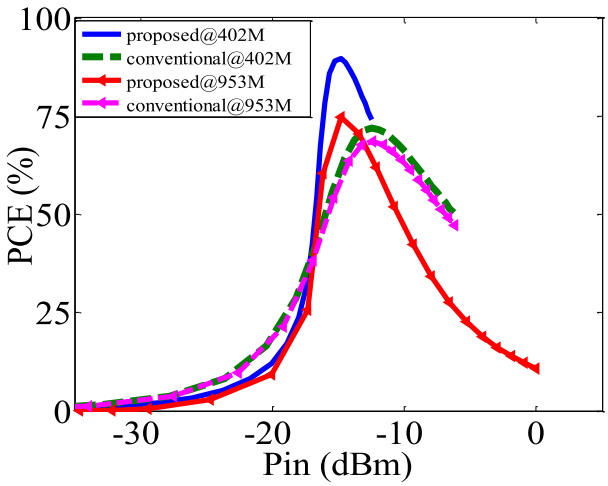

FIGURE 8. PCE comparison between the proposed rectifier (with DTR) and the conventional rectifier (without the DTR).

To discuss the performance of the fabricated rectifier compared to other published designs, a figure of merit (FoM) is proposed as given by (14). It can exactly evaluate various rectifiers' performance in different frequency bands by frequency normalization to a normalized value (f_0), for instance, $f_0 = 5$ MHz. Higher FoM implies better rectifier performance at lower RF input power and minimum number of stages (N).

$$FoM = \frac{PCE \times VCR}{N} \log_{10}\left(\frac{f}{f_0}\right) \tag{14}$$

VCR is the voltage conversion ratio, which defined as the ratio of the average output voltage to the peak AC input voltage [24].

Performance summary and comparison with other designs are shown in Table 1. It is noted that the proposed rectifier achieved higher FoM compared to other published state-of-the-art works.

The design presented in [18] has good PCE because it relys on two techniques to improve the rectifier performance, one is ''Threshold voltage compensation'', and the other is ''Leakage current reduction''. Even though, it doesn't provide any experimental proof and it has also large numbers of MOS transistors so that the die area is almost three times of our

TABLE 1. Performance summary and comparison.

Reference	**This work**		[9]	[10]	[12]	[17]	[18]	[19]	[20]	[24]
CMOS Process (μm)	**0.18**	**0.18**	0.18	0.04	0.18	0.18	0.18	0.5	0.18	0.18
Frequency (MHz)	**402**	**953**	433	900	10	40.68	13.56	13.56	953	10
(N) stages	**1**	**1**	4	8	1	1	1	1	1	1
PCE_{max} *(%)*	**86**	**70**	34	42	80	85.8	87	80.2	67.5	92.5
P_{in} *(dBm)*	**-16.5**	**-16.8**	-7	-20.2	3.9	0.79	11.98	13.8	-12.5	-
V_{out} *(V)*	**0.52**	**0.38**	2	1	2	3.15	2.92	3.12	0.6	0.96
Area (mm^2)	**0.024**	**0.024**	0.15	0.255	0.608	0.046	0.0768	0.18	-	1.72
R_L*(kΩ)*	**10**	**10**	100	250	2	8	2	0.5	10	2
C_L *(pF)*	**2**	**2**	3	-	200	10^5	200	10^7	1.13	200
VCR(%)	**81**	**80**	-	-	74	89.7	88.6	82	70	76.8
FoM	**1.327**	**1.27**	-	-	0.18	0.7	0.33	0.28	1.08	0.21

proposed circuit. Furthermore, it also requires very high RF input power to operate satisfactory.

IV. CONCLUSIONS

An improved dynamic threshold reduction technique to improve the PCE of a full-wave rectifier topology at very low input RF power using PMOS transistors is proposed. The proposed rectifier has been fabricated using 0.18 μm CMOS technology. The measurement results shows a significant enhancement in PCE at 402 MHz and 953 MHz input frequency, it achieved PCE 86% and 70% at 402 MHz and 953 MHz input frequency respectively. Moreover, the core area of chip excluding pads is 0.024 mm^2, which is almost 50% smaller than that of the previously proposed rectifier [17]. The FoM of the proposed rectifier is 1.327 which is the highest among the rectifiers so far proposed in CMOS technology.

REFERENCES

[1] Q. Li, J. Wang, and Y. Inoue, "A high efficiency CMOS rectifier with ON-OFF response compensation for wireless power transfer in biomedical applications," in *Proc. 14th Int. Symp. Integr. Circuits (ISIC)*, Dec. 2014, pp. 91–94.

[2] M. Xia and S. Aissa, "On the efficiency of far-field wireless power transfer," *IEEE Trans. Signal Process.*, vol. 63, no. 11, pp. 2835–2847, Jun. 2015.

[3] P. S. Yedavalli, T. Riihonen, X. Wang, and J. M. Rabaey, "Far-field RF wireless power transfer with blind adaptive beamforming for Internet of Things devices," *IEEE Access*, vol. 5, pp. 1743–1752, 2017.

[4] O. Jonah and S. V. Georgakopoulos, "Wireless power transfer in concrete via strongly coupled magnetic resonance," *J. Chem. Inf. Model.*, vol. 53, no. 9, pp. 1689–1699, 2013.

[5] S. Hekal, A. B. Abdel-Rahman, H. Jia, A. Allam, A. Barakat, and R. K. Pokharel, "A novel technique for compact size wireless power transfer applications using defected ground structures," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 2, pp. 591–599, Feb. 2017.

[6] Z. Hameed and K. Moez, "A 3.2 V–15 dBm adaptive threshold-voltage compensated RF energy harvester in 130 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 4, pp. 948–956, Apr. 2015.

[7] S. S. Chouhan and K. Halonen, "Threshold voltage compensation scheme for RF-to-DC converter used in RFID applications," *Electron. Lett.*, vol. 51, no. 12, pp. 892–894, May 2015.

[8] Y. Chang, S. S. Chouhan, and K. Halonen, "A scheme to improve PCE of differential-drive CMOS rectifier for low RF input power," *Analog Integr. Circuits Signal Process.*, vol. 90, no. 1, pp. 113–124, Jan. 2017.

[9] K. Gharehbaghi, Ö. Zorlu, F. Koçer, and H. Külah, "Threshold compensated UHF rectifier with local self-calibrator," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 6, pp. 575–577, Jun. 2017.

[10] L. Zöscher *et al.*, "Threshold voltage compensated RF-DC power converters in a 40 nm CMOS technology," in *Proc. Austrochip Workshop Microelectron.*, Oct. 2016, pp. 30–34.

[11] K. Kotani and T. Ito, "High efficiency CMOS rectifier circuit with self-Vth-cancellation and power regulation functions for UHF RFIDs," in *Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC)*, Nov. 2007, pp. 119–122.

[12] S. S. Hashemi, M. Sawan, and Y. Savaria, "A high-efficiency low-voltage CMOS rectifier for harvesting energy in implantable devices," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 4, pp. 326–335, Aug. 2012.

[13] S. S. Chouhan and K. Halonen, "The design and implementation of DTMOS biased all PMOS rectifier for RF energy harvesting," in *Proc. IEEE Int. New Circuits Syst. Conf.*, vol. 1, no. 3, Jun. 2014, pp. 444–447.

[14] J. Shin, I.-Y. Chung, Y. J. Park, and H. S. Min, "A new charge pump without degradation in threshold voltage due to body effect," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1227–1230, Aug. 2000.

[15] L. Grasso, G. Palmisano, and R. Guerra, "A CMOS full-wave rectifer with threshold compensation based on inherent body-voltage control," in *Proc. IEEE Eur. Microw. Conf.*, Oct. 2016, pp. 938–941.

[16] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950-MHz rectifier circuit for sensor network tags with 10-m distance," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 35–41, Jan. 2006.

[17] M. Zargham and P. G. Gulak, "High-efficiency CMOS rectifier for fully integrated mW wireless power transfer," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2012, pp. 2869–2872.

[18] S. R. Khan and G. Choi, "High-efficiency CMOS rectifier with minimized leakage and threshold cancellation features for low power bio-implants," *Microelectron. J.*, vol. 66, pp. 67–75, Aug. 2017.

[19] H.-M. Lee and M. Ghovanloo, "An integrated power-efficient active rectifier with offset-controlled high speed comparators for inductively powered applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 8, pp. 1749–1760, Aug. 2011.

[20] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3011–3018, Nov. 2009.

[21] M. Mahmoud, A. B. Abdel-Rahman, G. A. Fahmy, A. Alam, H. Jia, and R. K. Pokharel, "Dynamic threshold compensated, low voltage CMOS energy harvesting rectifier for UHF applications," in *Proc. IEEE 59th Int. Midwest Symp. Circuits Syst.*, vol. 1, Oct. 2016, pp. 1–4.

[22] C.-J. Li and T.-C. Lee, "2.4-GHz high-efficiency adaptive power," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 2, pp. 434–438, Feb. 2014.

[23] M. H. Ouda, W. Khalil, and K. N. Salama, "Self-biased differential rectifier with enhanced dynamic range for wireless powering," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 5, pp. 515–519, May 2017.

[24] S. Hashemi, M. Sawan, and Y. Savaria, "A novel low-drop CMOS active rectifier for RF-powered devices: Experimental results," *Microelectron. J.*, vol. 40, no. 11, pp. 1547–1554, Nov. 2009.

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