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LED Driver Based on Boost Circuit and LLC Converter

JIANGUANG MA, XUEYE WEI, LIANG HU, AND JUNHONG ZHANG
School of Electronic and Information Engineering, Beijing Jiaotong University, Beijing 100044, China
Corresponding author: Jianguang Ma (14111042@bjtu.edu.cn)

ABSTRACT In order to reduce the size and cost of a medium-power light-emitting diode (LED) driver, a novel single-stage LED driver integrating a boost converter with a half-bridge LLC resonant converter has been proposed. This topology is composed of a boost power factor correction circuit operating in a discontinuous conduction mode and an isolated LLC circuit unit with soft-switching characteristics. The proposed LED driver only adopted two switch components, thus benefiting from control simple and without employing an extra switch driver and a control circuit. The operating principle and characteristics of the proposed LED driver are analyzed in detail. In addition, experimental results of a laboratory prototype for supplying a 100-W/70-V LED lighting systems from 220-V/50-Hz ac line voltage are presented to verify well the correctness of the theoretical analysis and parameters' design.

INDEX TERMS LED driver, single stage, LLC converter, boost circuit.

I. INTRODUCTION

With the superior advantage of high efficiency, color rendering, the high brightness light-emitting diode (LED) is more and more popular in various lighting applications, for example, street lights, black lights, indoor lighting and so on. It is has many outstanding advantages such as high light efficacy, energy-saving, long lifespan and high reliability compared with conventional incandescent lighting source [1], [2]. Usually, an LED driver necessary to adopt various conditions to LED lighting requirements, for example, input voltage and input current. In most common for obtain constant current supplying, typical LED driver consists of two stages structure, a ac-dc stage for power factor correction (PFC), an dc-dc stage for regulating the LED driver output voltage and current [3], [4]. Therefore they employ many semiconductor devices, resulting in a control complex and increase the cost. So, it is not suitable for small-medium power applications.

In recent years, for two-stage structure of LED driver, many researchers made an in-depth and detail studies, achieving high power factor and low total harmonic distortion. Furthermore, in the two-stage LED driver the constant output current regulation is more easily implemented due to the bus voltage existence. Reference [5] proposed a CLCL resonant dc/dc converter for two-stage LED driver system, in which adopted the soft switch characteristic; however, it is needed to add an additional inductor and resonant capacitor formed the CLCL structure and the switch work in ''quasi-ZCS'' mode. For the two-stage structure in the LED driver, the flyback topology has been developed, which is reduce the number of device and control complexity [6], [7]. Xie *et al.* [8] parented a two-stage LED driver based on a flyback circuit with the current-sharing transformer. However, the zero voltage switching state of the primary switches is difficult guaranteed. In [9] a CLL type resonant converter is adopted in the proposed two-stage LED driver system. The soft switch capability of both the primary side and secondary devices is obtained, therefore efficiency was improved.

In order to continuously improving efficiency about the LED driving system, LLC resonant converter has been adopted in various conditions. LLC resonant converter is popularly adapted because of its soft switching characteristic, resulting in low noise from the switches. LLC resonant circuit enables a high operation in an entire load range because of the low switching loss with zero voltage switch (ZCS) mode and zero current switch (ZCS) mode [10]–[12]. In addition, the LLC resonant circuit is widely employed for electric isolation applications due to high-frequency transformer. Nevertheless, in low power applications, the flyback is more suitable than LLC resonant because of the flyback only needs one switch device.

In term of LED driver efficiency, the single stage is higher compared with the two-stage LED driver, especially in small middle power applications. Hence, many single stages LED driver have been studied. Generally, the single stage formed by a PFC circuit and a dc/dc circuit by integrating technique. In [13] a single-stage LED driver is proposed for the street

lighting based on two boost circuit working in boundary conduction mode (BCM). The driver composed of two boost circuit and a half bridge LLC resonant converter by sharing the two switches. However, in this topology the input voltage is divided by two capacitors, the current stress will be increased at the same power level. A novel single stage light emitting diode (LED) driver based on double LLC resonant converter for high voltage gain condition is presented [14]. This driver is made up of two resonant tanks, which integrated by boost circuit and LLC resonant converter. However, this topology used to cope with the lower input voltage between 9 and 16V, it not suitable for universal line voltage.

In this paper, a novel LED driver based on boost circuit and LLC resonant converter are proposed, and it is applied industrial LED lighting system. This driver composed of two parts: the boost cell and the LLC resonant converter. The boost circuit will work in a discontinuous conduction mode (DCM) which can achieve power factor correction function. Therefore the boost circuit can help to ensure low total harmonic distortion (THD) and a high power factor (PF). While the LLC resonant converter working at a suitable frequency, the primary switches operate in ZVS state and the secondary switches operate in ZCS state, which leads to a low switching loss. Through the switch sharing technique, LLC resonant converter integrated with a boost circuit to obtain the simple structure. The function characteristic of the boost circuit and LLC resonant converter are not interaction affected by the sharing technique of the switches. Compared with the traditional two-stage ac/dc LED driver, the proposed circuit only adopted one controller, thus, the switches count and cost are significantly reduced.

Other sections of the paper are organized as follows. In section II, introduces the proposed circuit configuration and presents its operating principles. Its design considerations are discussed in section III and experimental verification of an implemented prototype of the proposed converter are provided in section IV. Finally, the conclusion is drawn in section V.

II. CIRCUIT CONFIGURATION AND ITS OPERATING PRINCIPLES

A. CIRCUIT CONFIGURATION

The proposed novel single-stage LED driver based on boost circuit and LLC resonant converter diagram configuration is shown in Fig. 1. On the contrary, the traditional two-stage LED driver based on boost circuit and LLC resonant converter is depicted in Fig. 2. As illustrated in Fig. 2. The v_{in} is normal ac input voltage, the diodes form the full bridge rectifier circuit. As shown in Fig. 1, the boost stage of the proposed LED driver is made up of an input voltage V_{in}, a choke inductance L, an active switch S_1, a diode D_2, an input capacitance C_1. Here, the inductor current works in DCM, the circuit high PF can be obtained. Whereas the LLC converter is composed of two active switches S_1 and S_2, a resonant tank contains a block dc capacitor C_{r}, a transformer T including a leakage inductance L_{s}, a magnetizing

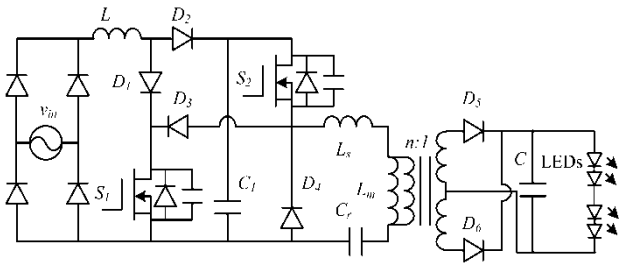

FIGURE 1. The configuration of proposed single-stage LED driver circuit.

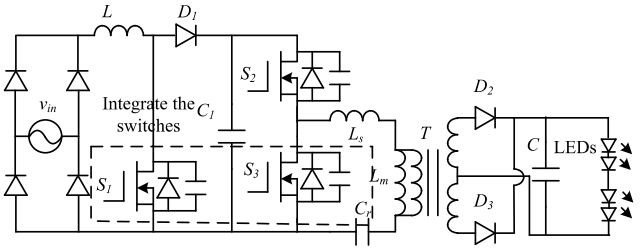

FIGURE 2. The two-stage converter based on boost circuit and LLC resonant converter.

inductance L_{m}, an ideal transformer with turn ratio n. The secondary of the transformer is a center tap full-wave rectifier. LEDs are the equivalent model of LED lamp. Compared with the conventional two-stage solution, one MOSFET and one control circuit are reduced, and two diodes are added. Therefore, the two circuits boost and LLC are integrated together by sharing the switch S_1. Due to the cost of the MOSFET is high than that of the diode, so the total cost reduced.

Fig. 3 illustrates the main voltage and current waveforms in a switching cycle at the steady state. To detail analysis the operation of circuit, the proposed novel LED driver has divided into eight subintervals in an entire operating period, as shown in Fig. 4.

For the convenience analysis the circuit in the steady-state condition, some assumptions are made as follows.

1) All the active switches are ideal, therefore the stray inductance and parasitic can be neglected.

2) The capacitance C and C_1 are large enough that the bus voltage and output voltage ripple can be ignored.

3) The intrinsic parameters of diodes are calculated as the passive devices.

4) The frequency of the resonant is sufficiently large than input line voltage frequency.

5) The dead time between the primary switches is small enough to be neglected.

B. OPERATION PRINCIPLE

1) Interval 1 $[t_0 - t_1]$ [Fig. 4(a)] Interval 1 begins when the switches S_1 and S_2 are turned off. The resonant capacitor C_{r}, leakage inductor L_{s} and magnetizing inductor L_{m} occurs. Diode D_5 and D_6 are both reverse biased,

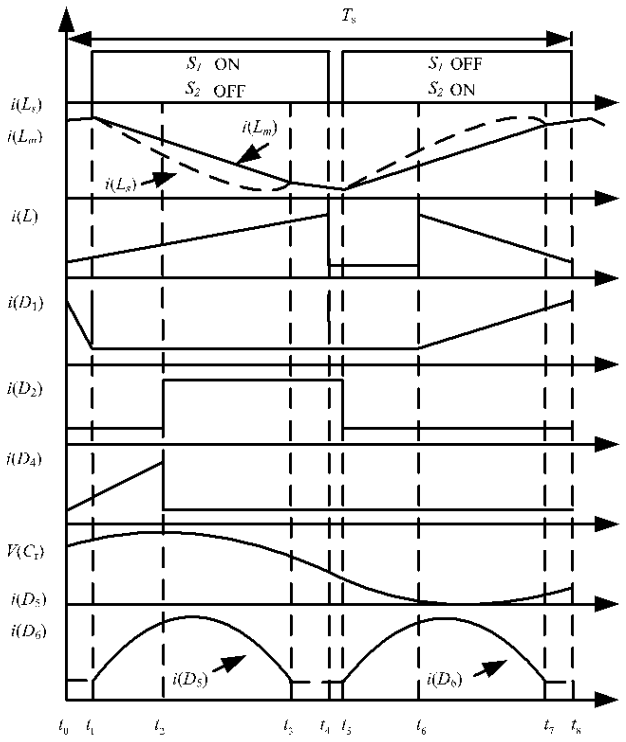

FIGURE 3. The key waveform of the converter.

the diode D_2 conducts. The energy stored in inductor L and capacitor C_1. During this stage, the magnetizing inductor current i_{Lm} equal to the leakage inductor current i_{Lm}, the input power is no longer transferred to the secondary, and the power to the load is only supplied by the output capacitor C. The magnetizing inductor current and leakage inductor current can be obtained.

$$i_{Ls}(t) = i_{Lm}(t) = \frac{V_T}{Z_p}\cos\omega_p(t-t_1) \quad (1)$$

$$V_{Cr}(t) = V_{Cr}(t_0) + \frac{i_{Ls}(t_0)}{C_r}(t-t_1) \quad (2)$$

$$V_{DS-S1}(t) = V_{in} - \frac{i_{Lm}(t_0)}{2c_{oss1}}(t-t_1) \quad (3)$$

$$V_{DS-S2}(t) = \frac{i_{Lm}(t_0)}{2c_{oss2}}(t-t_1) \quad (4)$$

Where, the characteristic impedance Z_p, the primary voltage of transformer V_T and resonant angular frequency ω_p are defined as:

$$Z_p = \sqrt{(L_s+L_m)/C_r} \quad \omega_p = 1/\sqrt{(L_s+L_m)C_r}$$
$$V_T = \sqrt{[Z_1 i_{Ls}(t_1)]^2 + [V_{Cr}(t_1)]^2}$$

Here, c_{oss} is the parasitic capacitance of the switches. The ZVS conditions of switches S_1 and S_2 can be described as follows:

$$\frac{1}{2}L_s i_{pri}(t_1)^2 \geq \frac{1}{2}(2c_{oss})(V_{DS-Q2})^2 \quad (5)$$

2) Interval 2 $[t_1 - t_2]$ [Fig. 4(b)] In this interval, switch S_1 turn ON with ZVS and switch S_2 still turn OFF. At this time, the diode D_5 reverse biased and D_6 forward biased, respectively. The magnetizing inductor L_{m} is clamped by the secondary voltage. The magnetizing inductor L_{m} does not participates in resonance. The magnetizing current i_{Lm} and leakage inductor current i_{Ls} are linearly and sinusoidal decrease, respectively. The difference between i_{Ls} and i_{Lm} is transferred to the output stage. The inductor L is charged by input power, the current i_{L} increase, diode D_1 and D_4 forward biased.

$$i_{Lm}(t) = i_{Lm}(t_1) + \frac{nV_o}{L_m}(t-t_2) \quad (6)$$

$$i_{Ls}(t) = i_{L2}(t_1) + \frac{V_{boost} - V_{Cr}(t_1)}{Z_r}\sin\omega_r(t-t_2) \quad (7)$$

Where, V_{boost} is the output voltage of the boost stage, the characteristic impedance, and angular frequency are expressed as follows: $Z_r = \sqrt{L_s/C_r}$, $\omega_r = 1/\sqrt{L_s C_r}$

3) Interval 3 $[t_2 - t_3]$ [Fig. 4(c)] In this interval, S_1 turn on and S_2 is still OFF, and diode D_1 and D_3 forward biased, D_2 and D_4 reverse biased. In the circuit, the inductor L charge, the current i_{L} is increased. The difference between i_{Ls} and i_{Lm} is transferred to the output stage.

$$i_{Lm}(t) = i_{Lm}(t_2) + \frac{-nV_o}{L_m}(t-t_3) \quad (8)$$

$$i_{Ls}(t) = \frac{I_o}{n} - \frac{V_{in}}{Z_r}\sin\omega_r(t-t_3) \quad (9)$$

$$V_{Cr}(t) = V_{Cr}(t_2) + \int_{t2}^{t} i_{Lm}(t)dt \quad (10)$$

4) Interval 4 $[t_3 - t_4]$ [Fig. 4(d)] In this interval, the magnetizing inductance L_{m} participates in the resonance. Then the power to the load only supplied by the output capacitor C. At the end of this stage, the switches of S_1 and S_2 are both turned OFF, which is dead time. In the circuit, inductor L charge, the current i_{L} increase, reach their peak value. Then, the circuit operation of the first half switch cycle is finished. The voltage and current during this interval can be expressed as follows:

$$i_{Ls}(t) = i_{Ls}(t_3) + \frac{V_T}{Z_p}\sin\omega_p(t-t_4) \quad (11)$$

$$V_{Cr}(t) = +\frac{i_{Ls}(t_3)}{C_r}(t-t_3) \quad (12)$$

$$V_{DS-Q1}(t) = V_{in} - \frac{i_{Lm}(t_3)}{2c_{oss1}}(t-t_4) \quad (13)$$

$$V_{DS-Q2}(t) = \frac{i_{Lm}(t_3)}{2c_{oss2}}(t-t_4) \quad (14)$$

Since then, the operation for intervals 5-8 whose operating circuit and equivalent circuit during the interval are similar to prior half cycle. Therefore, they are not discussed here.

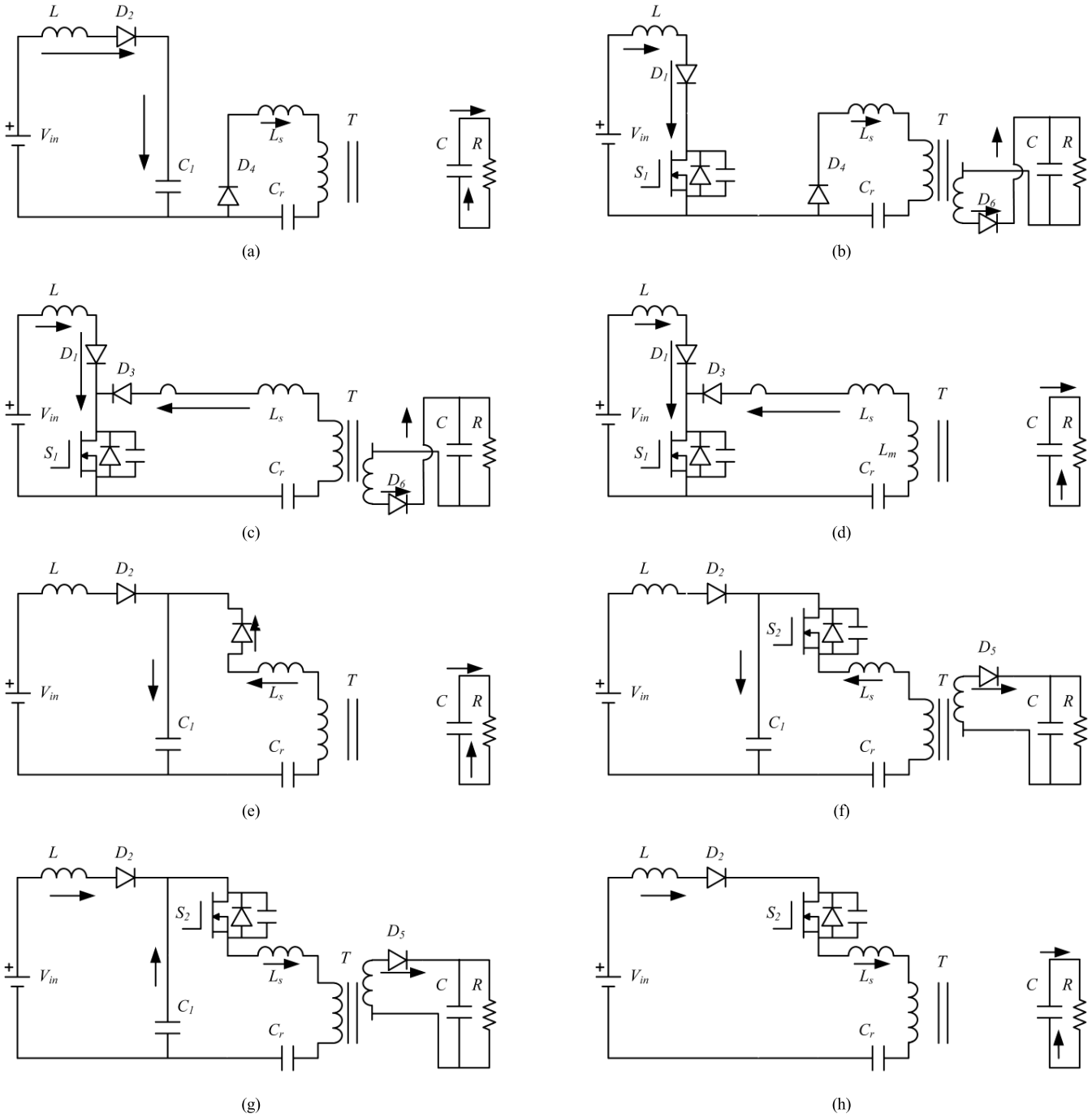

FIGURE 4. Operating circuits of the proposed LED driver for each operational model (a) model 1 ($t_0 - t_1$); (b) model 2 ($t_1 - t_2$); (c) model 3 ($t_2 - t_3$); (d) model 4 ($t_3 - t_4$); (e) model 5 ($t_4 - t_5$); (f) model 6 ($t_5 - t_6$); (g) model 7 ($t_6 - t_7$); (h) model 8 ($t_7 - t_8$).

III. DESIGN CONSIDERATIONS ARE DISCUSSED

According to the subinterval analysis above part, the proposed novel LED driver can operate with desired goal. The boost circuit as a PFC function and the LLC as a dc/dc regulate output current. To reasonable design the parameters of the converter. The two units of the LED driver are analyzed, respectively.

A. BOOST PFC CIRCUIT

In this paper, the boost circuit used to achieve PFC function and generated a constant bus voltage for LLC stage input, when the current of inductor L work in DCM state. The input line voltage assumed constant in one operating period.

$$v_{in}(t) = V_m \sin \omega t \tag{15}$$

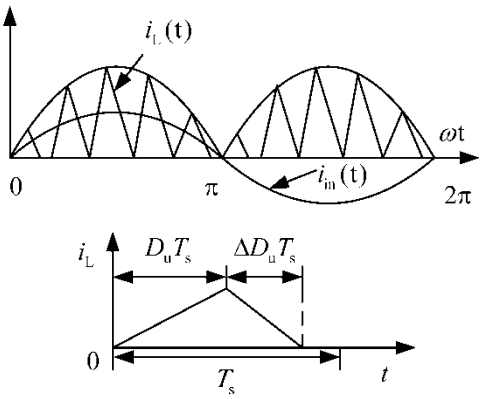

FIGURE 5. Operating waveforms of $i_{L(t)}$ and i_{Lp}.

Here, V_m denote the amplitude, ω is the angular frequency of the input voltage.

The rectified input line voltage can be described in (16).

$$V_{rec}(t) = V_m \left|\sin \omega t\right| \tag{16}$$

Where, $\omega = 2\pi f_l$, f_l is the input line voltage frequency, because of the input line voltage frequency is significantly small than operating frequency, so that the voltage V_{rec} can be assumed is a constant voltage in one period.

The average input current in one switching period that can be expressed as:

$$I_{in}(t) = \frac{1}{2}\frac{t_{on}}{T_s} I_{Lp}(t) \tag{17}$$

Where, I_{Lp} is the peak current of inductor L in one period and is the turn on time of switch S_1, is the switching period.

The peak current of inductor L is:

$$I_{Lp}(t) = \frac{V_{rec}(t)}{L} \cdot D_u T_s \tag{18}$$

Where, D_u is the duty ratio of S_1, $D_u = t_{on}/T_s$.

As we all know, the boost circuit operates in DCM state in one period achieving PCF function. At the time T_{on} the switch S_1 is start to turn OFF, the current of inductor reach peak value, at the time T_{dis} the switch S_1 is continue turn OFF, and the current of inductor reset zero value. According to Fig. 5, T_{dis} and ΔD_u can be expressed as, respectively.

$$T_{dis} = T_{on} + T'_{off} \tag{19}$$

$$\Delta D_u = \frac{T'_{off}}{T_s} \tag{20}$$

From the above equation, the relationship of duty ratio ΔD_u and D_u should be satisfied the following:

$$\Delta D_u < (1 - D_u) \tag{21}$$

Therefore using equation (22), the average input current of the boost circuit in one operating period can be written as:

$$i_{in}(t) = \frac{D^2 T_s V_m}{2L} \sin \omega t \tag{22}$$

From the equation it can be seen that the input current shape in phase with input line voltage then the unity PF is achieved when the boost circuit work in DCM state.

$$\frac{V_{bus}}{V_m} = \frac{D_u + \Delta D_u}{\Delta D_u} \tag{23}$$

Where, V_{bus} is the output voltage of the boost unit. Due to the stored energy capacitor, C_1 can be regarded as large significantly. So V_{bus} can be assumed equal to V_C, i.e., $V_{bus} = V_C$.

The power from input ac source delivers to the LLC resonant converter is equal to P_o. Assuming that the loss of the proposed boost stage can be neglected, the efficiency is 100%, that is

$$P_o = P_{in} = \frac{1}{2} V_m I_{in} \tag{24}$$

$$P_{in} = \frac{1}{2\pi}\int_0^{2\pi} v_{in} i_{in} d\omega = \frac{V_m^2 D_u^2}{4Lf_s} \tag{25}$$

$$\frac{I_o}{I_{in}} = \frac{\Delta D_u}{D_u + \Delta D_u} \tag{26}$$

Where, I_o is the output current of the boost.

Therefore, the duty ratio of S1 can be calculated as:

$$D_u = \sqrt{\frac{4P_0 L f_s}{V_m^2}} \tag{27}$$

Where, $f_s = 1/T_s = \omega/2\pi$.

According to the above output power equation, the value of inductor L can be obtained.

$$L = \frac{D_u^2 V_m^2}{4P_0 f_s} \tag{28}$$

When the circuits work in DCM state, the duty ratio is already known. Here, assuming that$V_{rec} = V_m$. Especially, the current maximum and average values of diode D_1, $I_{D-\max}$ can be calculated as

$$I_{D1} = \frac{1}{2} I_L \cdot D_u^2 = \frac{D_u^2 V_m}{2Lf_s} \tag{29}$$

$$I_{D1-\max} = I_{L-\max} = \frac{D_u V_m}{Lf_s} \tag{30}$$

Where, I_{D1} and $I_{D1-\max}$ are the average current and maximum current flow through diode D_1 in an entire switching cycle, respectively.

B. LLC RESONANT CONVERTER

In this paper, the conventional fundamental harmonic approximation (FHA) method is used for analysis the LLC operating state. According to FHA, the model of LLC resonant converter was established, as illustrated in Fig. 6. The equivalent circuit of LLC resonant converter is shown in Fig. 7. When the resonant tank is excited by an effective sinusoidal input ac source, the practical resonant circuit can be turned into a linear circuit. In LLC resonant converter equivalent model

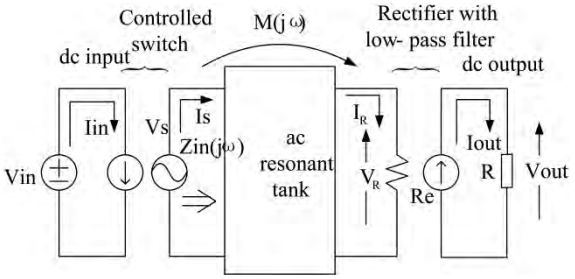

FIGURE 6. LLC resonant converter equivalent model with FHA.

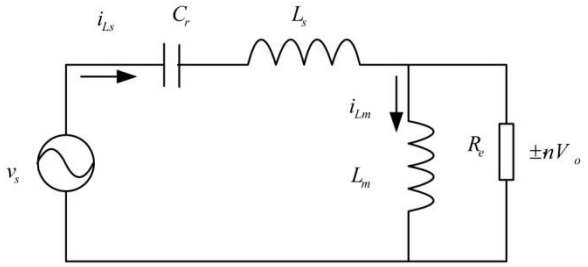

FIGURE 7. LLC resonant converter equivalent circuit diagram.

with FHA, the input ac source of the resonant tank can be expressed as follow:

$$v_s = \frac{2}{\pi} V_{in} \sin(2\pi \cdot f_s \cdot t) \tag{31}$$

$$I_{in} = \frac{2}{\pi} \|i_s\| \cos(\varphi_s) = \frac{2}{\pi} \|v_s\| \mathrm{Re}(\frac{1}{Z_i}) \tag{32}$$

Here, assuming loss can be neglected, the equivalent load can be described as follow:

$$R_e = \frac{8}{\pi^2} n^2 R_{LED} \tag{33}$$

To construct an LLC resonant converter, the first thing should be calculated the voltage gain, therefore according to Fig. 6 the defined variable can be expressed as

$$\frac{V_{out}}{V_{in}} = \|M(j\omega)\| \tag{34}$$

Where, $M(j\omega)$ is the LLC resonant converter voltage conversion ratio, V_{out} is the output voltage of the LED driver, V_{in} is the input voltage of the LLC resonant converter, in other words, is V_{bus}.

In addition to the previous mentioned, ignoring the conduction loss, the input impedance of the LLC circuit can be expressed as:

$$z_{in}(x,k,Q) = z_R \cdot [Q \cdot \frac{x^2 \cdot k^2}{1 + x^2 \cdot k^2 \cdot Q^2} + j(x - \frac{1}{x} + \frac{x \cdot k}{1 + x^2 \cdot k^2 \cdot Q^2})] \tag{35}$$

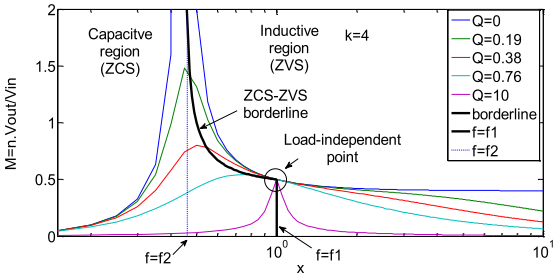

FIGURE 8. Voltage gain along with normal frequency for different Q values.

Using the same FHA method, the voltage gain can be calculated as follows:

$$|M(x,k,Q)| = \frac{1}{2} \cdot \frac{1}{\sqrt{\left[1 + \frac{1}{k} \cdot (1 - \frac{1}{x^2})\right]^2 + Q^2 \cdot (x - \frac{1}{x})^2}} \tag{36}$$

Where, $f_1 = \frac{1}{2\pi\sqrt{L_s \cdot Cr}} f_2 = \frac{1}{2\pi\sqrt{(L_s + L_m)Cr}}$, $x = f_s/f_1$, $k = L_m/L_s$, $Z_R = \sqrt{L_s/C_r}$, $Q = Z_R/\mathrm{Re}$.

Moreover, by using equation (36), the output power of the LLC resonant converter can be calculated as follows:

$$P_{o-LLC} = \frac{V_o^2}{R_{led}} = \frac{V_o^2 \sqrt{\frac{V_{bus}^2}{4n^2 V_o^2} - [\frac{L_s}{L_m}(\frac{f_s^2}{f_2^2} - 1)\frac{f_1^2}{f_s^2}]^2}}{\frac{\pi^2}{8}\frac{\sqrt{L_s/C_r}}{n^2}\left|\frac{f_s}{f_1} - \frac{f_1}{f_s}\right|} \tag{37}$$

Here, V_o is the output power of the LLC resonant converter, R_{led} is the equivalent resistant of LED lamp, V_{bus} is the bus voltage of the novel driver, f_s is the switching frequency.

From formula (36), it is obvious that the voltage gain M is related with the operating frequency of the LLC converter, and the curve M varying with k is illustrated in Fig. 8. Moreover, Fig.8 shows the voltage gain of LLC resonant converter. Therefore, to guarantee the primary side switches work in the ZVS state and the secondary side diodes work in ZCS state, the LLC resonant converter switching frequency should satisfy the condition: $f_2 < f_s < f_1$. For achieve high operating efficiency, the working frequency should be near the frequency f_1. It is obvious that the operating characteristic of the LLC resonant converter with different quality factor is steady. In addition, Fig. 8 shows the borderline between the capacitive region and the inductive region. All the curve with different quality factor Q must be intersected at the load independent point. In the same way, according to formula (36) Fig. 9 shows the LLC resonant converter voltage gain with different k values, which the quality factor Q is the fixed value. As seen, the greater the value of k, the steeper the curve, the voltage conversion ratio is greater. It is clear that, for the lower input voltage of the LLC resonant converter, the voltage gain range is limited. Furthermore, based on the equation (35) Fig.10 illustrates the LLC resonant converter input impedance with different quality factor Q values. As can be seen, above resonance ($x > 1$) input impedance

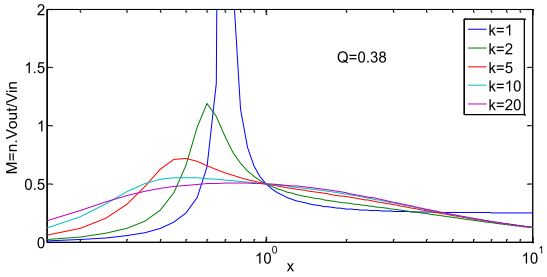

FIGURE 9. The LLC resonant converter voltage gain with different *k* values.

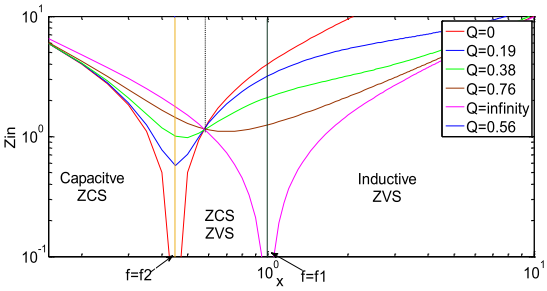

FIGURE 10. The LLC resonant converter input impedance with different Q values.

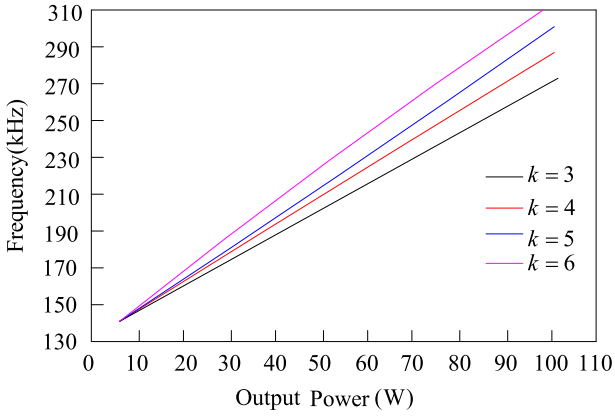

FIGURE 11. Curves of the frequency with varying output power and *k* value.

is always inductive region (ZVS); current lags the voltage. While frequency blow $f_2(x > 1)$ input impedance is always a capacitive region (ZVS); current leads the voltage. In general, the ZVS-ZCS borderline is defined by input impedance equal to zero, i.e., $Z_{in}(j\omega) = 0$. According to Fig. 11, the relationship of the output power and frequency with different k value is given. It is obvious that the operation frequency of the LLC converter rise significantly with increasing output power especially for the higher values of k. Fig. 12 shows the relationship between the bus voltage and working frequency with different values of k. It can be seen that the higher bus voltage value, the higher operation frequency along with k values, the bus voltage is the variation in the frequency from limited lowest-value to highest-value state. Fig. 13 illustrates the relationship between the bus voltage and output power

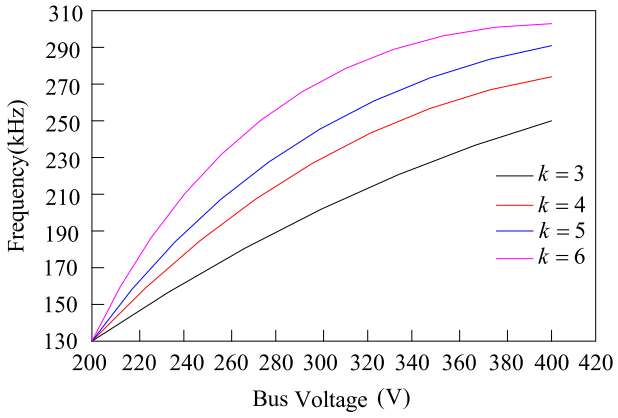

FIGURE 12. Relationship between the bus voltage and frequency with different *k* values.

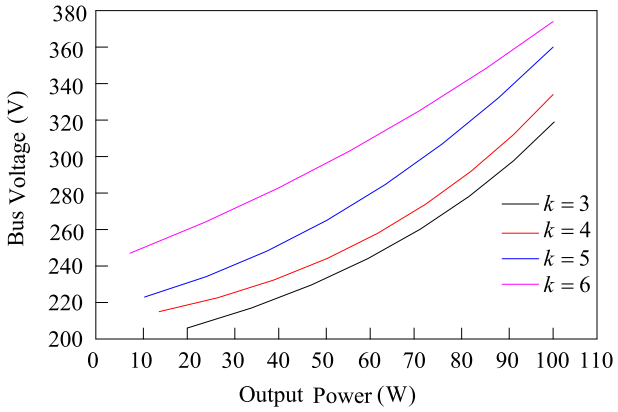

FIGURE 13. Curves of bus voltage with varying output power and *k*.

with the change of k values. As can be seen, the larger value of k is, the smaller variation range of output power is. It is easy concluded that, the value of k is too large and too small are both harmful to converter normal operation.

According to the preceding analysis, an effective and accurate equivalent circuit can be obtained by using Kirchhoff's circuit principle, as shown in Fig. 7. The LLC equivalent input impedance $Z_{in}(j\omega)$ and voltage gain can be calculated as follows:

$$Z_{in}(j\omega) = \frac{1}{j\omega C_r} + j\omega L_s + j\omega L_m // R_e = \frac{R_e(\omega L_m)^2}{(\omega L_m)^2 + R_e^2} + j\left(\frac{R_e^2 \omega L_m}{(\omega L_m)^2 + R_e^2} + \omega L_s - \frac{1}{\omega C_r}\right) \tag{38}$$

$$M(j\omega) = \frac{j\omega L_m // R_e}{Z_{in}(j\omega)} = \frac{j\omega L_m // R_e}{\frac{R_e(\omega L_m)^2}{(\omega L_m)^2 + R_e^2} + j\left(\frac{R_e^2 \omega L_m}{(\omega L_m)^2 + R_e^2} + \omega L_s - \frac{1}{\omega C_r}\right)} \tag{39}$$

Here, L_s is the leakage inductance, L_m is the magnetizing inductance of the transformer, C_r is the blocking capacitance, V_o is the output voltage, R_e is the equivalent resistance from

the secondary side converter to primary side, n is the turn ratio of the transformer.

IV. EXPERIMENTAL VERIFICATION OF THE PROPOSED CONVERTER

In order to verify the correction of the previous theory analysis and further design consideration, a LED driver rated power at 100-W, the 70V output voltage was designed and implemented in laboratory prototype. The proposed driver is designed for supplying an LED string composed of two 50W white LEDs modules by a 220V/50Hz line voltage. The 50W LED module employed here is from OSRAM brand, which is 35V/1.5A, and the luminous flux is 4000LM. Then, the output current of the LED driver is 1.5A, which is 5 LEDs in parallel. The output voltage of LED driver is 70V, which is 20 LEDs in series. The static equivalent resistance of LED lamp can be calculated with the forward voltage and flow current.

$$R_{LED} = \frac{V_{LED}}{I_{LED}} = \frac{V_{th} + R_d \times I_o}{I_o} \tag{40}$$

Where, V_{th} is the threshold voltage, R_d is the resistance parameters of the LED equivalent circuit, and I_o is the output current.

The LED driver output power can be expressed as follow:

$$P_o = P_{in}/\eta = \frac{V_o}{R_{LED}} \tag{41}$$

Where, η is the efficiency of the driver and P_o is the output power. Assume that is equal to 90%.

Because the lowest normal line input voltage is 85V and the constant duty ratio is 50%. According to above-known parameters, the inductor L can be calculated:

$$L = \frac{D_u^2 V_m^2}{4P_0 f_s} = \frac{0.5^2(\sqrt{2} \times 85)^2}{4 \times 100 \times 130 \times 10^3} = 69(\mu\text{H}) \tag{42}$$

Here, high-frequency ferrite material PC40 is used for the inductor L core. To avoid the core saturation, the max magnetic flux density is set to 0.8 times of the saturation magnetic flux density. The inductor L is free from saturation effect, which means the boost circuit can operate in DCM conduction and as the PCF function.

The maximum current stresses on diode D_1 namely $I_{D-\max}$ can be calculated as

$$I_{D1-\max} = I_{L-\max} = \frac{D_u V_m}{L f_s} = \frac{0.5 \times \sqrt{2} \times 85}{69 \times 10^{-6} \times 130 \times 10^3} = 6.6(\text{A}) \tag{43}$$

The magnetizing inductance L_m and leakage inductance L_s can be calculated as follows, respective:

$$L_s = \frac{1}{4\pi^2 f_1^2 C_r} \tag{44}$$

$$L_m = \frac{1}{4\pi^2 f_2^2 C_r} - L_s \tag{45}$$

Here, the core of the transformer is PQ32, then the primary and secondary turns can be calculated as follows.

$$N_P = \frac{nV_o \Delta T}{\Delta B A_e} \times 10^4 \tag{46}$$

$$N_s = \frac{N_p(V_{in} + V_D)}{V_o} \tag{47}$$

The output filter capacitor C_o capacitance value is calculated according to [19].

$$C_o \geq \frac{I_o \cdot V_{ripple}}{4\pi \cdot f_s \cdot V_o \cdot V_{Co\_ripple}} \tag{48}$$

Where, I_o is output current of the LED driver, f_s is the switching frequency, V_{ripple} is the allowed output voltage ripple, V_o is the voltage stresses on LED lamp, as well as V_{Co_ripple} represents the maximum peak-to-peak.

The control method employed for the proposed LED driver is pulse frequency modulation (PFM) because of LLC part need variable frequency control strategy.

In order to realize high efficiency and good dynamic of the system, the control circuit comprises six parts, the sampling circuit, the protecting circuit, the input signal photocoupler isolation circuit, the digital controller, the driver photocoupler isolation circuit, the driver circuit, as depicted in Fig. 14. The detail signal processing of the proposed driver follows. First, the output current and output voltage is sampled, filtered and amplified. Here, LM321 from the national semiconductor is adopted as the precision preamplifier and voltage follower. Second, similarly, input voltage is sampled through divide voltage resistive, voltage follower and amplifier. Then, the sampled signal input to the digital controller. Third, photocoupler chip PC357 is chosen to isolate the sampled signal and microcontroller Unit (MCU). Fourth, a TMS320F28335 manufactured by Texas Instruments is used for the digital controller. The sampled output current, output voltage, and input voltage analog signal are converted into digital signals in the ADC module of the control unit. A pulse frequency modulation (PFM) square wave with an approximately 50% duty cycle is generated by the MCU, which can be used for driving the switches. Fifth, driver photocoupler circuit is added as HCPL2232 between the digital controller and the driver circuit for electrical isolation function. Sixth, chip IR2110 is adapted to drive the switch.

Table 1 shows the specifications of the proposed prototype converter. For the high-frequency integration transformer, we selected the PQ32 ferrite core, which has an effective magnetic path length of 55.5 mm. Under the lowest input voltage and maximum output power condition, the voltage gain of the converter is lowest, and the low switching frequency f_s is chosen as 136kHz. Due to the ferrite core is used, the maximum magnetic density ΔB could be chosen as 0.3-0.4.

According to equation (49), the primary minimum number turns of the transformer can be approximately obtained as

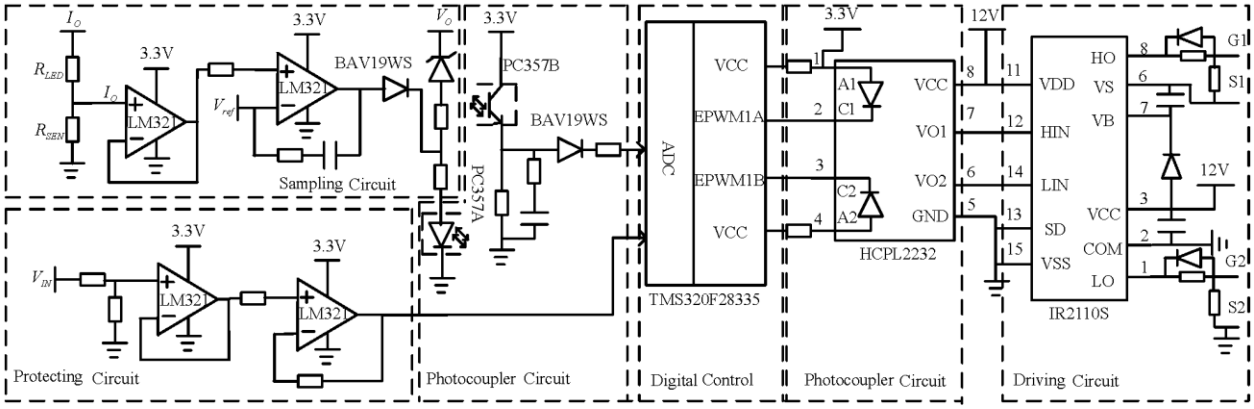

FIGURE 14. The control circuit of the proposed converter.

TABLE 1. Design specifications.

Parameters	Values
Input voltage *Vin*	220VAC
The output voltage *Vout*	70V/1.43A (100W)
Switching frequency f_s	250kHz
Minimum resonant frequency f_2	136 kHz
Maximum resonant frequency f_1	270 kHz
Resonant capacitor *Cr*	15nF
Resonance inductance L_s	25uH
Magnetic inductance L_m	124 uH
Magnetic inductance and leakage inductance ratio	4
Transformer turns ratio *n*	1.5(9/6)

TABLE 2. Components of the proposed converter.

Parameters	Values
Rectifier bridge diodes	1N4004
Secondary rectifier diodes(D_5-D_6)	STPS3150(150V,0.67VF)
Primary side diodes(D_1-D_2)	STTH3R06(600V, 1.7VF)
Switches (S_1-S_2)	STF3LN80K5(800V,2A)
Transformer (*T*)	PQ32(TDK/PC44)
Resonant capacitor (C_r)	Vishay(15nF/MKP)
Driver chip	IR2110
Driver isolation optocoupler	HCPL-2232
feedback isolation optocoupler	PC357
Digital controller	TMS320F28335
Sensed current resistor	0.05 Ω /2W

follows:

$$N_{p-\min} = \frac{nT_{s-\min}(V_{LED} - V_F)(L_m - L_s)}{L_m \Delta B A_e} \tag{49}$$

Where, n is the turns ratio of the transformer, $T_{s-\min}$ is the minimum switching period i.e., $1/f_{s-\min}$, A_e is the effective area of the ferrite core, V_F is the voltage drop of the output rectifier diode. The detail components of the proposed converter are summarized in Table 2.

Fig. 15 (a) illustrates the measured waveform of the gate voltage of the switch Q_1 and Q_2 under normal ac input and full load condition. It is clear that the proposed topology operates with the resonant frequency range and the symmetric duty cycle, which is consistent with the aforementioned analysis.

Fig. 15 (b) shows the gate voltage, drain voltage of switches S_2 at full load for the proposed converter. Also, the drain-source voltage of the switches fall to zero before the turn-on gate signal is applied, which indicated that ZVS state is achieved for greatly reduce the turn ON losses of the switches.

According to Fig. 15(c), the primary side current i_p flow through the primary side winding under nominal input voltage and full load condition. It is clear that the ZVS state of the primary switch is achieved by the energy stored in the leakage inductance of the main transformer at full load condition. The resonant tank by operating with the resonant frequency and the low RMS current with the zero offset current.

From the secondary side current i_s in Fig. 15 (d) it can be seen that, the proposed converter for LED driver, which enables the secondary switch turn off losses to be minimized. From this figure, it is noted that the secondary side diodes has low turn off losses and wide ZCS state range, which conform to the previously mentioned theoretical analysis.

As shown in Fig. 15 (e) the voltage across the resonant capacitor V_{Cr} is charge and discharged by the primary current i_{pri}. The switching frequency used in the experiment can have a slight difference compared with the theoretical analysis because of the duty ratio loss resulting from the transformer leakage inductance.

Fig. 15 (f) presents the experimental voltage waveform of half bridge middle point and the resonant capacitor. In the primary switch ZVS conditions are achieved, thus it is operated with very low switching losses.

Fig. 15 (g) shows input voltage v_{in} and input current i_{in} of the proposed driver. It is observed that the input current is approximately sinusoidal and in phase to the input voltage without any phase shifting, and a high PF is achieved. Therefore, the boost circuit shows described function as PFC stage.

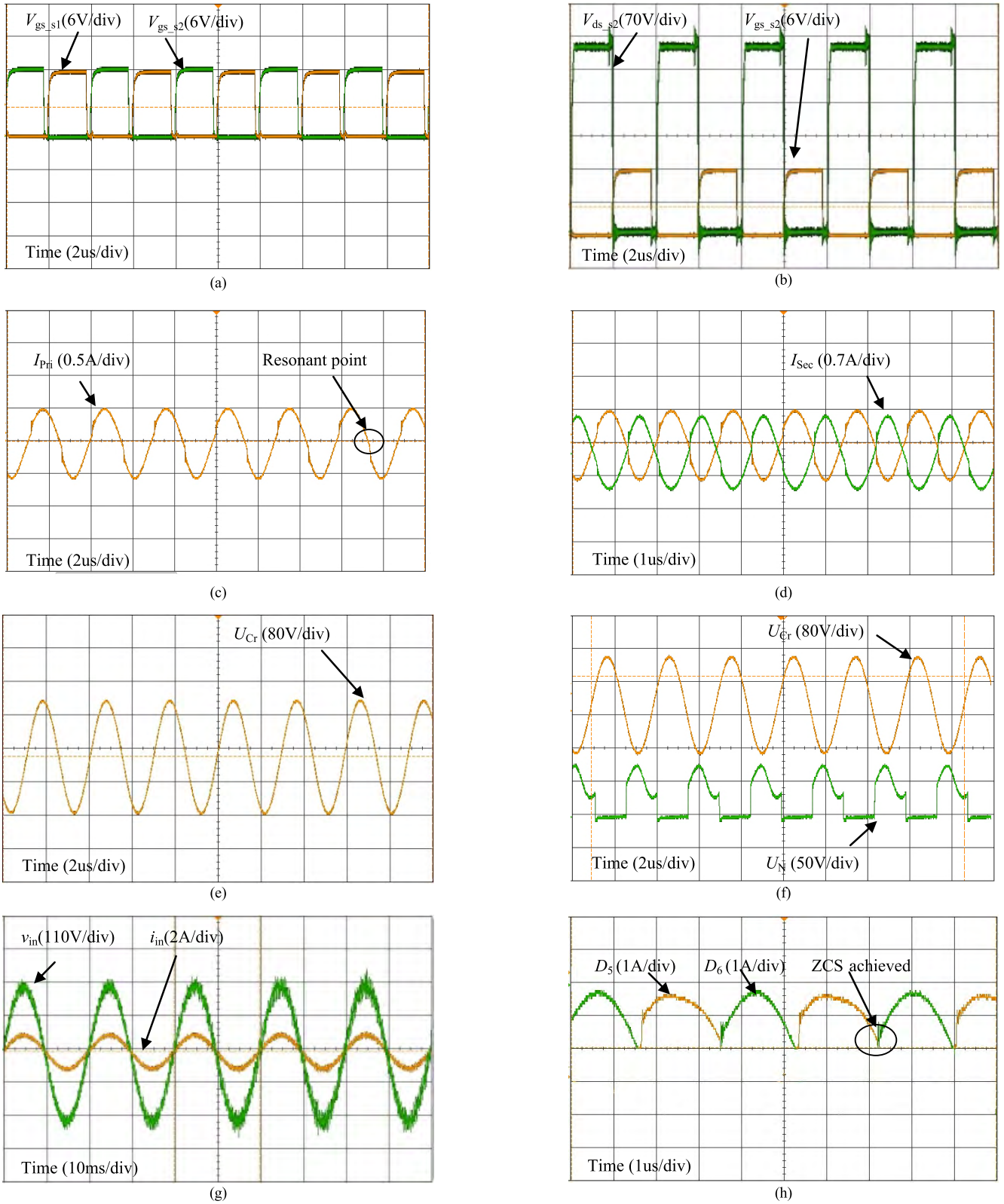

FIGURE 15. Experimental curves of the proposed converter: (a) Experimental waveform of S_1 and S_2 gate voltages, (b) Gate voltage, drain voltage of switches S_2 at full load (c) Primary winding current at rate output power (d) Secondary winding current at rate output power. (e) The waveform of the resonant capacitor voltage. (f) The voltage waveform of half bridge middle point and resonant capacitor (g) Input voltage and input current. (h) Currents through the secondary rectifier diodes.

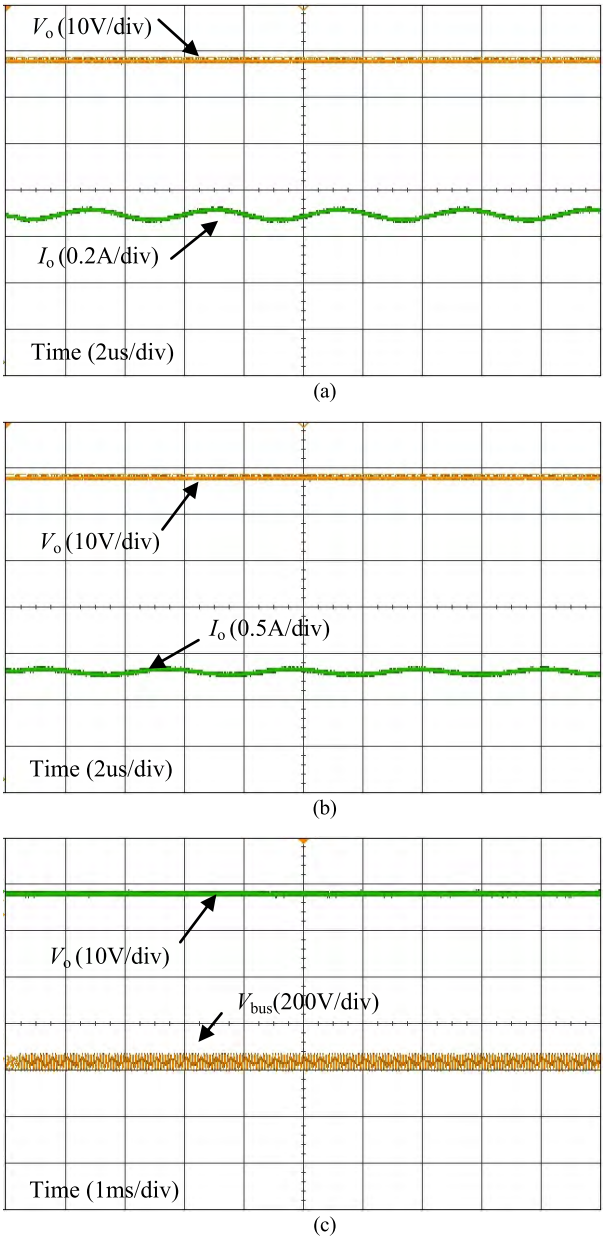

FIGURE 16. Curves of the output voltage, bus voltage, and output current: (a) Waveform of the voltage and current (half load). (b) Waveform of the voltage and current (full load). (c) Bus voltage and output voltage (220Vac input).

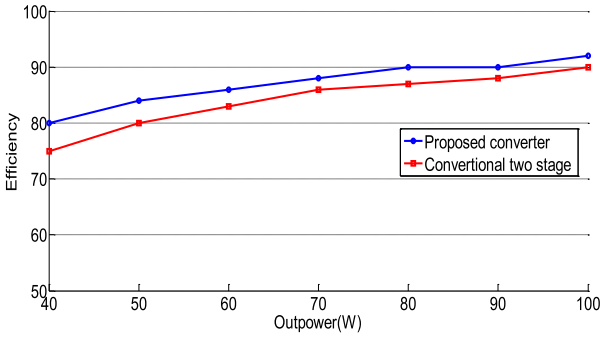

FIGURE 17. Measured efficiency of the prototype with the proposed LED driver.

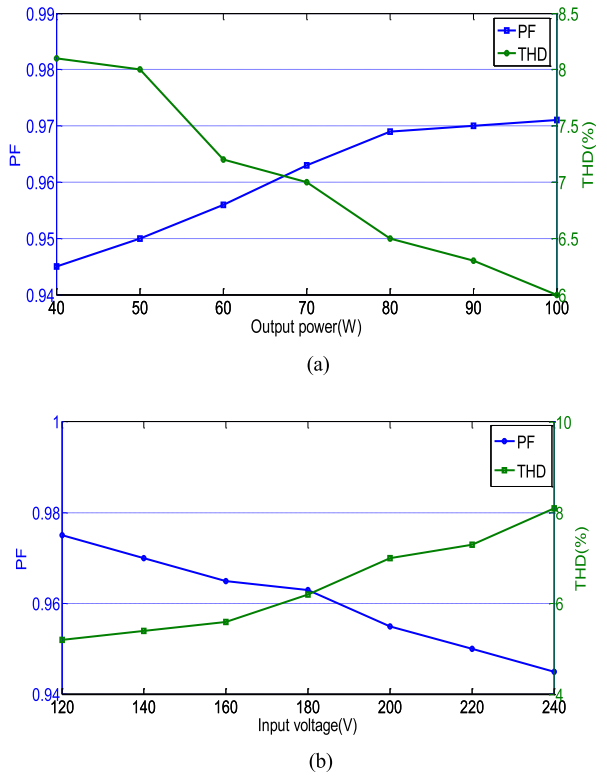

FIGURE 18. Test results of PF and THD. (a) Power factor and THD with output power changing. (b) Power factor and THD with input voltage changing.

Fig. 15 (h) shows the currents through secondary rectifier diodes D5 and D6. The measured waveforms indicate that the two rectifier diodes are turn off under the ZCS condition at full load, which are the help to significantly reduce the switching loss.

Fig. 16 shows the waveforms of the output current and voltage of the proposed converter. Fig. 16(a) shows the output voltage and output current in half-load; the output voltage is 70V; the output current is 0.75A. Fig. 16(b) shows the output voltage and output current in full load; the output voltage is 70V; the output current is 1.4A. The output voltage almost keeps constant through the whole range of output power. The measured bus voltage and output voltage are shown in Fig. 16(c), the average bus voltage and peak-peak values are approximately 610V and 50V, respectively. Although the bus voltage peak-peak value is relatively high, the output voltage is not affected because of the switches integration, which is in agreement with theoretical analysis.

Fig. 17 shows the measured efficiency variations of the proposed single-stage converter and conventional two stages as a function of output power. It is evident that when the load range is from 40W to 100W, the efficiency is always higher than 80%, and the efficiency of the proposed single-stage LED driver is always higher than the conventional two-stage converter. According to this Fig. 17 the more power becomes

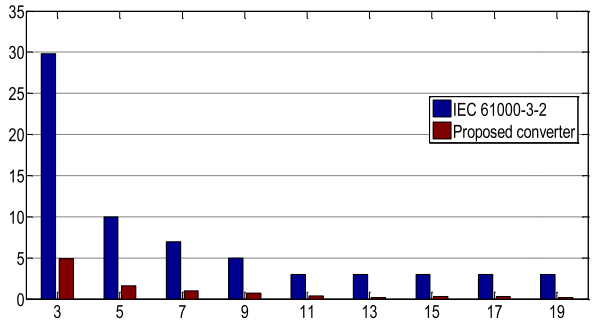

FIGURE 19. Input-current harmonics compared with IEC 61000-3-2 Class C standard.

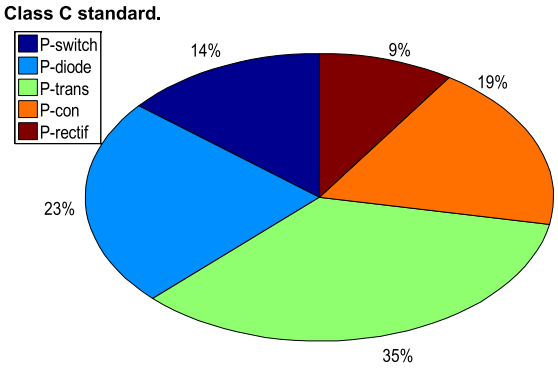

FIGURE 20. The proposed converter loss distribution.

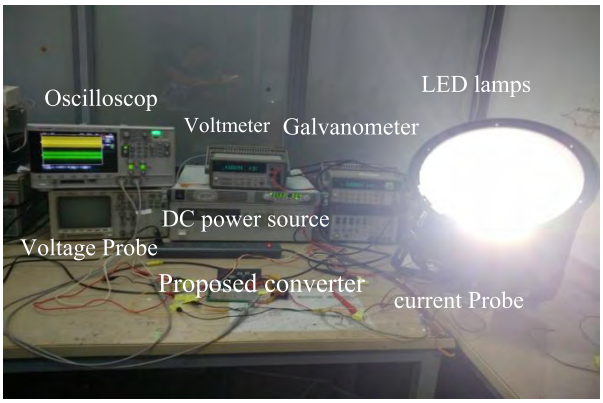

FIGURE 21. Photo of the experimental system.

the less circulating current pass through switches which lead to increase efficiency. As depicted in Fig. 18(a), it can be seen that with the output power change from 40W to 100W, the total harmonic distortion (THD) is the change from 6.1% to 8% and the PF remains above 0.95, which keep in a low level. Fig. 18(b) shows the curves of the converter PF and THD with changing input voltage. As shown in Fig. 18(b), when the input voltage changed from 120Vac to 240Vac, the THD is changing from 5.6% to 8.3% and PF remains above 0.94. According to IEC 61000-3-2 standard, the input harmonics components are established as a Class D device when the out power in full load. The measured harmonics content compared with IEC 61000-3-2 Class D regulation is shown in Fig. 19. Fig. 20 gives the loss distribution of the proposed converter at the full load. P-switch, P-diode, P-trans, P-con, and P-rectifier are the switching loss, the diodes loss, the transformer loss, the conduction loss and the rectifier diodes loss. The transformer loss takes the main part of the whole loss. The transformer loss includes ferrites loss and copper loss. On the basis of the switches integration method, the number of switchers can be further minimized, the switching losses could significantly reduce, and the system efficiency greatly improved. Fig. 21 shows the photograph of the experimental system for the proposed LED driver.

V. CONCLUSION

In this paper, a novel single-stage AC/DC converter based on the boost circuit and an LLC series resonant circuit are proposed. Because the DCM boost circuit is operated by integrating the switches of the half-bridge LLC resonant converter, the performance of the converter was realized, including power factor correction, voltage gain, and the soft switching characteristic of the LLC resonant converter. Two circuit functions are not affected by switch integration. Moreover, the integrated switches equally share the stresses of current and voltage, which further improve the performance of the driver. A 100W prototype was built, the experimental results well verify the proposed theoretical and the driver efficiency is as much as 91.5% in full load.

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JIANGUANG MA was born in Xingtai, Hebei, China. He received the B.S. degree in electronic engineering from the Hebei University of Science and Technology, Shijiazhuang, China, in 2010, and the M.S. degree from the Inner Mongolia University of Technology, Hohhot, China, in 2014.

He is currently pursuing the Ph.D. degree in electronic engineering with Beijing Jiaotong University, Beijing, China. His current research interests include power electronics, ac/dc converter, resonant converter, and light-emitting diode lighting systems.

XUEYE WEI was born in Weifang, Shandong, China, in 1963. He received the B.S. and M.S. degrees from Tianjin University in 1985 and in 1988, respectively, and the Ph.D. degree from the Beijing Institute of Technology in 1994.

He is currently a Professor and a Ph.D. Supervisor with Beijing Jiaotong University. His current research interests include renewable science and technology, measurement and process control, and digital signal processing.

LIANG HU was born in Shijiazhuang, Hebei, China, in 1988. He received the B.S. and M.S. degrees in electronic engineering from Yunnan University, Kunming, Yunnan, in 2010 and 2013, respectively.

He is currently pursuing the Ph.D. degree in electronic engineering with Beijing Jiaotong University, Beijing, China. His current research interests include power electronics, renewable energy systems, and digital signal processing.

JUNHONG ZHANG was born in Handan, Hebei, China, in 1975. She received the B.S. and M.S. degrees from Beijing Jiaotong University in 1998 and 2003, respectively, where she is currently pursuing the Ph.D. degree in traffic information and control engineering. She is currently a Lecturer with the Beijing University of Civil Engineering and Architecture. Her research interests include computer simulation and photovoltaic power generation technology.