Development of Power Electronic Distribution Transformer Based on Adaptive PI Controller

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ABSTRACT In recent years, power electronic distribution transformers (PEDTs) have become an attractive replacement for conventional transformers. This is due to their smaller size, improved dynamic performance, and better power quality. However, their operation with a conventional controller such as a proportional integral (PI) does not give satisfactory performance. Thus, improved dynamic performance and high power quality of the PEDT can be achieved with an intelligent control. In this paper, a novel design topology and an improved controller for a PEDT are proposed. The proposed controller is based on the adaptive PI-fuzzy logic controller (API-FLC). The FLC is applied to adapt the PI controller gains when there is a sudden change in the system parameters. The PEDT with the novel controller is designed to achieve constant dc link voltages, sinusoidal voltage, and current with unity power factor under different operating conditions. The model is simulated and validated using MATLAB/Simulink software. Different operating conditions, including voltage sag, voltage harmonics, sudden load change, and short circuit, have been investigated. The results obtained with the API-FLC controller give a better dynamic performance and improved power quality when compared to the conventional PI controller. Therefore, the PEDT based on API-FLC has the advantages of eliminating transient power quality problems and improving system efficiency.

INDEX TERMS Power electronics transformer, multilevel converter, fuzzy logic control.

I. INTRODUCTION

The power-electronic distribution transformer (PEDT) is a new transformation device based on the power electronics on both primary and secondary sides. A PEDT is also referred to as a solid-state transformer [1]. PEDTs were first proposed by William [2]. Currently, PEDTs are used in many applications for delivering electric power to consumers. Examples of such applications are in wind turbines, tidal power plants, solar energy plants, energy storage DC fast chargers, Var compensation, harmonic elimination, and smart grid distribution systems [3]. The increased use of PEDTs is due to their advantages over conventional transformers. These advantages are their better energy storage capability, smaller size, lower weight, voltage sag/swell compensation, harmonics elimination, power factor correction, and fault isolation [4], [5].

Recently, several researchers have focused on the design topologies and control of PEDTs [6]–[8]. Generally, there are two approaches to designing PEDTs. The first approach does not have a DC-link while the second has a DC-link. In the first approach, the transformer size and stress factor are noticeably reduced. However, this type has the drawback that it is difficult to implement feedback control and power factor improvement [9]–[11]. On the other hand, the second approach has better control, a higher power factor, and a lower stress factor [1], [12]. This is because this type consists of three parts: an input stage, an isolation stage, and an output stage. The input stage is a three-phase AC/DC converter used to convert AC voltage to DC voltage, while the isolation stage is a DC/DC converter connected with a high-frequency (HF) transformer to provide galvanic isolation and transformation. The output stage of the DC-link type acts as a three-phase DC/AC, which provides the desired AC voltage with 50 Hz frequency.

The proportional integral (PI) controller is most commonly used in power electronic converter applications. It has a simple control structure that delivers good DC link voltage regulation, an improved power factor (PF), and less total harmonic
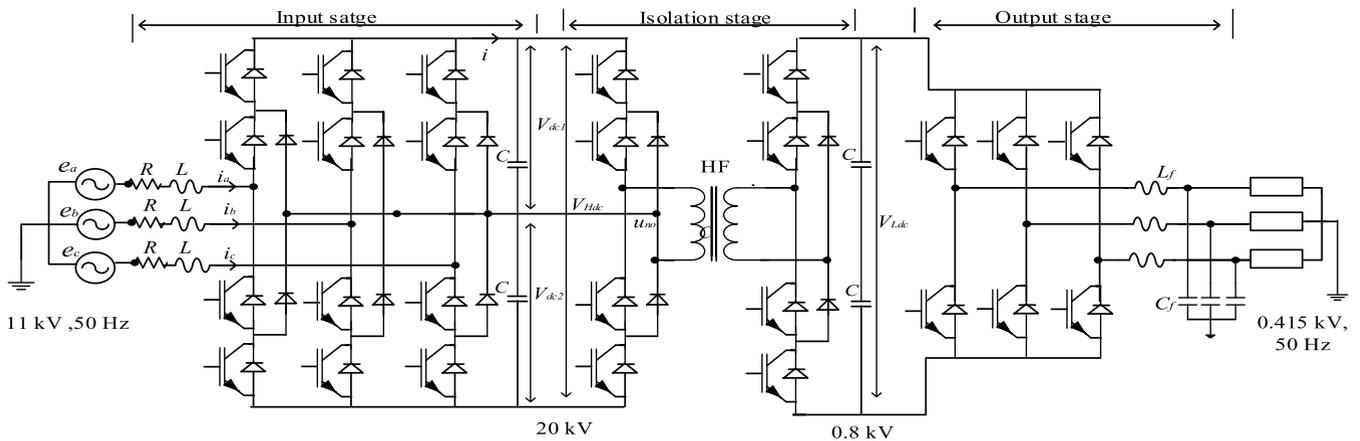
FIGURE 1. The proposed topologies of the PEDT.

distortion (THD) when operated in the fixed range [13], [14]. However, the PI controller is inadequate when there is a transient or continuous disturbance during the system operation. Furthermore, the fixed PI control gain values have a slow dynamic response, large overshoot, and oscillations during varying operating conditions.

Recently, intelligent controllers such as fuzzy logic controllers (FLCs), artificial neural networks, and linear quadratic regulators have become increasingly useful when the system dynamics are not well known or contain significant nonlinearities [15]. Among the various intelligent control techniques, the FLC, which was proposed earlier by Zadeh [16], incorporates features that make it attractive. Some of these features include its ability to handle linear and nonlinear systems, its advantage of not requiring a system dynamic model for control, and the fact that it provides good dynamic performance. Many researchers have proposed advanced control techniques for power electronics circuits based on fuzzy logic [17]–[19]. A key disadvantage of the FLC is the challenges faced during hardware and software implementation as a result of the high computational burden [20]. To overcome these challenges, a hybrid fuzzy–PI controller was proposed in [21], where the FLC was used to adapt the gain of the conventional PI controller based on the error (*e*) and change of error (*ce*) when there is variation in the operating conditions. This combination gives a significant improvement in system dynamic performance.

This paper presents the development of a PEDT based on an adaptive proportional integral–fuzzy logic controller (API-FLC) to improve the dynamic performance and power quality. The PEDT control was developed based on the PI controller with a fuzzy logic controller adaptation. The FLC is used to modify the PI gain when there is a transient disturbance in terms of voltage sag, sudden load change, and short circuit fault. The dynamic performance and power quality of the proposed API-FLC were compared with those of a PI controller. The API-FLC delivers better dynamic responses and improved power quality. The rest of the paper is organized as follows: Section II presents the principle operation of

the PEDT while Section III describes the PEDT modeling and control strategies. Section IV presents and discusses the results. Lastly, the conclusion is presented in Section V.

II. OPERATING PRINCIPLE OF PEDT

The proposed topology of the PEDT is presented in Figure 1. It has three stages: an input stage, an isolation stage, and an output stage. The input stage is a three-phase three-level PWM converter, acting as a rectifier to convert the AC grid voltage and current to DC. The three-level rectifier is used in the input stage to improve the power factor of the system, reduce the THD on the grid side, and regulate the high voltage of the DC-link. The isolation stage consists of double-half-bridge three-level converters connected to an HF transformer between them. The first half-bridge converter generates the HF square-wave voltage from the DC voltage. Then the HF transformer steps down the HF square-wave voltage and the second half-bridge converter rectifiers back the HF voltage to the DC voltage. The last stage is the output stage, consisting of a two-level three-phase DC/AC inverter, which regenerates the desired AC waveforms. In the proposed topology, the three-level converter is used in the input stage and the isolation stage to achieve a high voltage level as well as to improve the power quality of the PEDT. On the other hand, each stage of the PEDT has an independent control unit. A PI controller adapted with fuzzy logic control (API-FLC) is proposed for the PEDT in order to improve the dynamic response and power quality. The next sections present a detailed discussion of the control system of each stage.

III. PEDT MODELING AND CONTROL STRATEGIES

The control is the heart of a PEDT and each stage has independent control. The following subsections provide the modeling and control of each stage in detail.

A. MODELING AND CONTROL FOR THE INPUT STAGE

The input stage is a three-level three-phase Pulse Width Modulation (PWM) rectifier (Figure 1). The mathematical model

in the *abc* frame of the three-level PWM rectifier is:

$$e_a = L\frac{di_a}{dt} + Ri_a + s_{a1}v_{dc1} - s_{a2}v_{dc2} + u_{no} \quad (1)$$

$$e_b = L\frac{di_b}{dt} + Ri_b + s_{b1}v_{dc1} - s_{b2}v_{dc2} + u_{no} \quad (2)$$

$$e_c = L\frac{di_c}{dt} + Ri_c + s_{c1}v_{dc1} - s_{c2}v_{dc2} + u_{no} \quad (3)$$

and the DC capacitor voltages are:

$$C_d\frac{dv_{dc1}}{dt} = s_{a1}i_a + s_{b1}i_b + s_{c2}i_c - i \quad (4)$$

$$C_d\frac{dv_{dc2}}{dt} = -s_{a2}i_a - s_{b2}i_b - s_{c2}i_c - i \quad (5)$$

where e_a, e_b, and e_c are the three-phase input AC voltages and L is the inductance between the grid and the converter, R is the resistance between the grid and the converter, V_{dc1} and V_{dc2} are the DC-link voltage, i is the rectifier output current, C_d is the DC-link capacitor, S_a, S_b, and S_c are the switching functions, and u_{no} is the voltage between the grid neutral point and the three-level rectifier neutral point on the DC side.

For the modeling and design of the controller, it is useful to convert three-phase *a, b, c* variables into a rotating *d–q* frame. This reference frame theory is based on Park's transformation [22]. The three-level PWM rectifier in the synchronous rotation *d–q* coordinate can be formulated by:

$$L\frac{di_d}{dt} = -Ri_d + \omega Li_q - s_{d1}v_{dc} + s_{d2}v_{dc} + e_d \quad (6)$$

$$L\frac{di_q}{dt} = -Ri_q - \omega Li_d - s_{q1}v_{dc} + s_{q2}v_{dc} + e_q \quad (7)$$

and the DC capacitor voltages are:

$$C_d\frac{dv_{dc1}}{dt} = \frac{3}{2}(s_{d1}i_d + s_{q1}i_q) - i \quad (8)$$

$$C_d\frac{dv_{dc2}}{dt} = -\frac{3}{2}(s_{d2}i_d + s_{q2}i_q) - i \quad (9)$$
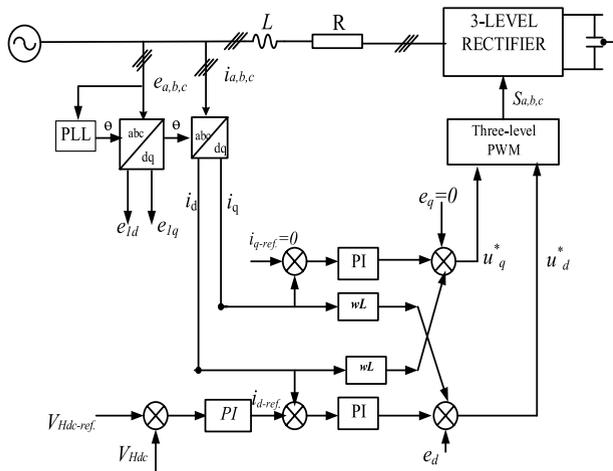
FIGURE 2. Block diagram of the input stage using the PI controller.

The comprehensive decoupled *d–q* controller for the inner current loop and voltage outer loop is presented in Figure 2. The double closed-loop controller of the input stage of the

PEDT can be obtained using a PI controller according to Eqs. (6), (7), and (8). The output DC voltage and the reference voltage are compared in order to implement the control for the outer voltage loop. The difference between the output and reference voltages was passed to the PI controller to generate a reference value for controlling the inner current $i_{d-.ref.}$, while $i_{q-ref.}$ was set to zero to achieve unity power factor. Then the reference currents were compared with the measured currents i_d and i_q, and the error was passed to the PI controller. The output of the PI in the current loop for the *d–q* axis, the measured voltage e_{d1} and e_{q1}, and the measured current multiplied by ωL are added to generate the voltage reference to drive the gate drive of the converter.

B. ISOLATION STAGE AND OUTPUT STAGE MODELING AND CONTROL

The isolation stage of the PEDT consists of a high-voltage half-bridge three-level converter and a low-voltage half-bridge converter with a high-frequency transformer in between as shown in Figure 1. The power flows from the primary converter with a leading phase angle into the secondary converter with lagging phase angles. The transferred power is controlled by the phase shift between two square-wave voltages, and the magnitude of the DC link voltages is given by the following relation [23]:

$$P_o = \frac{V_{Hdc}V'_{Ldc}.d.\phi(\pi - |\phi|)}{\pi\omega L} \quad (10)$$

where V_{Hdc} denotes a high-voltage DC link, V'_{Ldc} is the low-voltage DC link referred to the high DC link voltage on the primary side, L is the leakage inductance, $\omega = 2\pi f_w$, f_w is the switching frequency, and ϕ is the phase shift of the PWM signal between the primary and secondary sides.
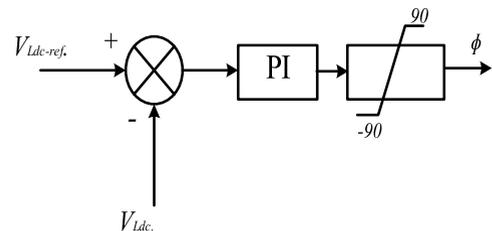
FIGURE 3. The isolation stage control using the PI controller.

Figure 3 illustrates the control structure for the isolation stage based on the PI controller. To generate the PWM signal, the lower DC link voltage is compared to the reference voltage and the estimated error is passed to the PI controller to generate the control signal to drive the half-bridge three-level converters.

The output stage is a two-level three-phase converter as presented in Figure 1. The output stage of the developed PEDT has similar characteristics to the input stage as explained above in Section III-A. Equations (6) to (8) can also be used to model the output converter. So there is no difference between the high-voltage and low-voltage side converters.

The PI control gain (K_P and K_I) was tuned under the normal operating condition based on Ziegler-Nichols tuning. The PI controller gain parameters were set to zero ($K_P = 0$, $K_I = 0$) and then the proportional gain K_P was increased slowly until the system reached the critically stable region (oscillatory state). The corresponding critical value of the proportional gain K_P was referred to the ultimate gain K_u and the measured period of oscillation T was referred to the ultimate period T_u. These two ultimate values were then used to calculate the PI controller parameters. The PI parameter has a fixed value during the variable operating conditions. This leads to poor system dynamic performance when there is a transient disturbance. To overcome this issue, the conventional PI controller was modified to give better dynamic performances in the nonlinear operation, which will be discussed in the next section.
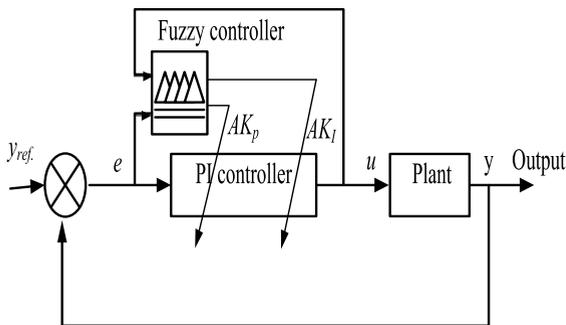
FIGURE 4. PI controller adapted with fuzzy controller.

C. PI CONTROL ADAPTED WITH FUZZY LOGIC CONTROL

The API-FLC was designed based on the PI controller and the FLC auto-tuning part. The FLC auto-adjusts the PI controller gain parameters online to extend the operating range of the controller to handle linear and nonlinear operation. Figure 4 presents the structure of the proposed API-FLC, which consists of two inputs and two output signals. The first input to the FLC is the error (e), which is the difference between the reference and measured values, and the second input is the PI controller output signal (u). The two outputs of the FLC automatically adjust the signal of the K_P and K_I terms of the PI controller. When the system is operating under the steady-state condition, the system is controlled by the initial PI controller gains until a small change in the error is observed by the FLC. When a large disturbance occurs due to load current change or short-circuit faults, the FLC automatically updates the PI gains based on the error (e) signal and the change in the PI output control signal (u). By detecting the possible deviation from the inputs of the FLC, it is possible to automatically set the PI controller parameters for set-point changes and load disturbances.

The fuzzy rules of the controller were developed based on the effect of increasing or decreasing the PI controller parameters on the settling time, rise time, and overshoot. The fuzzy membership functions for each input and output are given as follows: five membership functions were used to maintain
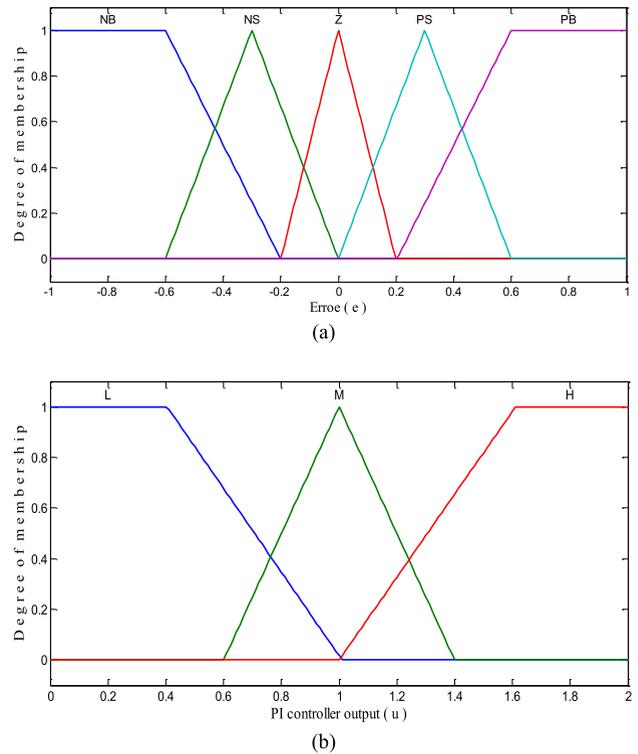
FIGURE 5. Inputs membership function for FLC.

the error (e) within a specified range. The variable (e) was defined as negative big (NB), negative small (NS), zero (Z), positive big (PB), and positive small (PS), as shown in Figure 5 (a). Three membership functions for the output of the PI controller (u) were defined as low (L), medium (M), and high (H), as presented in Figure 5(b). Five membership functions have been used for the two outputs (proportional gain (K_P) and integral gain (K_I)). The fuzzy subsets of the five outputs were classified as very high (VH), high (H), medium (M), low (L), and very low (VL), as seen in Figure 6. This led to $3 * 5 = 15$ rules for K_P and $3 * 5 = 15$ rules for K_I, as listed in Tables 1 and 2.

The structure of the FLC rules to modulate the PI controller gain is written as follows:

If "e" is NB and "u" is L, then "K_P" is VH and "K_I" is H.

..

..

If "e" is PB and "u" is H, then "K_P" is H and "K_I" is M.

The defuzzification method used was based on Centroid, and the defuzzification center average was defined as [24]:

$$\mu(K_P, K_I) = \frac{\sum_{i=1}^{n} c_i \mu_i}{\sum_{i=1}^{n} \mu_i} \quad (11)$$

where $\mu(K_P, K_I)$ are fuzzy gain outputs, c_i is the fuzzy center of the membership function, and μ_i denotes the membership value for the fuzzy set.
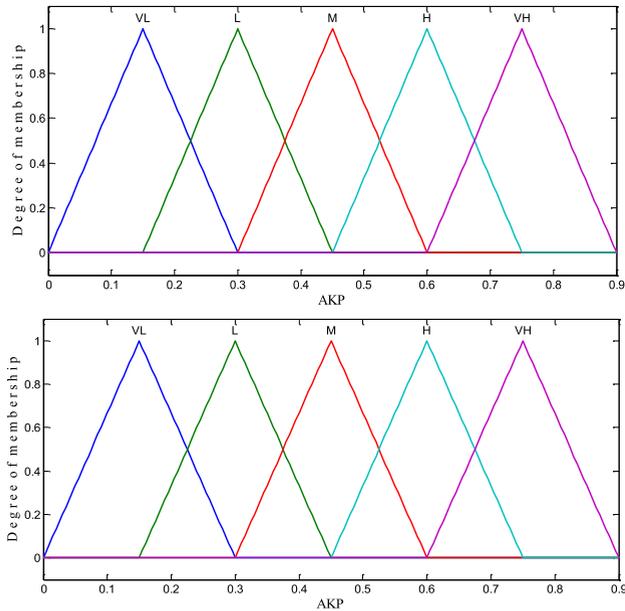
FIGURE 6. Outputs membership function for FLC.

TABLE 1. Fuzzy Rules, AK_P

u/e	NB	NS	Z	PS	PB
L	VH	H	M	L	M
M	H	M	L	L	H
H	M	L	VL	VL	H

TABLE 2. Fuzzy Rules, API-FLC AK_I

u/e	NB	NS	Z	PS	PB
L	H	M	L	VL	VL
M	M	L	L	M	VL
H	M	VL	VL	H	M

FIGURE 7. Input stage control of the PEDT based on API-AFLC.
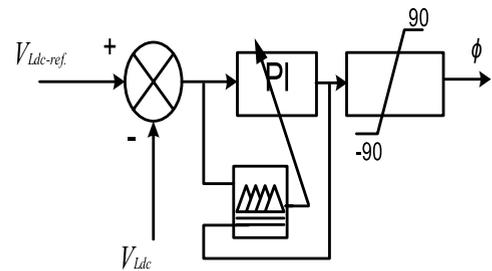
FIGURE 8. The isolation stage control based on API-AFLC.

TABLE 3. Simulation Parameters Considered to Evaluate the PEDT

Symbol	Parameter	Value
S	Power rating	100 kVA
V_{in}	Input voltage (L-L)	11 kV
V_o	Output voltage (LL)	0.415 kV
L	Input inductance	0.25 H
R	Input resistance	0.07 Ω
C_{dc1}, C_{dc2}	High DC link capacitance	20 μF
V_{Hdc}	High-voltage DC link	20 kV
C_{dc1}, C_{dc2}	Low DC link capacitor	30 mF
V_{Ldc}	Low-voltage DC link	0.8 kV
f_{sw}	Switching frequency	10 kHz
L_f	Output filter	4 mH, 30 kvar
R_f	Load	100 kW

The controller is improved by replacing the PI controller in Figure 2 by the API-FLC. The structure of the proposed adaptive controller for the input stage based on the API-FLC strategy is shown in Figure 7.

The isolation stage controller based on API-FLC is illustrated in Figure 8. The lower DC link voltage is compared to the reference voltage and the estimated error is passed to the API-FLC to generate the control signal to drive the half-bridge three-level converters.

In order to evaluate the performance of the developed PEDT and the API-FLC, a modeling and simulation work was conducted on the overall system. Several parameters were considered for the system simulation, which is summarized in Table 3. The parameters were selected based on the power rating and the system design values [25]. The modeling and simulation was implemented using MATLAB/Simulink when the system was subjected to disturbances on the primary and secondary sides. Different simulation cases were considered in this study, which include applying voltage sag, injecting voltage harmonics, sudden load change, and short-circuit faults.

IV. RESULTS AND DISCUSSION

The dynamic performance and power quality of the developed PEDT were evaluated by introducing disturbances at the primary and secondary of the transformer. The system performance investigation was based on voltage sag, harmonic distortion, rapid load changes, and short-circuit faults.

A. VOLTAGE SAG

The performance of the PEDT was investigated under supply voltage sag on the primary side of the transformer.
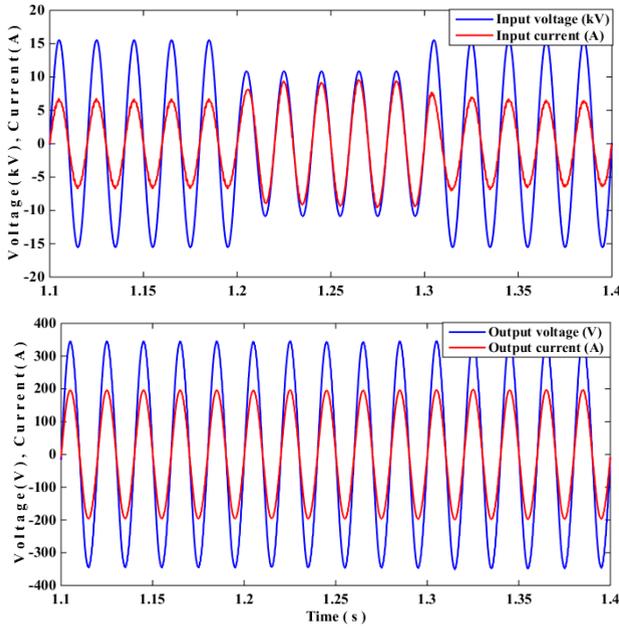
FIGURE 9. PEDT input-output voltage and current response with API-FLC.
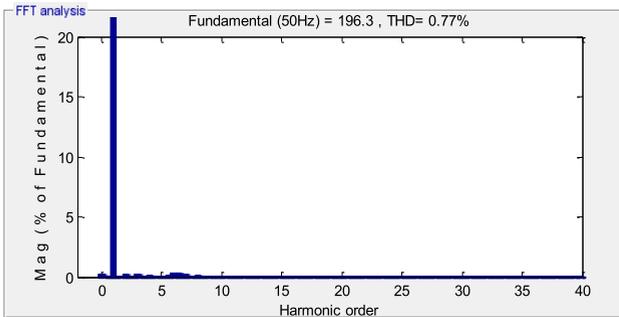
FIGURE 10. Output current THD with PI controller.
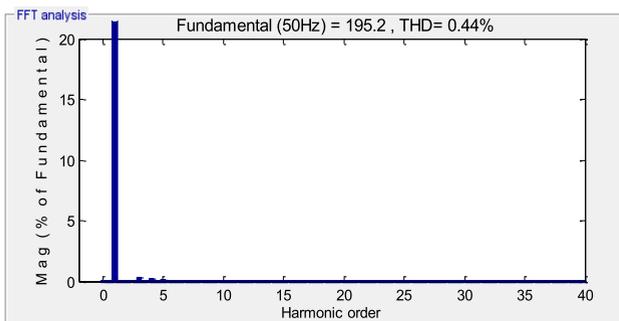
FIGURE 11. Output current THD with API-FLC.

FIGURE 12. PEDT high-voltage DC link.
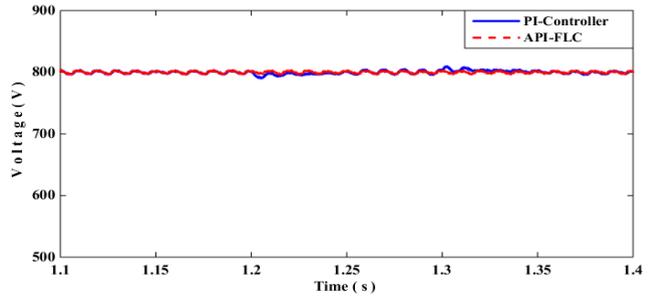
FIGURE 13. PEDT low-voltage DC link.
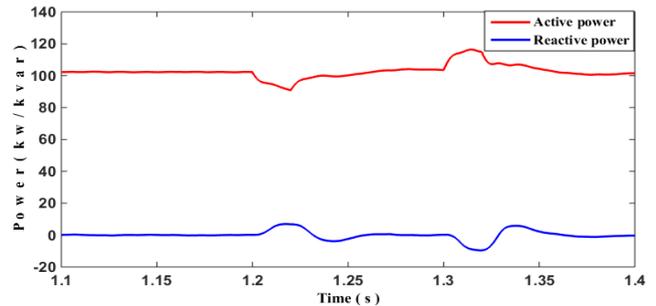
FIGURE 14. PEDT input active and reactive power.
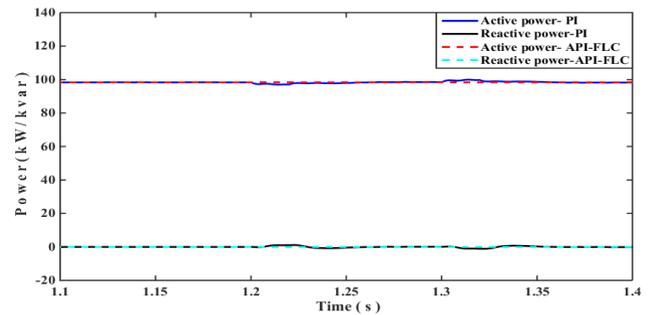
FIGURE 15. PEDT output active and reactive power.

Figures 9 to 15 show the comparison of performance parameters between the proposed API-FLC and the conventional PI controller. The PEDT input voltage and current are 11 kV and 5.25 A, respectively. A 30% voltage sag was introduced at the transformer input side from 1.2 to 1.3 s as shown in Figure 9. The output voltage and current waveforms show that the API-FLC adequately compensates the voltage sag by preventing it from propagating to the secondary side.

The THD for both the PI and the API-FLC controller are presented in Figures 10 and 11 respectively. The PI controller has an output current THD of 0.77%, while that of the API-FLC is 0.44%. The API-FLC has fewer harmonics, showing the controller's capability to improve power quality.

The dynamic responses of the PEDT high-voltage DC link with both the API-FLC and the PI controller are presented in Figure 12. The DC voltage varied between 18.67 and 21.51 kV, while the API-FLC showed slight variation between 19.72 and 20.39 kV. The API-FLC has a better response to the input voltage sag by limiting the output voltage deviation from the steady-state value of 20 kV as compared to the PI controller. Also, Figure 13 shows that the low DC link voltage based on the PI controller varies between 795 and 806.4 V whereas the proposed API-FLC remains constant at the reference voltage of 800 V. This is due to the ability of the proposed controller to adapt the PI parameters to enhance the system response.

The input-output active and reactive power responses during voltage sag occurring on the grid side of PEDT are presented in Figures 14 and 15. The input active and reactive powers changed slightly whilst the output power remained constant with the API-FLC. The PEDT response with the proposed API-FLC has better response in the output AC voltage at the transformer secondary and improved active and reactive powers as compared to the PI controller.

TABLE 4. Summary of API-FLC and PI Controller's Performances Under Voltage Sag

Parameter	API-FLC	PI controller
High DC link voltage peak overshoot	0.39 kV	1.51 kV
High DC link voltage peak undershoot	0.28 kV	1.33 kV
High DC link voltage setting time after the voltage sag	1.31 s	1.36 s
Low DC link voltage peak overshoot	0.0 V	6.4 V
Low DC link voltage peak undershoot	0.0 V	5 V
Output active power peak overshoot	0.12 kW	0.42kW
Output active power peak undershoot	0.12 kW	o.33 kW
THD input current	1.98%	2.42%
THD output current	0.44%	0.77%
Input/output power factor	1	1

A summary of the performance parameters of the API-FLC and the PI controller is presented in Table 4, showing that the API-FLC has a dynamic response with better total harmonic distortions.

B. VOLTAGE HARMONIC

The effectiveness of API-FLC against the voltage harmonic was investigated. Low fifth- and seventh-order harmonics with input voltage amplitudes of 10 and 15%, respectively, were applied on the input side of the PEDT between 1.2 and 1.3 s as shown in Figure 16. The output voltage during the harmonics remains sinusoidal and is not affected by the voltage harmonic of the primary side. The API-FLC effectively eliminates the effect of the input voltage harmonic on the PEDT secondary side.

Figure 17 shows that the input current THD when the fifth- and seventh-order harmonics are applied on the primary side is 13.89%. The transformer secondary output current in Figure 18 has 0.54% THD, which is very low as compared to the injected primary voltage harmonic. However, the output
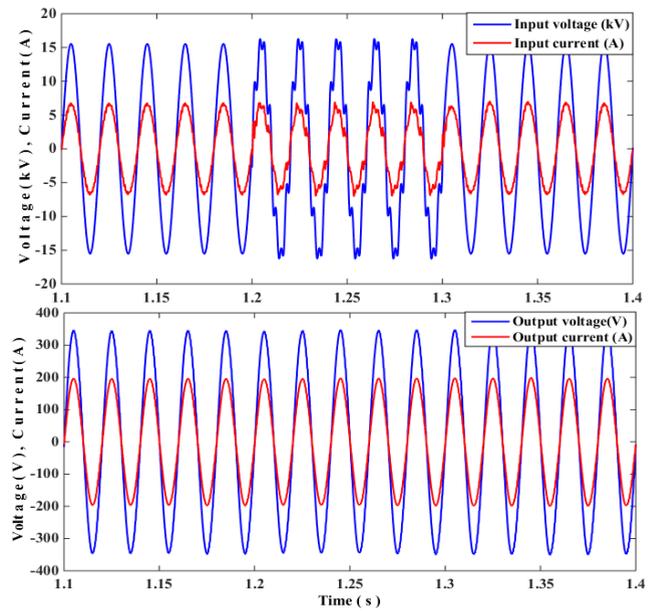
FIGURE 16. PEDT input-output voltage and current response under voltage harmonics.
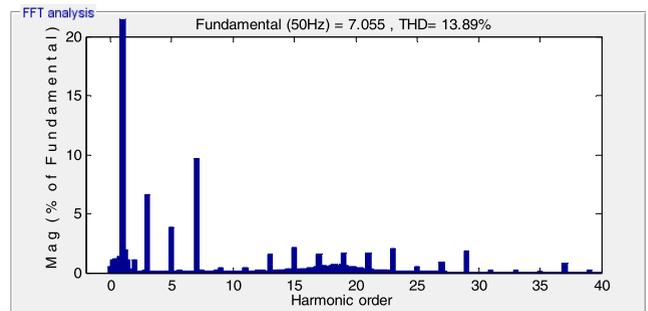
FIGURE 17. PEDT input current THD with API-FLC.
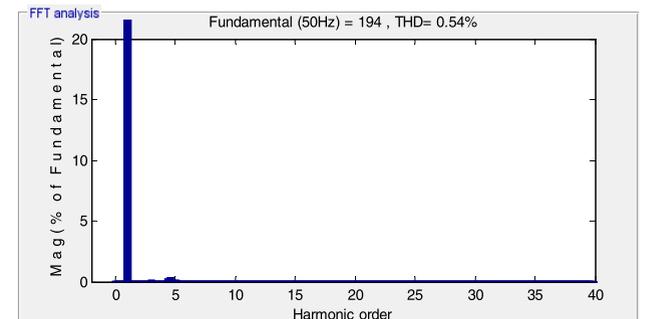
FIGURE 18. PEDT output current THD with API-FLC.

THD level is lower than the limit of 5% specified by the IEEE-519 standard. This proves that the proposed API-FLC successfully isolates the primary harmonics, preventing them from propagating to the secondary side.

The transient responses of high and low DC voltages are presented in Figures 19 and 20, respectively, when the voltage harmonic was applied between 1.2 and 1.3 s. The result
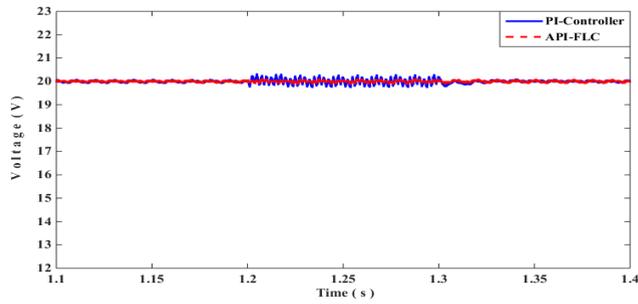
FIGURE 19. PEDT high-voltage DC link under-voltage harmonic.
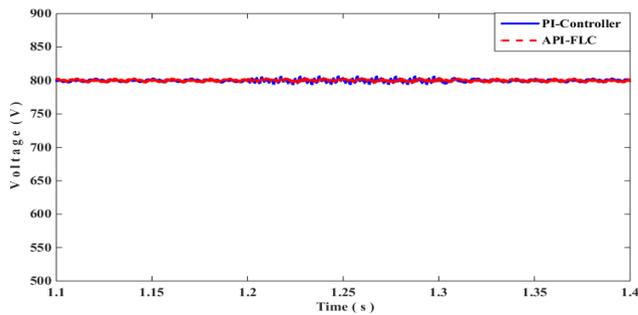
FIGURE 20. PEDT low-voltage DC link under-voltage harmonic.
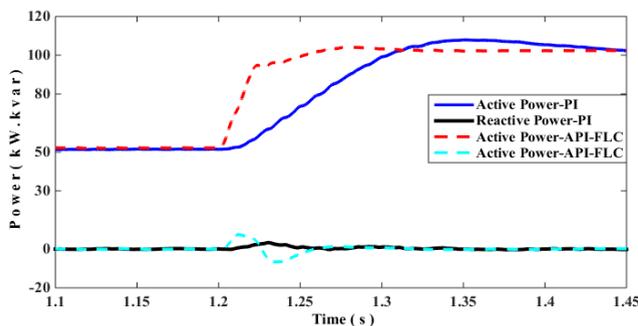
FIGURE 21. PEDT input active and reactive power for 50% load change.

FIGURE 22. PEDT output active and reactive power under 50% load change.
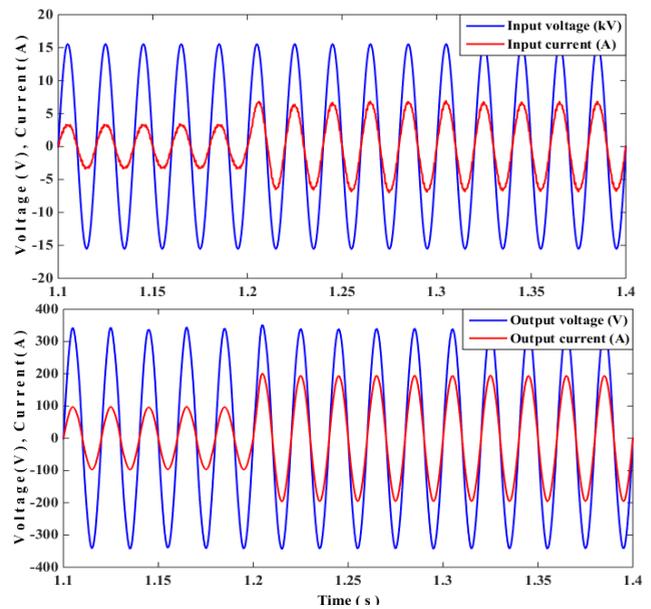
FIGURE 23. PEDT input-output voltage and current response to load change with API-FLC.

shows that there were oscillations at the input and output of the PEDT with the PI controller while that of the API-FLC is constant during the harmonic injection. This is due to the ability of the proposed API-FLC to adapt the PI gain parameters online to enhance the system response during the voltage harmonic.

C. LOAD CHANGE
The effect of a sudden load change from 50 to 100 kW on the secondary side of the PEDT after 1.2 s is presented in Figure 21. The input active and reactive powers of the PEDT with API-FLC and the PI controller are shown in Figure 22. As observed, the API-FLC has a better response with less overshoot and a fast settling time of 1.3 s compared to the PI controller's settling time of 1.45 s.

The load current changed from 68.6 to 137.2 A on the secondary side of the PEDT after 1.2 s when the load power

was increased from 50 to 100 kW as presented in Figure 23. The input voltage is sinusoidal and remains constant during the rapid load change and also in phase with the input current, while the input current is increased from 2.62 to 5.25 A on the grid side. This is logical because the controller should have increased the input current in proportion to the load demand. Also, at the transformer secondary side, the output voltage remained constant with the sudden load change. The API-FLC controller was able to regulate the input and output voltages without transient disturbance during the rapid load current change. This is due to the fast response of the API-FLC that adjust the modulation index to enhance the system response during the sudden load change.

A summary of the comparison of the performance parameters of API-FLC and the PI controller is presented in Table 5. The parameters show that the API-FLC has an improved dynamic response in terms of a fast rise time and short settling time.

TABLE 5. API-FLC and PI Controller's Performances Under Sudden Load Change

Parameter	API-FLC	PI controller
Input active power rise time after a sudden load change	1.25 s	1.3 s
Input active power settling time after a sudden load change	1.32 s	1.45 s
Input active power peak overshoot	4.1 kW	7.7 kW
THD input current	1.98%	2.42%
THD output current	0.44%	0.77%
Input/output power factor	1	1
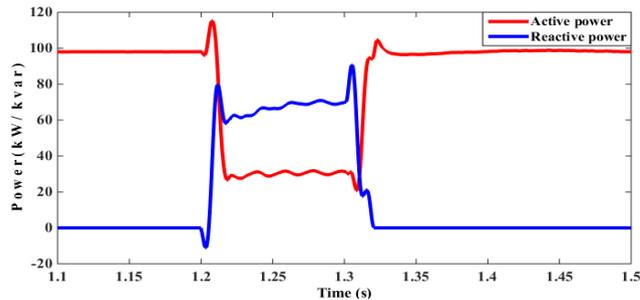
FIGURE 24. PEDT short-circuit output active and reactive power.

D. SHORT-CIRCUIT FAULT

The PEDT output active and reactive powers when there is a short-circuit fault on the secondary side of the transformer are presented in Figure 24. The short-circuit fault starts after 1.2 to 1.3 s. During the short-circuit fault, the active power decreases from 98 to 26 kW and the reactive power increases from zero to 72 kvar. The input active and reactive power responses to the short-circuit fault at the primary side are presented in Figure 25. The API-FLC has an undershoot of 54 kW, while the undershoot for the PI controller is 75.56 kW. The API-FLC was able to reduce the undershoot by 28.5% as compared to the PI controller.
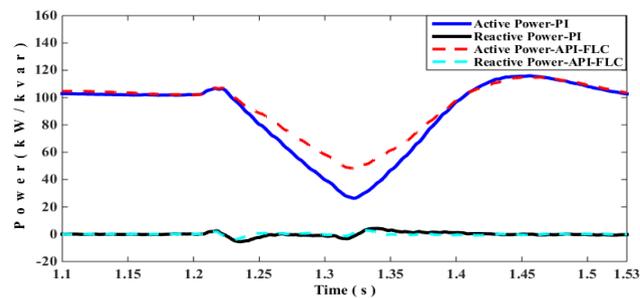
FIGURE 25. PEDT short-circuit input active and reactive power.

Figure 26 shows the high-voltage DC link during the short-circuit fault. The voltage was regulated around the steady-state value of 20 kV and the API-FLC has a better response with less oscillation and a fast settling time. Figure 27 shows the lower DC link voltage variation around 800 V during a short circuit; the voltage varies between 871 and 740.4 V with the PI controller and between 825 and 763.8 V with the
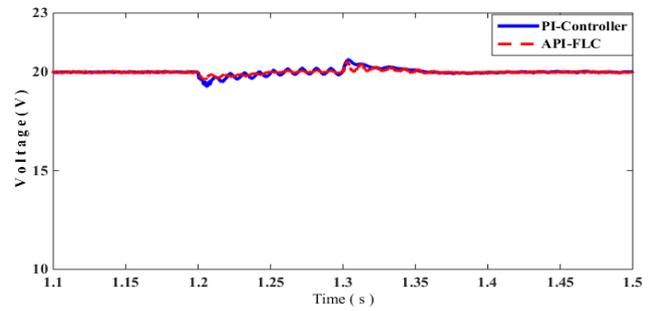
FIGURE 26. PEDT short-circuit high-voltage DC link.
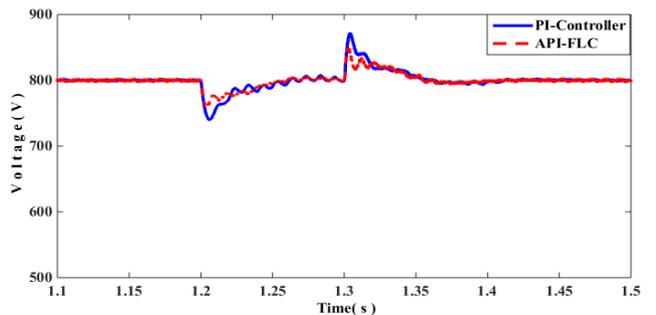
FIGURE 27. PEDT short-circuit low-voltage DC link..
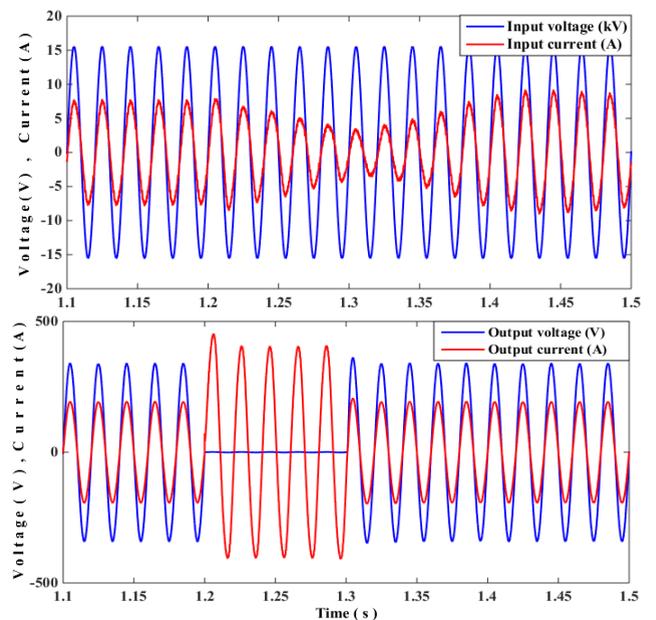
FIGURE 28. PEDT input-output short-circuit fault voltage and current responses.

API-FLC. The API-FLC has less overshoot as compared with the PI controller.

The input and output voltage and current during the short-circuit fault are shown in Figure 28. The input current is decreased due to the lower power transfer from the transformer primary to the secondary side. Meanwhile, the input voltage is constant, showing the effectiveness of the API-FLC

in controlling the PEDT. The output current is limited to twice its steady-state peak value of 194 A by the proposed API-FLC as compared to the higher values obtainable from most frequently used controller. This is in order to avoid damage to the converter semiconductor devices. The output voltage recovered to the steady-state value immediately after the short-circuit fault was cleared.

V. CONCLUSION

In this paper, a novel topology of a power electronic distribution transformer has been designed based on a three-level converter. An adaptive PI controller was proposed by adjusting the gain parameters of the PI controller online with fuzzy logic control when a disturbance occurs to enlarge the control operating range. The performance of a PI controller adapted with fuzzy logic control (API-FLC) under different dynamic operating conditions, including the voltage sags, rapid load changes, and short-circuit faults, has been investigated with the developed controller. The API-FLC controller gave a better dynamic response as compared to the PI controller. It was also observed that the THD of the proposed PEDT was maintained below the standard value given by IEEE-519 (5%) and unity power factor was achieved, which is a good advantage of the developed controller. The API-FLC was able to compensate the disturbance and eliminated the harmonic distortion. Therefore, the developed API-FLC has the advantage of providing a stable control system in both steady and dynamic conditions of the transformer.

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