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Organic Thin Film Transistors With Multi-Finger Contacts as Voltage Amplifiers

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ABSTRACT Low-voltage p-type organic transistors with two types of multi-finger source/drain contacts were fabricated on glass and polyethylene naphthalate. They exhibited threshold voltage between −0.3 and −0.5 V and field-effect mobility between 0.2 and 0.4 $cm^2/V{\cdot}s$. Their transconductance in saturation operation varied from ~25 to ~60 μS and scaled with the gate dielectric capacitance and transistor dimensions. All transistors operated beyond 1 kHz, while the transistors with the shortest channel length ($L = 20$ μm and $W = 4.03$ mm) exhibited a cutoff frequency of 13.4 kHz. The transistors were used to build simple voltage amplifiers by adding a resistor R_d on the drain side of the transistor. Higher R_d required higher supply voltage V_{dd} but resulted in the increased voltage gain. A voltage gain in excess of 8 V/V was obtained for V_{dd} of −12 V and R_d of 220 kΩ when transistor with medium value of transconductance of 37 μS was used. Consequently, the voltage gain of 10 V/V is achievable, making such transistor structures viable for sensor development.

INDEX TERMS Amplifiers, analog circuits, organic thin film transistors, sensors.

I. INTRODUCTION

The consumer uptake of wearable electronics [1] has been propelled by technology-savvy and health-aware consumers around the world. The calculator watch was the first wearable technology reported in the1980s [2]. Today, fitness bands and smart watches that monitor physical activity and record vital signs are becoming smaller and more esthetically pleasing while incorporating a whole spectrum of technologies [3]. Although they represent a commercially-successful first generation of wearable electronics, the future wearable electronics is envisioned to be highly flexible/conformal and even embedded in textiles [4]. Here, technologies that provide such mechanical attributes, in addition to desired electronic performance, are needed.

The low cost, ease of manufacturing, and ability to fabricate organic thin film transistors (OTFTs) on a variety of substrates [5], including textiles [6], make such technology suitable for wearable sensors. Some applications reported to date include highly flexible organic thin film transistors (OTFTs) used as mechanical strain sensors on PET substrate [7], pH detection devices [8], and multi-functional sensors for detecting temperature changes, light intensity, pressure and nitrogen flow [9]. Being an integral part of an analog sensor, the OTFT can provide two functions. It can act as a signal transducer by converting the physical stimulus to voltage [10] and a signal amplifier. The transconductance and geometry of the transistor play an important role for the latter.

The OTFT transconductance can be increased by several means. If the gate dielectric capacitance and the field-effect mobility are fixed, one way to increase the drain current is by increasing the ratio of the channel width to channel length (W/L), i.e. to increase W and/or reduce L [11]. To date the main focus was on the reduction in L and the demonstration of digital circuits with high operation frequency [12], [13]. When OTFTs with $L = 1$ μm and $W = 10$ μm were used, the transconductance of 12 μS was achieved and ring oscillators based on such transistors exhibited megahertz operation [12]. In such a case the W/L ratio of 10 was used to minimize the transistor parasitic capacitances and thus realize high switching speed. Wearable analog sensors however would not demand such speeds and OTFTs operating at ~1 kHz would satisfy many applications. Yet, the ability of the transistors to amplify signals remains essential.

If the demand on the transistor operation frequency is relaxed, increasing the channel width W becomes an option.

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One of the little explored pathways for increasing W is the use of multi-finger source/drain contacts [14]. Such transistors offer high W/L ratio and therefore high drain current while keeping the overall transistor area reasonably small. This paper significantly advances the state-of-the-art of such transistor structures by achieving low-voltage operation, hysteresis-free transistor characteristics, and, to our knowledge, the highest transconductance for OTFTs on plastic substrate reported to date. Simple voltage amplifier based on such transistors is also shown for the first time. Finally, the chosen transistor dimensions are compatible with the minimum line features achievable by printing [15], making the transistors with multi-finger source/drain contacts viable for large-scale printed electronics.

II. EXPERIMENTAL DETAILS

Low-voltage bottom-gate, top-contact p-type transistors based on dinaphtho[2,3-b:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT) were fabricated according to the procedure described in [16] either on glass (Ossila, U.K.) or PEN (Optfine PQA1, DuPont Teijin). The gate dielectric bi-layer consisted of aluminum oxide (AlO_x) prepared by UV/ozone oxidation [17] and an octadecyl phosphonic acid ($C_{18}PA$) (Strem Chemicals) monolayer prepared in vacuum [16]. The thickness of the gate dielectric was 11 nm for transistors on glass or 17 nm for transistors on PEN. Dinaphtho[2,3-b:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT) purified by sublimation was purchased from Sigma Aldrich, U.K. The thickness of DNTT was 20 nm. The thickness of the gold source/drain contacts was 50 nm.

The fabrication procedure was as follows. A 30-nm-thick aluminum layer was evaporated on the substrate at a rate of ∼ 2 Å/s. Part of each gate electrode was coated with a 40-nm-thick Au to prevent its oxidation. Next, AlO_x was prepared by exposing the aluminum to UV/ozone (UVOCS, USA) in ambient atmosphere. To prevent the contamination of the oxidizing surface, the UV/ozone cleaner was enclosed under a Hepa filter. Approximately 20 nm of $C_{18}PA$ was grown in Mini-SPECTROS (K. J. Lesker, U.K.) evaporation chamber enclosed in a N_2-filled glove box (Jacomex, France). The evaporation rate was about 3 Å/s and the substrate was kept at room temperature. Afterwards, the substrate temperature was raised to ∼ 160°C for 3 hours to remove all physisorbed molecules and to form a monolayer. Next, a 20-nm-thick DNTT layer was thermally evaporated at a rate of 0.5 Å/s at room temperature. Finally, a 50-nm-thick Au layer was evaporated at a rate of ∼ 3 Å/s to complete the transistors. Two different source-drain masks were used (Ossila, U.K.): (a) $L = 20$ μm and $W = 4.03$ mm and (b) $L = 50$ μm and $W = 18.23$ mm. In addition, four different gate widths were used to allow the additional control of W.

The measurements of the transistors and corresponding metal-insulator-metal (MIM) structures were performed with Agilent B1500A semiconductor device analyzer under dark ambient conditions. The instrument was also equipped with a capacitance module and an arbitrary waveform generator. The transfer and output characteristics of the OTFTs were measured in a sweep mode. The gate-to-source voltage V_{gs} (or drain-to-source voltage V_{ds}) was swept from 0 to −2V and back to 0 V. The threshold voltage and field-effect mobility were extracted from the transfer characteristics measured in saturation using MOSFET equations. Subthreshold slope, on-current, off-current and on/off current ratio were also extracted from the saturation curve.

III. EXPERIMENTAL RESULTS

Fig. 1(a) shows a cross-section of the transistor. The total thickness of the gate dielectric is ∼11 nm and ∼17 nm for the OTFTs on glass and PEN, respectively. Fig. 1(b) and 1(c) show the top views of the transistors with different multi-finger source-drain contacts. Both types of transistors were fabricated on the glass and PEN.

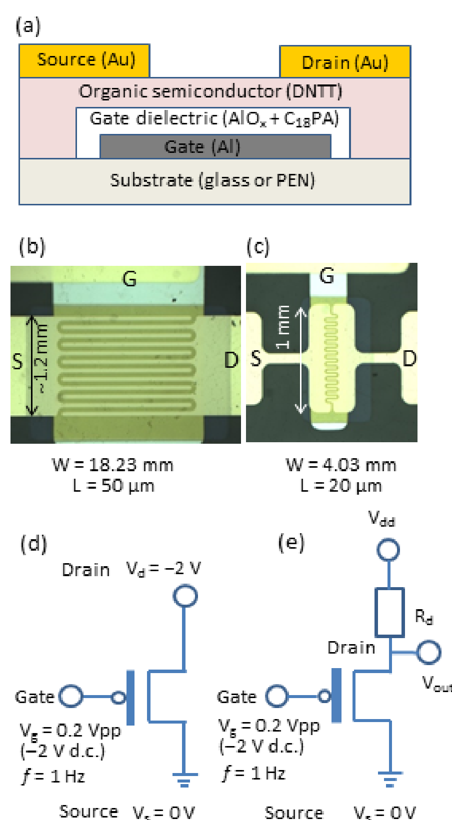

FIGURE 1. **Cross-section of an organic transistor (a); top-view of a wide-gate (b) and narrow-gate (c) transistor with multi-finger source/drain contacts; transconductance measurement setup (d) and voltage amplifier circuit (e).**

Fig. 2 shows transfer and output characteristics of a wide-gate (Fig. 1(b)) and narrow-gate (Fig. 1(c)) transistors on PEN. The threshold voltage V_{th} and the field-effect mobility μ in the saturation regime are listed in the figures together with the transconductance G_m, calculated by the derivation of the transfer characteristic at $V_{gs} = V_{ds} = -2$ V, and the gate dielectric capacitance. Whether fabricated on glass or PEN, both transistor structures provide the on-current

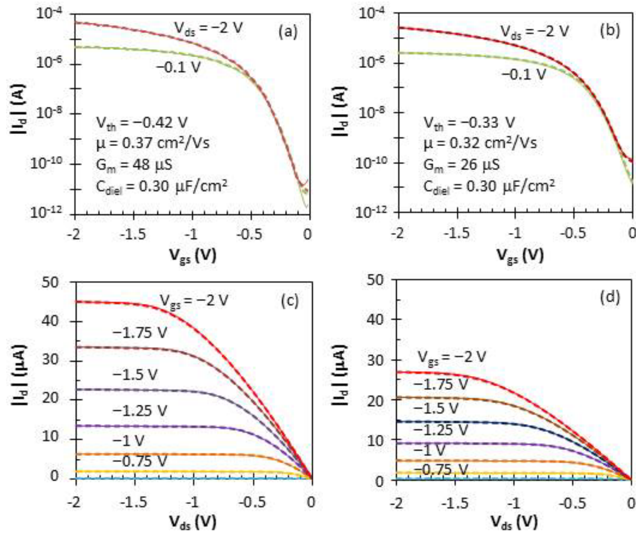

FIGURE 2. Transfer (a,b) and output (c,d) characteristics of a wide-gate (a,c) and narrow-gate (b,d) organic transistor on PEN. All curves were measured from 0 to −2 V (solid lines) and back (dashed lines).

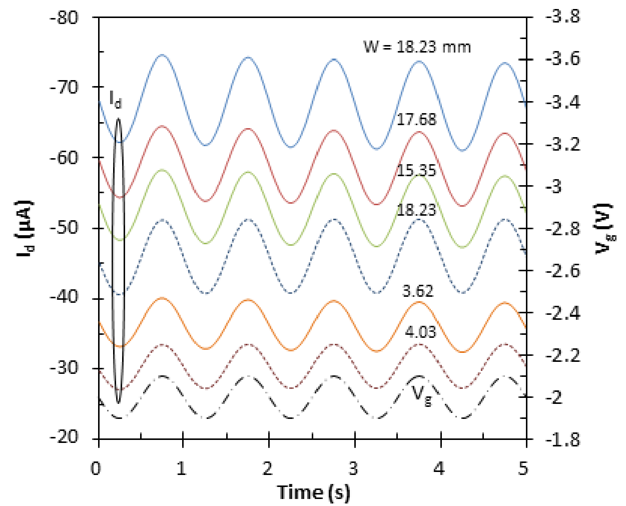

FIGURE 3. Drain current versus time for transistors with different gate widths, given in mm. W of 4.03 mm or less corresponds to narrow-gate transistors. Solid and dashed curves depict transistors fabricated on glass and PEN, respectively. The channel lengths L are listed in Fig. 1.

(measured at $V_{gs} = V_{ds} = -2$ V) in the 10^{-5} A range, off-current of $\sim 10^{-11}$–10^{-10} A, gate leakage current (measured at $V_{gs} = V_{ds} = -2$ V) less than 10^{-10} A, subthreshold slope of ~100 mV/decade, and transconductance G_m between ~25 and ~60 μS.

Previously the geometry of multi-finger source/drain contacts was studied in OTFTs based on 6,13-bis(triisopropylsilylethynyl) pentacene [14]. These transistors required high driving voltages of 40 V and the hysteresis in their transfer characteristics increased to ~15 V as the number of fingers increased from 1 to 4. The turn-on voltage of our transistors is close to zero, leading to very low threshold and operation voltages. In addition, the transfer and output characteristics are hysteresis-free in spite of a large number of fingers.

Next, the ac transconductance was measured by applying a sinusoidal voltage of 1 Hz (see Fig. 1(d)). The transconductance was calculated as follows:

$$g_m = \frac{i_d}{v_g} \tag{1}$$

where i_d is the measured peak-to-peak modulation in the drain current and v_g is the gate bias sinusoidal voltage of 0.2 V peak-to-peak (Vpp). The d.c. offset of the gate voltage and the drain voltage were held at −2 V, to allow the transistors to operate in the saturation regime.

Examples of a.c. transconductance measurements are shown in Fig. 3. The figure depicts the measured drain current for transistors with different gate widths against time. Transistors with wide and narrow gates both on the glass and PEN are shown. For transistors fabricated on glass the transconductance g_m calculated according to (1) increased from ~31 to ~62 μS as the W/L increased. For transistors fabricated on PEN the transconductance increased from ~26 to ~53 μS as the W/L increased. These values are similar to those obtained by differentiating the transfer characteristic for $V_{ds} = V_{gs} = -2$ V. They also surpass the highest reported values to date [12] by a factor of 2 to 5.

The transconductance of the transistor in the saturation regime can be expressed as:

$$g_m = \frac{W}{L}\mu C_{diel}\left(V_{gs} - V_{th}\right) \tag{2}$$

where W is the channel width, L is the channel length, μ is the field-effect mobility, C_{diel} is the gate dielectric capacitance, V_{gs} is the gate-to-source voltage, and V_{th} is the threshold voltage. In the saturation regime, the transconductance depends on the gate voltage V_{gs} and is independent of the drain voltage V_{ds}.

As seen in Fig. 3, the measured I_d and its modulation is higher for wide-gate transistors (Fig. 1(b)) compared to narrow-gate ones (Fig. 1(c)) because the wide-gate transistors possess larger W/L ratio. In addition, as the W/L of the wide-gate transistors increases, so does the transconductance. This behavior is in agreement with (2). The transistors fabricated on PEN exhibited slightly lower transconductance when compared to those on glass. While the OTFTs on PEN exhibited slightly higher field-effect mobility, their lower gate dielectric capacitance (0.30 μF/cm^2 compared to 0.42 μF/cm^2 for OTFTs on glass) led to reduced μC_{diel} product.

To investigate the maximum operation frequency (cut-off) of both transistor structures the transconductance was measured as a function of ac frequency. Fig. 4 shows the transconductance of wide- and narrow-gate transistors. The transconductance of the narrow-gate transistor is ~ 32 μS up to ~ 10 kHz and its cut-off frequency is 13.4 kHz. However, the wide-gate transistor shows a slightly different behavior. The transconductance at low frequencies is ~ 60 μS and remains approximately constant up to ~ 2 kHz. For higher frequencies g_m initially increases and then decreases,

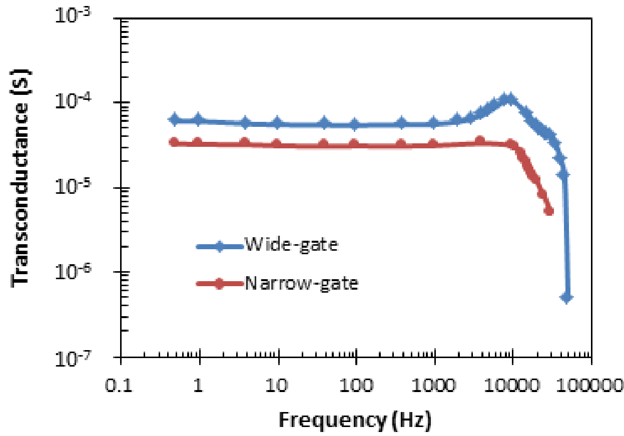

FIGURE 4. Transistor transconductance as a function of ac frequency.

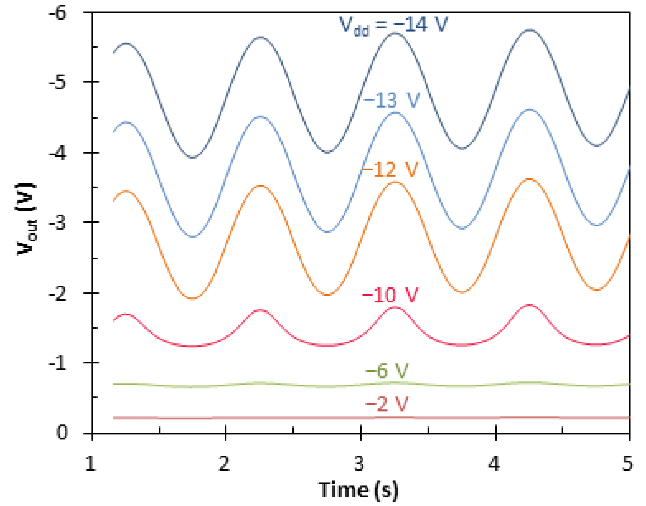

FIGURE 5. V_{out} of the transistor amplifier of Fig. 1(e) for $R_d = 220$ kΩ and different V_{dd}. V_{in} was identical to V_g of Fig. 3.

reaching the maximum value of ∼ 105 µS around 9 kHz. Although this anomaly requires further investigation, both types of transistors are suitable for working with frequencies up to 1 kHz.

Finally, a simple voltage amplifier was built according to Fig. 1(e). Again, sinusoidal voltage of 1 Hz was applied to the transistor gate and the modulated output voltage was measured below resistor R_d. Three different resistor values were used; 5.6 kΩ, 47 kΩ and 220 kΩ. For each transistor and resistor combination, a range of supply voltages V_{dd} was used and the drain current I_d and the output voltage V_{out} were measured. The ac voltage gain was calculated as follows:

$$g_v = \frac{v_{out}}{v_g} \tag{3}$$

where v_{out} is the measured peak-to-peak modulation in the output voltage and v_g is the gate bias modulation of 0.2 Vpp. An example of the measured output voltage is shown in Fig. 5 for $R_d = 220$ kΩ and different V_{dd} voltages. Peak-to-peak v_{out} increases with increasing V_{dd} until V_{dd} reaches ∼ −12 V. Further increase in $|V_{dd}|$ does not affect the output voltage v_{out}.

The transistor operation point V_{ds} and ac voltage gain g_v, calculated using (3), are plotted against V_{dd} in Fig. 6, for three different R_d values. The ac voltage gain increases with increasing R_d, reaching ∼ 8.4 V/V for R_d = 220 kΩ. The gain saturates when the transistor reaches saturation operation. The data of Fig. 6 suggests that regardless of the value of R_d, V_{ds} operation point of at least −2.5 V is needed to reach the maximum voltage gain when V_g oscillates around −2 V. One can also infer that the resistance between source and drain is ∼100 kΩ, a factor of ∼10 smaller when compared to DNTT transistors with standard source/drain contacts with L = 30 µm and W = 1 mm [10]. This decrease is important for the reduction in both V_{dd} and R_d.

IV. DISCUSSION

Based on the circuit of Fig. 1(e) V_{out} can be expressed as:

$$V_{out} = V_{dd} - R_d \cdot I_d \tag{4}$$

where the drain current I_d is a function of V_{gs} and V_{ds}. If the ac modulation of the gate voltage is turned off, V_{out} becomes the operation point V_{ds} of the transistor. Equation (4) was used to calculate V_{ds} from the known values of V_{dd}, R_d and the measured I_d. The calculated values are shown as ×-symbols in Fig. 6. The agreement between the measured and calculated values confirms the validity of (4). In analogy to [18] the differentiation of (4) leads to:

$$dV_{out} = -R_d \cdot dI_d, \tag{5}$$

where

$$\begin{aligned} \mathrm{dI_d} &= \left.\frac{\partial \mathrm{I_d}}{\partial \mathrm{V_{gs}}}\right|_{\mathrm{V_{ds}}} \mathrm{dV_{gs}} + \left.\frac{\partial \mathrm{I_d}}{\partial \mathrm{V_{ds}}}\right|_{\mathrm{V_{gs}}} \mathrm{dV_{ds}} \\ &= g_m dV_{gs} + g_d dV_{ds} \\ &= g_m dV_{gs} + g_d dV_{out} \end{aligned} \tag{6}$$

where g_m is the transconductance and g_d the drain conductance of the transistor. The minus sign in (5) means that the phase of the sinusoidal drain current and the output voltage are shifted by 180°. Since the drain current follows the changes in the gate voltage (see Fig. 3), i.e. they are in phase, a phase shift of 180° between the output and gate voltages exists (see Fig. 5).

Combining (5) and (6) leads to the voltage gain:

$$g_v = -\frac{g_m}{g_d + \frac{1}{R_d}}, \tag{7}$$

When the transistor operates in the saturation regime, the drain conductance becomes zero, namely $g_d = 0$. Consequently, the voltage gain can be expressed as:

$$|g_v| = g_m R_d \tag{8}$$

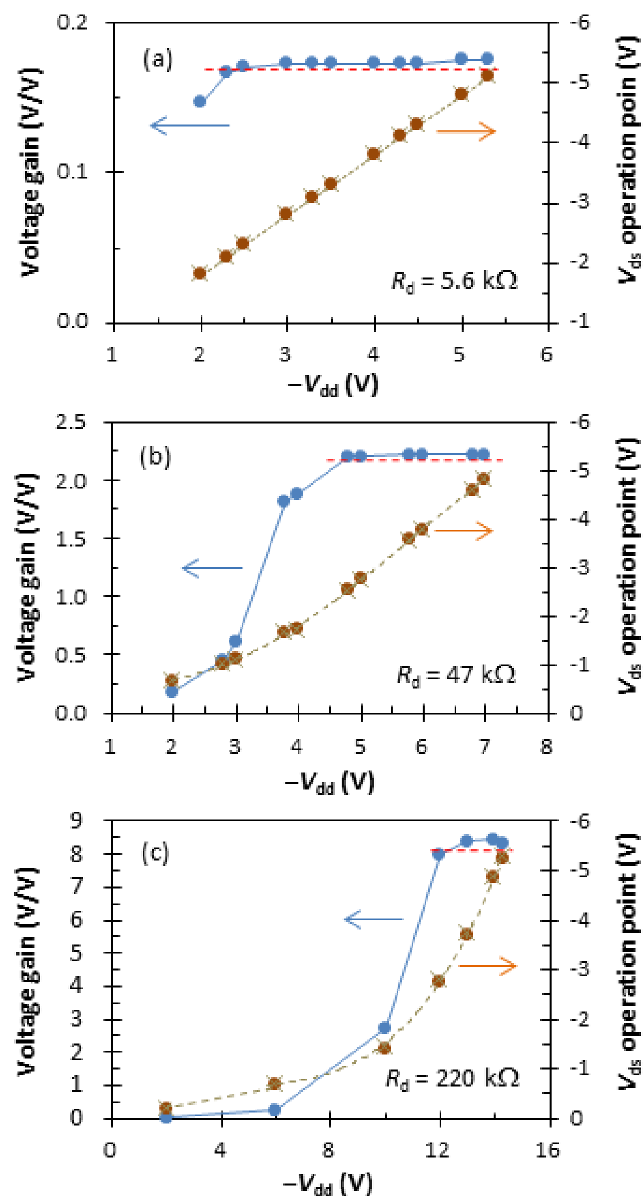

FIGURE 6. Voltage gain of the transistor amplifier of Fig. 1(e) for three values of R_d. V_g was identical to that of Fig. 3. The voltage gain was calculated using (3). The solid dots show the measured data. The ×-symbols correspond to calculations using (4). The red dashed lines correspond to calculations using (8).

The voltage gain becomes constant and proportional to the transconductance of the transistor and the resistor R_d. The saturation of the voltage gain is observed in Fig. 6 for all values of R_d. In addition, based on (8) the voltage gain of the transistor shown in Fig. 6(a) should be 30 μS × 5.6 kΩ = 0.168, whereas the measured value is 0.173 V/V. The calculated voltage gain of the transistor of Fig. 6(b) is 46 μS × 47 kΩ = 2.16 whereas the measured value is 2.20 V/V. Finally, the calculated voltage gain of the transistor shown in Fig. 6(c) is 37 μS × 220 kΩ = 8.14, whereas the measured value is ∼ 8.40 V/V. The achieved agreement confirms the validity of the above model for the voltage amplifier of Fig. 1(e) based on the organic transistor. This behavior resembles the one observed for similar voltage amplifiers based on organic electrochemical transistors (OECT) [18], even though OTFT and OECT operate very differently. While OECT is a 'normally-on' transistor that requires diffusion of ions into the transistor active area to curtail the drain current, OTFT is a 'normally-off' transistor where the field-effect controls the drain current.

To summarize, low-voltage, p-type DNTT transistors with two multi-finger source/drain contacts were studied. Owing to high W/L ratio their a.c. transconductance varies from ∼25 to ∼60 μS. The transistor characteristics are hysteresis-free and both transistor types operate beyond 1 kHz. In addition, simple voltage amplifiers were demonstrated by adding a resistor R_d on the drain side of the transistor. For practical applications one would prefer high voltage gain of the transistor while keeping the supply voltage V_{dd} as low as possible. Figs. 5 and 6 show that V_{dd} must be high enough to allow the transistor to operate in saturation. In such a case the output voltage is sinusoidal. To achieve the voltage gain higher than one, a suitable resistor R_d must be selected. As the R_d increases, the voltage gain in saturation increases, but so does the required V_{dd}. When $R_d = 47$ kΩ, a −5 V supply voltage provides voltage gain of 2.2 V/V. Increase of R_d to 220 kΩ leads to a gain of ∼8.4 V/V but V_{dd} of at least −12 V is required. This is because a larger voltage drop occurs across the resistor R_d. Ultimately there is a trade-off between the gain and the supply voltage.

REFERENCES

[1] S. J. Strath and T. W. Rowley, "Wearables for promoting physical activity," *Clin. Chem.*, vol. 64, no. 1, pp. 53–63, Jan. 2018.

[2] M. Dehghani and R. M. Dangelico, "Smart wearable technologies: Current status and market orientation through a patent analysis," in *Proc. IEEE Int. Conf. Ind. Technol. (ICIT)*, Piscataway, NJ, USA, Mar. 2017, pp. 1570–1575.

[3] R. Wright and L. Keith, "Wearable technology: If the tech fits, wear it," *J. Electron. Resour. Med. Libraries*, vol. 11, no. 4, pp. 204–216, 2014.

[4] F. Carpi and D. De Rossi, "Electroactive polymer-based devices for e-textiles in biomedicine," *IEEE Trans. Inf. Technol. Biomed.*, vol. 9, no. 3, pp. 295–318, Sep. 2005.

[5] A. Tewari *et al.*, "High-mobility and low-operating voltage organic thin film transistor with epoxy based siloxane binder as the gate dielectric," *Appl. Phys. Lett.*, vol. 107, no. 10, p. 103302, Sep. 2015.

[6] Y. Kim *et al.*, "Flexible textile-based organic transistors using graphene/Ag nanoparticle electrode," *Nanomaterials*, vol. 6, no. 8, p. 147, Aug. 2016.

[7] P. Cosseddu, S. Lai, and A. Bonfiglio, "Highly flexible and low voltage organic thin film transistors for wearable electronics and e-skin applications," in *Proc. IEEE-NANO*, Piscataway, NJ, USA, Jul. 2015, pp. 1317–1319.

[8] I. Manunza, A. Sulis, and A. Bonfiglio, "Organic semiconductor field effect transistors for unconventional applications: Flexible sensors and wearable devices," in *Proc. Int. Workshop Wearable Implantable Body Sensor Netw. (BSN)*, Piscataway, NJ, USA, Apr. 2006, pp. 208–211.

[9] M. Song, J. Seo, H. Kim, and Y. Kim, "Ultrasensitive multi-functional flexible sensors based on organic field-effect transistors with polymer-dispersed liquid crystal sensing layers," *Sci. Rep.*, vol. 7, no. 1, 2017, Art. no. 2630.

[10] S. Hannah, A. Davidson, I. Glesk, D. Uttamchandani, R. Dahiya, and H. Gleskova, "Multifunctional sensor based on organic field-effect transistor and ferroelectric poly(vinylidene fluoride trifluoroethylene)," *Organic Electron.*, vol. 56, pp. 170–177, May 2018.

[11] S. Kang *et al.*, "Geometric effect of channel on device performance in pentacene thin-film transistor," *Jpn. J. Appl. Phys.*, vol. 43, no. 11A, pp. 7718–7721, Nov. 2004.
[12] U. Zschieschang *et al.*, "Megahertz operation of flexible low-voltage organic thin-film transistors," *Organic Electron.*, vol. 14, no. 6, pp. 1516–1520, Jun. 2013.
[13] H. Klauk, U. Zschieschang, and M. Halik, "Low-voltage organic thin-film transistors with large transconductance," *J. Appl. Phys.*, vol. 102, no. 7, p. 074514, Oct. 2007.
[14] J.-H. Kwon *et al.*, "Hysteresis effects by source/drain interdigitated-finger geometry in 6,13-bis(triisopropylsilylethynyl)pentacene thin-film transistors," *Electrochem. Solid-State Lett.*, vol. 12, no. 8, pp. H285–H287, 2009.
[15] H. Kim, R. C. Y. Auyeung, S. H. Lee, A. L. Huston, and A. Piqué, "Laser-printed interdigitated Ag electrodes for organic thin film transistors," *J. Phys. D, Appl. Phys.*, vol. 43, no. 8, p. 085101, Mar. 2010.
[16] S. Hannah *et al.*, "Interplay between vacuum-grown monolayers of alkylphosphonic acids and the performance of organic transistors based on dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene," *ACS Appl. Mater. Interfaces*, vol. 8, no. 38, pp. 25405–25414, 2016.
[17] S. Gupta *et al.*, "Ozone oxidation methods for aluminum oxide formation: Application to low-voltage organic transistors," *Organic Electron.*, vol. 21, pp. 132–137, Jun. 2015.
[18] M. Braendlein, T. Lonjaret, P. Leleux, J.-M. Badier, and G. G. Malliaras, "Voltage amplifier based on organic electrochemical transistor," *Adv. Sci.*, vol. 4, no. 1, p. 1600247, 2017.

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