

Received May 29, 2018, accepted June 27, 2018, date of publication August 1, 2018, date of current version September 5, 2018. Digital Object Identifier 10.1109/ACCESS.2018.2861886

Through-Glass Vias for Glass Interposers and MEMS Packaging Applications Fabricated Using Magnetic Assembly of Microscale Metal Wires

MIKU J. LAAKSO^(D), SIMON J. BLEIKER¹, JESSICA LILJEHOLM^{1,2}, GUSTAF E. MÅRTENSSON³, (Member, IEEE), MIKHAIL ASIATICI^(D),⁴, ANDREAS C. FISCHER^{1,2}, GÖRAN STEMME¹, (Fellow, IEEE), THORBJÖRN EBEFORS^{2,5}, (Senior Member, IEEE), AND FRANK NIKLAUS¹, (Senior Member, IEEE)

¹Department of Micro and Nanosystems, KTH Royal Institute of Technology, 114 28 Stockholm, Sweden

⁴School of Computer and Communication Sciences, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland

Corresponding author: Miku J. Laakso (mikul@kth.se)

This work was supported in part by the Knut and Alice Wallenberg Foundation as a part of the Working on Venus project, in part by the ENIAC Joint Undertaking and Vinnova (ENIAC JU) under Grant 324189, in part by the European Research Council through the ERC Starting Grant M&Ms 277879, and in part by the Swedish Foundation for Strategic Research under Grants GMT14-0071 and RIF14-0017.

ABSTRACT A through-glass via (TGV) provides a vertical electrical connection through a glass substrate. TGVs are used in advanced packaging solutions, such as glass interposers and wafer-level packaging of microelectromechanical systems (MEMS). However, TGVs are challenging to realize because via holes in glass typically do not have a sufficiently high-quality sidewall profile for super-conformal electroplating of metal into the via holes. To overcome this problem, we demonstrate here that the via holes can instead be filled by magnetically assembling metal wires into them. This method was used to produce TGVs with a typical resistance of 64 m Ω , which is comparable with other metal TGV types reported in the literature. In contrast to many TGV designs with a hollow center, the proposed TGVs can be more area efficient by allowing solder bump placement directly on top of the TGVs, which was demonstrated here using solderpaste jetting. The magnetic assembly process can be parallelized using an assembly robot, which was found to provide an opportunity for increased wafer-scale assembly speed. The aforementioned qualities of the magnetically assembled TGVs allow the realization of glass interposers and MEMS packages in different thicknesses without the drawbacks associated with the current TGV fabrication methods.

INDEX TERMS Chip scale packaging, femtosecond laser, glass interposer, laser ablation, multichip modules, robotic assembly, self-assembly, spin-on glass, thermal expansion, through-glass via, through-silicon vias, TSV.

I. INTRODUCTION

Mobile and wearable electronics and the Internet of Things (IoT) require integration of multiple functionalities in small packages with vertical interconnections [1], [2]. Such packages can be realized using approaches that include wafer-level packaging of microelectromechanical systems (MEMS) [3], replacement of surface mounted components by integrated passive devices in radio frequency (RF) systems [4]–[6], and interposers providing interconnections between system components in 2.5D and 3D integration [7] or in organic fanout wafer level packages [8]–[10]. A key element in all of

these approaches is the need for through-substrate vias that provide vertical electrical connections through the substrate. In the past, most of the through-substrate-via research has focused on through-silicon vias (TSVs) in silicon substrates. However, for packaging applications, glass substrates with through-glass vias (TGVs) have several benefits in comparison to silicon substrates with TSVs. Because glass is a good electrical insulator, it provides low substrate losses for RF applications, reduces electrical coupling between TGVs in comparison to TSVs, and removes the need for a separate electrical insulation layer on the sidewalls of via holes.

²Silex Microsystems AB, 175 43 Järfälla, Sweden

³Mycronic AB, 183 53 Täby, Sweden

⁵MyVox AB, 129 38 Hägersten, Sweden

Glass substrates are available in large low-cost panel formats and have extremely smooth surfaces without the need to employ costly polishing processes [11], [12]. As a lid wafer in MEMS devices, glass allows visual inspection of the sealed devices [13]. Transparency is also sometimes required for optical MEMS applications. The coefficient of thermal expansion (CTE) of glass can be adjusted; this allows mitigation of thermal stress for interposer applications because the CTE of glass can be selected in an optimal way between the low CTE of a silicon chip and the high CTE of an organic printed circuit board (PCB) [14]. Even though glass performs well as packaging material, its use is limited due to challenges associated with the available TGV fabrication methods, as discussed below.

The most common method of filling TSVs with metal is super-conformal electroplating, but it cannot be easily applied to many TGVs with comparably rough via-hole sidewalls. Super-conformal electroplating uses an advanced chemistry that causes the plating speed to change according to a local geometry in a via hole [15]. This is to prevent voids and metal overburden. Very well-defined via holes in silicon are formed with deep reactive ion etching (DRIE) using the so-called Bosch process, but similar holes in glass, suitable for superconformal plating, are challenging to produce. Specifically, it is difficult to excel simultaneously at fabrication speed, sidewall surface quality, aspect ratio, and sidewall tilt control when creating via holes in glass [16].

The strict requirement of well-defined via holes imposed by super-conformal plating can be avoided by other hole filling methods [17], each having their specific advantages and disadvantages. In bottom-up plating the electroplating is started from the bottom of the via hole instead of from the sidewalls. However, this process is slow, suffers from poor adhesion to via sidewalls, and is difficult to use in blind via holes [13], [15]. Blind via holes do not reach through the original substrate thickness, thus allowing the use of a thick and stable substrate during processing. As an alternative, plating only a thin metal liner on the via-hole sidewalls works also in blind vias and speeds up and simplifies the plating process [18]. These hollow vias also allow space for the higher rate of thermal expansion of the via metal in comparison to the substrate [15]. As a drawback, the hollow vias complicate subsequent photolithography on the substrates and prevent solder bump placement on top of the vias [19]. The solder bumps provide vertical connections between substrates in packaging applications and their placement next to the TGVs instead of on top of them requires more surface area and reduces integration density. Because polysilicon has a low CTE close to that of many glass materials, chemical-vapordeposited and doped polysilicon can replace metals as a TGV conductor in order to alleviate thermal stresses. However, the resistance of a doped polysilicon TGV can be as high as hundreds of ohms, thus limiting compatibility with high currents and low-loss requirements [13].

Instead of manufacturing holes into glass, it is possible to reflow glass around conductive via material. A structured silicon wafer can be used as a mold for glass reflow, and the silicon forming the mold can act as the conductive part of a TGV, resulting in resistances reported to be in the range of 180–260 Ω [20]. When lower resistances are needed, silicon can be etched away and replaced with metal [21], or glass can be flown directly around prefabricated and prepositioned metal rods [13], [22]. A commercial product of the latter type has the minimum via pitch of 150 µm [13] and a via positioning accuracy of $\pm 50 \,\mu\text{m}$ [22], both inferior to what can be achieved using DRIE of silicon. In addition, this approach allows only wafers that are thicker than 350 µm [13], which precludes applications such as mobile electronics that often require thin packages. In general, glass reflow processes require additives to be mixed to glass in order to decrease its glass-transition temperature and to adjust its CTE to be close enough to that of the mold material. This can negatively affect the optical and RF properties of the glass substrate [21], and the resulting CTE may not be optimal for the final packaging application. Taken together, the issues with all the available TGV fabrication methods leave a clear need for a fast method to completely fill via holes with metal while simultaneously minimizing thermal stresses at the TGVs in the resulting glass substrates.

To this end, we demonstrate the use of magnetic-fieldassisted self-assembly (magnetic assembly) [23]-[25] for the fabrication of metal TGVs in a glass substrate suitable for glass interposers and MEMS packaging [1]. In magnetic assembly, a magnetic field is used to pull ferromagnetic metal rods into the via holes in a substrate. The metal rods are cut from a commercially available wire, and they are fixed in the via holes for example by using polymer. Earlier work on magnetic assembly [23]-[25] has only dealt with vias in silicon substrates; this work, in contrast, demonstrates magnetically assembled vias in glass substrates. Challenges of magnetic assembly in glass, caused by the need for short via holes, are solved by using a new magnetic assembly procedure that utilizes multiple magnets placed next to each other for the assembly of a single substrate. We also show, utilizing an assembly robot, that parallelized magnetic assembly has the potential to increase the speed of assembly on wafer scale [2]. Resistance measurements indicate that magnetically assembled nickel TGVs have a low resistance, comparable to other metal TGVs reported in the literature. Jetting of solder paste is used to demonstrate the possibility of depositing solder directly on top of the magnetically assembled TGVs. In order to reduce the stress caused by metal cores in magnetically assembled TGVs in various types of glass substrates, we analyze and compare the CTEs of different metals to those of glass substrate materials. Result from this analysis indicate that combining Kovar metal alloy with borosilicate or silicon-matched glass provides a low mismatch strain at temperatures below ~450 °C, and combining Invar metal alloy with fused silica provides a low mismatch strain at temperatures below ~125 °C. Both of these metal alloys provide a lower mismatch strain than gold and copper do.

II. METHODS

A. FABRICATION OF TGVS AND SOLDER BUMPS

Magnetic assembly of TGVs was demonstrated using a 150 mm diameter glass wafer (alkali-free alkaline earth boroaluminosilicate glass, Eagle XG, Corning). This 300 µm thick wafer contained prefabricated blind holes that were 120 µm deep, 70 µm wide at the opening, and had pitches of 350 µm and 220 µm. The nickel rods to be assembled into the via holes were prepared by cutting them from commercially available nickel wire (California Fine Wire Company) that had the diameter of 44 µm. The cutting process, which reflected the one described by Fischer et al. [23], consisted of embedding the nickel wire in a photoresist on a carrier wafer and using a dicing saw to cut the wire into rods with a nominal length of 167 µm. The dicing saw created burr defects at the ends of the wires which can cause problems for the magnetic assembly. Similarly to what was reported by Asiatici et al. [25], we removed these burrs with a short wet etch (5 minutes at 50 °C in 16:1:1:2 H₃PO₄:C₂H₄O₂:HNO₃:H₂O) before releasing the rods by dissolving the photoresist matrix on the carrier wafer.

As in the earlier work [23]–[25] on magnetic assembly for TSVs, TGV assembly was initially tested using a single magnet. However, these tests revealed that even though a high ratio of filled holes was achieved, the nickel rods disassembled from the holes when the magnet was no longer underneath the hole array. This is in contrast to previous observations with via holes in silicon where spontaneous disassembly of the metal rods rarely occurred. We explain this difference by comparing the via-hole shapes in silicon and glass. Whereas silicon holes fabricated with DRIE have vertical sidewalls and a high aspect ratio, the holes in our glass wafer have a slightly conical shape with a rounded bottom and a low aspect ratio (see Fig. 2g). The geometry of the via holes in glass allowed the rods to disassemble as a result of even minute external excitations caused by, for example, the horizontal component of a magnetic field, vibrations, or airflow. A solution to this problem is to keep the magnetic field in place until the metal rods are permanently fixed into the via holes. We achieved this condition by using multiple magnets for the assembly; this removes the need to move the magnet from underneath an area to the next one after a successful assembly, in contrast to what was done in the earlier magnetic assembly works. In order to magnetically assemble the nickel rods into the via holes, a 1 mm thick magnetic sheet (Supermagnete, Germany) made of strontiumferrite particles mixed into flexible plastic was temporarily attached underneath the glass wafer using a weak adhesive on the magnetic sheet, and twelve neodymium (Nd-Fe-B) magnets were placed underneath this sheet (see Fig. 1a). The function of the sheet was to keep the neodymium magnets in close contact with the backside of the wafer while still allowing them to be moved laterally. The strontium-ferrite sheet had a lower magnetic coercivity and flux than the neodymium magnets meaning that the magnetic field and the assembly



FIGURE 1. a) Photograph of a glass wafer with a magnetic sheet and twelve permanent magnets underneath. Between the magnets and the wafer is a flux-detector foil that visualizes the shape of the magnetic field. The foil contains nickel particles that show black in green gelatinous suspension. b) A close up of a single magnet with nickel rods on top and via holes ready to be assembled.

process were dominated by the neodymium magnets. Nickel rods deployed on the glass wafer were erected by the strong magnetic field of the neodymium magnets. Magnetic assembly was done by manually moving one neodymium magnet at the time while the magnetic field gradient at the edges of the neodymium magnets forced the rods to follow the lateral movement of the magnets (see Fig. 1b).

The continued TGV fabrication process, following the magnetic assembly, is illustrated in Fig. 2. The process started by drop casting spin-on glass (400F, Filmtronics) on the wafer surface in order to bind the metal rods into the via holes (see Fig. 2a). Spin-on glass (SOG), in this case methylsilsesquioxane, has good gap filling properties and is often used to create passivation layers on silicon wafers. Air bubbles trapped in the via holes were removed by degassing in vacuum, with pressures reaching down to 0.01 bar. Degassing, followed by prebaking in an oven at 70 °C, partly solidified the SOG. The magnets were removed from underneath the wafer before curing the SOG at temperatures reaching up to 250 °C. Thereafter, excess SOG and the protruding ends of the metal rods were ground away and the wafer was cured at 425 °C in a nitrogen atmosphere (see Fig. 2b). In order to



FIGURE 2. Illustration of TGV fabrication process: a) nickel rods fixed into holes, b) protruding ends of nickel rods and excess SOG removed by grinding, c) metal layer sputtering and plating followed by patterning, d) wafer thinning by wet etching, e) nickel reveal, and f) metal deposition and patterning followed by solder-paste jetting. g) Cross-sectional SEM image of a TGV after the first 250 °C cure of the SOG. The lower part of the nickel rod is hidden underneath the SOG because the cross-section cut does not precisely follow the orientation of the rod in the hole. h) SEM image of SOG dome revealed by wafer thinning. i) SEM image of nickel rod revealed from underneath the SOG dome. j) Optical microscope image of the solder-paste deposits on TGVs before solder reflow.

compensate for SOG shrinking during the cure, a new layer of SOG was applied and the grinding and curing process was repeated. An SEM image of a cross-section of a TGV is shown in Fig. 2g.

After argon sputter-cleaning, a metal layer consisting of a 150 nm thick TiW layer and a 1 µm thick gold layer was sputtered on the substrate surface. This was followed by electroplating (EPM 202F, Rena) of a 5 µm thick additional gold layer using a cyanide-free gold plating solution (Microfab Hue Au R, Enthone) in combination with a current density of 1.5 mA/cm^2 . The metal layer was patterned to define the metal areas that connect neighboring TGVs together in pairs. The pattern was created with direct ablation of material using a femtosecond laser (Spirit 1040-4-SHG, Spectra-Physics). Femtosecond lasers allow micrometer precision in material removal because their extremely-short pulse length creates only a small heat-affected-zone around the ablated volume [26], [27]. The laser beam was focused on the wafer surface using an objective with a 0.10 numerical aperture while a computer-controlled stage moved the wafer at a speed of 100 µm/s. The laser wavelength was 1040 nm, repetition rate 200 kHz, and nominal power 4 W. Residues from the laser processing that were left on the wafer surface were cleaned by tape peeling and rinsing with acetone and isopropanol (see Fig. 2c).

VOLUME 6, 2018

The blind vias in the glass substrate were revealed by wet etching from the backside. Before glass etching, the glass wafer was temporarily bonded, using a polymer layer, to a silicon carrier wafer in order to provide support for the glass wafer. After bonding, the wafer was etched to a thickness of 120 µm using 50 vol% hydrofluoric acid (HF) solution, achieving an etch rate of $\sim 25 \,\mu\text{m/min}$ (see Fig. 2d). The wet etch process revealed SOG domes, each containing a nickel wire, protruding from the surface (see Fig. 2h). This is because SOG has a lower etch rate than the glass wafer, presumably due to the presence of residual carbon in the SOG. A layer of glass surrounding the SOG dome had a higher etch rate than the bulk glass, which limits the etch depth because the etchant starts to penetrate between the bulk glass and the SOG along this layer. We assume that this layer, appearing porous in Fig. 2h, belongs to a damage zone created during the via-hole formation. The SOG domes were removed by mechanical grinding and any remaining SOG was removed with femtosecond laser ablation. The revealed nickel surfaces were finally cleaned by a wet nickel etch step resulting in a clean metal (see Fig. 2e and 2i). A metal layer consisting of 150 nm of TiW and 3 µm of gold was sputtered on the wafer. This metal layer, like the one on the front side of the wafer, was patterned using femtosecond laser ablation. The pattern formed a daisy chain structure connecting adjacent TGVs

(see 2f and 2j). The surface was cleaned, as before, with tape peeling and acetone/isopropanol rinse.

The deposition of solder paste on top of the TGVs was performed using a novel jetting technology (MY700 Jetprinter, Mycronic AB, Täby, Sweden). Developed specifically for high-viscosity functional electronic fluids, this jetting technology utilizes a piezo-induced volumetric displacement that causes a dramatic pressure pulse that forces fluid through a single 100 µm-wide nozzle at frequencies of up to 300 Hz. The fluid in this case was a SnAgCu 305 solder paste (96.5%) Sn, 3% Ag, and 0.5% Cu from Tamura, Japan). The paste consists of spherical metallic alloy granules together with an organic resin-based fluid binder in an 86 wt% mixture. Droplets with a target diameter of 210 µm and approximate volume of 1.8 nL were jetted, with a nominal 12 µm standard deviation of the position accuracy, on the previously deposited Au layer that acted as an under-bump metallization (see Fig. 2f and 2j). After deposition, solder-paste reflow was done in a commercial vapor-phase oven (VP800, Asscon Systemtechnik, Germany). The oven was filled with perfluoropolyether vapor with the maximum temperature of 230 °C and temperature gradients in the range of 0.7-1.8 °C/s.

B. RESISTANCE MEASUREMENTS

Resistance measurements were performed to characterize the electrical functionality of the magnetically assembled TGVs, allowing comparisons to other metal TGV types. Resistances were measured before solder deposition using a probe station in a four-terminal configuration. Each measured unit consisted of two TGVs connected in series. The total of 83 TGV pairs from which a resistance value was obtained included 57 pairs with a pitch of 350 µm and 26 pairs with a pitch of 220 µm. The measured resistance is the sum of resistances from three sources: the nickel rods, metal layers on both sides of the wafer, and interfaces between nickel and metal layers. Since the metal layers on both sides of the wafer were quite thick, different pitches of TGVs cause only a minor effect on the measured resistance. The measured resistance data had a positively skewed distribution that was characterized by estimating its probability density function. This allowed us to locate the main mode of the distribution, i.e. the most probable value of the TGV-pair resistance within this distribution. The probability density function was obtained through kernel density estimation using Gaussian kernel and Sheather-Jones plug-in bandwidth [28].

C. IMPACT OF MAGNETIC-ASSEMBLY PARALLELIZATION ON WAFER-SCALE ASSEMBLY TIME

Using multiple magnets for the assembly of a single wafer was found to allow successful magnetic assembly of TGVs. In order to decrease the time required for the magnetic assembly on wafer scale, we investigated the possibility to parallelize the magnetic-assembly process by placing multiple magnets underneath the wafer and moving them simultaneously. It can be anticipated that the total assembly time is inversely related to the amount of magnets simultaneously assembling separate die areas on a wafer. In order to obtain a better picture of the achievable wafer-scale assembly times, we characterized the variations in assembly rates between the different magnets during parallel assembly. In order to remove variations from assembly by hand, a robot was used to move the magnets in these experiments. As in the previous works on magnetic assembly, via holes in silicon substrates, with a low tendency for disassembly, were used in these experiments. This provides an established platform where the progression of the assembly process can be easily observed and modeled.

The experiments were divided into two parts using two separate wafers and two or four assembly magnets, respectively. The magnets were attached to a holder which was moved by the robot arm while the wafer was kept stationary (see Fig. 3). The 350 µm-thick silicon wafers had via holes with vertical sidewalls, fabricated using the DRIE Bosch process. The holes reached through the full silicon thickness and ended on a thick thermally-grown silicon dioxide layer at the bottom side of the wafer. The diameter of the holes was 55 um and the ferromagnetic metal rods assembled into the holes had a diameter of 45 µm. Each area to be assembled consisted of 100 holes arranged in a square array (10×10 holes) with a 350 µm pitch between the holes. Around 3000 metal rods were placed on each array before the start of the assembly. Each magnet moved linearly underneath a single array sweeping from one side of the array to the other side and back again in two seconds while moving the total distance of \sim 30 mm, i.e. 15 mm each way (see Fig. 3b). The number of filled holes was observed with an optical microscope between the sweeps. Assembly was continued until all the holes were filled in all the arrays.



FIGURE 3. a) Setup for parallel assembly with a robot. b) Schematic top view of the movement of the magnets underneath hole arrays in a silicon substrate.

The experimental data on the progress of the assembly follow a similar trend in all the arrays. This allows us to fit a simple model to the assembly data from which a quantitative measure describing the speed of assembly in each array can be extracted. This measure is less susceptible to fluctuations between single measurements than simply comparing the number of sweeps needed to completely fill an array. The model is based on the assumption that the probability of filling a single hole during a single sweep stays constant over the whole assembly and is the same for all the holes in an array. From these assumptions, it follows that the proportion of the number of unfilled holes N(n) to the total number of the holes N_0 in the array can be described as a function of the number of sweeps *n* using an exponential decay function

$$\frac{N(n)}{N_0} = e^{-\frac{n}{m}},\tag{1}$$

where m is a parameter describing the mean number of sweeps needed to fill a single hole in the array. The collected assembly data from each array were separately fitted with this function using m as a fitting parameter.

D. THEORETICAL ANALYSIS OF CTE COMPATIBILITY BETWEEN TGV METALS AND SUBSTRATE MATERIALS

Thermal expansion differences between metal and substrate in TGVs can cause stress and reliability problems. These problems are pronounced if the TGV does not have a hollow center because this removes the possibility for metal to expand into the empty space at the center of the TGV. We compared thermal expansion rates of various metals to those of glass substrate materials in order to quantify their mutual compatibility. Metals in the comparison included the typical through-via metals of gold and copper together with some metals suitable for magnetic assembly: nickel, Invar (Fe 64, Ni 36 wt%), and Kovar (Fe 54, Ni 29, Co 17 wt%). Tungsten was also included in the comparison because it is used in reflow based TGVs [13], [22]; however, tungsten cannot be easily deposited to form completely filled TGVs. That is because the high stress of deposited tungsten allows only complete filling of narrow via holes [29]-[31], which are difficult to fabricate in glass substrates. We selected three different glasses, having a range of CTEs, that are suitable for different TGV applications: (1) fused silica provides the best RF performance and ultraviolet light transmittance; (2) Eagle XG provides a good CTE matching to silicon, e.g. making it suitable for sealing of silicon MEMS structures; and (3) borosilicate glass has a CTE between those of silicon and organic printed-circuit-board materials, which allows for a controlled distribution of thermal stresses in interposer applications [14].

Thermal expansion data used in our comparison are provided in the literature in four different formats: raw relativeexpansion data and three versions of CTE. The CTEs describe the rate of the change of relative thermal expansion. In addition to different formats, these data sets also rely on different reference temperatures T_r . The data formats and the reference temperatures were converted so that they are directly comparable to each other. The first of the thermal expansion formats, the relative expansion ϵ_{T_r} (also called engineering strain or nominal strain), is defined as

$$\epsilon_{T_r}(T) = \frac{L(T) - L(T_r)}{L(T_r)}, \qquad (2)$$

where L(T) is the length of an object at a temperature T and L_{T_r} is the length of the object at the reference temperature [32]. The relative expansion (i.e. strain) in (2) is

zero when the temperature *T* equals T_r . The three CTE formats are mean CTE $\bar{\alpha}_{T_r,T}$ [32], a CTE type called semiinstantaneous CTE in this article (also called the ASTM definition) $\alpha^A_{T_r,T_1,T_2}$ [33], and instantaneous CTE $\alpha_{T_r}(T)$ [32], [33]. The mean CTE gives the mean value of the rate of relative thermal expansion from the reference temperature to a temperature *T* of the data point and is defined as

$$\bar{\alpha}_{T_r,T} = \frac{\epsilon_{T_r}(T)}{T - T_r} \,. \tag{3}$$

The semi-instantaneous CTE gives the mean value of the rate of relative thermal expansion in a temperature range from T_1 to T_2 , while still referring relative expansion to the length $L(T_r)$ at the reference temperature [33]. The semi-instantaneous CTE is defined as

$$\alpha^{A}_{T_{r},T_{1},T_{2}} = \frac{\epsilon_{T_{r}}(T_{2}) - \epsilon_{T_{r}}(T_{1})}{T_{2} - T_{1}}.$$
(4)

The instantaneous CTE gives the instantaneous rate of the relative thermal expansion at temperature T and is defined as

$$\alpha_{T_r}(T) = \frac{d\epsilon_{T_r}(T)}{dT} \,. \tag{5}$$

The mean CTE format can be converted to the semiinstantaneous format without resorting to curve fitting by using equation [33]

$$\alpha^{A}_{T_{r},T_{1},T_{2}} = \frac{\bar{\alpha}_{T_{r},T_{2}}(T_{2}-T_{r}) - \bar{\alpha}_{T_{r},T_{1}}(T_{1}-T_{r})}{T_{2}-T_{1}}.$$
 (6)

The semi-instantaneous CTE is in turn comparable to the instantaneous CTE because $\lim_{T_1 \to T_2} \alpha^A_{T_r,T_1,T_2} = \alpha_{T_r}(T)$ [33]. The reference temperatures in semi-instantaneous and instantaneous CTE formats can be changed, and thus unified, using equation

$$\alpha_{T_{r^2}}(T) = \frac{\alpha_{T_{r^1}}(T)}{1 + \int_{T_{r^1}}^{T_{r^2}} \alpha_{T_{r^1}}(T) \, dT},\tag{7}$$

where T_{r1} is the original reference temperature and T_{r2} is the unified reference temperature [25].

Equation (6) was applied to Kovar [34] and Eagle XG [35] data, which were given originally in the mean CTE format. Gold and nickel data [36] were given in a raw format of relative thermal expansion. These data points were interpolated with lines whose slopes give the semi-instantaneous CTEs between the points. The semi-instantaneous CTE data were sampled and moving averages were calculated by taking an unweighted mean of data points within 10 °C on both sides of each data point. This approach reduces noise in the data and avoids possible inaccuracies associated with polynomial fitting. The rest of the CTEs for Invar [25], tungsten [37], copper [38], borosilicate glass [39], silicon [40], and fused silica [41] were given in the instantaneous format described by polynomial curves. The reference temperatures of all the instantaneous and the semi-instantaneous CTEs were unified to 25 °C using (7). Finally, a quantified measure of thermal

compatibility is given by mismatch strain [42], created by a temperature change from T_r to T,

$$\epsilon_{m,T_r}(T) = \int_{T_r}^T \left[\alpha_{C,T_r}(T) - \alpha_{S,T_r}(T) \right] dT , \qquad (8)$$

where α_{C,T_r} is the CTE of the conductor and α_{S,T_r} is the CTE of the substrate [25]. The reference temperature T_r of the CTEs is also the starting point of the integration in (8), since both the conductor and substrate materials are strain free at the temperature T_r as can be seen from (2).

III. RESULTS AND DISCUSSION

A. THROUGH-GLASS VIAS AND SOLDER BUMPS

We aimed to demonstrate that magnetic assembly can be used to fabricate TGVs. Even though shallow via holes with a tilted sidewall profile created a challenge for magnetic assembly, our new magnetic-assembly process using multiple magnets allowed the metal rods to stay in the via holes before being fixed in place by the spin-on glass. Moreover, compared to the prior work on filling via holes in silicon [23]-[25], we extended the applicability of magnetic assembly into blind vias, which allows us to retain a thick and easy-to-handle substrate through large parts of the fabrication process for cases where a thin final substrate is required. An example of a functional TGV pair is shown in Fig. 4 in a crosssectional view. The completely filled TGVs allowed us to successfully deposit and reflow solder paste directly on the TGVs, thus increasing the integration density. A 3D representation of the resulting conductive structure, generated from computed tomography (CT) images, is presented in Fig. 5. Because electrical resistance is a central performance measure of a TGV, the resistance distribution of 83 magnetically assembled TGV pairs was analyzed. The distribution has the main mode, i.e. the most probable value, at $127 \text{ m}\Omega$, thus indicating a nominal single-TGV resistance having the most probable value of $64 \text{ m}\Omega$ (see Fig. 6). The distribution is positively skewed with a tail at higher resistances; when including even the outliers in Fig. 6, the distribution has the median value at $173 \,\mathrm{m}\Omega$, thus indicating a nominal single-TGV resistance having the median value of $87 \text{ m}\Omega$. All the resistance values include contact resistances and interconnect resistances.



FIGURE 4. Cross section SEM showing a functional TGV pair. The lines cut in the metal layer on top of the wafer define the areas connecting adjacent TGVs in series for the purpose of resistance measurements (cf. Fig. 2f and 2j).



FIGURE 5. Computed tomography (CT) rendering of a TGV pair after successful reflow of the solder paste on top of the TGVs.



FIGURE 6. Histogram showing the measured resistances of the TGV pairs measured from loose (dark) and tight (light) pitch arrays stacked on top of each other. The vertical grey line shows the location of the median of the distribution. The median was calculated from all the measured resistances, including the outliers. The orange curve shows the probability density function around the main mode of the distribution. The location of the main mode, i.e. the most probable resistance, is marked with a vertical orange line.

We have demonstrated that magnetic assembly is a suitable method for the fabrication of TGVs and that solder bumps can be placed directly on top of the TGVs. This approach also works for blind via holes in combination with wafer thinning to obtain thin glass substrates. It should be noted that magnetic assembly is not only limited to the via dimensions demonstrated here but can be applied for a variety of TGV lengths and widths. Possible limitations for the TGV dimensions are the minimum commercially available metal wire diameter of around 10-15 µm [23], the need of the metal rod to be longer than its width for it to orientate correctly in the magnetic field, and the maximum length of the metal rod limited by the extend and shape of the magnetic field that is needed to force the rod to stay in an upright orientation. The blind TGVs fabricated in this work contained imperfections where some of the nickel rods were not reaching the bottom of the via holes. These small variations in the depth into which the nickel rods reached were compensated

by continuing the wet wafer-thinning process past the length of the via holes; this allowed a larger number of the metal rods to reach the surface of the wafer. However, the etchant started to penetrate between the spin-on glass and the viahole sidewall, thus limiting the amount of wafer thinning after the SOG domes were revealed. A possible explanation for the unwanted etchant penetration is that porous substrate material, created by hole formation [16], is present on the surface of the via-hole sidewalls and that this porous material is more susceptible to the etchant (see Fig. 2g and 2h). The effects of the varying reach of the nickel rods in the via holes can be seen as imperfections in Fig. 4; on the left side the nickel rod does not completely reach the wafer surface and would have benefited from further wafer thinning, whereas on the right side the rod reaches the surface, but wet HF etching has started to create a groove between the rod and the via-hole sidewall. We see at least two possibilities for improving the wafer thinning process in the future. Firstly, if the faster etch rate at the edges of the via hole is due to a damaged layer of substrate material originating from the via hole formation, the damaged layer could be removed and thus the problem remedied by HF etching this layer already before the magnetic assembly process. This could reduce the penetration of the etchant into the interface between the spinon glass and the via sidewall. Secondly, the final stages of the wet wafer thinning could be replaced by mechanical grinding and chemical-mechanical polishing (CMP), thus avoiding this problem altogether.

The resistances obtained for magnetically assembled TGVs in this work are comparable to the resistances of other metal TGVs reported in the literature [18], [21], [43]. Bottomup plated nickel TGVs have been reported to have a resistance of about $40 \text{ m}\Omega$ [43]. Bottom-up plated copper TGVs have been reported to have a resistance of $153 \pm 23 \text{ m}\Omega$ of which $74\,\mathrm{m}\Omega$ was attributed to the copper in the via and the rest $(79 \text{ m}\Omega)$ to the contact resistance between copper and the surface metal layer [21]. A gold TGV with a hollow center, fabricated using metal plating starting from the sidewalls, is reported to have a resistance of 28 m Ω including the surface metallization [18]. In our magnetically assembled TGVs, $6 \,\mathrm{m}\Omega$ of the most probable single-TGV resistance of $64 \,\mathrm{m}\Omega$ can be attributed to the resistance of a single nickel rod, if a resistivity value of $7.12 \times 10^{-8} \Omega \cdot m$ [44] is used for nickel. The remaining portion $(58 \text{ m}\Omega)$ of the resistance of a single TGV can be attributed to the metal interconnect layers and the contact resistances between these layers and the nickel rods. Apart from the most probable resistance, a tail of higher resistances was observed in the measurements. This tail can possibly be attributed to the structural defects in the TGVs originating from some nickel rods not completely reaching the wafer surface. This can hamper the cleaning of the nickel rod surface, thus increasing the contact resistance between the nickel rod and the metal interconnect layer. In the future, reducing the spread of the resistances would improve the maturity of our proposed TGV fabrication method. This could be done by reducing the structural defects and improving cleaning and oxide removal of the ends of the nickel rods before metal deposition. The TGV resistance could also be lowered by coating the ferromagnetic metal rods by gold. This kind of coating also allows realization of ferromagnetic TGVs with good performance for RF applications [24].

B. PARALLELIZATION DECREASES WAFER-SCALE ASSEMBLY TIME

We investigated whether parallelization of the magneticassembly process can decrease the wafer-scale assembly time in comparison to a serial magnetic assembly using a single magnet. Since the total speed of the parallel assembly of a full wafer is determined by the slowest assembling magnet, we investigated the consistency of the time required to fill the 100 via holes in each array. Two and four arrays were assembled simultaneously, each with a separate magnet, until a complete filling of all the holes was achieved. An example of a completely filled array is shown in Fig. 7. In order to compare assembly times between the arrays, the progression of the filling of the arrays was recorded at regular intervals and the model given in (1) was fitted to each of the results (see Fig. 8). The number of sweeps needed to completely fill the arrays varied between five and ten sweeps, corresponding to assembly times between ten and twenty seconds, respectively. The model fits the data reasonably well and indicates that the mean number of sweeps needed to fill a single hole in an array, i.e. the model parameter m used to compare the filling speeds between the arrays, varied between 1.1 and 2.5 sweeps.



FIGURE 7. Top-view optical microscope images of the same array after one sweep and after eight sweeps. Filled holes can be clearly distinguished from the unfilled ones.

The consistency of the assembly times between different areas on a substrate indicates that a parallelized process using an assembly robot can decrease the wafer-scale assembly time. The model used to characterize the assembly times gave a reasonably good fit of the data, thus indicating that the main properties of the assembly process can be described with the exponential-decay model and the associated parameter m. The parameter m has some variation between the arrays, possibly originating from geometrical differences between the via holes. The same is expected for various via-hole geometries in glass substrates. Other possible reasons for the variations in the parameter m can include, for example,



FIGURE 8. Measured ratio of empty holes in each array after a number of sweeps together with fits using the function in (1). Inset shows the mean number of sweeps needed to fill a single hole in each array together with 95% confidence limits.

slightly different amounts of wires used to assemble the arrays and the variations of a magnet movement path in relation to an array. Even though the value of the parameter m is not the same for all the arrays within 95% confidence limits, the variation of the assembly speeds between the arrays can be seen as small; the variation is measured to be of the order of tens of seconds whereas the duration of an alternative viafabrication process, for example metal plating, is measured in several tens of minutes or more. Since the variation of *m* is low, parallel assembly magnets complete their areas in a similar timescale without any individual magnet delaying the wafer-scale process. Even though the values of mobtained using silicon substrates require further investigation in glass, we have found that parallelized assembly with a robot can significantly decrease the wafer-scale assembly time, possibly down to the scale of the assembly time of a single die. Therefore, parallelization using a robot appears as a promising approach for increasing the throughput of magnetic assembly.

C. REDUCED THERMAL EXPANSION MISMATCHES IN TGVS

In our theoretical analysis, we found for every glass substrate material a thermally compatible metal that was also suitable for magnetic assembly (see Fig. 9). At temperatures below \sim 450 °C (723.15 K), the CTE of Kovar matches the CTE of borosilicate glass and is close to the CTEs of silicon and silicon-matched glasses such as Eagle XG, which was used as substrate material in this study. Fused silica has an extremely low CTE that greatly differs from those of gold and copper, whereas it is well matched by the CTE of Invar in a temperature range between room temperature and \sim 125 °C (398.15 K). Nickel, which was used as a TGV metal in this study, has a lower CTE than copper in the entire temperature range and also outperforms gold at low temperatures. Tungsten has a CTE that is compatible with silicon-matched glasses and borosilicate, but as discussed in section II-D,



FIGURE 9. Instantaneous and semi-instantaneous CTEs of substrate materials (dashed lines) and conductor materials (solid lines) as a function of temperature.

tungsten cannot be used in fully filled TGVs without utilizing a glass reflow process.

For the purpose of quantifying the level of matching between the CTEs of substrate and conductor materials in TGVs, we use the mismatch strain in (8). For simplicity, we have excluded the material layer binding the metal rods into the via holes from this analysis. On top of the CTEs, the mechanical behavior of a TGV at high temperatures is also affected by other material properties, such as the elastic modulus and yield strength, which impact the material deformations resulting from the thermal-expansion mismatch in the TGV. In the current study, we focus on identifying substrate-conductor pairs where the thermal-expansion mismatch is minimal in the first place, and therefore we have not considered the impact of the other properties. The mismatch strain is based on two temperatures: the reference temperature T_r and the temperature extreme T that the TGV experiences, either in use or during the fabrication process. The temperature T_r in (8) is used for two different purposes. Firstly, it is the reference temperature of the CTEs of the conductor material $\alpha_{C,T_r}(T)$ and the substrate material $\alpha_{S,T_r}(T)$. Secondly, it is the strain-free temperature at which a TGV structure obtains its final form during the fabrication process. The second usage of T_r is represented by the starting point of the integration in (8). For the first usage, the reference temperature T_r of the CTEs was set to 25 °C in our analysis, but depending on the fabrication process, this is not necessarily the strain-free temperature of the TGV. However, adjusting the reference temperature of the CTEs using (7) gives only a small change to the CTE curves; for example, the CTE of $10 \times 10^{-6} \text{ K}^{-1}$ changes its value by 0.1% if T_r is changed by 100 K. This means that only a negligible error is introduced to a mismatch-strain calculation using (8) if the CTE curves $\alpha_{C,T_r}(T)$ and $\alpha_{S,T_r}(T)$ are not corrected to reflect the strain-free temperature of the fabrication method. In contrast, adjusting the starting point of the integration in (8) has a significant effect on the mismatch strain. Therefore,

without changes necessary to the CTE curves, the mismatch strain in Fig. 9 is represented by the area between the CTE curves of the conductor and the substrate in the temperature range between the strain-free temperature of the TGV and the temperature extreme T that the TGV experiences. In magnetic assembly, the strain-free temperature is the temperature at which the material fixing the metal rod in the via hole, i.e. SOG in this work, reaches its final form. Hence, the low mismatch strain of Invar TGVs in fused silica is best realized if the Invar rods are fixed into the via holes with a material that solidifies at a low temperature. Kovar is less sensitive to this solidification temperature because Kovar's CTE is close to those of borosilicate and silicon-matched glass types in a wider temperature range. As the result of the analysis above, we have identified metals suitable for magnetic assembly, i.e. Kovar and Invar, that have a good thermal-expansion matching to a variety of glass substrates.

IV. CONCLUSIONS

We have shown that magnetic assembly can be used to fabricate TGVs. The magnetically assembled TGVs achieved resistances comparable to those of other metal TGVs, making them suitable for similar applications. Magnetic assembly was demonstrated to work in glass substrates with challenging short and blind via holes that had slanted sidewalls. This was done by using multiple magnets simultaneously for the assembly. Parallelizing the assembly process through the use of multiple magnets and an assembly robot was found to have the potential to greatly reduce wafer-scale assembly time. The magnetically assembled TGVs do not have a hollow center; this allows solder bump placement directly on top of the TGVs, thus leading to a high integration density. However, the lack of a hollow center can also result in stresses due to thermal-expansion mismatch between the substrate material and the metal in the via hole. To address this, theoretical analysis was used to identify metals that are both suitable for magnetic assembly and that have a good thermal-expansion compatibility with a range of glass types. In conclusion, magnetic assembly shows promise to rapidly fabricate TGVs with low resistances, high integration densities, and low thermal-expansion mismatch between the metal and the glass substrate. TGVs with these properties can find applications in glass interposers and MEMS packaging, thereby realizing the excellent properties of glass as a package material.

ACKNOWLEDGMENTS

The authors would like to thank Cecilia Aronsson and Mikael Bergqvist for their help in cleanroom processing and tooling, respectively.

REFERENCES

[1] M. J. Laakso, J. Liljeholm, A. C. Fischer, G. Stemme, T. Ebefors, and F. Niklaus, "Maskless manufacturing of through glass vias (TGVs) and their test structures," in *Proc. IEEE 30th Int. Conf. Micro Electro Mech. Syst. (MEMS)*, Las Vegas, NV, USA, Jan. 2017, pp. 753–756. [Online]. Available: http://ieeexplore.ieee.org/document/7863517/

- [3] A. C. Fischer *et al.*, "Integrating MEMS and ICs," *Microsyst. Nanoeng.*, vol. 1, p. 15005, May 2015. [Online]. Available: http://www.nature.com/articles/micronano20155
- [4] V. Sridharan *et al.*, "Design and fabrication of bandpass filters in glass interposer with through-package-vias (TPV)," in *Proc. IEEE 60th Electron. Compon. Technol. Conf.*, Jun. 2010, pp. 530–535. [Online]. Available: http://ieeexplore.ieee.org/document/5490917/
- [5] Y. Sato et al., "Ultra-miniaturized and surface-mountable glass-based 3D IPAC packages for RF modules," in *Proc. IEEE 63rd Electron. Compon. Technol. Conf. (ECTC)*, May 2013, pp. 1656–1661. [Online]. Available: http://ieeexplore.ieee.org/document/6575795/
- [6] T. Ebefors et al., "The development and evaluation of RF TSV for 3D IPD applications," in Proc. IEEE Int. 3D Syst. Integr. Conf., Oct. 2013, pp. 1–8. [Online]. Available: http://ieeexplore.ieee.org/document/6702382/
- [7] V. Sukumaran et al., "Design, fabrication, and characterization of ultrathin 3-D glass interposers with through-package-vias at same pitch as TSVs in silicon," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 5, pp. 786–795, May 2014. [Online]. Available: http://ieeexplore.ieee.org/document/6740002/
- [8] R. Mahajan et al., "Embedded multi-die interconnect bridge (EMIB)— A high density, high bandwidth packaging interconnect," in Proc. IEEE 66th Electron. Compon. Technol. Conf., May/Jun. 2016, pp. 557–565. [Online]. Available: http://ieeexplore.ieee.org/document/7545486/
- [9] D.-C. Hu, Y.-P. Hung, Y. H. Chen, R.-M. Tain, and W.-C. Lo, "Embedded glass interposer for heterogeneous multi-chip integration," in *Proc. IEEE* 65th Electron. Compon. Technol. Conf., May 2015, pp. 314–317. [Online]. Available: http://ieeexplore.ieee.org/document/7159610/
- [10] R. Li, C. Jin, S. C. Ong, T. G. Lim, K. F. Chang, and S. W. Ho, "Embedded wafer level packaging for 77-GHz automotive radar front-end with through silicon via and its 3-D integration," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 9, pp. 1481–1488, Sep. 2013. [Online]. Available: http://ieeexplore.ieee.org/document/6410394/
- [11] A. Shorey, J. Keech, G. Piech, B.-K. Wang, and L. Tsai, "Glass substrates for carrier and interposer applications and associated metrology solutions," in *Proc. IEEE ASMC SEMI Adv. Semiconductor Manuf. Conf.*, May 2013, pp. 142–147. [Online]. Available: http://ieeexplore.ieee.org/document/6552803/
- [12] B. K. Wang, Y.-A. Chen, A. Shorey, and G. Piech, "Thin glass substrates development and integration for through glass vias (TGV) with copper (Cu) interconnects," in *Proc. IEEE 7th Int. Microsyst., Packag. Assem. Circuits Technol. Conf.*, Oct. 2012, pp. 247–250. [Online]. Available: http://ieeexplore.ieee.org/document/6420306/
- [13] P. Dixit and K. Henttinen, "Via technologies for MEMS," in Handbook of Silicon Based MEMS Materials and Technologies, M. Paulasto-Kröckel, Ed., 2nd ed. Amsterdam, The Netherlands: Elsevier, 2015, ch. 38, pp. 694–712, doi: 10.1016/B978-0-323-29965-7.00038-5.
- [14] Y. J. Lin, C. C. Hsieh, C. H. Yu, C. H. Tung, and D. C. H. Yu, "Study of the thermo-mechanical behavior of glass interposer for flip chip packaging applications," in *Proc. IEEE 61st Electron. Compon. Technol. Conf.*, May/Jun. 2011, pp. 634–638. [Online]. Available: http://ieeexplore.ieee.org/document/5898579/
- [15] Z. Wang, "3-D integration and through-Silicon vias in MEMS and microsensors," J. Microelectromech. Syst., vol. 24, no. 5, pp. 1211–1244, Oct. 2015. [Online]. Available: http://ieeexplore.ieee.org/document/7163513/
- [16] L. A. Hof and J. A. Ziki, "Micro-hole drilling on glass substrates— A review," *Micromachines*, vol. 8, no. 2, p. 53, Feb. 2017. [Online]. Available: http://www.mdpi.com/2072-666X/8/2/53
- [17] T. R. Anthony, "Forming electrical interconnections through semiconductor wafers," J. Appl. Phys., vol. 52, no. 8, pp. 5340–5349, Aug. 1981, doi: 10.1063/1.329392.
- [18] U. Shah, J. Liljeholm, J. Campion, T. Ebefors, and J. Oberhammer, "Low loss high linearity RF interposers enabled by through-glass vias," *IEEE Microw. Wireless Compon. Lett.*, to be published.
- [19] B. Khorramdel et al., "Inkjet printing technology for increasing the I/O density of 3D TSV interposers," *Microsyst. Nanoeng.*, vol. 3, Apr. 2017, Art. no. 17002. [Online]. Available: http://www.nature.com/articles/micronano20172

- [20] W. Li et al., "A new fabrication process of TGV substrate with silicon vertical feedthroughs using double sided glass in silicon reflow process," *J. Mater. Sci. Mater. Electron.*, vol. 28, no. 4, pp. 3917–3923, Feb. 2017. [Online]. Available: http://link.springer.com/10.1007/s10854-016-6005-0
- [21] S.-W. Lee, S.-K. Lee, and J.-H. Park, "High-density through-wafer copper via array in insulating glass mold using reflow process," *Jpn. J. Appl. Phys.*, vol. 54, no. 4, p. 047202, Apr. 2015. [Online]. Available: http://iopscience.iop.org/article/10.7567/JJAP.54.047202
- [22] M. Töpper et al., "3-D thin film interposer based on TGV (through glass vias): An alternative to Si-interposer," in Proc. IEEE 60th Electron. Compon. Technol. Conf., Jun. 2010, pp. 66–73. [Online]. Available: http://ieeexplore.ieee.org/document/5490887/
- [23] A. C. Fischer, S. J. Bleiker, T. Haraldsson, N. Roxhed, G. Stemme, and F. Niklaus, "Very high aspect ratio through-silicon vias (TSVs) fabricated using automated magnetic assembly of nickel wires," *J. Micromech. Microeng.*, vol. 22, no. 10, p. 105001, Oct. 2012. [Online]. Available: http://iopscience.iop.org/article/10.1088/0960-1317/22/10/105001
- [24] S. J. Bleiker et al., "High-aspect-ratio through silicon vias for high-frequency application fabricated by magnetic assembly of goldcoated nickel wires," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 5, no. 1, pp. 21–27, Jan. 2015. [Online]. Available: http://ieeexplore.ieee.org/document/6965577/
- [25] M. Asiatici, M. J. Laakso, A. C. Fischer, G. Stemme, and F. Niklaus, "Through silicon vias with invar metal conductor for high-temperature applications," *J. Microelectromech. Syst.*, vol. 26, no. 1, pp. 158–168, 2017. [Online]. Available: http://ieeexplore.ieee.org/document/7747468/
- [26] K. Sugioka and Y. Cheng, "Overview of ultrafast laser processing," in Ultrafast Laser Processing: From Micro-to Nanoscale, K. Sugioka and Y. Cheng, Eds. New York, NY, USA: Pan Stanford, 2013, pp. 1–36. [Online]. Available: https://www.taylorfrancis.com/books/9789814303699
- [27] K. Sugioka and Y. Cheng, Femtosecond Laser 3D Micromachining for Microfluidic and Optofluidic Applications. New York, NY, USA: Springer-Verlag, 2014, doi: 10.1007/978-1-4471-5541-6.
- [28] S. J. Sheather, "Density estimation," *Statist. Sci.*, vol. 19, no. 4, pp. 588–597, 2004, doi: 10.1214/08834230400000297.
- [29] G. Parès et al., "Through silicon via technology using tungsten metallization," in Proc. IEEE Int. Conf. IC Design Technol., May 2011, pp. 1–4. [Online]. Available: http://ieeexplore.ieee.org/document/5783204/
- [30] D. Malta, "TSV formation overview," in *Handbook of 3D Integration: 3D Process Technology*, P. Garrou, M. Koyanagi, and P. Ramm, Eds. Hoboken, NJ, USA: Wiley, 2014, pp. 65–77, doi: 10.1002/9783527670109.ch05.
- [31] S. Marschmeyer et al., "Modular integration of annular TSV structures filled with tungsten in a 0.25 μm SiGe:C BiCMOS technology," *Micro*electron. Eng., vol. 137, pp. 153–157, Apr. 2015. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0167931714004274
- [32] M. Niffenegger and K. Reichlin, "The proper use of thermal expansion coefficients in finite element calculations," *Nucl. Eng. Des.*, vol. 243, pp. 356–359, Feb. 2012. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0029549311010387
- [33] V. Bhattachar, "Instantaneous coefficient of linear thermal expansion— A new definition," *J. Test. Eval.*, vol. 25, no. 5, pp. 479–484, 1997, doi: 10.1520/JTE11357J.
- [34] Carpenter Technology Corporation, Philadelphia, PA, USA. (1990). CarTech Kovar Alloy: UNS K94610, Technical Datasheet. [Online]. Available: https://www.cartech.com/en/product-solutions/cartech-kovar-alloy/
- [35] Corning Incorporated. (2017). Eagle XG Slim Glass, Product Information Sheet. [Online]. Available: https://www.corning.com/media/worldwide/cdt/documents/EAGLE_PI_ Sheet_2017.pdf
- [36] F. C. Nix and D. MacNair, "The thermal expansion of pure metals: Copper, gold, aluminum, nickel, and iron," *Phys. Rev.*, vol. 60, no. 8, pp. 597–605, Oct. 1941, doi: 10.1103/PhysRev.60.597.
- [37] R. K. Kirby and T. A. Hahn, "Standard reference material 737: Tungsten-thermal expansion," Nat. Bur. Standards, Washington DC, USA, Tech. Rep., May 1976. [Online]. Available: https://www-s.nist.gov/srmors/certificates/archive/737.pdf
- [38] W. P. Reed, "Standard reference material 736: Copper— Thermal expansion," Nat. Inst. Standards Technol., Gaithersburg, MD, USA, Tech. Rep., Oct. 1990. [Online]. Available: https://www-s.nist.gov/srmors/certificates/archives/736.pdf

- [39] T. A. Hahn, "Standard reference material 731: Borosilicate glass—Thermal expansion," Nat. Bur. Standards, Washington DC, USA, Tech. Rep., Jul. 1972. [Online]. Available: https://www-s.nist.gov/srmors/certificates/archives/731.pdf
- [40] Y. Okada and Y. Tokumaru, "Precise determination of lattice parameter and thermal expansion coefficient of silicon between 300 and 1500 K," *J. Appl. Phys.*, vol. 56, no. 2, pp. 314–320, Jul. 1984. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.333965
- [41] W. P. Reed, "Standard reference material 739: Fused-silica thermal expansion," Nat. Inst. Standards Technol., Gaithersburg, MD, USA, Tech. Rep., Dec. 1991. [Online]. Available: https://www-s.nist.gov/srmors/certificates/archives/739.pdf
- [42] S.-K. Ryu, K.-H. Lu, X. Zhang, J.-H. Im, P. S. Ho, and R. Huang, "Impact of near-surface thermal stresses on interfacial reliability of through-silicon vias for 3-D interconnects," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 1, pp. 35–43, Mar. 2011. [Online]. Available: http://ieeexplore.ieee.org/document/5555956/
- [43] X. Li, T. Abe, Y. Liu, and M. Esashi, "Fabrication of high-density electrical feed-throughs by deep-reactive-ion etching of Pyrex glass," *J. Microelectromech. Syst.*, vol. 11, no. 6, pp. 625–630, Dec. 2002. [Online]. Available: http://ieeexplore.ieee.org/document/1097781/
- [44] J. R. Rumble, Ed., CRC Handbook of Chemistry and Physics, 98th ed. Boca Raton, FL, USA: CRC Press, 2018, ch. 12, pp. 41–42. [Online]. Available: http://hbcponline.com



MIKU J. LAAKSO received the B.Sc. degree in physics and the M.Sc. degree from the Atomic, Molecular, and Material Physics Program, University of Oulu, Finland, in 2013 and 2014, respectively. He is currently pursuing the Ph.D. degree with the Department of Micro and Nanosystems, KTH Royal Institute of Technology, Sweden. His current research interests include ultrashortpulse-laser-based processing, 3-D manufacturing, and methods for microsystem assembly and packaging.







JESSICA LILJEHOLM was born in 1987. She received the M.Sc. degree in chemistry and chemical engineering from the KTH Royal Institute of Technology in 2011. She performed her master's thesis work at Expancel's R&D Department, where she is an Analyst Engineer. Thereafter, she started as a R&D Project Manager with Silex Microsystems, the largest pure play MEMS foundry, in late 2011. She has been active in several of Silex customer programs as well as EU pro-

grams related to new TSV developments, such as CAJAL4EU and EPAMO. She currently holds an industrial Ph.D. position at Silex Microsystems, which will aim for research within poly MEMS-Polymer-Based Integration Platforms for Future Generation Miniaturized Heterogeneous MEMS Systems. In 2013, she received the Best Paper for the 2013 IWLPC in San Jose, CA, USA.



GUSTAF E. MÅRTENSSON (M'15) received the M.Sc. degree in engineering physics with a specialization in fluid mechanics and the Ph.D. degree in fluid mechanics from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2000 and 2006, respectively. He currently divides his time between the role as Expert Complex Fluids with Mycronic AB and an affiliated Researcher with the Department of Biotechnology, KTH Royal Institute of Technology. His research interests range

from the dynamics of complex fluids, the development of novel electronic materials, and innovative production technologies for the electronics industry.



GÖRAN STEMME (F'06) received the M.Sc. degree in electrical engineering and the Ph.D. degree in solid-state electronics from the Chalmers University of Technology, Gothenburg, Sweden, in 1981 and 1987, respectively. He joined the Department of Solid State Electronics, Chalmers University of Technology, in 1981, where he became an Associate Professor and the Head of the Silicon Sensor Research Group in 1990. Since 1991, he has been a Professor with the KTH Royal

Institute of Technology, Stockholm, Sweden, where he is currently the Head of the Department of Micro and Nanosystems, School of Electrical Engineering. His research on micro and nanotechnology and systems spans over a broad range of techniques and application fields, such as medical technology, microfluidics, and heterogeneous integration. He is a member of the Royal Swedish Academy of Sciences (KVA).



MIKHAIL ASIATICI received the B.Sc. degree in electronics engineering from the Politecnico di Torino in 2012 and the M.Sc. degree in nanotechnologies for ICTs from the Politecnico di Torino, the INP Grenoble, and the École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, in 2014. From 2014 to 2015, he was a Ph.D. candidate with the Micro and Nanosystems Department, KTH Royal Institute of Technology, Stockholm, Sweden, with a focus on inertial

MEMS sensors and integration for high temperature applications. He is currently pursuing the Ph.D. degree with the School of Computer and Communication Sciences, EPFL. His research interests include heterogeneous computing and DDR memory controllers.



THORBJÖRN (TOBY) EBEFORS (SM'13) received the M.Sc. degree in electrical engineering and applied physics from the Linköping Institute of Technology, Sweden, in 1995, and the Licentiate of Engineering degree (Thesis title: Three-dimensional Microstructures based on Polyimide Joints) and the Ph.D. degree (Thesis title: Polyimide V-groove joints for Three-dimensional Silicon Transducers) from the KTH Royal Institute of Technology, Stockholm, Swe-

den, in 1998 and 2000, respectively. In 2000, he became an Assistant Professor with the Department of Signals, Sensors and Systems, the Royal Institute of Technology, where he was a Supervisor and a part-time Project Leader with the Microsystem Technology Group. He has also taken a very active part in developing and giving courses and lectures in microsystems systems technology. From 2000 to 2017, he was with SILEX Microsystems AB, Järfälla, as a Chief Technologist. He is one of the co-founders of SILEX, the world largest pure play MEMS foundry. In 2017, he co-founded MyVox AB, where he currently acts as the COO leading activities on integrating IC and piezo-MEMS. His research is devoted to microsystem technology based on micromachining of silicon and 3-D integration. He has published over 50 research journal and conference papers and is an inventor of over 50 pending and granted patents.



ANDREAS C. FISCHER received the Diploma degree in microsystems engineering from the University of Freiburg, Germany, in 2008, and the Ph.D. degree in microsystem technology from the KTH Royal Institute of Technology, Sweden, in 2013. From 2015 to 2016, he was a Post-Doctoral Fellowship with the Institute of Applied Physics and Nanotechnology, Karlsruhe Institute of Technology, Germany. Since 2017, he has been an Engineering Manager with Silex Microsystems

AB, Järfälla, Sweden. His main expertise lies in the development and manufacturing of MEMS and NEMS devices, heterogeneous integration of MEMS and IC technology, and advanced wire bonding technology.



FRANK NIKLAUS (SM'12) received the M.Sc. degree in mechanical engineering from the Technical University of Munich, Germany, in 1998, and the Ph.D. degree in MEMS from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2002. Since 2013, he has been a Professor with the Department of Micro and Nanosystems, KTH Royal Institute of Technology, where he is currently the Head of the Micro and Nanofabrication Group. His current research interests include

innovative manufacturing, integration, and packaging technologies for MEMS and NEMS.

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