

Received May 26, 2018, accepted July 2, 2018, date of publication July 11, 2018, date of current version August 7, 2018.

Digital Object Identifier 10.1109/ACCESS.2018.2855044

# A General Dimension Reduction Method for the Dispersion Modeling of Semiconductor Devices

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This work was supported in part by the Singapore Ministry of Education Academic Research Fund Tier 2 under Grant MOE2014-T2-2-151 and in part by the Suzhou Science and Technology Council, China, under Grant SYG201618.

**ABSTRACT** This paper presents a general dimension reduction method for the dispersion modeling of current and charge sources of semiconductor devices including HEMTs, LDMOS, and HBTs. The dimensions that are easily handled are represented by the existing empirical or physical functions, while those dimensions that are difficult to tackle with or have limited measurement data are represented by the Taylor expansion. In this paper, an AlGaIn/GaN HEMT was taken as the example device to illustrate how this method can be applied to handle the comprehensive dispersion effects induced by thermal and charge trapping. The dimensions of terminal voltages ( $V_{gs}$ ,  $V_{ds}$ ) are characterized by the 10-parameter Angelov function, while the remaining dispersion-related dimensions (channel temperature  $T_j$  and drain trap state  $\phi_D$ ) are expressed by the Taylor expansion. The constructed drain current source ( $I_{ds}$ ) model is able to predict a number of pulsed  $I$ - $V$ s with various channel temperature and quiescent biases. Finally, the analytical large signal model was implemented in the advanced design system, and several  $RC$  sub-circuits with multiple time constants were exploited to implement the dispersion model in the simulator. Good agreement has been achieved for both small-signal and large-signal characteristics of the investigated devices.

**INDEX TERMS** Dimension reduction, Taylor expansion, empirical model, semiconductor devices, AlGaIn/GaN HEMT, LDMOS, large signal model, dispersion, charge trapping, self-heating, thermal.

## I. INTRODUCTION

Good transistor models are essential for efficient computer-aided-design (CAD) of nonlinear microwave and RF circuits, monolithic microwave integrated circuits (MMICs), power amplifiers (PAs) and nonlinear RF systems [1]. Empirical models have shown great success for industrial applications in the last decades due to its robustness, good accuracy, and high simulation efficiency [2]–[17]. However, to accommodate rapidly evolving semiconductor material technologies and systems (e.g., GaAs pHEMTs, InGaAs pHEMT, SOI, LDMOS, GaN HEMTs, etc.), the complexity of empirical models persistently increases to capture the comprehensive dispersion effects like self-heating and charge trapping [12]–[17], which make the conventional modeling work sophisticated and time-consuming. In addition, the increasing complexity of the model may lead to overfitting problems, especially when limited data are available for the

model construction. In consequence, those models may give nonphysical response.

In this work, a general dimension reduction method is developed to address the multi-dimensional problems in the current semiconductor device modeling technique. The terminal voltage related dimensions are described by the existing well-defined empirical functions, whilst other dimensions (such as thermal and traps) which are tough to deal with are represented by Taylor expansion. In this way, the comprehensive dispersion effects in the emerging semiconductor devices can be easily modeled. Moreover, the proposed approach can be easily adopted in current empirical models and it is independent of semiconductor materials and processes, which would effectively shorten the development procedure for future compact modeling of semiconductor devices.

Wide bandgap semiconductor like AlGaIn/GaN HEMT is becoming an attractive alternative for the design of high

power RF circuits and MMICs [18]–[28]. The desirable characteristics of high power density and high frequency operation not only boost the microwave system performance, but also contribute to the integration and minimization of circuits and modules. However, these high power density devices exhibit strong dispersion effects like self-heating and charge trapping when they are pushed hard to achieve increased efficiency and output power [29]–[33], which would lead to significant deviation and degradation of the circuit performance. As a result, a model which is able to accurately predict these side effects is crucial for the computer aided design (CAD). Therefore, in this paper, we take AlGaIn/GaN HEMT as the example to illustrate how the proposed dimension reduction method can be applied for the accurate modeling of dispersion effects.

A commercial  $2 \times 400 \mu\text{m}$  (2 fingers with  $400\text{-}\mu\text{m}$  gate width) GaN HEMT from Dynax Semi., Inc. with the product ID C324009149, is employed for the investigation. In this work, the input of the current and charge sources of the GaN HEMT are composed of terminal voltages ( $V_{gs}$ ,  $V_{ds}$ ) and auxiliary variables (channel temperature  $T_j$  and drain trap state  $\phi_D$ ). The dimensions of port voltages are characterized by 10-element Angelov function [2], [3], while the dispersion states are represented by Taylor expansion. Narrow pulsed I-V (PIV) equipment (400ns pulse width with duty cycle of 0.1% for both gate pulser and drain pulser) is exploited to sample the I-Vs of the GaN HEMT with frozen dispersion state. The final current source model is expressed as the linear combination of several empirical functions, and the proportion of each function is determined by the dispersion states.

A large signal model is implemented in Advanced Design System (ADS). Extensive simulations have been carried out to validate the proposed model. Excellent agreement has been achieved between the measurement and simulation for both static and RF characteristics, including pulsed/continuous I-V, multi-bias S-parameters, power sweeps, and load-pull contour, etc.

Concrete theory and detailed modeling procedure are provided in this paper, which is a comprehensive extension to our previous work [34]. Section II introduces the proposed dimension reduction method. The dispersion modeling of the drain current of GaN HEMT is demonstrated in Section III-A; Section III-B describes the measurement setup for pulsed I-Vs and the validation of the drain current source model; Section III-C introduces the modeling of nonlinear intrinsic capacitances. Section IV shows the validation of the large signal model for the investigated GaN HEMT; the conclusion is drawn in Section V; and an extra example of the thermal modeling of LDMOS is given in the Appendix to demonstrate the generality of the proposed method.

## II. GENERALLY DIMENSION REDUCTION METHOD

Let us first define a multivariable function  $f(\mathbf{p}, \mathbf{q})$ , where

$$\mathbf{p} = (x_1, x_2, \dots, x_N) |_{1 \times N}, \mathbf{q} = (y_1, y_2, \dots, y_M) |_{1 \times M}$$

The dimension  $\mathbf{q}$  is behaving as monotonic or quasi-linear within the interest region, which will be represented by Taylor expansion; the dimension  $\mathbf{p}$  is highly nonlinear and is characterized by well-defined empirical or physical functions. Then the function  $f(\mathbf{p}, \mathbf{q})$  can be approximated by expanding dimension  $\mathbf{q}$  at quiescent point  $\mathbf{q}_0$  [35]

$$f(\mathbf{p}, \mathbf{q}) \approx f(\mathbf{p}, \mathbf{q}_0) + \nabla f(\mathbf{p}, \mathbf{q})|_{\mathbf{q}=\mathbf{q}_0} \cdot (\mathbf{q} - \mathbf{q}_0)^T + \frac{1}{2} (\mathbf{q} - \mathbf{q}_0) \cdot \mathbf{H}f(\mathbf{p}, \mathbf{q})|_{\mathbf{q}=\mathbf{q}_0} \cdot (\mathbf{q} - \mathbf{q}_0)^T \quad (1)$$

where  $\mathbf{q}_0$  is the expansion point,  $\nabla f(\mathbf{p}, \mathbf{q})|_{\mathbf{q}=\mathbf{q}_0}$  is the Jacobian, and  $\mathbf{H}f(\mathbf{p}, \mathbf{q})|_{\mathbf{q}=\mathbf{q}_0}$  is the Hessian matrix at point  $\mathbf{q}_0$ . They are given by

$$\begin{aligned} \nabla f(\mathbf{p}, \mathbf{q})|_{\mathbf{q}=\mathbf{q}_0} &= \left. \frac{\partial f(\mathbf{p}, \mathbf{q})}{\partial \mathbf{q}} \right|_{\mathbf{q}=\mathbf{q}_0} \\ &= \left( \frac{\partial f}{\partial y_1}, \frac{\partial f}{\partial y_2}, \dots, \frac{\partial f}{\partial y_M} \right)_{\mathbf{q}=\mathbf{q}_0} \end{aligned} \quad (2)$$

$$\mathbf{H}f(\mathbf{p}, \mathbf{q})|_{\mathbf{q}=\mathbf{q}_0} = \left. \frac{\partial \left( \frac{\partial f(\mathbf{p}, \mathbf{q})}{\partial \mathbf{q}} \right)^T}{\partial \mathbf{q}} \right|_{\mathbf{q}=\mathbf{q}_0} \quad (3)$$

The key of the expansion procedure is to determine the Jacobian and Hessian matrices. The dimension  $\mathbf{q}$  of the original function  $f(\mathbf{p}, \mathbf{q})$  is reduced, and the function form is degenerated to (1). To illustrate how we apply this dimension reduction method in device modeling, the modelling of GaN HEMT drain current source is demonstrated as an example.

## III. MODELING OF GAN HEMTs

The intrinsic nonlinear model for the investigated GaN HEMT is shown in Fig.1, which consists of the nonlinear capacitances, the current source and the corresponding trapping and thermal sub-circuits. The microphotographs of the investigated GaN HEMT device and the on-wafer PIV measurement system are illustrated in Fig.2. Detailed model extraction procedure is given in Fig.3. The procedure includes the extraction of extrinsic parasitics, construction of intrinsic nonlinear current/charge sources, and the tuning strategy for the final large signal model generation.

### A. GENERAL DIMENSION REDUCTION METHOD FOR DRAIN CURRENT SOURCE MODELLING

Based on our experiment results shown in Fig.4, the gate trap can be safely neglected, as the pulsed I-V characteristics do not vary significantly under different gate quiescent voltages. Thus only drain trap is considered in this work.

As given in Table 1, the drain current source is dependent on both terminal voltages ( $V_{gs}$ ,  $V_{ds}$ ) and auxiliary variables including channel temperature ( $T_j$ ) and drain trap state ( $\phi_D$ ).

The dispersion states can be identified from the PIVs, which are given by

$$\phi_D = V_{DSQ} \quad (4)$$

$$T_j = T_{amb} + P_{diss} \times R_{th} \quad (5)$$

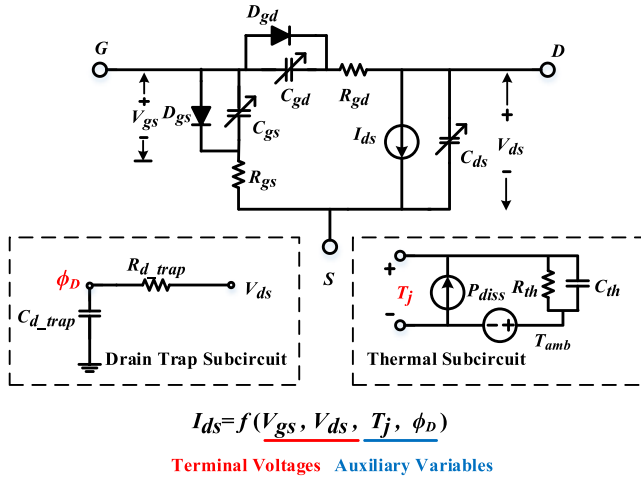


FIGURE 1. Adopted intrinsic large signal model topology for GaN HEMT.

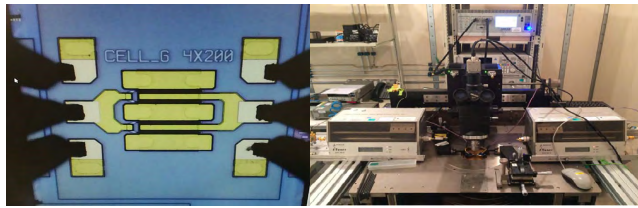


FIGURE 2. (a) Microphotograph of the investigated GaN HEMT device from Dynax Semi., Inc. (b) Setup of the on-wafer load-pull system (Focus Tuner, model 1808-2C) and the PIV system (AMCAD PIV system).

TABLE 1. Input variables of drain current source.

Terminal Voltage		Dispersion Effects	
Gate	Drain	Drain Trap	Channel Temp.
$V_{gs}$	$V_{ds}$	$\phi_D$	$T_j$
Empirical function		Taylor expansion	

where  $V_{DSQ}$  is the drain-source quiescent bias of the PIVs, or more precisely, the averaging drain-source voltage.  $T_{amb}$  is the ambient temperature.  $P_{diss}$  is the average dissipated power, and  $R_{th}$  is the thermal resistance.

It should be noted that, the drain trap  $\phi_D$  in TABLE 1 is the maximum of the drain voltage, which can be obtained by implementing an envelope tracking circuit. However, this requires more advanced measurements like double pulsed I-V or time domain data collected from a nonlinear vector network analyzer (NVNA) [1]. As these measurements are not available to us currently, we choose the averaging drain-source voltage to represent the drain trap state. As a matter of fact, the well-known ASM-HEMT compact model [36] also utilizes the averaging gate and drain voltage to linearly modify the threshold voltage and access resistance to capture the trap effects. As will be shown in the following sections, the proposed model predicts small and large signal characteristics with satisfying accuracy. Thus we believe this

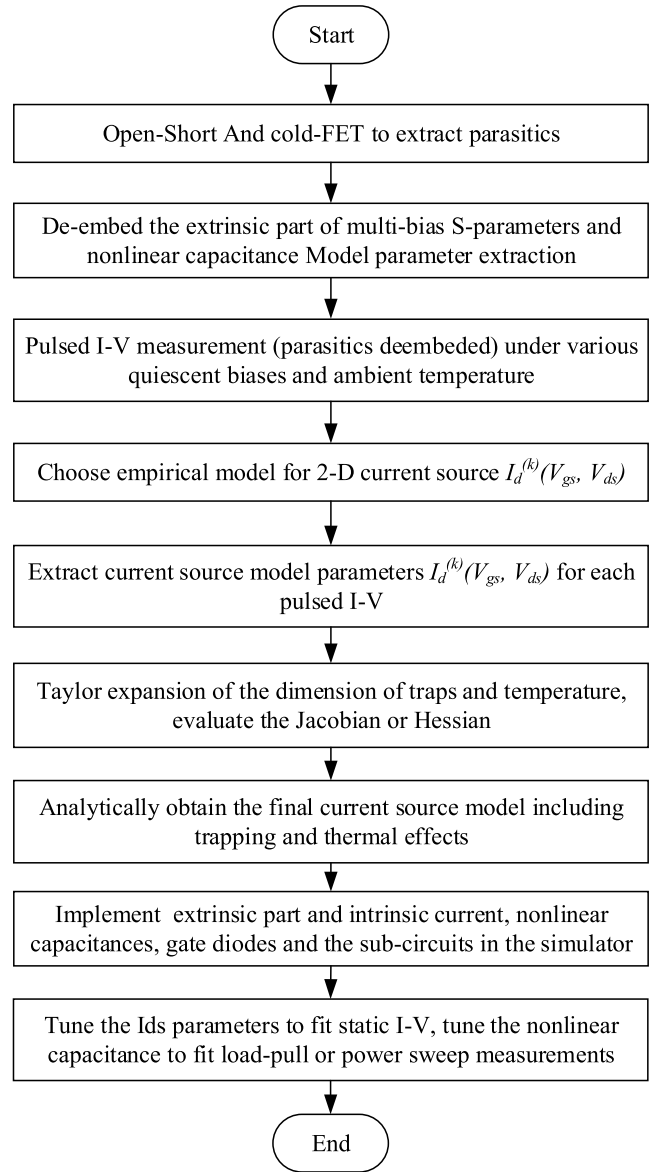


FIGURE 3. Design flow for the large signal model development of GaN HEMTs.

approximation does not introduce much error for GaN HEMT device modelling.

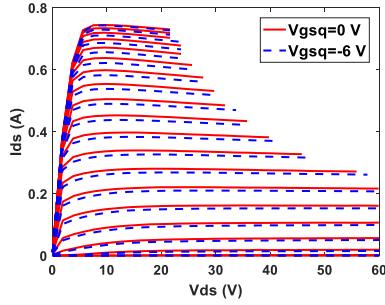
Let us denote  $\mathbf{p} = (V_{gs}, V_{ds})$  and  $\mathbf{q} = (\phi_D, T_j)$ , then the drain current source can be expressed as

$$I_d(V_{gs}, V_{ds}, \phi_D, T_j) = I_d(\mathbf{p}, \mathbf{q}) \quad (6)$$

Here  $I_d(\mathbf{p}, \mathbf{q})$  is approximated by its first order expansion for simplicity, which is given by

$$I_d(\mathbf{p}, \mathbf{q}) \approx I_d(\mathbf{p}, \mathbf{q}_0) + \nabla I_d(\mathbf{p}, \mathbf{q})|_{\mathbf{q}=\mathbf{q}_0} \cdot (\mathbf{q} - \mathbf{q}_0)^T \quad (7)$$

For a given dispersion state  $\mathbf{q}_k = (\phi_D^{(k)}, T_j^{(k)})$ , the current source is expressed as  $I_d(\mathbf{p}, \mathbf{q}_k)$ . For convenience, let us denote  $I_d^{(k)}(\mathbf{p}) = I_d(\mathbf{p}, \mathbf{q}_k)$ ,  $\mathbf{J}_{I_d} = \nabla I_d(\mathbf{p}, \mathbf{q})|_{\mathbf{q}=\mathbf{q}_0}$ ,



**FIGURE 4.** Comparison of measured pulsed I-V with different quiescent biases of  $V_{gsq} = 0\text{ V}$ ,  $V_{dsq} = 0\text{ V}$  and  $V_{gsq} = -6\text{ V}$ ,  $V_{dsq} = 0\text{ V}$ , with  $V_{gs}$  from  $-2.75\text{ V}$  to  $2\text{ V}$ .

by substituting  $I_d^{(k)}(\mathbf{p})$  into (7), we have

$$I_d^{(k)}(\mathbf{p}) \approx I_d^{(0)}(\mathbf{p}) + \mathbf{J}_{Id} \cdot (\mathbf{q}_k - \mathbf{q}_0)^T, \quad k = 1, 2, \dots, K \quad (8)$$

Rearrange (8) as

$$\mathbf{A} \cdot \mathbf{J}_{Id}^T = \mathbf{b} \quad (9)$$

where

$$\mathbf{A} = \begin{bmatrix} \mathbf{q}_1 - \mathbf{q}_0 \\ \mathbf{q}_2 - \mathbf{q}_0 \\ \vdots \\ \mathbf{q}_K - \mathbf{q}_0 \end{bmatrix} = \begin{bmatrix} (\phi_D^{(1)} - \phi_D^{(0)}) & (T_j^{(1)} - T_j^{(0)}) \\ (\phi_D^{(2)} - \phi_D^{(0)}) & (T_j^{(2)} - T_j^{(0)}) \\ \vdots & \vdots \\ (\phi_D^{(K)} - \phi_D^{(0)}) & (T_j^{(K)} - T_j^{(0)}) \end{bmatrix} \quad (10)$$

$$\mathbf{b} = \begin{bmatrix} I_d^{(1)}(\mathbf{p}) - I_d^{(0)}(\mathbf{p}) \\ I_d^{(2)}(\mathbf{p}) - I_d^{(0)}(\mathbf{p}) \\ \vdots \\ I_d^{(K)}(\mathbf{p}) - I_d^{(0)}(\mathbf{p}) \end{bmatrix} \quad (11)$$

Then the Jacobian  $\mathbf{J}_{Id}$  can be determined from (9) uniquely. Here we will show the solution in two cases:

- 1) The number of equations is equal to the number of variables to be determined, i.e.  $K = \dim(\mathbf{b}) = \dim(\mathbf{J}_{Id})$

In this case, the Jacobian  $\mathbf{J}_{Id}$  is given by

$$\mathbf{J}_{Id}^T = \mathbf{A}^{-1} \cdot \mathbf{b} \quad (12)$$

- 2) The number of equations is larger than the number of variables to be determined, i.e.  $K = \dim(\mathbf{b}) > \dim(\mathbf{J}_{Id})$ . In this case, the Jacobian  $\mathbf{J}_{Id}$  can be solved by regression in the sense of least-square, and it is given by

$$\mathbf{J}_{Id}^T = (\mathbf{A}^T \mathbf{A})^{-1} \mathbf{A}^T \cdot \mathbf{b} \quad (13)$$

The Jacobian will be the linear combination of  $I_d^{(k)}(\mathbf{p})$ , while  $I_d^{(k)}(\mathbf{p}) = I_d^{(k)}(V_{gs}, V_{ds})$  is the I-V characteristics with frozen dispersion state  $\mathbf{q}_k = (\phi_D^{(k)}, T_j^{(k)})$ , which can be obtained from narrow pulsed I-V measurement, and further fitted by empirical or other well-defined analytical functions.

**TABLE 2.** Measurement setup for pulse I-Vs.

PIVs	$V_{GSQ}$ (V)	$V_{DSQ}$ (V)	$T_{amb}$ (°C)	$P_{diss}$ (W)	$\phi_D$ (V)	$T_j$ (°C)
$I_d^{(0)}$	-3	0	25	0	$\phi_D^{(0)} = 0$	$T_j^{(0)} = 25$
$I_d^{(1)}$	-3	48	25	0	$\phi_D^{(1)} = 48$	$T_j^{(1)} = 25$
$I_d^{(2)}$	-3	48	125	0	$\phi_D^{(2)} = 48$	$T_j^{(2)} = 125$

Given any new terminal voltages and dispersion states, the I-V response will be simulated from (7).

Generally, the first order approximation given by (7) is enough for most applications. However, if dispersions exhibit strong nonlinearity over the interested region, then higher-order approximation should be utilized, and the detailed theory is given in the appendix.

## B. PULSE I-V MEASUREMENT AND DRAIN CURRENT SOURCE MODEL

Since the dimension ( $\mathbf{q} = [\phi_D, T_j]$ ) to be expanded is 2 in our case, it requires at least 3 pulsed I-V datasets to determine the quiescent expansion point as well as the Jacobian. The detailed measurement setup for PIVs are listed in Table 2.

In Table 2,  $V_{GSQ}$  and  $V_{DSQ}$  are the corresponding quiescent gate and drain bias for PIVs;  $P_{diss}$  is the quiescent dissipated power, which is 0 for the three PIVs since they are all biased at pinch off region;  $T_{amb}$  is the ambient temperature;  $\phi_D$  is the drain trap state, which can approximately identified as the quiescent drain bias as indicated in (4); the channel temperature  $T_j$  which includes ambient temperature and self-heating effects is evaluated by (5).

By substituting the information of PIVs in Table 2 to (8)-(11), we obtain

$$\mathbf{A} = \begin{bmatrix} (\phi_D^{(1)} - \phi_D^{(0)}) & (T_j^{(1)} - T_j^{(0)}) \\ (\phi_D^{(2)} - \phi_D^{(0)}) & (T_j^{(2)} - T_j^{(0)}) \end{bmatrix} = \begin{bmatrix} 48 & 0 \\ 48 & 100 \end{bmatrix} \quad (14)$$

$$\mathbf{b} = \begin{bmatrix} I_d^{(1)} - I_d^{(0)} \\ I_d^{(2)} - I_d^{(0)} \end{bmatrix} \quad (15)$$

The Jacobian is easy to be evaluated by substituting (14) and (15) into (12), and it is given by

$$\mathbf{J}_{Id}^T = \begin{bmatrix} F_D \\ F_T \end{bmatrix} = \mathbf{A}^{-1} \cdot \mathbf{b} = \begin{bmatrix} \frac{1}{48} & 0 \\ -\frac{1}{100} & \frac{1}{100} \end{bmatrix} \cdot \begin{bmatrix} I_d^{(1)} - I_d^{(0)} \\ I_d^{(2)} - I_d^{(0)} \end{bmatrix} \quad (16)$$

The Jacobian can be further expressed as

$$F_D(\mathbf{p}) = F_D(V_{gs}, V_{ds}) = \frac{1}{48} \cdot (I_d^{(1)} - I_d^{(0)}) \quad (17)$$

$$F_T(\mathbf{p}) = F_T(V_{gs}, V_{ds}) = \frac{1}{100} \cdot (I_d^{(2)} - I_d^{(1)}) \quad (18)$$

The final drain current source model can be obtained by substituting the Jacobian (16)-(18) to (7)

$$\begin{aligned}
 I_d(V_{gs}, V_{ds}, \phi_D, T_j) &= I_d(\mathbf{p}, \mathbf{q}_0) + \mathbf{J}_{Id} \cdot (\mathbf{q} - \mathbf{q}_0)^T \\
 &= I_d^{(0)} + [F_D \ F_T] \cdot [\phi_D - \phi_D^{(0)} \ T_j - T_j^{(0)}]^T \quad (19)
 \end{aligned}$$

With the information of  $\mathbf{q}_0 = (\phi_D^{(0)}, T_j^{(0)})$  in Table 2, (19) can be rearranged as

$$\begin{aligned}
 I_d(V_{gs}, V_{ds}, \phi_D, T_j) &= I_d^{(0)} + \frac{1}{48} \cdot (I_d^{(1)} - I_d^{(0)}) (\phi_D - 0) \\
 &\quad + \frac{1}{100} (I_d^{(2)} - I_d^{(1)}) (T_j - 25) \quad (20)
 \end{aligned}$$

At this stage, no optimization is involved, and the next step is to utilize empirical function to individually fit each pulsed I-V dataset  $I_d^{(k)}(V_{gs}, V_{ds})$ . For III-V FETs, the empirical function can be Angelov [2], EEHEMT [37], or Fager Model [38], [39]. In this work, a 10-parameter Angelov model is used for simple demonstration [2]

$$I_d^{(k)}(V_{gs}, V_{ds}) = I_{pk} \cdot [1 + \tanh(\sinh(\psi))] \cdot \tanh(\alpha V_{ds}) \quad (21)$$

$$\varphi = P_{1m} (V_{gs} - V_{pk}) + \sum_{n=2}^3 P_n (V_{gs} - V_{pk})^n \quad (22)$$

$$P_{1m} = P_1 (1 + B_1 / \cosh(B_2 \cdot V_{ds})) \quad (23)$$

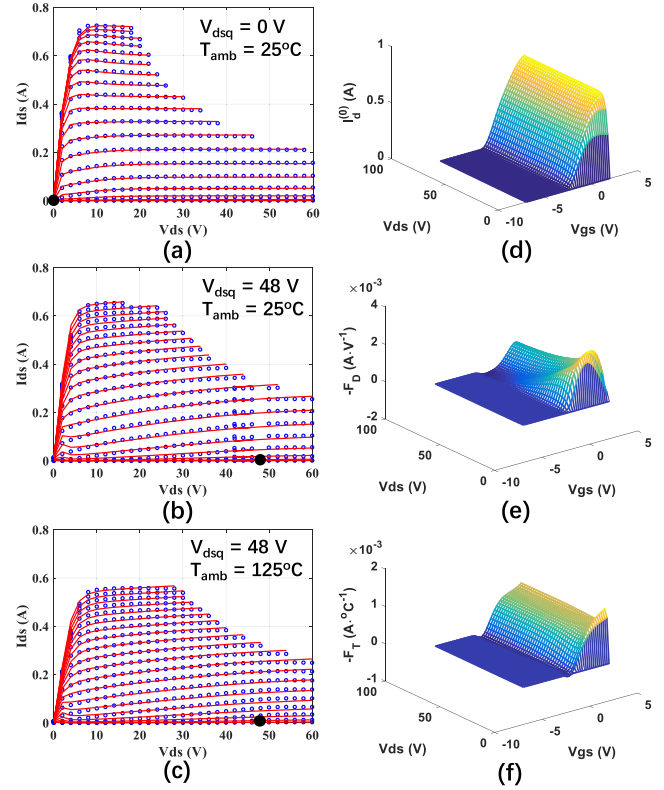
$$V_{pk} = V_{pks} + D_{vpks} (\tanh(\alpha_s \cdot V_{ds}) - 1) \quad (24)$$

$$\alpha = \alpha_r + \alpha_s (1 + \tanh(\psi)) \quad (25)$$

The optimized parameters for all  $I_d^{(k)}(V_{gs}, V_{ds})$  are given in Table 5 in the Appendix. Fig.5 (a)-(c) shows the measured and fitted three pulsed I-Vs  $I_d^{(k)}(V_{gs}, V_{ds})$ . The solid black circle represents the quiescent bias for each pulsed I-V, and they are all biased at pinch off region to avoid self-heating. By comparing Fig.5 (a) and Fig.5 (b), it is easy to conclude that the trap level increases as the drain quiescent bias increases. From Fig.5 (b) and Fig.5 (c), it is also clear to see the current collapse due to the thermal effects. Fig.5 (d)-(f) shows the mesh of expansion point  $I_d^{(0)}$ , trap coefficient  $F_D$  and thermal coefficient  $F_T$  with  $V_{gs}$  from  $-7$  V to  $2$  V,  $V_{ds}$  from  $0$  V to  $80$  V.

The physical meaning of dispersion coefficients can be interpreted as the degree of the current collapse due to the dispersion effects. Due to the well defined empirical function of  $I_d^{(k)}$ , these dispersion related coefficients exhibit expecting behaviour within or even beyond measurement range.

Though dispersion modeling of GaN HEMT using Taylor expansion was proposed by previous work [40], the Jacobian and Hessian matrices are stored as look up tables or artificial neural networks. As is known to us, one of the major problems for table or neural based approaches is that the model may be unpredictable beyond measurement region, especially when the devices are driven to the region of high power, or the region below cut off, where the values for look-up tables are



**FIGURE 5.** (a)-(c) show the comparison of measured (solid lines) and predicted (symbols) pulsed I-Vs ( $I_d^{(k)}$ ), with  $V_{gs}$  from  $-3$  V to  $1.5$  V, step of  $0.25$  V, and  $V_{ds}$  from  $0$  V to  $60$  V, step of  $2$  V: (a)  $I_d^{(0)}$ ,  $V_{GSQ} = -3$  V,  $V_{DSQ} = 0$  V,  $T_{amb} = 25^\circ\text{C}$ ; (b)  $I_d^{(1)}$ ,  $V_{GSQ} = -3$  V,  $V_{DSQ} = 48$  V,  $T_{amb} = 25^\circ\text{C}$ ; (c)  $I_d^{(3)}$ ,  $V_{GSQ} = -3$  V,  $V_{DSQ} = 48$  V,  $T_{amb} = 125^\circ\text{C}$ . (d)-(f) show the mesh of expansion point  $I_d^{(0)}$ , trap coefficient  $F_D$  and thermal coefficient  $F_T$  with  $V_{gs}$  from  $-7$  V to  $2$  V,  $V_{ds}$  from  $0$  V to  $80$  V.

not defined. As a result, non-convergence or non-physical simulation results will easily occur. For table based method, the high order harmonics depend on the interpolation and extrapolation algorithms used during the simulation. Finally, compared with empirical model, the neural or table based models are difficult to be tuned with load-pull or large signal time domain measurement data, which will potentially limit their industrial applications.

Substituting the information of  $I_d^{(k)}$  in Table 2 into (20), we can obtain

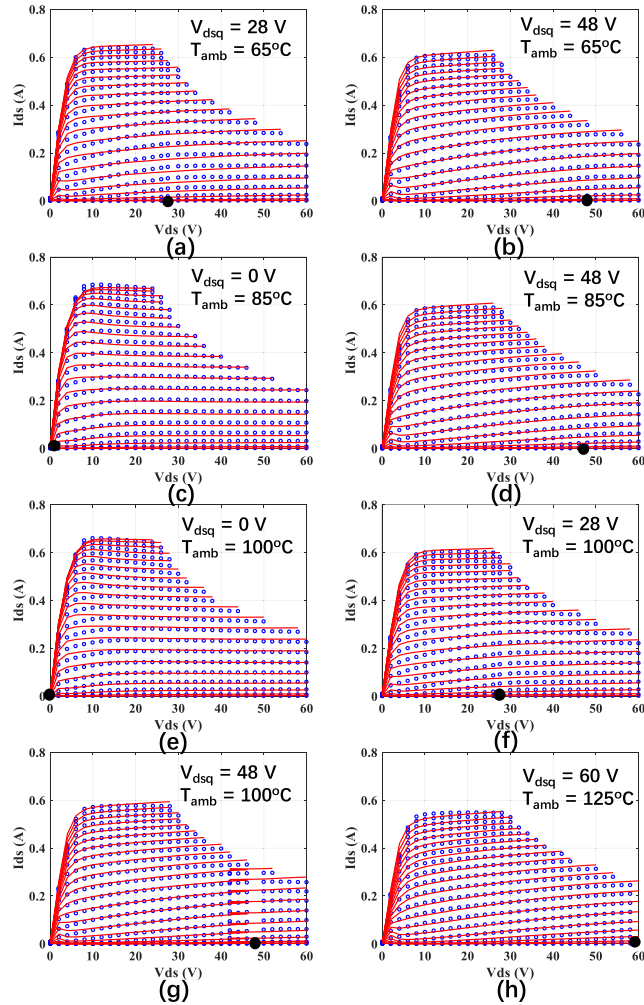
$$I_d(V_{gs}, V_{ds}, \phi_D = 0, T_j = 25) = I_d^{(0)}(V_{gs}, V_{ds}) \quad (26)$$

$$I_d(V_{gs}, V_{ds}, \phi_D = 48, T_j = 25) = I_d^{(1)}(V_{gs}, V_{ds}) \quad (27)$$

$$I_d(V_{gs}, V_{ds}, \phi_D = 48, T_j = 125) = I_d^{(2)}(V_{gs}, V_{ds}) \quad (28)$$

The results of (26)-(28) are not surprising, since those three pulsed I-Vs are exploited for the model construction, thus can be uniquely recovered. The model predictions in Fig.5 (a)-(c) are also the results simulated from the final drain current source model as presented in (20).

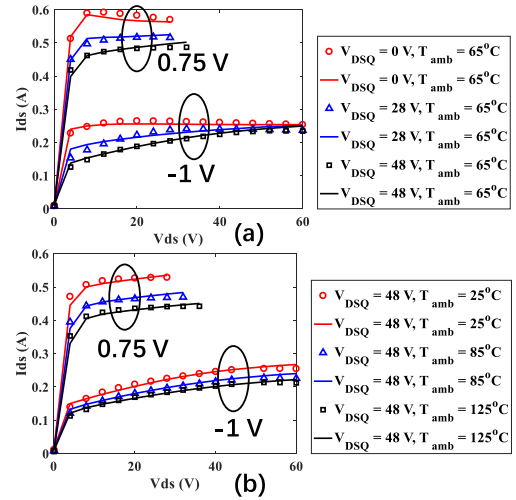
More pulsed I-Vs have been utilized to further validate our drain current source model as demonstrated in Fig.6.



**FIGURE 6.** Comparison of measured (symbols) and predicted PIVs (solid lines) by the final  $I_{ds}$  model, they are all biased at  $V_{GSQ} = -3$  V (below threshold voltage) with various quiescent drain bias and ambient temperature (a)  $V_{DSQ} = 28$  V,  $T_{amb} = 65^\circ\text{C}$ ; (b)  $V_{DSQ} = 48$  V,  $T_{amb} = 65^\circ\text{C}$ ; (c)  $V_{DSQ} = 0$  V,  $T_{amb} = 85^\circ\text{C}$ ; (d)  $V_{DSQ} = 48$  V,  $T_{amb} = 85^\circ\text{C}$ ; (e)  $V_{DSQ} = 0$  V,  $T_{amb} = 100^\circ\text{C}$ ; (f)  $V_{DSQ} = 28$  V,  $T_{amb} = 100^\circ\text{C}$ ; (g)  $V_{DSQ} = 48$  V,  $T_{amb} = 100^\circ\text{C}$ ; (h)  $V_{DSQ} = 60$  V,  $T_{amb} = 125^\circ\text{C}$  for  $V_{GS}$  from  $-2.75$  V to  $2$  V, step of  $0.25$  V,  $V_{ds}$  from  $0$  V to  $60$  V with step of  $2$  V.

By simply substituting the quiescent bias and channel temperature into (20), our model has been verified and we are able to accurately predict the drain current for various drain trap and thermal states. The pulsed I-Vs are all biased (marked as black solid circles) below threshold voltage to avoid self-heating. The channel temperature is controlled by the thermal chuck, and the trap state is controlled by quiescent drain bias. The current collapse due to drain traps can be observed by comparing Fig.6 (a)-(b), (c)-(d), and (e)-(g), while the current collapse due to thermal effects can be observed by comparing Fig.6 (b)(d)(g).

Fig.7 enables us to take a closer look on how the traps and thermal effects are correctly captured by the model. Fig.7 (a) shows the measured and simulated drain currents with the quiescent drain bias values of  $0$  V,  $28$  V and  $48$  V under the same ambient temperature of  $65^\circ\text{C}$ , and it is clear that the



**FIGURE 7.** Comparison of measured (symbols) and predicted pulsed I-Vs (solid lines) at  $V_{GSQ} = -3$  V, various quiescent drain biases and ambient temperature (a)  $V_{DSQ} = 28$  V,  $35$  V, and  $48$  V,  $T_{amb} = 25^\circ\text{C}$ ; (b)  $V_{DSQ} = 28$  V,  $T_{amb} = 25^\circ\text{C}$ ,  $85^\circ\text{C}$ , and  $125^\circ\text{C}$ ; (c)  $V_{DSQ} = 48$  V,  $T_{amb} = 25^\circ\text{C}$ ,  $65^\circ\text{C}$ , and  $125^\circ\text{C}$ ;

model is able to accurately predict the current collapse as the trap levels up. Fig.7 (b) presents the drain current under the ambient temperature of  $25^\circ\text{C}$ ,  $85^\circ\text{C}$  and  $125^\circ\text{C}$  with the same drain bias of  $48$  V. The significant current degradation due to the trap and thermal effects is accurately captured by the model, which is of great importance for the circuit design.

### C. NONLINEAR CAPACITANCE MODELLING

In this work, Angelov empirical capacitance models are utilized for simple demonstration.

#### 1) NONLINEAR GATE-SOURCE CAPACITANCE

The nonlinear gate-source capacitance is given by [2]

$$C_{gs} = C_{gsp} + C_{gs0} \cdot (1 + \tanh[\varphi_1]) (1 + \tanh[\varphi_2]) \quad (29)$$

$$\varphi_1 = P_{10} + P_{11} \cdot V_{gs} + P_{12} \cdot V_{ds} \quad (30)$$

$$\varphi_2 = P_{20} + P_{21} \cdot V_{ds} \quad (31)$$

The parameters of  $C_{gs}$  is given in the Appendix Table 6.

#### 2) NONLINEAR GATE-DRAIN CAPACITANCE

The nonlinear gate-drain capacitance is given by [2]

$$C_{gd} = C_{gdp} + C_{gd0} \cdot (1 + \tanh[\varphi_3]) \cdot (1 + \tanh[\varphi_4]) + 2P_{42} \quad (32)$$

$$\varphi_3 = P_{30} - P_{31} \cdot V_{ds} \quad (33)$$

$$\varphi_4 = P_{40} + P_{41} \cdot V_{gd} - P_{42} \cdot V_{ds} \quad (34)$$

The parameters of  $C_{gd}$  is given in the Appendix Table 7.

#### 3) NONLINEAR DRAIN-SOURCE CAPACITANCE

The Drain-source capacitance is simply modeled by

$$C_{ds} = C_{dsp} + C_{ds0} \cdot \tanh(P_{50}(V_{ds} - P_{51})) \quad (35)$$

The parameters of  $C_{ds}$  is given in the Appendix Table 8.

#### 4) CHARGE IMPLEMENTATION

With the consideration of the simulation convergence, all the nonlinear capacitances are implemented as charge sources [2]

$$Q_{gs} = \int C_{gs}(V_{gs}, V_{ds}) \cdot dV_{gs} \quad (36)$$

$$Q_{gd} = \int C_{gd}(V_{gs}, V_{gd}) \cdot dV_{gd} \quad (37)$$

$$Q_{ds} = \int C_{ds}(V_{ds}) \cdot dV_{ds} \quad (38)$$

The detailed expressions of the charges are available in [2].

#### D. GATE DIODE MODELING

The gate diodes are given by [33]

$$ID_{gd} = I_{gd0} \cdot \left( e^{k_{gd} \cdot V_{gd}} - 1 \right) \quad (39)$$

$$ID_{gs} = I_{gs0} \cdot \left( e^{k_{gs} \cdot V_{gs}} - 1 \right) \quad (40)$$

The parameters of the gate diodes are listed in the Table 9 in the Appendix.

#### IV. LARGE SIGNAL MODEL VERIFICATION

The large signal model has been implemented in Advanced Design System, and delivered to our collaborator Dynax Semi., Inc. for comprehensive verification in the form of PDK.

Due to the measurement or process uncertainty, the final large signal model has to be tuned based on the dc and RF characteristics, including continuous I-V, power sweep, load-pull contour, and so on. The following sub-section introduced the tuning procedure, and the remaining sub-sections present extensive model validations.

##### A. MODEL TUNING

The step-by-step model tuning is given by the following procedure.

##### 1) TUNE THE I-V COEFFICIENTS BASED ON STATIC I-V MEASUREMENTS

After implementing the large signal model in ADS, the parasitic resistances are slightly tuned to best fit the S-parameters, which will lead to some discrepancy of the static I-V performance, like knee voltage shift and intrinsic gate voltage shift. Thus, the model should be slightly tuned for the final application. Recall the drain current model from equation (20) here

$$I_d(V_{gs}, V_{ds}, \phi_D, T_j) = I_d^{(0)} + \frac{1}{48} \cdot \left( I_d^{(1)} - I_d^{(0)} \right) (\phi_D - 0) + \frac{1}{100} \left( I_d^{(2)} - I_d^{(1)} \right) (T_j - 25) \quad (41)$$

The static I-V are simulated based on the combination of three independent I-V expressions. Trap and thermal level will determine the portion of each I-Vs. For static I-V, the

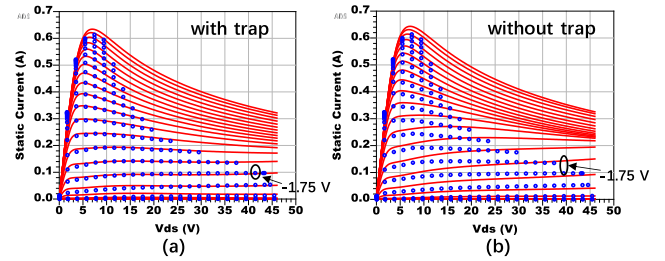


FIGURE 8. Comparison of measured (blue symbols) and simulated (red lines) static drain current with  $V_{gs}$  from -2.75 V to 2 V, step of 0.25 V,  $V_{ds}$  from 0 V to 60 V, under the ambient temperature of 25°C.

trap state equals to the drain voltage  $\phi_D = V_{ds}$ , and assuming the ambient temperature is 25°C, then (41) can be rearranged by

$$I_{DC}(V_{gs}, V_{ds}) = I_d(V_{gs}, V_{ds}, V_{ds}, 25 + P_{diss}R_{th}) = \left( 1 - \frac{V_{ds}}{48} \right) I_d^{(0)} + \left( \frac{V_{ds}}{48} - \frac{P_{diss}R_{th}}{100} \right) I_d^{(1)} + \frac{P_{diss}R_{th}}{100} I_d^{(2)} \quad (42)$$

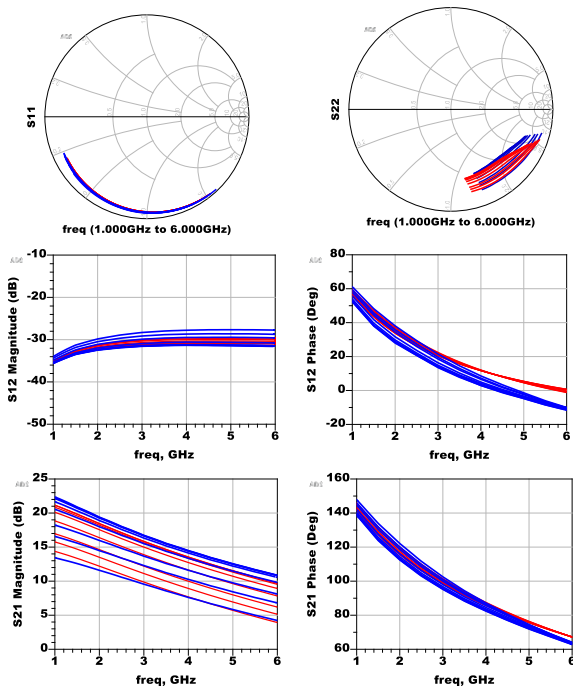
It is easy to observe that the  $I_d^{(0)}$  imposes major influence on the static current under low drain voltage, while the  $I_d^{(2)}$  mainly influences on high power region, and  $I_d^{(1)}$  imposes major influence on the high drain voltage with low gate bias region. According to the above analysis, the static I-V can be tuned efficiently. In this model, the knee voltage is be tuned by the  $\alpha_r$  in  $I_d^{(0)}$  with the final value of 0.954 compared with the initial value of 0.868. The final current is scaled with a factor of 1.05 to account for the effects of the parasitics. The rest parameters remain unchanged. Thermal resistance is tuned to be 25°C/W.

##### 2) TUNE THE NONLINEAR CAPACITANCE BASED ON POWER SWEEP AND LOAD-PULL CONTOUR

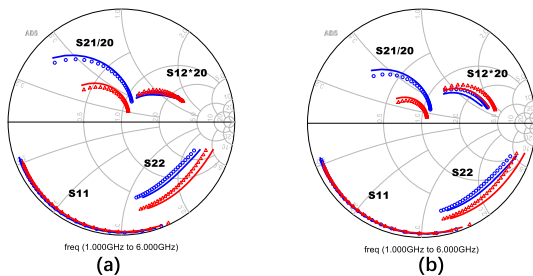
From our experience, slight tuning of the coefficient  $C_{gs0}$  in gate-source capacitance and  $C_{gd0}$  in gate-drain capacitance could achieve satisfactory results on power sweep, and by making the drain-source capacitance nonlinear, the center point for power-added efficiency contour could be improved. The final model parameters for the nonlinear capacitances are listed in the appendix.

##### B. STATIC I-V VALIDATION

As shown in Fig.8 (a), this model is able to predict the static current accurately from low to high gate bias region. In addition, the current collapse due to the self-heating is also correctly captured, which validates the proposed thermal model. In order to observe the trapping effects, the trap coefficient is set to be zero, and the static I-V overestimates the drain current without the consideration of trapping modeling, as clearly illustrated in Fig.8 (b).



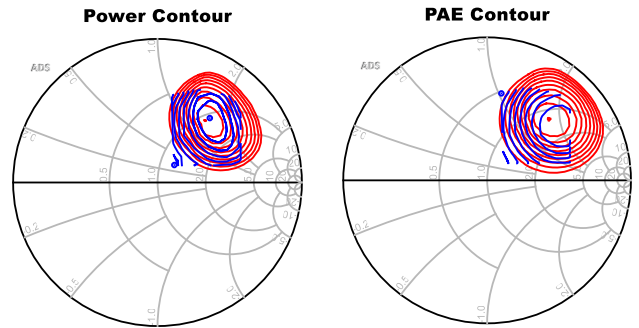
**FIGURE 9.** Comparison of measured (blue) and simulated (red) S-parameters from 1 GHz to 6 GHz under the ambient temperature of 25°C biased at  $V_{ds} = 48$  V,  $V_{gs} = -1.7$  V to  $-2.3$  V, step of 0.1 V;



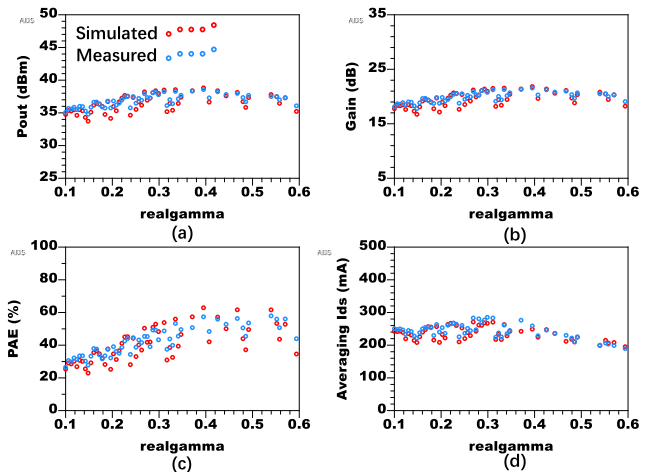
**FIGURE 10.** Measured (symbols) and simulated (lines) S-parameters from 1 GHz to 6 GHz under the ambient temperature of 25°C biased at (a)  $V_{ds} = 10$  V,  $V_{gs} = -1.5$  V (b)  $V_{ds} = 28$  V,  $V_{gs} = -2$  V, at the temperature of 25°C (blue circle), and 125°C (red triangle).

**C. SMALL-SIGNAL S-PARAMETERS VALIDATION**

S-parameter simulations of the GaN HEMT Model with the drain bias of 48 V, gate bias of  $-2.3$  V to  $1.7$  V, are performed over the frequency from 1 to 6 GHz, which agree well with the measurements as shown in Fig. 9. As small signal model is derived from the drain current source and other nonlinear capacitances, the good agreement indicates that the intrinsic nonlinear current source and capacitances are well modeled, and the parasitic extrinsic and intrinsic elements are also correctly extracted. As the application frequency of this device is relatively low, the kink effects on S22 due to the high trans-conductance is not that significant [40]. The temperature induced small signal performance variations are also accurately predicted, as shown in Fig.10. This indicates that



**FIGURE 11.** Comparison of measured (blue) and simulated (red) output power ( $P_{out}$ ) contour, and power-added efficiency (PAE) contour of class AB amplifier with the input power of 17 dBm, excitation frequency of 2.7GHz, drain bias voltage 48 V, bias current 3%  $I_{max}$  (24 mA), and ambient temperature of 25°C for the constant source reflection coefficient of  $\Gamma_S = -0.35925 + j*0.80074$ , second harmonic load reflection coefficient of  $\Gamma_{L2} = -0.04508 - j*0.02962$ , and third harmonic load coefficient of  $\Gamma_{L3} = -0.17751 + j*0.24885$ .



**FIGURE 12.** Comparison of measured (blue) and simulated (red) output power ( $P_{out}$ ), power-added efficiency (PAE), and averaging drain current of class AB amplifier against various load conditions, with the input power of 17 dBm, excitation frequency of 2.7GHz, drain bias voltage 48 V, bias current 3%  $I_{max}$  (24 mA), and ambient temperature of 25°C for the constant source reflection coefficient of  $\Gamma_S = -0.35925 + j*0.80074$ .

the temperature influence on the drain current is successfully captured in the proposed model.

**D. LOAD-PULL VALIDATION**

Fig. 11 shows the comparison of the load-pull contours of the output power and power-added efficiency. The simulated maximum output is 38.5 dBm, which is close to the measurement of 38.6 dBm, with an error of 0.28%, and the optimum load point is also well predicted. The simulated maximum power-added efficiency is 60.9%, which is also near the measurement of 58.9%, with an error of 3.4%, and the optimum load point is also around the measured one. Table 3 shows the optimal load conditions for maximum output power and power-added efficiency. This information is crucial for designing high performance power amplifiers.



TABLE 3. Optimal load found by contour.

Load-pull	Load Refl. for Max Pout	Max Pout	Load Refl. for Max PAE	Max PAE
Measured	0.5761 $\angle$ 51.1°	38.6 dBm	0.596 $\angle$ 35.4°	58.9%
Simulated	0.5565 $\angle$ 49.0°	38.5 dBm	0.632 $\angle$ 42.3°	60.9%

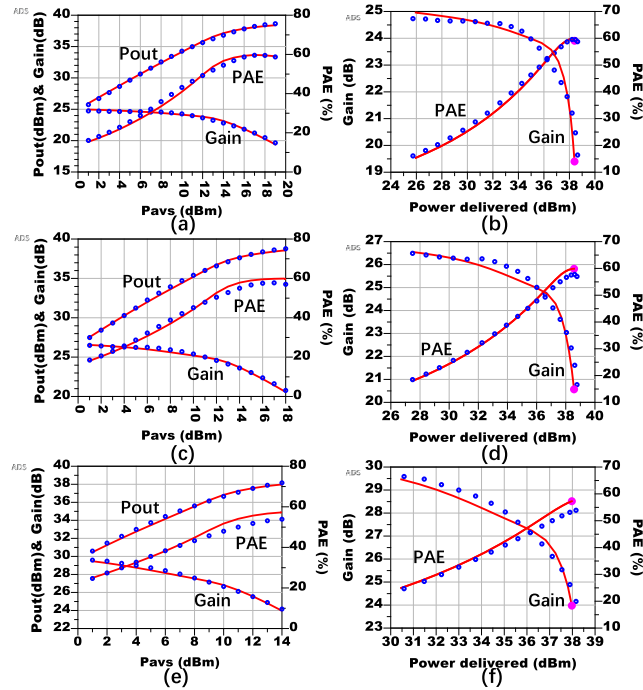


FIGURE 13. Comparison of measured (symbols) and simulated (solid lines) output power (Pout), transducer gain (Gain), and power-added efficiency (PAE) of Class AB amplifier with the excitation frequency of 2.7GHz, under ambient temperature of 25°C for (a-b)  $V_{dsq} = 48$  V,  $I_{dsq} = 21.9$  mA,  $\Gamma_S = -0.35925 + j*0.80074$ ,  $\Gamma_L = 0.48373 + j*0.35173$ , optimal PAE point; (c-d)  $V_{dsq} = 48$  V,  $I_{dsq} = 20.2$  mA,  $\Gamma_S = -0.35925 + j*0.80074$ ,  $\Gamma_L = 0.41294 + j*0.39474$ , optimal Pout point; (e-f)  $V_{dsq} = 48$  V,  $I_{dsq} = 20.3$  mA,  $\Gamma_S = -0.35925 + j*0.80074$ ,  $\Gamma_L = 0.36897 + j*0.48753$ . The pink solidlines in (b)(d)(f) are the saturated output power.

The predicted output power and power added efficiency under different loads are also in good agreement with measurement as shown in Fig. 12.

E. POWER SWEEP VALIDATION

In addition to the output power and PAE contour verification, the power sweep validation (under room temperature of 25°C) is conducted at the optimal PAE load, optimal output power load, and arbitrary load respectively. The results are presented in Fig.13. This model is able to accurately predict the gain compression up to 5 dB. The maximum absolute errors for these three output power performances are within 0.25 dB, and absolute errors of PAE are within 3% under optimal load conditions. It can be seen from Fig. 13 (b)(d)(f) that the saturated delivered power is also correctly captured, which is crucial for power amplifier design. In order

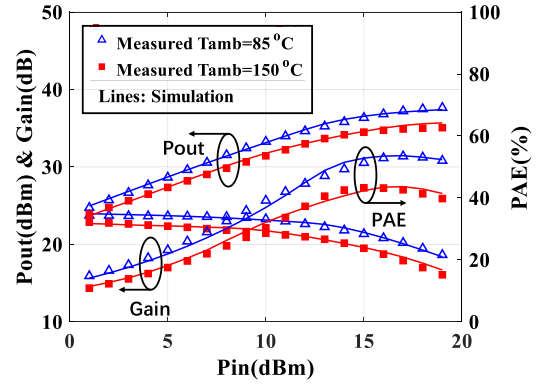


FIGURE 14. Single tone power sweep measurement (symbols) and simulations (lines) (class AB) for  $V_{dsq} = 48$  V,  $I_{dsq} = 20.2$  mA, at the optimal Pout load point, excitation frequency 2.7 GHz,  $T_{amb} = 85^\circ\text{C}$  and  $150^\circ\text{C}$ .

to verify the electro-thermal effects, the power sweep is also conducted under an ambient temperature of 85°C and 150°C. As shown in Fig. 14, the proposed model is able to predict the degradation of output power and efficiency when the temperature rises.

V. CONCLUSION

This paper presents a general dimension reduction method for the dispersion modeling for semiconductor devices. This methodology fully utilizes the existing knowledge for the device modeling by exploiting empirical or physical functions to describe the dimensions of the port voltages, and also greatly extends the ability to characterize the new dispersion effects by introducing the general Taylor expansion method. A GaN HEMT is employed as the example device to illustrate how this method can be applied to address the trap and thermal effects. The model is validated by accurately predicting the drain current under various trap and thermal states, and also the large signal characteristics including load-pull contour, power sweep, and so on. This approach is applicable to both current and charge source dispersion modeling, and can be conveniently adapted for various semiconductor devices including FETs, LDMOS, and HBTs, etc. (an extra example of dispersion modeling of LDMOS is given in the Appendix), which is valuable for both academic research and industry application.

ACKNOWLEDGMENT

The authors wish to thank Dynax Semi. Inc., for providing the GaN HEMT devices for investigation.

APPENDIX

A. SECOND-ORDER APPROXIMATION OF DIMENSION REDUCTION METHOD

Although Section II shows the Taylor expansion up to the second order, the modeling of dispersion effects of the example device GaN HEMT only utilize first order approximation for simple demonstration. In this part, we also provide more

details for the second order approximation. Recall that

$$f(\mathbf{p}, \mathbf{q}) \approx f(\mathbf{p}, \mathbf{q}_0) + \nabla f(\mathbf{p}, \mathbf{q})|_{\mathbf{q}=\mathbf{q}_0} \cdot (\mathbf{q} - \mathbf{q}_0)^T + \frac{1}{2} (\mathbf{q} - \mathbf{q}_0) \cdot \mathbf{H}_f(\mathbf{p}, \mathbf{q})|_{\mathbf{q}=\mathbf{q}_0} \cdot (\mathbf{q} - \mathbf{q}_0)^T \quad (43)$$

Let us denote  $\mathbf{J}_f = \nabla f(\mathbf{p}, \mathbf{q})|_{\mathbf{q}=\mathbf{q}_0}$ ,  $\mathbf{H}_f = \mathbf{H}_f(\mathbf{p}, \mathbf{q})|_{\mathbf{q}=\mathbf{q}_0}$ . The dimension of  $\mathbf{J}_f$  is  $1 \times M$ , while the dimension of  $\mathbf{H}_f$  is  $M \times M$ . Including the quiescent expansion point, there requires at least  $1 + M + M^2$  frozen dispersion states  $\mathbf{q}_k$ , which is too much for the realistic application. However, if we assume that the dispersion variables are independent from or not correlated to each other, then the Hessian matrix can be reduced to a diagonal matrix

$$\mathbf{H}_f \approx \begin{bmatrix} h_{11} & 0 & \cdots & 0 \\ 0 & h_{22} & & 0 \\ \vdots & \ddots & \ddots & \vdots \\ 0 & 0 & \cdots & h_{MM} \end{bmatrix} = \text{diag}(h_{11}, h_{22}, \dots, h_{MM}) \quad (44)$$

The total variables to be determined is reduced to  $1 + 2M$ . For the dimensions which shows strong linearity, the corresponding diagonal value of the Hessian can be set to be 0. The procedure to calculate the Jacobian and Hessian are similar to the one described in Section III.

### B. DIMENSION REDUCTION METHOD FOR THE DISPERSION MODELING OF LDMOS

Section III applies the dimension reduction method for the dispersion modeling of a GaN HEMT. In this sub-section, we will present one more example of the dispersion modeling of LDMOS based on second-order approximation.

The dimension of port voltage ( $V_{gs}, V_{ds}$ ) will be reserved and described by empirical function, while the dimension of channel temperature is represented by the second-order Taylor expansion:

$$I_d(\mathbf{p}, \mathbf{q}) \approx I_d(\mathbf{p}, \mathbf{q}_0) + \mathbf{J}_{Id} \cdot (\mathbf{q} - \mathbf{q}_0)^T + \frac{1}{2} (\mathbf{q} - \mathbf{q}_0) \cdot \mathbf{H}_{Id} \cdot (\mathbf{q} - \mathbf{q}_0)^T \quad (45)$$

where  $\mathbf{p} = (V_{gs}, V_{ds})$ ,  $\mathbf{q} = T_j$ .  $\mathbf{J}_{Id}$  and  $\mathbf{H}_{Id}$  are Jacobian and Hessian with the dimension of 1 by 1.

It requires at least 3 different dispersion states  $\mathbf{q}_k = T_j^{(k)}$  to obtain the expansion point, Jacobian and Hessian. Recall the notation  $I_d^{(k)}(\mathbf{p}) = I_d(\mathbf{p}, \mathbf{q}_k)$  as shown in Section III-A. By substituting  $I_d^{(k)}(\mathbf{p})$  into (45), we have

$$I_d^{(k)}(\mathbf{p}) \approx I_d^{(0)}(\mathbf{p}) + \mathbf{J}_{Id} \cdot (T_j^{(k)} - T_j^{(0)}) + \frac{\mathbf{H}_{Id}}{2} (T_j^{(k)} - T_j^{(0)})^2 \quad k = 1, 2, \dots, K \quad (46)$$

Rearrange (46) as

$$\mathbf{A} \cdot [\mathbf{J}_{Id}, \mathbf{H}_{Id}]^T = \mathbf{b} \quad (47)$$

where

$$\mathbf{A} = \begin{bmatrix} (T_j^{(1)} - T_j^{(0)}) & 0.5 \cdot (T_j^{(1)} - T_j^{(0)})^2 \\ (T_j^{(2)} - T_j^{(0)}) & 0.5 \cdot (T_j^{(2)} - T_j^{(0)})^2 \\ \vdots & \vdots \\ (T_j^{(K)} - T_j^{(0)}) & 0.5 \cdot (T_j^{(K)} - T_j^{(0)})^2 \end{bmatrix} \quad (48)$$

$$\mathbf{b} = \begin{bmatrix} I_d^{(1)}(\mathbf{p}) - I_d^{(0)}(\mathbf{p}) \\ I_d^{(2)}(\mathbf{p}) - I_d^{(0)}(\mathbf{p}) \\ \vdots \\ I_d^{(K)}(\mathbf{p}) - I_d^{(0)}(\mathbf{p}) \end{bmatrix} \quad (49)$$

Then the Jacobian and Hessian matrices can be determined from (47) uniquely. Here we will show the solution in two cases:

- 1) The number of equations is equal to the number of variables to be determined, i.e.  $K = \text{dim}(\mathbf{b}) = \text{dim}([\mathbf{J}_{Id}, \mathbf{H}_{Id}]) = 2$

In this case, the solution is given by

$$[\mathbf{J}_{Id}, \mathbf{H}_{Id}]^T = \mathbf{A}^{-1} \cdot \mathbf{b} \quad (50)$$

- 2) The number of equations is larger than the number of variables to be determined, i.e.  $K = \text{dim}(\mathbf{b}) > \text{dim}([\mathbf{J}_{Id}, \mathbf{H}_{Id}]) = 2$

In this case, the solution can be solved by regression in the sense of least square, and it is given by

$$[\mathbf{J}_{Id}, \mathbf{H}_{Id}]^T = (\mathbf{A}^T \mathbf{A})^{-1} \mathbf{A}^T \cdot \mathbf{b} \quad (51)$$

The Jacobian and Hessian matrices will be the linear combination of  $I_d^{(k)}(\mathbf{p})$ , while  $I_d^{(k)}(\mathbf{p}) = I_d^{(k)}(V_{gs}, V_{ds})$  is the I-V characteristic with frozen dispersion state  $\mathbf{q}_k = T_j^{(k)}$ , which can be obtained from narrow pulsed I-V measurement, and further fitted by empirical or other well-defined analytical functions (see [38], [42]). Given any new terminal voltages and channel temperature, the I-V response will be simulated from (45).

To fully validate the generality of the proposed dimension reduction technique, a commercial device of Ericsson's RF LDMOSFET PTF10107 is employed for model verification. The terminal voltage dependence is described by a simple 9-parameter equation, which is given by [42]

$$V_{sat} = V_{gs} - S_c \cdot \ln\left(\frac{V_{gs} - S_v}{S_c}\right) \quad (52)$$

$$V_T = T_v + \theta \cdot V_{ds} \quad (53)$$

$$V_{eff} = V_{sat} - V_T \quad (54)$$

$$V_{gm} = \frac{T_c}{2} \cdot \ln\left[1 + \exp\left(\frac{2 \cdot V_{eff}}{T_c}\right)\right] \quad (55)$$

$$\alpha_H = \alpha \cdot [1 - \tanh(\gamma \cdot V_{eff})] \quad (56)$$

$$I_d^{(k)}(V_{gs}, V_{ds}) = \beta \cdot V_{gm} \cdot \tanh(\alpha_H \cdot V_{ds}) \cdot (1 + \lambda \cdot V_{ds}) \quad (57)$$

Short pulse I-Vs under temperature of 34°C ( $T_j^{(0)}$ ), 74°C ( $T_j^{(1)}$ ) and 114°C ( $T_j^{(2)}$ ) are utilized for electro-thermal model

TABLE 4. Parameters of parasitics.

$C_{pg}$ (fF)	$C_{pd}$ (fF)	$L_g$ (pH)	$L_d$ (pH)	$L_s$ (pH)	$R_g$ ( $\Omega$ )	$R_d$ ( $\Omega$ )	$R_s$ ( $\Omega$ )
87.9	62.7	74.5	61.2	0.92	0.9431	2.2559	0.524

TABLE 5. Model parameters of drain current of GaN HEMT.

	$\alpha_r$	$\alpha_s$	$V_{pks}$	$D_{vpks}$	$P_1$
$I_d^{(0)}$	0.86756	-0.296	-0.6468	-0.048699	0.55661
$I_d^{(1)}$	0.4311	-0.0238	0.9922	0.6312	0.3955
$I_d^{(2)}$	0.3297	-0.020119	1.0626	0.70527	0.41696
	$B_1$	$B_2$	$P_2$	$P_3$	$I_{pk}$
$I_d^{(0)}$	0.28306	0.17388	-0.077045	0.034755	0.37099
$I_d^{(1)}$	-1.0932	-0.020119	1.0626	0.0214	0.4260
$I_d^{(2)}$	-1.0402	0.79214	-0.062245	0.015098	0.34518

TABLE 6. Parameters for cgs (pF) model.

$C_{gsp}$	$C_{gs0}$	$P_{10}$	$P_{11}$	$P_{12}$	$P_{20}$	$P_{21}$
0.91201	0.18765	4.7852	2.1986	0.00792	1.1497	0.0525

TABLE 7. Parameters for Cgd (pF) model.

$C_{gdp}$	$C_{gd0}$	$P_{30}$	$P_{31}$	$P_{40}$	$P_{41}$	$P_{42}$
0.03165	0.2848	-1.2446	0.0693	0.2586	1.359	0.1222

TABLE 8. Parameters for Cds (pF) model.

$C_{dsp}$	$C_{ds0}$	$P_{50}$	$P_{50}$
0.278	8.238	2.54E-4	32

TABLE 9. Parameters for gate current (A).

$I_{gs0}$	$k_{gs}$	$I_{gd0}$	$k_{gd}$
3.1E-3	1.2E-6	3.4E-7	5.1

construction, and the corresponding notation for I-Vs are  $I_d^{(0)}(\mathbf{p})$ ,  $I_d^{(1)}(\mathbf{p})$  and  $I_d^{(2)}(\mathbf{p})$  respectively.

According to equation (48)-(49), we have

$$A = \begin{bmatrix} (T_j^{(1)} - T_j^{(0)}) & 0.5 \cdot (T_j^{(1)} - T_j^{(0)})^2 \\ (T_j^{(2)} - T_j^{(0)}) & 0.5 \cdot (T_j^{(2)} - T_j^{(0)})^2 \end{bmatrix} = \begin{bmatrix} 40 & 800 \\ 80 & 3200 \end{bmatrix} \quad (58)$$

$$\mathbf{b} = \begin{bmatrix} I_d^{(1)}(\mathbf{p}) - I_d^{(0)}(\mathbf{p}) \\ I_d^{(2)}(\mathbf{p}) - I_d^{(0)}(\mathbf{p}) \end{bmatrix} \quad (59)$$

The Jacobian and Hessian matrices are given by

$$\begin{bmatrix} J_{Id} \\ H_{Id} \end{bmatrix} = A^{-1} \cdot \mathbf{b} = \begin{bmatrix} \frac{1}{20} & -\frac{1}{80} \\ -\frac{1}{80} & \frac{1}{1600} \end{bmatrix} \cdot \begin{bmatrix} I_d^{(1)}(\mathbf{p}) - I_d^{(0)}(\mathbf{p}) \\ I_d^{(2)}(\mathbf{p}) - I_d^{(0)}(\mathbf{p}) \end{bmatrix} \quad (60)$$

TABLE 10. Model parameters of drain current of LDMOSFET.

	$S_v$	$S_c$	$T_v$	$T_c$	$\theta$
$I_d^{(0)}$	-20.27	8.28	-20.67	0.041	0.0004
$I_d^{(1)}$	-15.87	6.62	-16.17	0.0395	0.0005
$I_d^{(2)}$	-18.71	7.24	-19	0.0352	0.0004
	$\alpha$	$\gamma$	$\lambda$	$\beta$	
$I_d^{(0)}$	1.04	5.38	0.013	8.4	
$I_d^{(1)}$	0.8514	5.29	0.0149	8.4	
$I_d^{(2)}$	0.8567	5.94	0.0138	8.4	

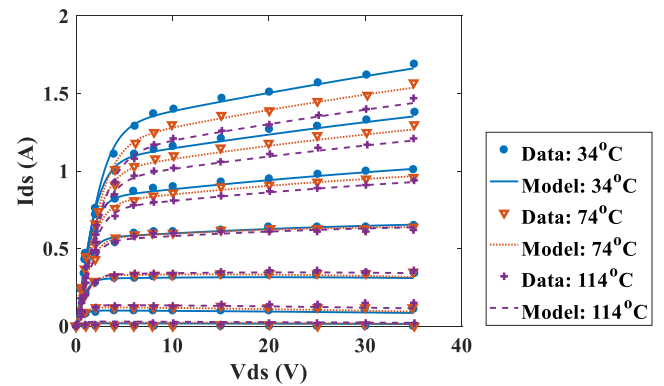


FIGURE 15. Measured and modeled pulsed I-Vs of commercial Ericsson's RF LDMOSFET PTF10107 under ambient temperature of 34°C, 74°C, and 114°C.

Equation (60) can be rearranged as

$$J_{Id} = -\frac{3}{80} I_d^{(0)} + \frac{1}{20} \cdot I_d^{(1)} - \frac{1}{80} \cdot I_d^{(2)} \quad (61)$$

$$H_{Id} = \frac{1}{1600} I_d^{(0)} - \frac{1}{800} \cdot I_d^{(1)} + \frac{1}{1600} \cdot I_d^{(2)} \quad (62)$$

With the Jacobian and Hessian, the final drain current model with temperature dependence is obtained

$$I_d(V_{gs}, V_{ds}, T_j) \approx I_d^{(0)} + J_{Id} \cdot (T_j - 34) + \frac{H_{Id}}{2} (T_j - 34)^2 \quad (63)$$

The final step for the current expression is to individually fit the I-V parameters for pulsed I-Vs ( $I_d^{(k)}$ ), and the parameters are given in the appendix Table 10. This model is demonstrated to accurately predict the pulsed I-Vs under various temperature, as indicated in Fig. 15.

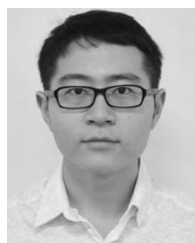
### C. MODEL PARAMETERS

See Tables 4–10.

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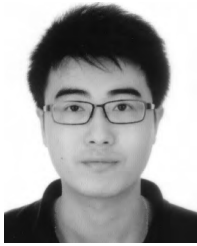
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