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# Phase Current Reconstruction for the Grid-Side Converter With Four-Switch Three-Phase Topology in a DFIG-WT

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**ABSTRACT** To increase the reliability of a doubly fed induction generator-based wind turbine (DFIG-WT), this paper proposes a fault-tolerant four-switch three-phase (FSTP) grid-side converter (GSC) with a phase current reconstruction strategy. The proposed strategy is effective when the semiconductor open-circuit fault and phase current sensor failure occur simultaneously, which is a kind of hybrid fault. Only one current sensor is applied for measuring the currents flowing between the ac and dc sides of the GSC, and the phase current information can be derived by combining this information with the switching states of FSTP GSC. In the proposed current reconstruction strategy, only two scenarios of duty ratio allocation are needed to be considered. In addition, the space vector pulsewidth modulation (SVPWM) technique is simplified by obtaining the unified expressions for the duty ratios for the remaining four switches in GSC, and the sector identification is removed. Besides, the voltage balancing on the dc bus is achieved. Furthermore, the limitation of the proposed current reconstruction strategy is presented, and the dead zones for SVPWM techniques in both six-switch three-phase and FSTP converters are analyzed. Simulations are carried out in MATLAB/Simulink to verify the proposed hybrid fault-tolerant strategy for the GSC in a 1.5-MW DFIG-WT.

**INDEX TERMS** Reliability, doubly-fed induction generator-based wind turbine, grid-side converter, four-switch three-phase, phase current reconstruction, space vector pulse width modulation.

## NOMENCLATURE

| | |
|---|---|
| $V, I, \phi$ | Constant values of voltage, current and flux |
| $v, i, \varphi$ | Instant values of voltage, current and flux |
| $V_{dc}, V_{ref}$ | DC-link voltage and reference voltage value |
| $V_m$ | Amplitudes of the three-phase voltages |
| $e$ | Instant values of voltage supply |
| $\Delta$ | Difference |
| $R_g, R_s, R_r$ | Resistances on the grid, stator and rotor |
| $L_m, L_{ls}, L_{lr}$ | Mutual inductance, stator leakage inductance and rotor leakage inductance |
| $L_g, L_s, L_r$ | Inductances on the grid, stator and rotor ($L_s = L_m + L_{ls}$; $L_r = L_m + L_{lr}$) |
| $\sigma$ | Leakage flux factor: $\sigma = 1 - [L_m L_m/(L_r L_s)]$ |
| $P, Q, PF$ | Active, reactive power and power factor |
| $d$ | Duty ratio |
| $f_{NOM}$ | Nominal grid frequency |
| $\theta_s, \theta_r$ | Grid voltage angle and rotor angle |
| $\omega_s, \omega_{slip}, \omega_r, \omega_m$ | Nominal grid angular frequency, slip angular frequency, electrical rotor angular speed and mechanical rotor angular speed |
| $T_s, T_{sw}$ | Sampling time and switching time |
| $k_p, k_i$ | Proportional and integral controller gains |

### SUBSCRIPTS & SUPERSCRIPTS

| | |
|---|---|
| *s, r, t* | Stator, rotor and total values |
| *g* | grid-side converter side value |
| *a, b, c* | Phases A, B, C |
| *A, B, C* | Points A, B, C |
| $C1$, $C2$ | Upper and lower DC-link capacitor |
| $dc1$, $dc2$ | Upper and lower capacitor related values |
| *avg* | Average value |
| $\alpha$, $\beta$ | Direct and quadrature components referred to the stationary reference frame |
| *d, q* | Direct and quadrature components referred to the synchrnous reference frame |
| $'$ | Reconstructed value |
| *_ref* | Reference value |
| *_ref*1 | Transient DC reference value |
| $*$ | Ideal value |

## I. INTRODUCTION

Doubly-fed induction generators (DFIGs) are widely applied in large-scale wind turbines due to their superiority in terms of the variable speed constant frequency (VSCF) operation, four-quadrant power regulation, and small volumes of the back-to-back power electronic converters [1]–[3]. The voltage sensors can be removed by applying stator or rotor flux orientation method in the vector control process [4]. In addition, many researchers made significant contributions to position sensorless control in DFIG [5]–[8]. However, few literatures focused on the solutions to current sensor failure in DFIG. In order to obtain the values of the three-phase currents through either the grid-side converter (GSC) or rotor-side converter (RSC), at least two phase current sensors are required. Besides, a DC-link current sensor is needed for protection purpose. According to [9], the sensors in wind turbines are prone to fail at the late stage of service time. When current sensor failure occurs, it is possible to obtain the reconstructed phase current values by using a single DC-link current sensor and the switching states of the semiconductor switches.

The method of measuring the phase currents by utilizing only one DC-link current sensor was first proposed in [10]. The main idea is calculating the three-phase currents by utilizing the sampled DC-link current values in specific switching states. However, dead zones are inevitable since minimum switch-on time has to be met, which is the sum of the signal settling time, the conversion time for analog/digital (A/D) converter, the turn-on time of switch, and the dead zone time between the two switching devices in the same bridge arm [11]. The measuring points are missing when the action time for corresponding active voltage vectors is not enough, which may result in erroneous phase current waveforms.

In the single current sensor based phase current reconstruction scheme, the sampling frequency is restricted by the frequency of PWM signals, and the phase current information can only be deduced from the DC link when nonzero switching states are presented [12]. Therefore, when the durations of nonzero states are too short, immeasurable regions will be induced. In [13] and [14], a switching state phase shift method is applied to ensure that the action time for each nonzero switching state in a specific switching period is long enough for current sampling. However, unsymmetrical PWM waveforms are created, which deteriorates the current quality, increases the switching losses and audible noise, and the regions of overmodulation are enlarged. As an alternative, additional measurement voltage vectors with the same amplitude can be inserted in a switching period [15]. However, the area for synthesizing the reference voltage vector in the space vector pulse width modulation (SVPWM) technique shrinks. In addition, the phase currents can be reconstructed based on current prediction strategies [16], [17]. Nevertheless, additional calculation is required, and the sampling of current still fails in the extremely low voltage region. A hybrid PWM technique was proposed in [18] to optimize the overall performance. However, the algorithm becomes complex by applying this technique. Moreover, in [19] an independent phase current reconstruction method without using null switching states was proposed, but the SVPWM strategy is complex. Furthermore, the severe sensor failure scenario was investigated in [20] for a late-stage DFIG wind turbine (DFIG-WT). Apart from the aforementioned approaches, overmodulation method [21], tri-state PWM (TSPWM) [22], double high-frequency (DHF) pulses injection method [23], and zero voltage vector sampling method (ZVVSM) [11], [24], [25] are also applied in the single DC-link sensor based phase current reconstruction strategy.

However, all these phase current reconstruction methods are carried out with the precondition that all the switches in the converters work in normal states. As is presented in [26], the semiconductor power devices are considered as the most fragile component in a power electronic converter. At the late stage of service time for DFIG-WTs, breakdown of switches in the back-to-back converters is likely to occur. With the consideration of minimizing the number of switching devices, the fault-tolerant topology with DC bus midpoint connection [27]–[29] is adopted in this paper, as only four switches are needed. This four-switch three-phase (FSTP) topology has been researched in the applications such as induction machines (IMs) [30], brushless DC (BLDC) machines [31], and permanent magnet synchronous machines (PMSMs) [32]. Besides, the operation of DFIG-WT with power switch open-circuit fault was evaluated in [33] and [34].

In this paper, the current sensor failure and semiconductor switch open circuit are simultaneously taken into consideration for a post-fault DFIG-WT. A simplified SVPWM strategy [35] is applied to remove sector identification, and a DC-bus voltage difference suppression scheme is proposed. The validation of the proposed current reconstruction method is demonstrated in an FSTP GSC based DFIG-WT.

This paper is organized as follows: In Section II, the proposed current reconstruction method in an FSTP GSC is

illustrated by the circuit structure and the relationship between the measured and actual phase current values. The proposed SVPWM technique in FSTP GSC is explained in Section III. In Section IV, the immeasurable regions are analysed for both SSTP and FSTP converters. The proposed control strategy is illuminated in Section V. In Section VI, simulations are conducted in Matlab/Simulink to demonstrate the validity of the proposed strategy. Finally the conclusions are drawn in Section VII.

## II. PROPOSED PHASE CURRENT RECONSTRUCTION SCHEME IN FSTP GSC

### A. THE CIRCUIT STRUCTURE

Since the semiconductor power switches and current sensors are prone to failure at the late stage of service time for DFIG-WT, a hybrid fault tolerant strategy by integrating FSTP topology based GSC and single DC-link current sensor based phase current reconstruction method is proposed in this paper to further enhance the reliability of DFIG-WT. The proposed phase current reconstruction scheme in FSTP GSC is illustrated in Figure. 1.

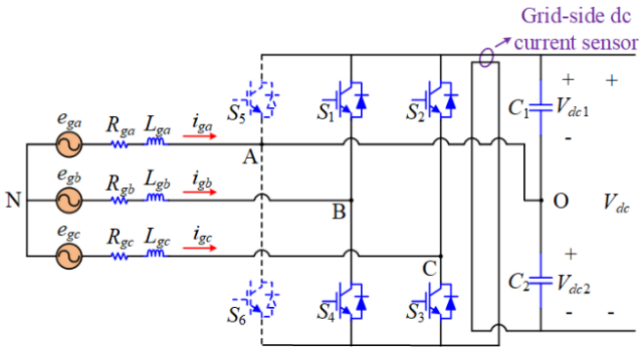


**FIGURE 1.** Proposed phase current reconstruction scheme for FSTP GSC.

In Figure. 1, only one DC-link current sensor is applied to capture the information of the current flowing from the GSC to the DC bus, and the positive directions of three-phase grid currents are defined as shown in this figure, representing the subsynchronous operational mode of DFIG. In this paper balanced three-phase grid voltages are considered, and the resistances $R_{ga} = R_{gb} = R_{gc} = R$, and the inductances $L_{ga} = L_{gb} = L_{gc} = L$. Assuming that the switch $S_5$ or $S_6$ breaks down and an open circuit is formed in the corresponding bridge arm, phase $A$ is directly connected to the DC-bus midpoint O. The DC-link capacitors used have the same capacitance ($C_1 = C_2 = C_{DC}$) and the initial voltages on these two capacitors are assumed to be the same ($V_{dc1} = V_{dc2} = 0.5V_{dc}$). Since three-phase star connection without neutral line is the most common connection method, the current value in the faulty phase can be derived when the information of the current values in the other two phases are available.

$$i_{ga} + i_{gb} + i_{gc} = 0 \tag{1}$$

The switching variables $S_b$ and $S_c$ are defined in this paper to identify the switching states of the two switches in the two healthy bridge arms. When $S_b = 1$, $S_1$ is on and $S_4$ is off; when $S_b = 0$, $S_1$ is off and $S_4$ is on. The situation is the same for $S_c$ when refer to the switching states of $S_2$ and $S_3$. Apart from the open-circuit fault in GSC, phase current sensor failure is also taken into account, and the values of phase currents through GSC are derived by using the information of the current flowing into the DC bus and the switching states of the four switches in GSC. The equivalent circuits for the FSTP GSC with the proposed current sampling method are displayed in Figure. 2 for all the switching states.

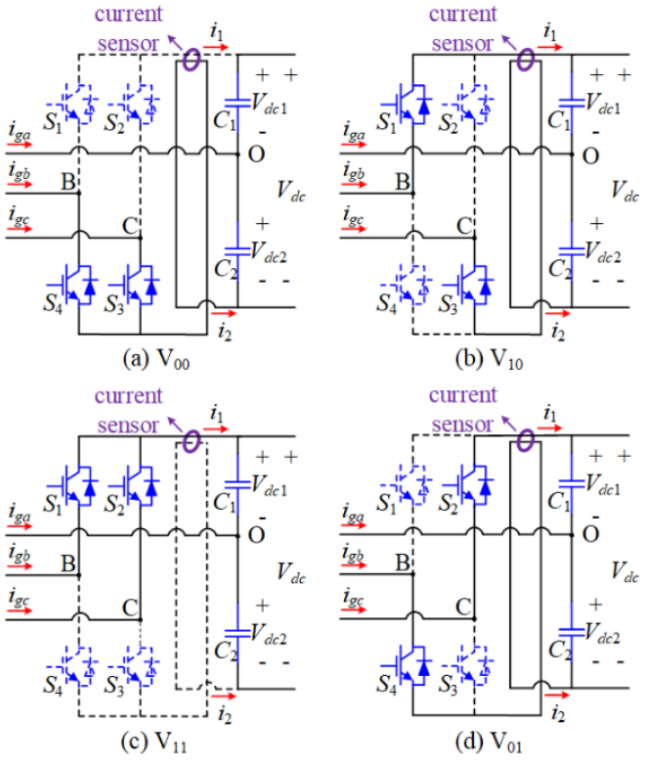


**FIGURE 2.** Proposed phase current reconstruction scheme for FSTP GSC.

Different from a six-switch three-phase (SSTP) converter, there are only four switching states in an FSTP one, and no zero voltage vector is intrinsically available. The subscripts denote the values for $S_b$ and $S_c$ respectively. For example, $V_{00}$ represents the situation that $S_b = S_c = 0$.

### B. RELATIONSHIP BETWEEN THE SAMPLED CURRENTS AND PHASE CURRENTS

In the proposed strategy, the difference between the currents $i_1$ and $i_2$ as shown in Figure. 2 are used for reconstructing the three-phase currents, because in this way the information of grid currents in all the three phases can be obtained. By sampling the values of $(i_1 - i_2)$ in various switching states during a switching period $T_{sw}$, the three-phase currents can be calculated. The values of $(i_1 - i_2)$ sampled in different switching states can be obtained according to Kirchhoff's current law, and the results can be obtained as

shown in TABLE 1. In this paper, the switching signals for the four switches are generated by comparing the duty ratios in the two healthy bridge arms with the triangular carrier frequency. The duty ratios are defined as $d_b$ and $d_c$, denoting the ratio of switch-on time of the upper power switch in the corresponding bridge arm to the switching period. Two cases are to be considered, which are $d_b > d_c$ and $d_b < d_c$, and the switching states applied in these two cases are different. When $d_b = d_c$, current sampling dead zones are formed, which will be discussed in detail in Section IV. The switching patterns for FSTP converter are shown in Figure. 3, with the sampling points of the current difference $(i_1 - i_2)$ identified.

**TABLE 1. Values of the measured currents in different switching states.**

| $(S_b, S_c)$ | Switching state | $i_1$ | $i_2$ | $i_1 - i_2$ |
|---|---|---|---|---|
| (0, 0) | $V_{00}$ | 0 | $-i_{ga}$ | $i_{ga}$ |
| (1, 0) | $V_{10}$ | $i_{gb}$ | $i_{gc}$ | $i_{gb} - i_{gc}$ |
| (1, 1) | $V_{11}$ | $-i_{ga}$ | 0 | $-i_{ga}$ |
| (0, 1) | $V_{01}$ | $i_{gc}$ | $i_{gb}$ | $i_{gc} - i_{gb}$ |

From Figure. 3, it can be seen that in a switching period five points are selected for current measurement. The current in phase A can either be obtained by sampling the current difference $(i_1 - i_2)$ when the value of carrier signal equals 1 or 0. $d_{avg}$ denotes the average value of $d_b$ and $d_c$, which can be expressed as

$$d_{avg} = (d_b + d_c)/2 \tag{2}$$

By comparing $d_{avg}$ with the carrier signal, the sampling points in the middle of $V_{10}$ or $V_{01}$ can be determined.

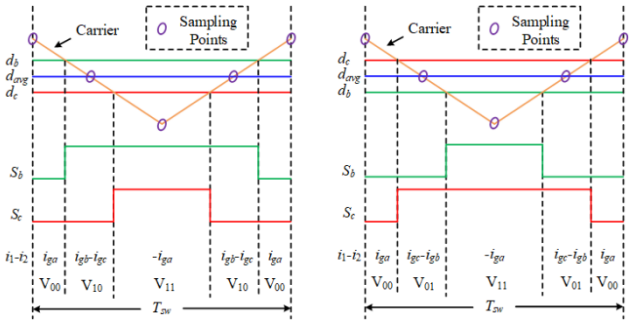


**FIGURE 3. Switching patterns for FSTP converter.**

## III. PROPOSED MODULATION TECHNIQUE OF FSTP GSC

In most cases SVPWM technique is employed to synthesize the reference voltage vector and form a circular locus in the two-dimensional space. In a conventional SSTP converter, there are eight switching states, with six active voltage vectors and two zero vectors, and the plane is divided into six sectors. In such a case, the reference voltage vector is synthesized by distributing reasonable action time for the two adjacent basic voltage vectors and the two zero vectors. However, in an FSTP converter, only four switching states are left and none of them is zero switching state. Therefore, the remaining inactive time in a switching period has to be fulfilled by adjusting the action time in the vectors with opposite components so that equivalent zero voltage vectors can be generated. The space vector diagram in an FSTP converter is illustrated in Figure. 4.

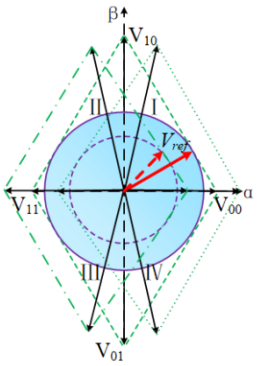


**FIGURE 4. Space vector distribution for an FSTP converter.**

When the upper and lower capacitor voltages are equal, the maximum DC-bus voltage utilization rate is obtained, and the larger circle indicates the range the reference voltage vector can reach. However, even under this situation, the utilization rate of DC-bus voltage is only half of that in the SSTP case. Once the upper and lower capacitor voltages have different values, the area of the circle becomes smaller, and the region defined by dash-dot lines ($V_{dc1} > V_{dc2}$) and that defined by dot lines ($V_{dc1} < V_{dc2}$) are presented. The relationship between the three-phase grid voltages and the DC-link capacitor voltages can be derived as shown in TABLE 2. The relationship can be summarized by the following equations.

$$\begin{cases} v_A = \dfrac{1}{3}V_{dc1}(-S_b - S_c) + \dfrac{1}{3}V_{dc2}(2 - S_b - S_c) \\ v_B = \dfrac{1}{3}V_{dc1}(2S_b - S_c) + \dfrac{1}{3}V_{dc2}(2S_b - S_c - 1) \\ v_C = \dfrac{1}{3}V_{dc1}(2S_c - S_b) + \dfrac{1}{3}V_{dc2}(2S_c - S_b - 1) \end{cases} \tag{3}$$

In order to minimize the conduction and switching losses, only three out of four switching states are utilized for synthesizing the reference voltage vector in a specific switching period. According to [35], when the two small basic voltage

**TABLE 2. Values of the measured currents in different switching states.**

| | $v_A$ | $v_B$ | $v_C$ | $v_\alpha$ | $v_\beta$ |
|---|---|---|---|---|---|
| $V_{00}$ | $\frac{2V_{dc2}}{3}$ | $-\frac{V_{dc2}}{3}$ | $-\frac{V_{dc2}}{3}$ | $\frac{2V_{dc2}}{3}$ | 0 |
| $V_{10}$ | $\frac{V_{dc2}-V_{dc1}}{3}$ | $\frac{2V_{dc1}+V_{dc2}}{3}$ | $-\frac{V_{dc1}+2V_{dc2}}{3}$ | $\frac{V_{dc2}-V_{dc1}}{3}$ | $\frac{V_{dc1}+V_{dc2}}{\sqrt{3}}$ |
| $V_{11}$ | $-\frac{2V_{dc1}}{3}$ | $\frac{V_{dc1}}{3}$ | $\frac{V_{dc1}}{3}$ | $-\frac{2V_{dc1}}{3}$ | 0 |
| $V_{01}$ | $\frac{V_{dc2}-V_{dc1}}{3}$ | $-\frac{V_{dc1}+2V_{dc2}}{3}$ | $\frac{2V_{dc1}+V_{dc2}}{3}$ | $\frac{V_{dc2}-V_{dc1}}{3}$ | $\frac{V_{dc1}+V_{dc2}}{\sqrt{3}}$ |

vectors are utilized for producing the equivalent zero voltage vector, minimized current ripples can be obtained. Therefore, in this paper only $V_{00}$ and $V_{11}$ are employed for equivalent zero voltage generation. Taking the case when the reference voltage vector is located in Sector I, the switching states $V_{00}$, $V_{10}$ and $V_{11}$ are employed. Based on the deduction processes in [35], the corresponding duty ratios are $d_{00}$, $d_{10}$ and $d_{11}$ are derived as

$$\begin{cases} d_{00} = \dfrac{V_{dc1} + v_{A\_ref} - v_{B\_ref}}{V_{dc}} \\ d_{10} = \dfrac{v_{B\_ref} - v_{C\_ref}}{V_{dc}} \\ d_{11} = \dfrac{V_{dc2} + v_{C\_ref} - v_{A\_ref}}{V_{dc}} \end{cases} \tag{4}$$

The ideal three-phase voltage reference values can also be expressed as shown below.

$$\begin{cases} {v_{A\_ref}}^* = V_m \cos(\theta_s) \\ {v_{B\_ref}}^* = V_m \cos(\theta_s - \dfrac{2\pi}{3}) \\ {v_{C\_ref}}^* = V_m \cos(\theta_s + \dfrac{2\pi}{3}) \end{cases} \tag{5}$$

Based on (4), the duty ratios $d_b$ and $d_c$ can be calculated as

$$\begin{cases} d_b = d_{10} + d_{11} = \dfrac{V_{dc2} + v_{B\_ref} - v_{A\_ref}}{V_{dc}} \\ d_c = d_{11} = \dfrac{V_{dc2} + v_{C\_ref} - v_{A\_ref}}{V_{dc}} \end{cases} \tag{6}$$

When the reference voltage vector $V_{ref}$ is located in other sectors, (6) is still applicable, which has been verified in [33] and [35]. Therefore, there is no need to identify the sector, which reduces the complexity of the algorithm. As only $d_b$ and $d_c$ are required in the procedure of obtaining the switching signals, no tedious calculation process is required.

## IV. IMMEASURABLE REGION ANALYSIS

### A. MINIMUM CURRENT SAMPLING TIME

When sampling the current values under the practical condition, a minimum period of time $T_{min}$ is required, i.e. the current measurement cannot be taken instantaneously. When a switch is activated, it takes some time to fully turn it on, which is referred as the rise time $t_r$. In addition, the dead zone time $t_d$ must be included, since short circuit in any bridge arm of GSC should be prohibited. Besides, as there is an inductance at the AC grid side of the converter in each phase, time is needed for the current to reach the desired value, which is the so called settling time $t_{set}$. Furthermore, to convert the analog signal into a digital one, the additional A/D conversion time $t_{A/D}$ is required. To sum up, the minimum current sampling time can be expressed as

$$T_{min} = t_r + t_d + t_{set} + t_{A/D} \tag{7}$$

In the proposed phase current reconstruction strategy, the current information is obtained from the instantaneous values of $(i_1 - i_2)$ at different sampling points in a switching period. When the action time for any of the switching states used for current sampling is smaller than $T_{min}$, the measurement will fail at this point and the calculation of three-phase currents can be wrong. For example, if the switch-on time for the switching state $V_{10}$ is smaller than $T_{min}$, there is no enough time for the current sensor to obtain the instantaneous value of $(i_1 - i_2)$ at this point, which is illustrated in Figure. 5(a). Assuming that $d_b$ and $d_c$ are both within the range (0, 1), the sampling points at the peaks and valleys are used for deriving the values of $i_{ga}$ and $(-i_{ga})$, respectively. However, overmodulation and undermodulation cases occur from time to time, which result in erroneous samplings for $i_{ga}$ and $(-i_{ga})$, and they are illustrated in Figures. 5(b)(c).

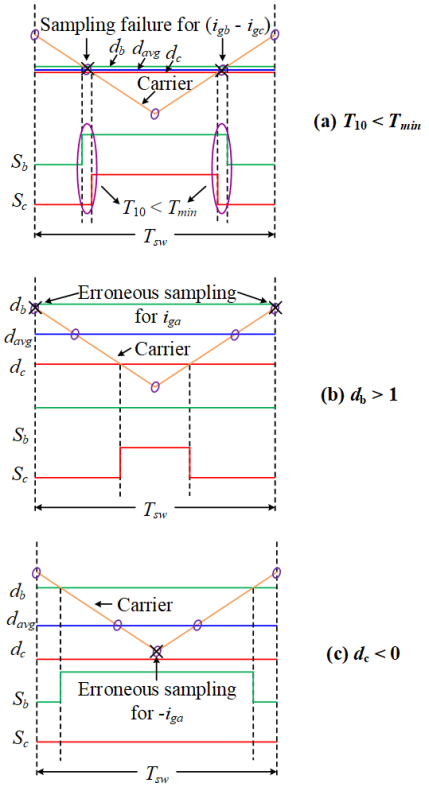


**FIGURE 5.** Problems during the current sampling process.

### B. CURRENT RECONSTRUCTION DEAD ZONES FOR SSTP AND FSTP CONVERTERS

When one of the switching states is activated for less than $T_{min}$, unsuccessful sampling of the difference between $i_1$ and $i_2$ is encountered, which happens when the reference voltage vector is near the sector boundary. Moreover, if the sampling time for two switching states is shorter than $T_{min}$, the reference voltage vector is in the low modulation region. The space vector diagrams for SSTP and FSTP converters with the current reconstruction dead zones identified are displayed in Figure. 6.

In the normal areas, current sampling can be successfully performed and correct values for three-phase currents can be

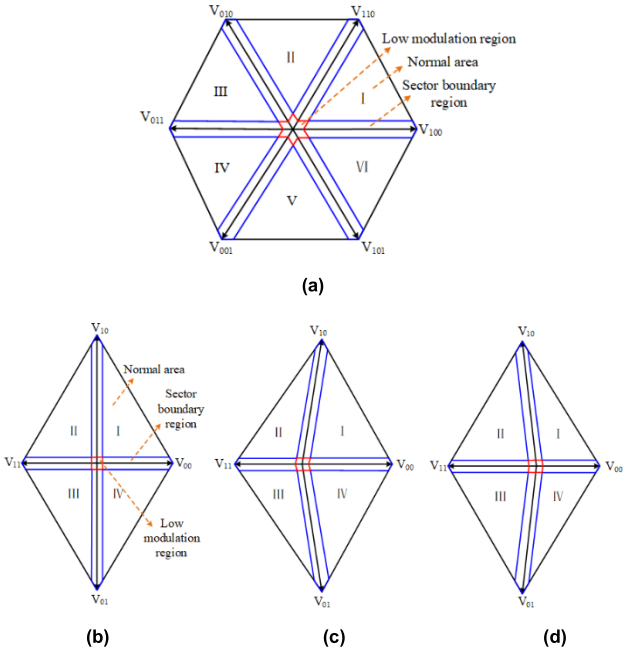


**FIGURE 6.** Current reconstruction dead zones in space vector diagrams. (a) SSTP. (b) FSTP $V_{dc1} = V_{dc2}$. (c) FSTP$V_{dc1} < V_{dc2}$. (d) FSTP $V_{dc1} > V_{dc2}$.

derived. However, when the reference voltage vector locates in the sector boundary regions or low modulation regions, sampling failure or erroneous current sampling is encountered. For SSTP converter, the sampling points can be set at the instants when zero voltage vectors are activated so that the immeasurable regions can be put outwards [11]. While for FSTP converter, the action time of the four switching states can be adjusted in order to ensure the minimum switch-on time of any of the vectors is $T_{min}$. However, the expense for both these two methods is the reduction of the utilization area of the DC-bus voltage.

## V. CONTROL OF THE PROPOSED FSTP GSC WITH ONE CURRENT SENSOR

In this paper the control of GSC is based on grid voltage oriented (GVO) vector control, since the three-phase grid voltages are assumed to be balanced and undistorted. The aim of the GSC controller is to keep a steady DC-bus voltage value, maintain high-quality sinusoidal three-phase grid currents, and obtain a unity power factor. For an FSTP GSC, the balancing of the upper and lower DC-link capacitor voltages is also required so that the maximum DC-bus voltage utilization rate can be achieved. The existence of the voltage difference between $V_{dc1}$ and $V_{dc2}$ is related to the currents flowing through the DC-bus midpoint, i.e., $i_{ga}$, $i_{C1}$ and $i_{C2}$.

The relationship among these currents can be derived according to Kirchhoff's current law as shown below.

$$i_{ga} = i_{C2} - i_{C1} \tag{8}$$

The currents $i_{C1}$ and $i_{C2}$ can also be expressed by

$$\begin{cases} i_{C1} = C_{DC}\dfrac{dV_{dc1}}{dt} \\ i_{C2} = C_{DC}\dfrac{dV_{dc2}}{dt} \end{cases} \tag{9}$$

Substitute (9) into (8), the current $i_{ga}$ is derived as

$$i_{ga} = C_{DC}\left(\frac{dV_{dc2}}{dt} - \frac{dV_{dc1}}{dt}\right) \tag{10}$$

By integrating both sides of (10), the expression for the DC-link voltage difference can be obtained as shown below.

$$\begin{aligned} \Delta V_{dc} &= V_{dc2} - V_{dc1} \\ &= \frac{1}{C_{DC}}\left[\int i_{ga} + V_{dc2}(0) - V_{dc1}(0)\right] \end{aligned} \tag{11}$$

In (11), $V_{dc1}(0)$ and $V_{dc2}(0)$ are the initial values for the upper and lower DC-link capacitor voltages, respectively. It can be seen that the voltage deviation is caused by the initial voltage offset and the integration of $i_{ga}$. The main idea of the DC-bus voltage deviation suppression control is to eliminate the effect induced by the instantaneous DC component of $i_{ga}$, and the control algorithm is displayed in Figure. 7.

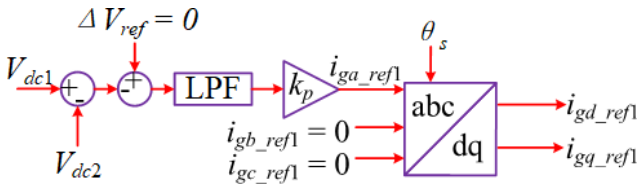


**FIGURE 7.** DC-bus voltage deviation suppression control.

In the proposed control strategy, a low-pass filter (LPF) is applied to remove the high-frequency components in the input signal, and a proportional controller is used for generating the compensation component in phase A.

The overall structure of the FSTP GSC control system can be divided into the outer voltage loop and inner current loop, which is shown in Figure. 8.

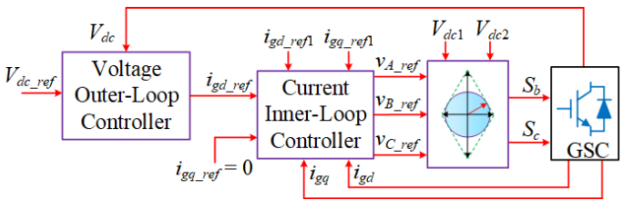


**FIGURE 8.** Dual-loop FSTP GSC control algorithm.

The $dq$ voltages on the AC side of GSC can be expressed by the following equations based on GVO vector control.

$$\begin{cases} v_{gscd} = e_{gd} - R_g i_{gd} - L_g\dfrac{di_{gd}}{dt} + \omega_s L_g i_{gq} \\ v_{gscq} = -R_g i_{gq} - L_g\dfrac{di_{gq}}{dt} - \omega_s L_g i_{gd} \end{cases} \tag{12}$$

Taking $i_{gd\_ref1}$ and $i_{gq\_ref1}$ into consideration, which are the $dq$ compensating current components derived in the

DC-link capacitor voltage deviation suppression control process, the design of grid-side current controllers can be achieved and expressed by

$$\begin{cases} L_g \dfrac{di_{gd}}{dt} = L_g \dfrac{di_{gd\_ref1}}{dt} + k_{pd}(i_{gd\_ref} + i_{gd\_ref1} - i_{gd}) \\ \qquad\qquad + k_{id} \displaystyle\int (i_{gd\_ref} + i_{gd\_ref1} - i_{gd})dt \\ L_g \dfrac{di_{gq}}{dt} = L_g \dfrac{di_{gq\_ref1}}{dt} + k_{pq}(i_{gq\_ref} + i_{gq\_ref1} - i_{gq}) \\ \qquad\qquad + k_{iq} \displaystyle\int (i_{gq\_ref} + i_{gq\_ref1} - i_{gq})dt \end{cases} \tag{13}$$

According to (12) and (13), the overall control system of the proposed FSTP GSC with phase current reconstruction scheme by using one current sensor is derived as illustrated in Figure. 9.

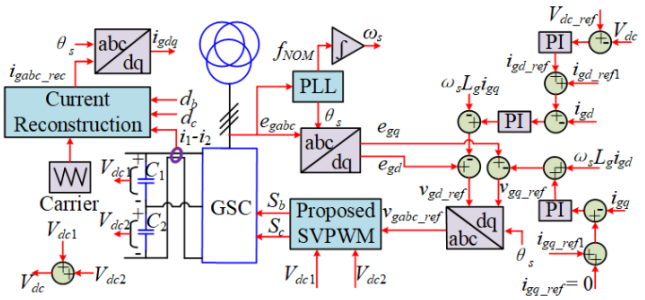


**FIGURE 9.** Control block diagram for FSTP GSC with phase current reconstruction.

In the proposed phase current reconstruction strategy, the sampled values of $(i_1 - i_2)$ can be obtained as $i_{ga}$ at $V_{00}$, $(-i_{ga})$ at $V_{11}$, $(i_{gb} - i_{gc})$ at $V_{10}$, and $(i_{gc} - i_{gb})$ at $V_{01}$. In order to avoid the erroneous current sampling when overmodulation occurs, the reconstructed phase A current $i'_{ga}$ is updated in the switching state $V_{11}$. If $d_b > d_c$, the reconstructed three-phase GSC side currents $i'_{gabc}$ in a switching period can be obtained as

$$\begin{cases} i'_{ga} = -(i_1 - i_2)V_{11} \\ i'_{gb} = 0.5 * [(i_1 - i_2)V_{10} + (i_1 - i_2)V_{11}] \\ i'_{gc} = 0.5 * [-(i_1 - i_2)V_{10} + (i_1 - i_2)V_{11}] \end{cases} \tag{14}$$

If $d_b < d_c$, $i'_{gabc}$ can be calculated as

$$\begin{cases} i'_{ga} = -(i_1 - i_2)V_{11} \\ i'_{gb} = 0.5 * [-(i_1 - i_2)V_{01} + (i_1 - i_2)V_{11}] \\ i'_{gc} = 0.5 * [(i_1 - i_2)V_{01} + (i_1 - i_2)V_{11}] \end{cases} \tag{15}$$

where

$$\begin{cases} (i_1 - i_2)V_{11} = -i_{ga} \\ (i_1 - i_2)V_{10} = i_{gb} - i_{gc} \\ (i_1 - i_2)V_{01} = i_{gc} - i_{gb} \end{cases} \tag{16}$$

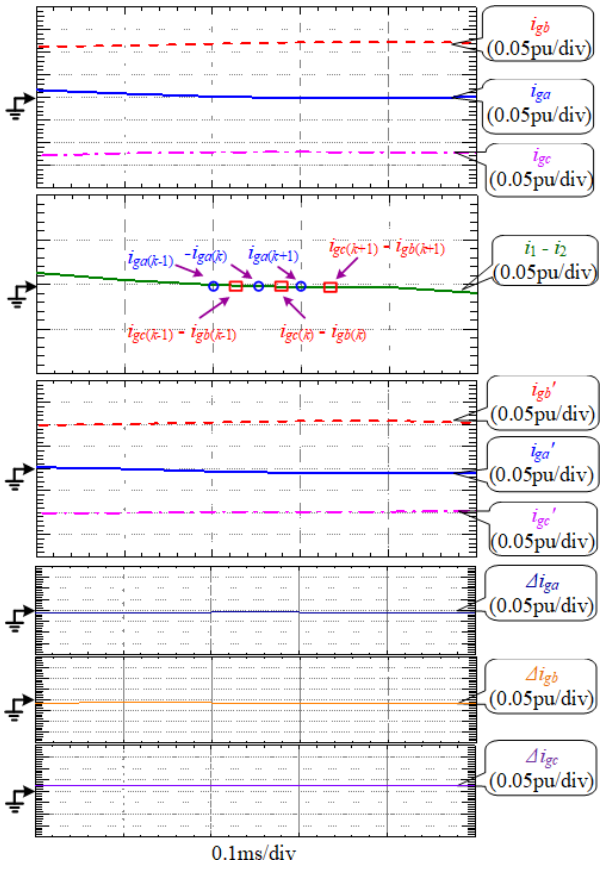


**FIGURE 10.** The actual three-phase GSC AC currents $i_{gabc}$, current difference between $i_1$ and $i_2(i_1 - i_2)$, the reconstructed GSC currents $i'_{gabc}$, and the three-phase current differences $\Delta i_{gabc}$ in the region of high wind speed (15m/s).

## VI. SIMULATION RESULTS

The proposed current reconstruction strategy in FSTP GSC for a 1.5MW DFIG-WT is verified in Matlab/Simulink. The initial rotor speed of DFIG is 1.2pu, and the wind speed drops from 15m/s to 8m/s at 1s. The sampling time is set as 5$\mu$s, and the system parameters are listed in TABLE 3.

In the region of high wind speed (15m/s), the values of $i_{gabc}$, $(i_1 - i_2)$, $i'_{gabc}$, and $\Delta i_{gabc}$ are displayed in Figure. 10. Similarly, the waveforms for the corresponding variables in the region of low wind speed (8m/s) are shown in Figure. 11.

From Figure. 10 and Figure. 11, it can be seen that the differences between the real three-phase GSC currents $i_{gabc}$ and the reconstructed ones $i'_{gabc}$ are all limited within 0.03pu for both the cases of high and low wind speeds, indicating precise tracking of the real values. In one switching period, five sampled values are obtained, but the calculation of the reconstructed current values is based on $(-i_{ga})$ and $(i_{gb} - i_{gc})$ [or $(i_{gc} - i_{gb})$], as illustrated in (14) – (16).

The values of controller gains used in the simulation are shown in TABLE 4.

To evaluate the performance of FSTP GSC, the three-phase total output currents, DC-bus voltage, and the upper and lower

**TABLE 3. Parameters of DFIG-WT.**

| Parameter | Value | Unit |
|---|---|---|
| Rated Apparent Power $S_g$ | 1.5 | MVA |
| Rated Frequency $F_{nom}$ | 50 | Hz |
| Rated Stator Voltage $V_s$ | 575 | V |
| Stator Resistance $R_s$ | 0.023 | pu |
| Rotor Resistance $R_r$ | 0.016 | pu |
| Stator Leakage Inductance $L_{ls}$ | 0.18 | pu |
| Rotor Leakage Inductance $L_{lr}$ | 0.16 | pu |
| Magnetizing Inductance $L_m$ | 2.9 | pu |
| Friction Factor $F$ | 0.01 | pu |
| Inertia Constant $H$ | 0.685 | s |
| Pairs of Poles $p$ | 3 | \ |
| DC Bus Capacitor $C_{DC}$ | 10000 | μF |
| Rated Wind Speed $v_w$ | 11 | m/s |

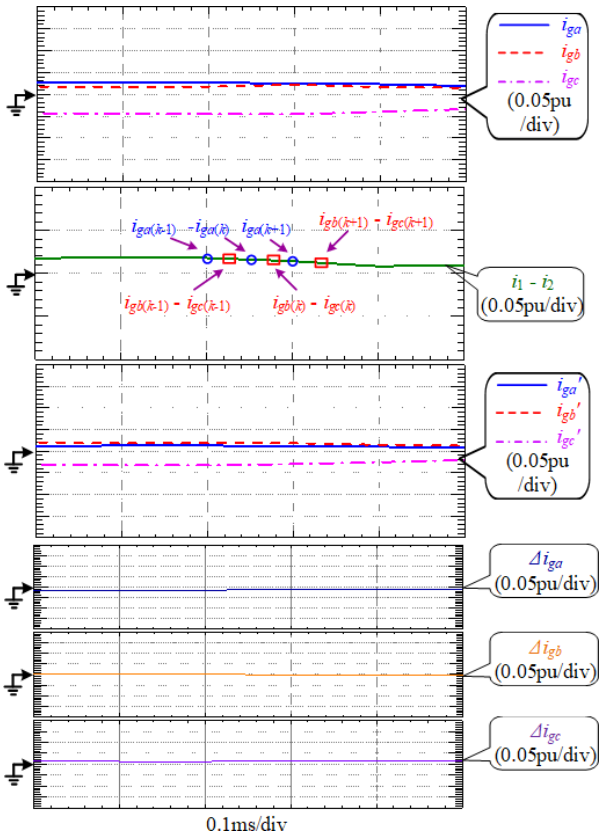


**FIGURE 11. The actual three-phase GSC AC currents $i_{gabc}$, current difference between $i_1$ and $i_2$($i_1 - i_2$), the reconstructed GSC currents $i'_{gabc}$, and the three-phase current differences $\Delta i_{gabc}$ in the region of low wind speed (8m/s).**

capacitor voltages are displayed in Figure. 12 and Figure. 13 when applying $i_{gabc}$ and $i'_{gabc}$, respectively.

It can be seen from Figure. 12 and Figure. 13 that there is no obvious difference for these two cases, meaning that the reconstructed GSC currents can be used to replace the functions of the three-phase current sensors. To inspect the effect

**TABLE 4. Controller gains.**

| | DC-Bus Voltage Controller | GSC Current Controller | RSC Current Controller | DC-Bus Voltage Deviation Suppression Controller |
|---|---|---|---|---|
| $k_p$ | 0.5 | 5 | 0.6 | 0.08 |
| $k_i$ | 100 | 500 | 8 | 0 |

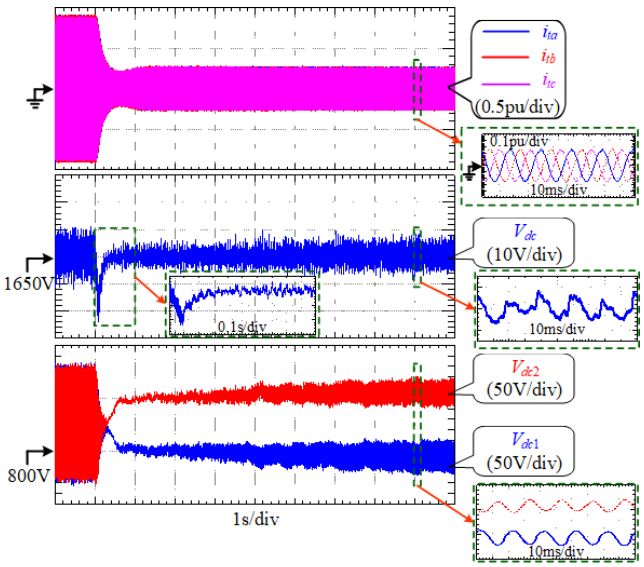


**FIGURE 12. The three-phase total output currents $i_{tabc}$, DC-bus voltage $V_{dc}$, and the upper and lower capacitor voltages $V_{dc1}$ and $V_{dc2}$ when applying the real three-phase GSC AC currents.**

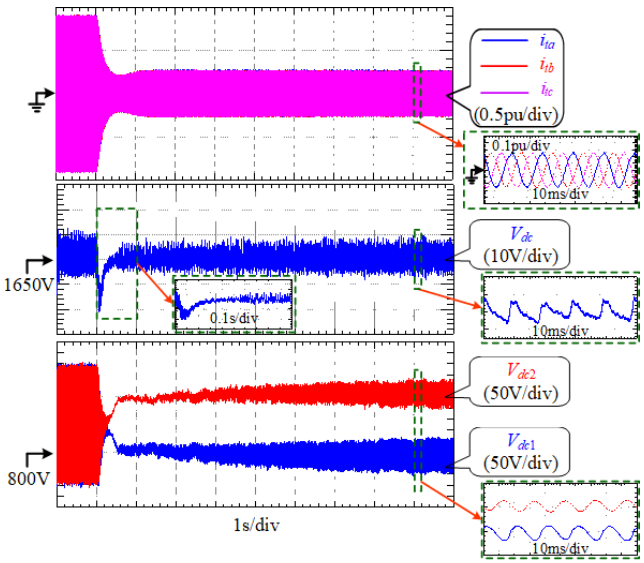


**FIGURE 13. The three-phase total output currents $i_{tabc}$, DC-bus voltage $V_{dc}$, and the upper and lower capacitor voltages $V_{dc1}$ and $V_{dc2}$ when applying the reconstructed three-phase GSC AC currents.**

of the voltage difference suppression strategy, the capacitor voltage difference $\Delta V_{dc}$ is displayed in Figure. 14.

In Figure. 14, the enlarged views of $\Delta V_{dc}$ for the high and low wind speed regions are shown. The voltage difference

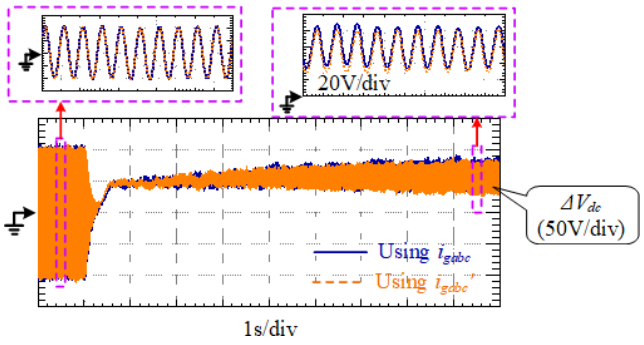


**FIGURE 14.** The capacitor voltage differences $\Delta V_{dc}$ when applying $i_{gabc}$ and $i'_{gabc}$ in the control process.

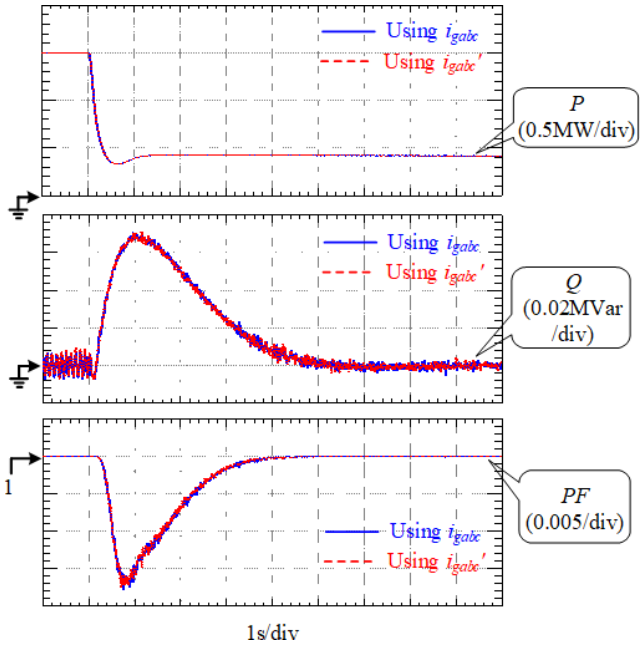


**FIGURE 15.** The total output active, reactive power *P* & *Q*, and the power factor *PF*.

between the upper and lower capacitors is approximately kept within 100V (6.1% of 1650V) when the wind speed is 15m/s, and it oscillates around 60V (3.6% of 1650V) in the low wind speed region. By using $i'_{gabc}$, the average value of $\Delta V_{dc}$ is slightly lower than that when applying $i_{gabc}$.

The overall performance of the FSTP GSC based DFIG-WT is also investigated according to the output power by using the real and reconstructed GSC currents in the control process. The active and reactive output power of DFIG-WT, along with the power factor, are depicted in Figure. 15.

From Figure 15, identical performances of DFIG-WT can be seen when using $i_{gabc}$ and $i'_{gabc}$, respectively. The real output power $P$ is 1.5MW in the high wind speed region, and after the wind speed change, it takes around 1s for it to reach a new steady value, which is around 0.4MW. For the reactive power $Q$, there is a rise to approximately 0.07MVar from 1s to 2s, and then it returns back to 0 after 6s. The power factor $PF$ is maintains at 1 at the beginning and the end of the simulation process. After the wind speed change, $PF$ drops to around 0.982, which is the lowest value in the whole period.

## VII. CONCLUSION

This paper contributes to increasing the reliability of DFIG-WT at the late stage of service time by proposing a current reconstruction strategy for FSTP GSC. The FSTP GSC can work normally even if the three-phase GSC AC current sensors and one bridge arm in GSC is open-circuited at the same time. In the proposed strategy, only one DC-link current sensor is required to measure the difference between the currents flowing through the two paths to the DC bus. By using the information obtained for the measured current difference and the switching states of the four switches, the reconstructed three-phase GSC AC currents can be derived in each switching period. The dead zones in SVPWM techniques for both the SSTP and FSTP converters are also analyzed. Moreover, the SVPWM technique is simplified by removing sector identification, and the DC-link capacitor voltage balancing is obtained.

From the simulation results, the following points can be derived:

(1) Good tracking performance of the reconstructed three-phase GSC AC currents can be obtained by using the proposed phase current reconstruction method.

(2) Almost identical performances of both the FSTP GSC and DFIG-WT can be derived when applying the real and reconstructed three-phase GSC currents.

(3) A lower average value of the capacitor voltage difference can be achieved by using $i'_{gabc}$ in the control process.

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